IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 10 June 2024, accepted 15 July 2024, date of publication 22 July 2024, date of current version 1 August 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3431643

RESEARCH ARTICLE

A Fast Startup 38.4-MHz Crystal Oscillator Achieving 99-nJ Startup Energy With Adaptive Chirping

ABDOLRAOUF RAHMANI[1], HARIKRISHNAN RAMIAH[1,2], (Senior Member, IEEE), KA-MENG LEI[3], (Senior Member, IEEE), CHEE CHEOW LIM[4], NAI SHYAN LAI[4], PUI-IN MAK[3], (Fellow, IEEE), AND RUI P. MARTINS[3], (Life Fellow, IEEE)

[1]Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
[2]Centre for Research in Industry 4.0, Faculty of Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
[3]State-Key Laboratory of Analog and Mixed-Signal VLSI, Institute of Microelectronics, Faculty of Science and Technology–ECE, University of Macau, Macau, China
[4]School of Engineering, Asia Pacific University of Technology & Innovation, Kuala Lumpur 57000, Malaysia

Corresponding author: Harikrishnan Ramiah (hrkhari@um.edu.my)

This work was supported in part by the RU Geran-Faculty Program under Grant GPF056B-2020; in part by the International Funding under Grant IF043-2021; in part by the Partnership Grant under Grant MG024-2022; in part by the Science and Technology Development Fund, Macau, SAR, under Grant SKL-AMSV(UM)-2023-2025 and Grant 0149/2022/A3; and in part by the University of Macau under Grant MYRG2022-00034-IME.

ABSTRACT Shortening the startup time of a crystal oscillator is critical in improving the energy efficiency of the Internet of Things (IoT) sensor nodes. This article presents an investigative study on the application of adaptive chirping using zero-phase cross-detection to reduce the startup time of a crystal oscillator that is robust to voltage, temperature and even process variations without any costly trimming. Post-layout simulations on a 38.4 MHz crystal resonator with 1.0 V supply and 65-nm CMOS process confirms the feasibility of this approach and its ability to effectively reduce the startup time by correcting both phase and frequency mismatches. The results showcase the promising potential of zero-phase adaptive chirp as a viable variation-tolerant technique allowing for a high frequency mismatch tolerance of 1.1×10^6 ppm-Δf.

INDEX TERMS CMOS, Internet-of-Things (IoT), crystal oscillator (XO), startup time, chirp injection, motional current, adaptive chirp injection, energy injection.

I. INTRODUCTION

In the era of wireless sensor networks and the Internet of Things (IoT), wireless sensor nodes play a vital role by efficiently collecting and transmitting data for analysis purposes. These battery-powered nodes for extended operation are deployed where battery replacement is inconvenient and costly, making power optimization a momentous concern. Hence, there is a continued scientific interest in power optimization at the device and network levels [1].

The power-hungry blocks within the wireless sensor nodes, such as low-noise amplifiers, phase-locked loops, data converters, etc., will intermittently operate to reduce the average power consumption. While such duty-cycling technique can extend the battery life, it requires the circuit block to wake up instantly to avert latency and reduce startup energy loss. One crucial circuit block that requires a long startup time (T_{start}) is the crystal oscillator (XO). The XO can provide a stable and precise frequency reference for the wireless sensor nodes. However, due to the high quality factor of the quartz crystal, it takes milliseconds for an MHz-range XO to reach the steady state after enabling the XO. This long T_{start} unavoidably constrains the latency of sensor nodes and correlates with increased depletion of energy. Reference [2] demonstrates that this startup loss accounts for a significant portion, approximately 42%, at each operational cycle of a transceiver at heavy duty cycling of 0.1%. Consequently, achieving additional power savings through heavy duty cycling necessitates a reduction in T_{start}.

The associate editor coordinating the review of this manuscript and approving it for publication was Teerachot Siriburanon.

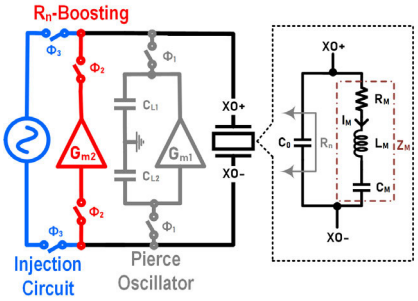


FIGURE 1. Crystal resonator connected in Pierce oscillator (grey), negative resistance boosting startup (red), and Injection startup (blue).

For a traditional XO in Pierce oscillator configuration (Fig. 1), using the linear oscillator model featuring a crystal resonator, the motional current in the core of the quartz crystal (i_M) grows exponentially – provided that the amplifier can promote the growth of oscillation – and is approximated as [3]:

$$i_M(t) \propto I_M(t=0).e^{\alpha t}, \tag{1}$$

$$\alpha \approx \frac{|R_n| - R_m}{2L_m}, \tag{2}$$

where R_m is the crystal's motional resistance, R_n is the negative resistance seen by the crystal's motional branch, and L_M is the motional inductance of the crystal. Then, we can obtain the T_{start} as:

$$T_{start} = \frac{Q}{\pi f_0}.\frac{1}{\alpha}.\ln\left(\frac{0.9I_M(t=t_{ss})}{I_M(t=0)}\right) \tag{3}$$

where Q is the quality factor of the quartz crystal and f_0 is the resonance frequency of the crystal.

There are two main methods to reduce T_{start}. The first one is R_n-boosting [2], [3], [4], [5], [6]. As presented in (1) and (3), boosting R_n increases the growing rate of i_M, and thus shortens T_{start}. The second method is energy injection. Its underlying principle is to inject energy into the crystal core using an auxiliary source (e.g., RC oscillator) and raise the initial i_M of the crystal before connecting the crystal with the core amplifier to reduce the time for the i_M to build up from thermal noise. However, the phase of the injecting source must be in-phase with the i_M throughout the injection to effectively raise i_M. Due to the high Q of the crystal, it requires a typical injection duration above hundreds of cycles to raise, which in turns requires an auxiliary oscillator with a frequency close to f_0. Hence, recent publications on energy injection techniques focus on safeguarding the robustness of the XO's startup amid the process, temperature, and voltage (PVT) variations [7], [8], [9], [10], [11]. Although techniques like two-step injection [8] have strong tolerance against VT, they require costly post-fabrication calibration, such as trimming, to compensate for the process variation.

Chirp injection on the other hand guarantees the performance of the startup by sweeping the injection frequency to cover the frequency deviation of the auxiliary oscillator due to voltage, temperature and even process variation. It does not require specific trimming on the startup circuit to guarantee the operation, thereby significantly reducing the manufacturing and operating costs of the XO. A drawback of the typical chirp injection method is low energy injection efficiency; since the power is spread to a wide frequency band, the energy injected into the crystal core is low compared with constant frequency injection [7] or dithering [4], [11].

TABLE 1. Crystal resonator and injection parameters used for analysis.

f_0	L_M	C_M	R_M	C_0	V_{INJ}
38.4 MHz	2.865m H	6f F	60 Ω	2p F	1 V

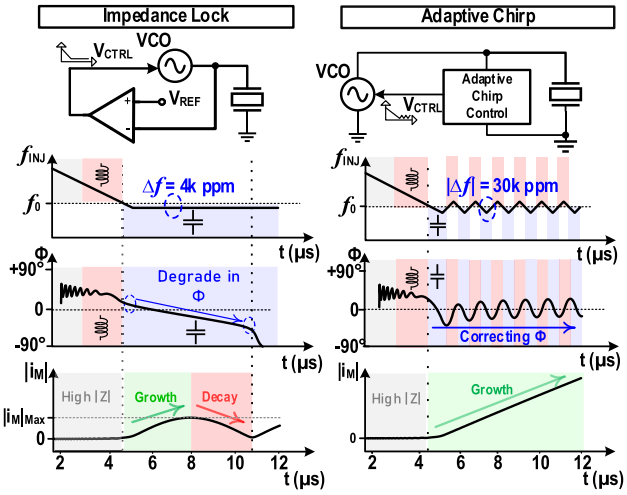


FIGURE 2. Comparison of operation between Impedance lock and the proposed adaptive chirp (fixed peak-to-peak frequency toggling of 30,000 ppm around the resonance) in terms of frequency, phase and motional current envelop profiles.

To this end,this article proposed a frequency and phase self-correcting energy injection method to expedite the XO startup that is robust against PVT variations. Dubbed Zero-Phase Adaptive Chirp (ZAC), it dynamically corrects the frequency and phase of the injection source by detecting the phase difference between the injection source and i_M. Simulated in the CMOS 65-nm process, the XO achieves a startup time of 170 μs, with a startup energy of 99 nJ. It tolerates a frequency deviation of +110% (from nominal value).

The rest of this article is as follows. Section II outlines the conceptual utilization of adaptive chirping to continuously correct the injection phase. Section III elaborates on the circuit implementation of adaptive chirp using zero-phase cross-detection. The circuit architecture of proposed startup technique is described in section IV. Section V presents the post-layout simulation results and benchmarks this work with the state-of-the-art. Finally, Section VI concludes the article.

II. FAST-STARTUP XO USING ADAPTIVE CHIRP

Crystal resonator is remarkable to offer an exceptionally high Q for excellent spectral purity. Yet, a drawback to this high Q is its slow startup behaviour. For a fast startup solution using

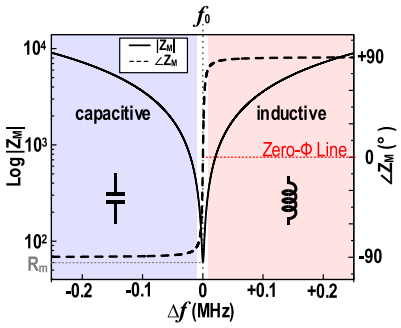


FIGURE 3. Frequency response of motional branch (Z_M) of crystal resonator, exhibiting both capacitive ($\Delta f < 0$) and inductive ($\Delta f > 0$) characteristics.

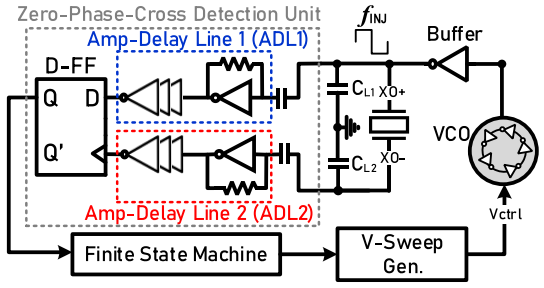


FIGURE 4. Proposed zero-phase XO startup system block diagram highlighting the zero-phase cross-detection unit.

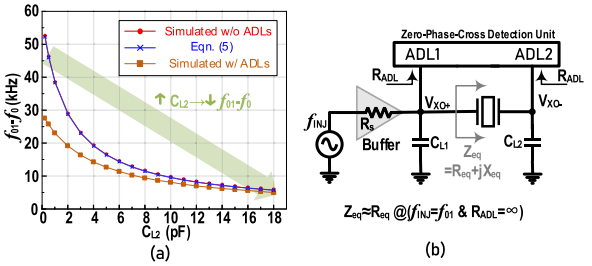


FIGURE 5. Panel (a) compares relative resonance frequencies between Equation (5) and simulations with/without ADL loading for different C_{L2} values. The simulations use the test-bench in panel (b) and parameters from Table 1, including Amp-Delay Lines from Figure 4.

energy injection, a stringent requirement on the frequency mismatch between the resonance and injection frequency to promote robust growth on the i_M [12] is necessary. In light of this, PVT-tolerant energy injection techniques such as chirp injection are attractive as they allow the auxiliary injection circuit to inject energy at resonance frequency to increase i_M and reduce T_{start} amid PVT variation without any trimming after manufacturing. Yet, as the injection energy is distributed to a wide band for covering PVT variation, without feedback to lock the auxiliary oscillator, the energy delivered to the crystal is limited where the XO needs additional time to reach the steady state after the injection. Alternatively, resonance searching techniques such as impedance-guided injection [7] have been proposed to lock the injection frequency near the resonance frequency.

Herein, based on impedance-guided injection, we proposed adaptive chirping for fast XO start-up (Fig. 2). The operation principle is by comparing the frequency and phase of the chirping signal to that of the motional current from the crystal. In [7], the injection unit is locked at a low crystal impedance, where the exact impedance magnitude is determined by reference voltage, V_{REF}, and assumed to lock at f_0. However, to ensure an effective injection, the frequency mismatch after locking must be below 530 ppm to establish a maximum motional current for given crystal parameters in Table 1, $C_{L1} = C_{L2} = 14$ pF, and $V_{XO+} = 0.9$ V as obtained below [12]:

$$\frac{\Delta f}{f_0} = \mp \frac{4V_{INJ}/\pi}{V_{XO+}} \cdot \frac{C_M}{(C_{L1} + C_{L2})/2 + C_0}, \tag{4}$$

where V_{XO+} is the steady-state oscillating amplitude, V_{INJ} is the amplitude of the injection signal, C_{L1} and C_{L2} are the load capacitances to two ends of the crystal, and C_0 is crystal's shunt capacitance. Locking within 530 ppm of f_0 requires a delicate design consideration accounting in the chirping sweep rate, VCO noise, comparator offset, V_{REF}, and delay in resonance detection under PVT variations. Consequently, due to Δf and uncorrected phase error (ϕ), the injection has to be disabled by a short duration when the maximum i_M, $|i_M|_{Max}$, has been reached.

In light of this challenge, we proposed adaptive chirp to relax such strict design requirements and enable ϕ correction under PVT variation. In principle, the chirping circuit sweeps the output signal's frequency (f_{INJ}) up and down about f_0 to correct the ϕ accumulated due to injection with Δf (Fig. 2). Initially, the chirping signal starts its operation with a frequency significantly higher than f_0 to guarantee it will cross f_0 amid PVT variations. Due to the frequency mismatch, the impedance of the resonator (Z_m) is determined mostly by the reactive components (either capacitive or inductive), which is higher than its impedance at f_0 ($\approx R_m$), as shown in Fig. 3. Hence, energy cannot be injected to the resonator initially and i_M maintains a weak magnitude. As f_{INJ} approaches f_0 (entering low-Z_m region), due to the positive Δf (initial $f_{INJ} > f_0$), the resonator exhibits an inductive impedance, resulting in a pulling of ϕ towards the positive. As f_{INJ} continues to decrease below f_0, the resonator transfers from inductive to capacitive. This transition leads to a pulling of ϕ towards the negative. Therein, the ϕ crosses the zero value. In principle, we can detect this zero-crossing point and invert the chirping direction (from down-chirping to up-chirping) to effectively correct the new ϕ. Similarly, upon reaching the up-chirping operation, the ϕ also crosses zero again, where we can again detect this point and invert the chirping direction. Hence, the circuit will generate an alternative up- and down-chirping sequence centred around f_0 to enable a continuous correction of ϕ. This coordinated approach facilitates sustained $|i_M|$ growth.

III. ZERO-PHASE LOCK AND ADAPTIVE CHIRP ANALYSIS

In this section, we will outline the implementation of both adaptive chirping and constant frequency lock injection

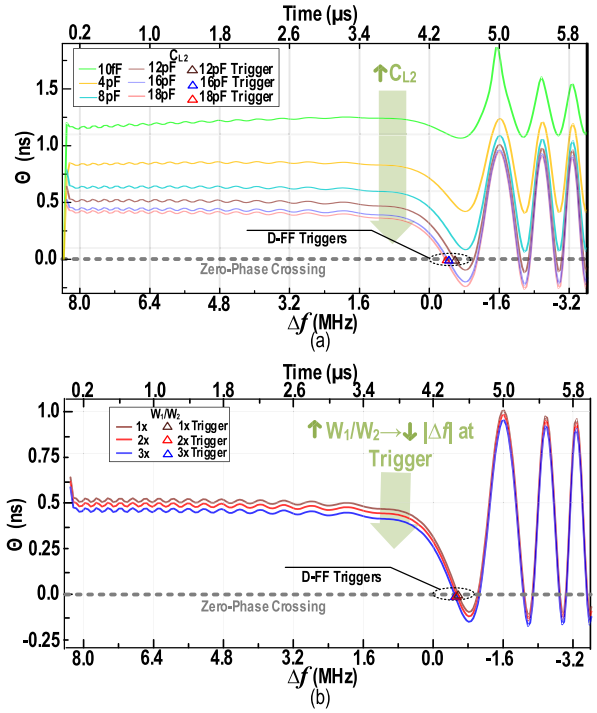


FIGURE 6. The θ (t) versus Δf for different (a) C_{L2} and (b) delay line sizing. We set a chirping rate of 2 MHz/μs in the simulations.

techniques through the utilization of a Zero-phase Cross-detection unit, referred to as Zero-phase Adaptive Chirping (ZAC) and Zero-phase Lock (ZL) injections, respectively.

Fig. 4 shows the proposed system configuration and the Zero-phase Cross-detection unit to detect the ϕ between i_{M} and V_{INJ} by using the transient phase difference between $V_{\mathrm{XO+}}$ and $V_{\mathrm{XO-}}$. The proposed system has an added capacitance, C_{L2}, in series to the crystal, resulting the resonance frequency seen by the injector into the crystal to shift as given by:

$$f_{01}^2 \approx f_0^2 \frac{C_0 + C_{L2} + C_M}{C_0 + C_{L2}}, \tag{5}$$

where f_{01} is the new resonance frequency seen into the crystal terminal in the presence of C_{L2} given no amp-delay line (ADL) loading (derived in Appendix). (5) evinces that f_{01} is independent of C_{L1} and R_{s} thereby it is independent of buffer loading and buffer driving strength respectively. Additionally, when $C_{\mathrm{L2}} \gg C_{\mathrm{M}}$ then $f_{01} \approx f_0$. Utilizing the crystal parameters in Table 1, Fig. 5(a) shows that (5) gives close approximation of f_{01} for different C_{L2}.

Additionally, at f_{01}, since the combination of crystal and C_{L2} induce zero-phase and a grounded capacitor provides a $-90°$ phase shift, the steady-state phase $\theta(\omega)$ at $V_{\mathrm{XO-}}$ with respect to $V_{\mathrm{XO+}}$ at f_{01} is $-90°$, which can be validated by the relationship below:

$$V_{XO-}(j\omega) = V_{XO+} \cdot \frac{1/j\omega C_{L2}}{Z_{eq}(j\omega)}. \tag{6}$$

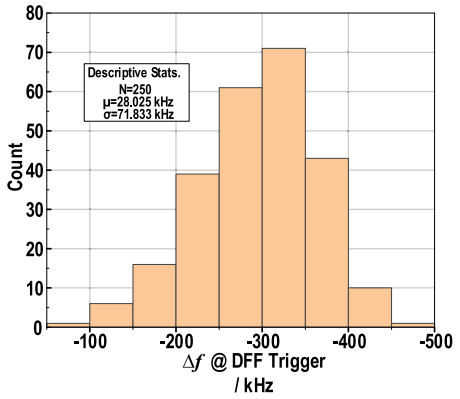


FIGURE 7. Monte-Carlo simulated Δf (at D-FF trigger) given C_{L2} = 14pF, and 2x W_1 /W_2 under 2 MHz/ μs down chirp.

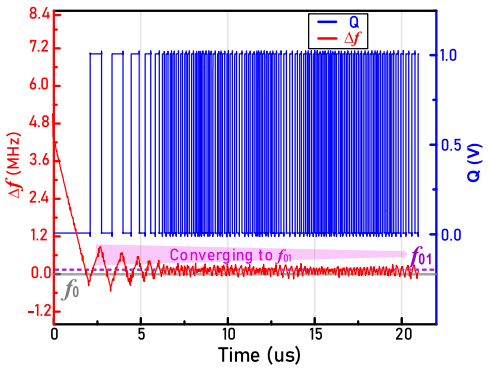


FIGURE 8. Frequency profile of the zero-phase adaptive chirp injection and the output from the D-FF.

From (6), we can obtain $\theta(\omega)$ as:

$$\begin{aligned} \theta(\omega) &= \angle V_{XO-}(j\omega) - \angle V_{XO+}(j\omega), \\ \theta(\omega) &= \angle {}^{1}\!/_{j\omega C_{L2}} - \angle Z_{eq}(j\omega), \end{aligned} \tag{7}$$

where Z_{eq} is the impedance seen by the buffer looking into the crystal, and it is equivalent to the impedance of crystal added to the impedance of C_{L2} given the assumption of no Amp-Delay Line (ADL) loading. Given no ADL loading equation (7) shows that when $\angle Z_{\mathrm{eq}}(j\omega) = 0°$, which occurs when $\omega \approx \omega_{01} (= 2\pi f_{01})$, $\theta(\omega)$ becomes $-90°$. Furthermore, the phase difference below and above ω_{01} is $-180°$ and $0°$, respectively.

The behavior mentioned above is valid in the steady state with no ADL loading, which forms a part of the transient response of the voltage difference between $V_{\mathrm{XO+}}$ and $V_{\mathrm{XO-}}$. This article hence proposes the detection of f_{01} by exploiting the change in the transient phase, $\theta(t)$, when the chirping f_{INJ} crosses f_{01}. Note that the complete solution to such dynamic system's differential equation in providing transient phase includes both steady-state and transient components along with the ADL loading. The transient component with loading resists immediate aligning with the steady-state phase of $-90°$; however, it is nevertheless pulled toward the steady-state component, as depicted with Fig. 6's transient result with ADL loading. The transient phase crossing behaviour

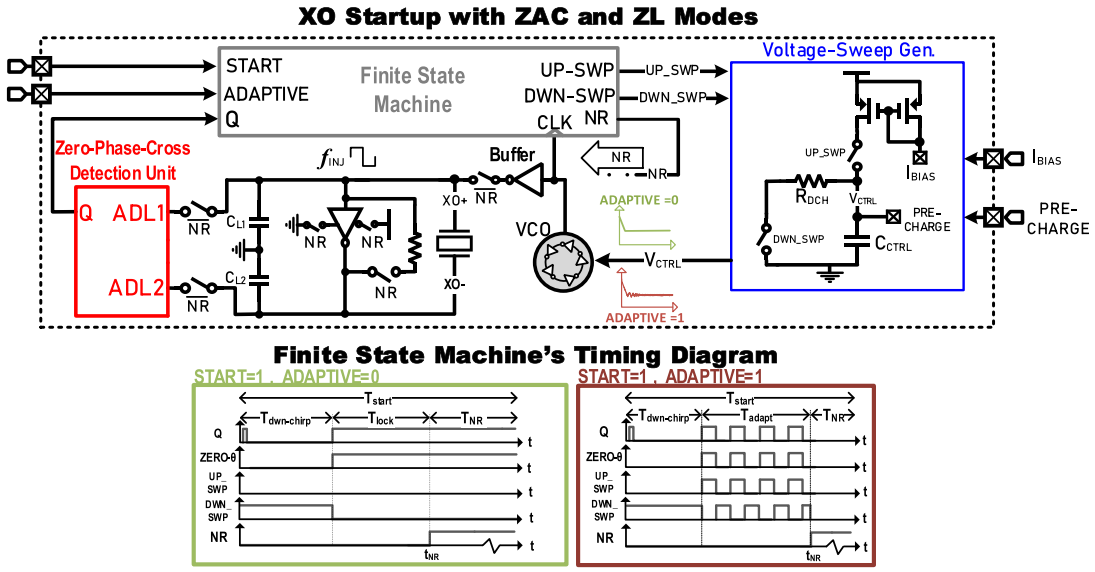


FIGURE 9. System architecture of the proposed crystal oscillator with zero-phase lock and zero-phase adaptive chirp startup modes.

when chirping through f_{01} is utilized to represent f_0 as opposed to low impedance thresholds in [7] and [9]. This behaviour is robust in detecting f_0, as it involves a single phase crossing point rather than a range of low voltage values. Moreover, such discrete crossing values can be exploited to implement adaptive chirping.

We utilized a zero-phase cross-detection unit to detect when the transient phase becomes zero. In principle as only the phases polarity of the signals is relevant, we can employ D-flip flop (D-FF) to detect the sequence of the transitions and thus the phase polarity. To guarantee the amplitudes of signals are capable in driving the logic circuits under PVT variations, we utilized a self-biased AC-coupled amplifier to amplify the signal swings, facilitating reliable triggering of the D-FF.

Detection of f_0 using zero-phase cross detection requires the design of C_{L2} and the relative delay difference between amplifier delay lines 1 and 2, as they will affect the zero-crossing point. To ensure zero-crossing with tolerance to D-FF's metastability and PVT variations, given crystal resonator parameters given in Table 1, C_{L2} of 14 pF is selected as the transient phase goes well below zero-phase. Furthermore, delay difference between the lines is adjusted via width ratio (W_1/W_2) and it is sized as 2x by a trade-off between consistent PVT operation and reduced footprint. Indeed, we utilized these two parameters to achieve coarse and fine-tuning on $\theta(t)$ such that $\theta(t) = 0°$ when $\Delta f = 0$ [Fig. 6(a) and (b)]. The Monte-Carlo simulated Δf (at D-FF trigger) in Fig. 7 proves zero-phase cross-detection unit's core functionality robustness against process variation.

The ZL technique can be realized by locking the injection frequency from the oscillator once the D-FF's output becomes high, corresponding to the first zero-phase cross-detection. This locking makes ZL, just like other resonance lock injections, slightly process sensitive. Notably, when compared to the analogue based resonance searching technique in [7], which utilized a comparator, the proposed zero-phase searching promises a superior power consumption due to its digital implementation.

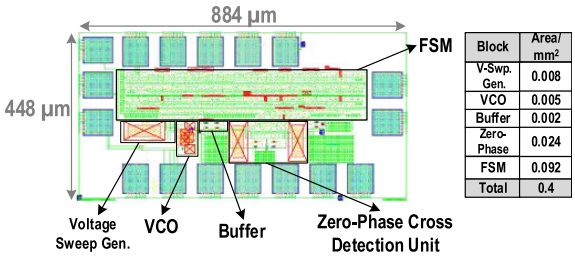
Similarly, the ZAC can be realized by inverting the chirping direction upon inversion of the D-FF's output, Q. Fig. 8 illustrates the operation of zero-phase cross-detection for ZAC showcasing how upon adaptive inversions of Q the frequency converges about $f_{01}(\approx f_0)$. This results in a lower frequency mismatch error compared to ZL. The adaptive frequency correction property also reduces the impact of variations on the injected frequency and crystal excitation. Additionally, the proposed adaptive injection provides phase correction, further enhancing variation tolerance (where phase correction is further discussed in Section V).

IV. CIRCUIT ARCHITECTURE

Fig. 9 illustrates the circuit architecture of the crystal oscillator with ZL and ZAC for fast startup. It includes primarily a digital CMOS finite state machine, voltage sweep generator, voltage-controlled ring oscillator, zero-phase cross-detection unit with digital CMOS D-FF, a weak buffer (implemented as a CMOS inverter) and self-biased inverting amplifier for Pierce oscillator configuration [13]. Whereby $C_{L1} = C_{L2}$ considering a conventional Pierce oscillator. The startup sequence and operation of ZL and ZAC injection (Fig. 9) is as follows:

1) The initial voltage of the sweep voltage generator, V_{CTRL}, is set by charging its capacitor, C_{CTRL}, using the PRECHARGE port.

2) When the startup is enabled, the V_{CTRL} starts to drop according to $\Delta V = V_{CTRL}(t = 0) \times exp(-\Delta t / R_{DCH} C_T)$, where C_T represents the aggregate of C_{CTRL}, parasitic capacitances, and the input capacitance of the VCO, with C_{CTRL}



Block	Area/ mm²
V-Swp. Gen.	0.008
VCO	0.005
Buffer	0.002
Zero-Phase	0.024
FSM	0.092
Total	0.4

FIGURE 10. Layout of XO with the proposed ZL and ZAC fast startup injection techniques.

being the predominant capacitance contributor. Hence, the VCO's frequency starts to decrease.

3) The zero-phase cross-detection unit detects the relative phase between V_{XO+} and V_{XO-}. To overcome the error due to the random noise, the FSM only accepts transition when the results from 3 periods are identical. The FSM uses the VCO's clock signal to count this duration using a digital counter.

4) When the f_{INJ} exceeds f_{01}, the zero-phase cross-detection unit detect this zero-phase point.

5) For ZL injection, when the crossing point is detected (zero-θ becomes 1 V), the DWN_SWP state turns to 0 V and consequently locks the injection frequency. The injection then continues until it reaches a preset duration, T_{lock}. For the ZAC injection, upon inversion of zero-θ, the DWN_SWP and UP_SWP states become 0 V and 1 V, respectively, leading to the charging of C_{CTRL} according to $\Delta V = I_{BIAS} \times \Delta t / C_T$. This results in an up-sweep of V_{CTRL} and an up-chirp of f_{INJ}. Another inversion of zero-θ inverts UP_SWP and DWN_SWP states again, causing a down-chirp of f_{INJ}. This process continues for a preset injection duration, T_{adapt}. After the injection durations for both ZL and ZAC injections, the NR state changes to 1 V at time t_{NR}(where this value will be discussed in Section V).

6) With NR state at 1 V, the injecting unit and zero-phase cross-detection unit are disabled, while the core amplifier unit, made from a self-biased inverter, is in place to sustain the oscillation in the steady state.

V. POST-LAYOUT SIMULATION RESULTS

To prove the core functionality of the proposed fast startup XO, we implemented and simulated with post-layout parasitics in the 65-nm CMOS process. Fig. 10 shows the system layout which occupies a total area of 0.4 mm^2. The capacitive loads of 14p F and voltage supply of 1 V is used for the oscillator. Furthermore, we have selected a crystal resonator with f_0 of 38.4 MHz driven by a small buffer (V_{XO+} = 150 mV peak-to-peak). To account for the PVT variations, the initial V_{CTRL} is set such that VCO's initial frequency is above f_0 in all corners using the same V_{CTRL} value. This is achieved by conducting a parametric sweep simulation of V_{CTRL} against VCO's frequency and ensuring that the resulting frequency for the selected V_{CTRL} is higher than f_0 across all PVT corners. Furthermore, the ring-VCO exhibits the fastest and slowest frequency down-sweep rates of 1.6 MHz/μs and 0.8 MHz/μs for the FF and SS corners, respectively.

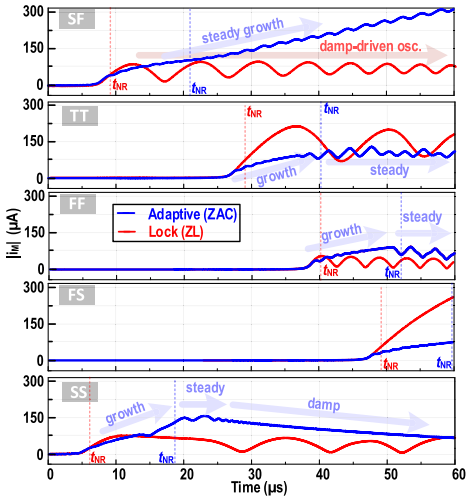
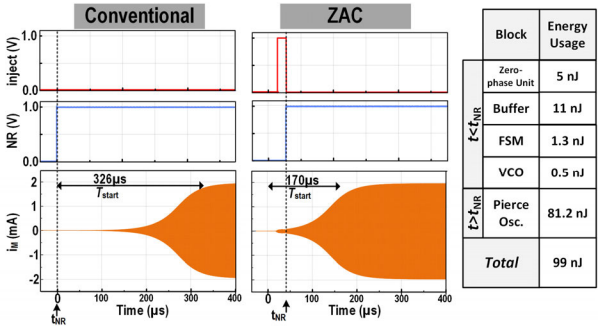


FIGURE 11. The growth of $|i_M|$ using ZAC and ZL. We set t_{NR} corresponding to 519 cycles and 70 cycles after the first zero-phase detection respectively.



	Block	Energy Usage
t<tNR	Zero-phase Unit	5 nJ
	Buffer	11 nJ
	FSM	1.3 nJ
	VCO	0.5 nJ
t>tNR	Pierce Osc.	81.2 nJ
	Total	99 nJ

FIGURE 12. Oscillation signal with a 38.4 MHz resonator, displayed without (left) and with (right) the proposed fast startup. The accompanying table indicates energy consumption with the proposed startup.

Fig. 11 shows $|i_M|$ for all process corners to highlight the phase-error correction property of ZAC relative to ZL. While ZL only exhibits damped driven oscillation, ZAC shows continuous growth (at SF), growth and sustain (at TT and FF) and growth, sustain and gradual damping (at SS) corresponding to broad effectiveness of adaptive chirp. Leveraging the closed-loop property and aiming to enhance the average $|i_M|$ across process variations, the selection of t_{NR} for ZAC and ZL, as inferred from studying Fig. 11, is 519 and 70 cycles respectively. These values equate to approximately 13.5 μs and 1.8 μs, based on a 38.4 MHz clock, following the initial zero-phase cross-detection. The extended injection duration of ZAC relative to ZL demonstrates its higher capacity for process variation tolerance. On the other hand, open loop injections, such as chirp injections, have to preset t_{NR} with respect to the start time. The startup time of the XO with ZAC and without startup aid is shown in Fig. 12. With ZAC, the startup time reduces from 326 μs to 170 μs. Furthermore, ZAC has reduced total startup energy from 152 nJ to 99 nJ. Whereby ZAC's energy before t_{NR} constitutes the consumptions in FSM (1.3 nJ), zero-phase cross detection (5 nJ), buffer (11 nJ), VCO (0.5 nJ).

TABLE 2. Performance summary and comparison with prior art.

	JSSC'19 [8]	ISSCC'23 [9]	JSSC'22 [7]	JSSC'16 [10]	Proposed #	
Technique	2-step PLL Injection	Automatic Phase-Error Correction	IGCI + Boosted R_n	Chirp + Boosted R_n	**Zero-Phase Lock**	**Zero-Phase Adaptive Chirp**
Technology (nm)	65	40	22	180	**65**	
Resonator Frequency (MHz)	54	16	38.4	39.25	**38.4**	
Steady state Voltage/ Supply voltage (V)	0.5/1.0	0.25/1.0†	0.8/1.0	1.4/1.5	**0.95/1.0**	
PVT Tolerant Injection	NO	NO	YES	YES	**YES**	**YES**
Frequency Mismatch Tolerance (ppm-Δf)	$5x10^3$	10^4	$4.7x10^4$ †	$1.25x10^6$ *	**$1.1x10^6$ ***	
$\Delta T_{start}/T_{start}$ over $Temp_{range}$	1.25%	4.5%	26%†	7%	**3%ˣ**	**3.8%**
Load Cap (pF)	6	6	3.75	6	**14**	
T_{start} (µs)	19	17.5	58	158	**175**	**170**
E_{START} (nJ)	34.9	9.2	45.6	349	**107**	**99**
Steady State Power (µW)	198	84	800	181	**450**	
Temperature Range (°C)	-40 to 85	-20 to 85	-40 to 40†	-30 to 125	**-20 to 80**	

Simulated Results.
† Value obtained from visual inspection of figures.
* Value obtained for corner case with highest value.
ˣ Achieved low variation at cost of lower $|i_M(t_{NR})|$

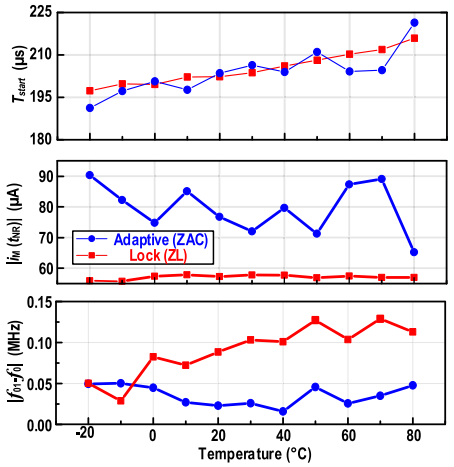


FIGURE 13. Simulated T_{start}, $|i_M(t_{NR})|$ and average frequency error against temperature variations.

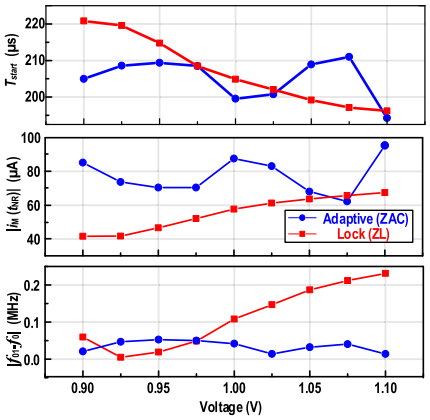


FIGURE 14. Simulated T_{start}, $|i_M(t_{NR})|$ and average frequency error against voltage variations.

The correlation between startup time and $|i_M(t_{NR})|$, as expressed in (3), informs the injection unit's efficiency. Fig. 13 illustrates $|i_M(t_{NR})|$ under ZAC across −20 to 80 °C, demonstrating a relative variation coefficient of 10.3%, with maximum and minimum $|i_M(t_{NR})|$ of 90 μA and 71 μA at −20°C and 50°C, respectively. These results correspond to a minimum and maximum T_{start} of 191 μs and 221 μs for −20 and 80°C with only a relative variation of 3.8%. In contrary, the constant frequency counterpart experiences a lower $|i_M(t_{NR})|$ by 39% (from average of 79 μA to 57 μA) and consequently a higher T_{start} from 203 μs to 205 μs, justifying ZAC's superior startup performance. Moreover, ZAC offers a lower average $|f_{01}$-$f_0|$ by 157% with respect to ZL (from 90 kHz to 35 kHz). The improved frequency accuracy of ZAC across temperature variations is attributable to its longer convergence duration toward f_{01}. This extended convergence duration significantly enhances ZAC's frequency detection variation tolerance by compensating for detection delays.

Fig. 14 illustrates the startup performance of the XO with ZAC and ZL against voltage variations (0.9 V to 1.1 V). The XO with ZAC shows a 14% relative change in $|i_M(t_{NR})|$ when the supply voltage varies by 10%, whereas that with ZL displays a higher relative variation of 18%. In addition to $|i_M(t_{NR})|$, the XO with ZAC also exhibits a lower average Δf of 35 kHz, in contrast to 113 kHz from that with ZL.

The $|i_M(t_{NR})|$ response for the XOs with ZAC and ZL across process corners yields an average value of 94 uA and 54 uA, with 219 μs and 233 μs average startup times, respectively (Fig. 15); the fastest and slowest startup of the XO with ZAC are at the SF and SS corners (178 μs and 308 μs). At FS despite starting with the highest initial frequency of 80 MHz (corresponding to 1.1×10^6 ppm-Δf) ZAC retains its correction property achieving 221 μs.

Table 2 summarizes and compares the performance with prior architectures. The proposed adaptive zero-phase

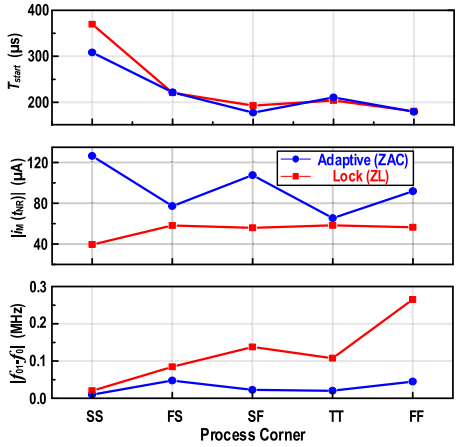


FIGURE 15. Simulated T_{start}, $|i_M(t_{NR})|$ and average frequency error against process corners.

injection technique supplements the PVT tolerant injection XO startup methods [7] and [10], enhancing them by providing an exceptional frequency mismatch tolerance of 1.1×10^6 ppm-Δf. While the proposed technique falls 12% short of the frequency mismatch tolerance achieved by the technique cited in [10], it compensates with superior 3.5× lower startup energy consumption (Es). The robustness of [10] and the proposed injection are attributed to the inherent chirping mechanism used. IGCI [7], also employing a chirping mechanism, enables quicker PVT-tolerant startup with respect to ZAC by utilizing a reduced C_L and lower steady-state voltages. However, this approach would entail an inherently higher oscillator phase noise cost [14], whereas the proposed design could demonstrate a superior performance. Moreover, owing to ZAC's correction property, which mitigates the error induced by the resonance frequency detector, the startup variation across the temperature range is 7× superior to that of IGCI's. Regardless of the higher power consumption and longer startup relative to other techniques, this investigative paper proposed and verified ZAC's Δf and ϕ correcting injection which showcases potential in PVT robust startup time reduction. For full exploitation of ZAC with lower steady-state power consumption and higher resonator excitation, optimization for a system with lower bias current Pierce oscillator and a higher injection voltage swing is planned respectively. For a given supply voltage, enhancing the injection voltage swing can be achieved by reducing the buffer output impedance, R_s, or by detaching C_{L1} during injection. Additionally, the verified operation with low injection voltage shows ZAC's prospect in ultra-low voltage startup systems. This potential is further explored in future research.

VI. CONCLUSION

In this paper, we utilized chirp injection to enhance the startup performance of crystal oscillators. Specifically, we employed adaptive chirping to cover the frequency deviations caused by PVT variations without any specialized trimming of the startup circuit. This approach offers significant cost savings in both manufacturing and operation. It provides a state-of-the-art startup time variation of merely 3.8% against temperature fluctuations, achieved without the need for trimming circuitry that is used for process compensation. The reduction in chip area, achieved by eliminating the need for trimming, along with the elimination of associated labor costs, leads to the savings in manufacturing expenses. Compared with conventional chirp injection methods that tend to have low energy injection efficiency due to their wide frequency band coverage, the proposed energy injection technique, zero-phase adaptive chirping, accelerates the crystal oscillator and also mitigates the impact of PVT variations. Post-layout simulations conducted in CMOS 65-nm process demonstrates the technique achieves a startup time of 170 μs with a startup energy consumption of 99 nJ. Moreover, the injection oscillator for energy injection can withstand a frequency deviation range of +110% from the nominal value, supporting the operation under different extreme operating corners. This innovative approach represents a promising advancement in crystal oscillator startup, offering improved robustness to PVT variations.

APPENDIX
DERIVATION OF (5)

With reference to Fig. 5(b), the impedance seen by buffer looking into the crystal, with ignoring the loading by Amp-Delay Lines, is

$$Z_{eq} = Z_3 + 1/j\omega C_{L2},$$

where Z_3 is the impedance of the crystal, and it is given as

$$Z_3 = 1/j\omega C_0 || (R_M + 1/j\omega C_M + j\omega L_M),$$
$$Z_3 = \frac{(aR_M + bd) + j\,(bR_M - ac)}{R_M^2 + c^2},$$
$$Z_3 = R_3 + jX_3,$$

where

$$a = \frac{\omega L_M - 1/\omega C_M}{\omega C_0},$$
$$b = -R_M/\omega C_0,$$

and

$$c = \omega L_M - 1/\omega C_M - 1/\omega C_0.$$

At f_{01} we have

$$Z_{eq} = R_{eq},$$

since at this frequency

$$X_{eq} = X_3 - 1/2\pi f_{01} C_{L2} = 0. \tag{1A}$$

Considering negligible $R_m(=0)$, using (1A) f_{01} is derived to be

$$f_{01}^2 = \frac{C_{L2} + C_0 + C_M}{C_0 + C_{L2}} \left(\frac{1}{L_M C_M}\right). \tag{2A}$$

Using crystal's series resonance frequency $f_0(= 1/2\pi\sqrt{(L_M C_M)})$, (2A) gives f_{01} as (5).

REFERENCES

[1] R. R. Rout and S. K. Ghosh, "Enhancement of lifetime using duty cycle and network coding in wireless sensor networks," *IEEE Trans. Wireless Commun.*, vol. 12, no. 2, pp. 656–667, Feb. 2013, doi: 10.1109/TWC.2012.111412.112124.

[2] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8-μ w steady-state power," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2624–2635, Sep. 2018, doi: 10.1109/JSSC.2018.2849012.

[3] A. Rusznyak, "Start-up time of CMOS oscillators," *IEEE Trans. Circuits Syst.*, vols. CS-34, no. 3, pp. 259–268, Mar. 1987, doi: 10.1109/TCS.1987.1086137.

[4] A. Karimi-Bidhendi, H. Pu, and P. Heydari, "Study and design of a fast start-up crystal oscillator using precise dithered injection and active inductance," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2543–2554, Sep. 2019, doi: 10.1109/JSSC.2019.2920084.

[5] M. Ding, Y.-H. Liu, P. Harpe, C. Bachmann, K. Philips, and A. Van Roermund, "A low-power fast start-up crystal oscillator with an autonomous dynamically adjusted load," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 4, pp. 1382–1392, Apr. 2019, doi: 10.1109/TCSI.2018.2880282.

[6] M. Miyahara, Y. Endo, K. Okada, and A. Matsuzawa, "A 64μs start-up 26/40MHz crystal oscillator with negative resistance boosting technique using reconfigurable multi-stage amplifier," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. 115–116, doi: 10.1109/VLSIC.2018.8502281.

[7] H. Luo, S. Kundu, T. Huusari, S. Shahraini, E. Alban, J. Mix, N. Kurd, M. Abdel-Moneum, and B. Carlton, "A fast startup crystal oscillator using impedance guided chirp injection in 22 nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 688–697, Mar. 2022, doi: 10.1109/JSSC.2021.3136237.

[8] K. M. Megawer, N. Pal, A. Elkholy, M. G. Ahmed, A. Khashaba, D. Griffith, and P. K. Hanumolu, "A fast startup CMOS crystal oscillator using two-step injection," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3257–3268, Dec. 2019, doi: 10.1109/JSSC.2019.2936296.

[9] Z. Cai, X. Wang, Z. Wang, Y. Yin, W. Zhang, T. Xu, and Y. Guo, "3.7 A 16MHz X0 with 17.5μs startup time under 104ppm-ΔF injection using automatic phase-error correction technique," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 2–4, doi: 10.1109/ISSCC42615.2023.10067675.

[10] S. Iguchi, H. Fuketa, T. Sakurai, and M. Takamiya, "Variation-tolerant quick-start-up CMOS crystal oscillator with chirp injection and negative resistance booster," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 496–508, Feb. 2016, doi: 10.1109/JSSC.2015.2499240.

[11] D. Griffith, J. Murdock, and P. T. Røine, "5.9 A 24MHz crystal oscillator with robust fast start-up using dithered injection," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Jan. 2016, pp. 104–105, doi: 10.1109/ISSCC.2016.7417928.

[12] K.-M. Lei, P.-I. Mak, and R. P. Martins, "Startup time and energy-reduction techniques for crystal oscillators in the IoT era," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 1, pp. 30–35, Jan. 2021, doi: 10.1109/TCSII.2020.3040419.

[13] E. Vittoz, "CMOS-Inverter Oscillator," in *Low-Power Crystal and MEMS Oscillators: The Experience of Watch Developments, in Integrated Circuits and Systems*. Cham, Switzerland: Springer, 2010, pp. 124–128.

[14] E. A. Vittoz, M. G. R. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: Theory and application," *IEEE J. Solid-State Circuits*, vols. SSC23, no. 3, pp. 774–783, Jun. 1988, doi: 10.1109/4.318.

ABDOLRAOUF RAHMANI received the B.E. degree (Hons.) in electrical and electronic engineering from the University of Malaya, Malaysia, where he is currently pursuing the M.Sc. degree with the Department of Electrical Engineering. His current research interests include crystal oscillator startup reduction and process robust design of analog integrated circuits.

HARIKRISHNAN RAMIAH (Senior Member, IEEE) received the B.Eng. (Hons), M.Sc., and Ph.D. degrees in electrical and electronic engineering and analog and digital IC design from Universiti Sains Malaysia, Penang, Malaysia, in 2000, 2003, and 2008, respectively.

In 2002, he was with Intel Technology Sdn. Bhd., Penang, performing high-frequency signal integrity analysis. In 2003, he was with Sires Labs Sdn. Bhd., Cyberjaya. He is currently a Professor with the Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia, working in the area of RF integrated circuit (RFIC) and RF energy harvesting circuit design. He is the Director of the Center of Research Industry 4.0 (CRI 4.0), University of Malaya. He has authored or co-authored several articles in technical publications. His main research interests include analog-integrated circuit design, RFIC design, VLSI system design, and radio frequency energy harvesting power management module design.

Prof. Ramiah is a member of the Institute of Electronics, Information, and Communication Engineers. He was a recipient of the Intel Fellowship Grant Award, from 2000 to 2008. He had received continuous international research funding in recognition of his work, from 2014 to 2021, such as the Motorola Foundation Grant. He is a Chartered Engineer of the Institute of Electrical Technology and a Professional Engineer registered under the Board of Engineers Malaysia.

KA-MENG LEI (Senior Member, IEEE) received the B.Sc. degree in electrical and electronic engineering and the Ph.D. degree in electrical and computer engineering from the University of Macau, Macau, in 2012 and 2016, respectively.

He was a Postdoctoral Fellow with Harvard University, from 2017 to 2019, where he was involved in developing the high-resolution portable nuclear magnetic resonance (NMR) spectrometer. He has been an Assistant Professor with the University of Macau, since 2019. He has published 29 refereed articles. He co-authored one book *Handheld Total Chemical and Biological Analysis Systems: Bridging NMR, Digital Microfluidics, and Semiconductors* (Springer 2018) and two book chapter *Micro-NMR on CMOS for Biomolecular Sensing* (Springer 2018) and *Ultra-Low-Voltage Clock References* (Springer 2023). His current research interests include ultralow voltage analog circuit techniques, sensors and analog front-end interfaces, and high-resolution portable NMR platform. He was a TPC Member of ICTA, in 2021 and 2022. He is serving as a member for the IEEE SSCS Young Professionals and coordinating the Webinars for Young Excellence Program. He was a (co-)recipient of the Chipidea Microelectronics Prize 2017 (Postgraduate), the Best Paper Award in ASQED 2013, the Distinguished Design Award from the IEEE Asian Solid-State Circuits Conference, in 2015, the Silkroad Award from the ISSCC 2016, the FDCT Macao Science and Technology Award for Postgraduates, in 2016, the 2016 Young Researcher Award from the Instituto International de Macau, and the IEEE SSCS Predoctoral Achievement Award, in 2017. He was on the Organizing Committee of IEEE A-SSCC 2019. He is an Associate Editor of IEEE Open Journal of Circuits and Systems.

CHEE CHEOW LIM was born in Kuala Lumpur, Malaysia. He received the B.Eng. degree (Hons.) in electrical and electronic engineering from Asia Pacific University of Technology & Innovation (APU), Malaysia, in 2014, and the Ph.D. degree in electrical engineering from the University of Malaya (UM), Malaysia, in 2019.

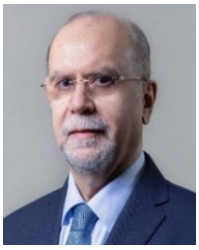
From 2021 to 2022, he was an Analog Engineer with Intel Corporation. He is currently a Lecturer with APU. His research interests include CMOS RF integrated circuits and systems with specialization in RF oscillators, and modeling, and characterization of passive inductors/transformers. He received the Best Undergraduate Final Year Project Award, in 2014, the IEEE ISSCC 2018 Student Travel Grant Award, and the IEEE SSCS Predoctoral Achievement Award, from 2018 to 2019.

NAI SHYAN LAI received the B.Eng. degree (Hons.) in electrical engineering and the Ph.D. degree in silicon-based nano-electronics and radiation detectors from the University of New South Wales, in 2007 and 2012, respectively. He is currently an Associate Professor with the School of Engineering, Asia Pacific University of Technology & Innovation, working in the area of micro- and nano-electronics. Since 2009, he has published most of his research work in IEEE TRANSACTIONS, *American Institute of Physics*, *American Physical Society*, and *Nature* journals. His research interests include semiconductor micro- and nano-fabrication, quantum dot devices, cryogenic temperature measurements, single electron transistors, quantum computation, and silicon microdosimeters.

PUI-IN MAK (Fellow, IEEE) received the Ph.D. degree from the University of Macau (UM), Macau, China, in 2006.

He is currently a Full Professor with the UM Faculty of Science and Technology, ECE Department, and the Associate Director (Research) of the UM Institute of Microelectronics and the State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests include analog and radio-frequency (RF) circuits and systems for wireless and multidisciplinary innovations.

Prof. Mak has been a fellow of U.K. Institution of Engineering and Technology (IET) for contributions to engineering research, education, and services, since 2018; a fellow of IEEE for contributions to radio-frequency and analog circuits, since 2019; and a fellow of U.K. Royal Society of Chemistry, since 2020. His involvements with IEEE are: a Member of Board-of-Governors of the IEEE Circuits and Systems Society, from 2009 to 2011; an Editorial Board Member of IEEE Press, from 2014 to 2016; a Senior Editor of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, from 2014 to 2015; an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUIT, in 2018, IEEE SOLID-STATE CIRCUITS LETTERS, in 2017, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, from 2010 to 2011 and from 2014 to 2015, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, from 2010 to 2013. He (co)-received the 2005 DAC/ISSCC Student Paper Award, the 2010 CASS Outstanding Young Author Award, the 2011 National Scientific and Technological Progress Award, 2015 the A-SSCC Distinguished Design Award, and the 2016 ISSCC Silkroad Award. In 2005, he was decorated with the Honorary Title of Value for scientific merits by Macau Government. He is/was the TPC Vice Co-Chair of ASP-DAC, in 2016; and a TPC Member of A-SSCC, from 2013 to 2016 and in 2019, ESSCIRC, from 2016 to 2017, and ISSCC, from 2017 to 2019. He was the Chairperson of the Distinguished Lecturer Program of the IEEE Circuits and Systems Society, from 2018 to 2019. He was a Best Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, from 2012 to 2013. He is/was a Distinguished Lecturer of the IEEE Circuits and Systems Society, from 2014 to 2015, and the IEEE Solid-State Circuits Society, from 2017 to 2018. He has been inducted as an Overseas Expert of the Chinese Academy of Sciences, since 2018.



RUI P. MARTINS (Life Fellow, IEEE) was born in April 1957. He received the bachelor's, Master's, and Ph.D. degrees, and the Habilitation degree in electrical engineering and computers from the Department of Electrical and Computer Engineering (DECE), Instituto Superior Técnico (IST), University of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He was a Full Professor of electrical engineering and computers with DECE, IST, University of Lisbon. He has been with DECE/IST, University of Lisbon, since October 1980. Since 1992, he has been on leave from the University of Lisbon and with DECE, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor, since August 2013. In FST, he was the Dean of the Faculty, from 1994 to 1997, and has been the Vice-Rector of UM, since 1997. From September 2008 to August 2018, he was the Vice-Rector (Research) and from September 2018 to August 2023, he was the Vice-Rector (Global Affairs). He was the Founding Chair of UMTEC (UM company), from January 2009 to March 2019, supporting the incubation and creation of Digifluidic, in 2018, the first UM Spin-Off, whose CEO is a SKLAB Ph.D. graduate. He was the Co-Founder of Chipidea Microelectronics (Macau) [now Synopsys-Macau], in 2001 and 2002. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 47 theses, Ph.D. (26), and masters (21). He has co-authored: seven books and 11 book chapters; 36 patents, USA (32), Taiwan (three), and China (one); 537 papers, in scientific journals (217) and conference proceedings (320); and other 64 academic works, in a total of 655 publications. He created 2003 the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in January 2011 to the State Key Laboratory (SKLAB) of China (the 1st in Engineering in Macau), being the Founding Director.

Prof. Martins was a member of the IEEE CASS Fellow Evaluation Committee, in 2013, 2014, and 2018. He received the Two Macao Government decorations: the Medal of Professional Merit (Portuguese-1999) and the Honorary Title of Value (Chinese-2001). He was the Founding Chair of the IEEE Macau Section, from 2003 to 2005, and the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM), from 2005 to 2008 [2009 World Chapter of the Year of the IEEE CAS Society (CASS)], the General Chair of the IEEE Asia-Pacific Conference on CAS–APCCAS'2008, the Vice-President (VP) Region Ten (Asia, Australia, and Pacific), from 2009 to 2011, and the VP-World Regional Activities and Membership of IEEE CASS, from 2012 to 2013, an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, from 2010 to 2013, nominated a Best Associate Editor, from 2012 to 2013. He was the Chair, in 2019; the IEEE Nominating Committee of Division I Director of CASS/EDS/SSCS, in 2014; and the IEEE CASS Nominations Committee, from 2016 to 2017. Plus, he was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference–ASP-DAC'2016, receiving the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award, in 2016. From 2005 to 2014, he was also the Vice-President and the President of the Association of Portuguese Speaking Universities (AULP), from 2014 to 2017. In July 2010, he was elected, unanimously, as a Corresponding Member of Lisbon Academy of Sciences, being the only Portuguese Academician working and living in Asia.