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RESEARCH ARTICLE

Comparative Study of the Normalized-Error-Based Control and Traditional Current-Mode Control for a Sixth-Order Boost Converter

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ABSTRACT Current-mode control is a commonly utilized control strategy for the step-up power converters because these converters' control-to-output transfer function contains right-half plane zeros. The main concern associated with the recent dual-loop current-mode controller (CMC) is that the integrator operates on the error term itself. Thus, integrand can assume extremely large values when error is large such as during transient response, and the controller output may saturate, especially when sufficiently large controller gains are used. If lower gain values of gains are used, the speed of response in the presence of small parameter variations could be much lower. Thus, there is a compromise between the transient response when error signal is large and speed of the response for small error signals. To address these concerns, an improved normalized-error based current-mode controller (NECC) is employed for voltage regulation in a sixth-order boost configuration. This controller's main characteristic is that the integrator now operates on a bounded integrand which is a normalized-error. This avoids the integrator saturation and also increase the room for tuning the controller gains. The state-space averaged model of the topology is given and a detailed stability analysis is shown. The main contribution of the paper is that a detailed comparative study of the traditional CMC and an improved NECC based on some simulation and experimental waveforms is provided. Both simulation and experimental outcomes clearly prove the superiority of the proposed NECC in terms of an improved speed and less overshoot of the output voltage response.

INDEX TERMS High-order boost converter, current-mode control, normalized-error.

I. INTRODUCTION

The boost-type power converters are needed in fields such as renewable energy systems, electric vehicles, etc. [1], [2], [3], [4], [5]. For instance, interest in renewable energy resources in general has surged due to recent increases in the cost of fossil fuels and new regulations aimed at reducing CO2 emissions. Thus, leading renewable energy technologies that are attracting a lot of attention include fuel cells and photovoltaics (PVs). However, an output of a PV module fluctuates due to sunlight, much as a voltage of a fuel cell normally fluctuates by a ratio around 2:1. Therefore, these renewable energy methods require a regulated dc–dc converter due to their low variable voltage [4].

The traditional boost converter which is of the second order is most common alternative. But the main issue associated with this orthodox boost converter is that its gain is low because of parasitic components of its passive components [6]. Due to practical limitations, a conventional boost converter's output voltage can only be around six times its supplied voltage [7]. Thus, in order to achieve a high gain, several isolated as well as non-isolated topologies are used recently [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26].

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However, using a transformer to build a topology would result in an increased size and expense of the converter if the application did not need isolation. It would also lead to increased losses. To address this concern, a high-order step-up dc-dc system is a suitable option to achieve large gain at a lower duty ratio. Thus, numerous topologies of such high-order transformer-less converters are presented in literature [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]. Initially the topologies with multiple active switches were used. For instance, the cascade converter used in [15] is capable of providing a high voltage while maintaining a high efficiency. But, the primary drawback of this system is its increased cost and complexity due to the use of two dc-dc converters having multiple active switches. Several power switches in the cascade converter not only led to more complexity of implementation as they need to be synchronized but also makes the analysis tedious. This makes topologies with a single active switch a preferred choice. Some of these higher order topologies with a single active switch include the multilevel boost converters of [23], the hybrid boost converter of [24], converters with a voltage multiplier cell of [12], the quadratic boost converters of [25], and Luo converter discussed in [11] to name a few.

Among these, the sixth-order high step-up converter of [7] is an attractive solution. This configuration employs a switched-capacitor approach, offer a large gain without employing a large switching duty cycle and permit the usage of a reduced voltage and resistance semiconductor switch in order to decrease costs as well as on-state losses.

Despite such several advantages offered by this high-order dc-dc converter, there is a scarcity of work on its control. First, since it is a boost-type dc-dc converter, its open-loop transfer function (ratio of output voltage vs duty ratio) is of non-minimum phase in nature. This does not allow the designer to implement its control by simply employing voltage feedback. This is due to the fact that if an open-loop transfer function has right-half s-plane zeroes, the resulting closed-loop transfer function would be unstable as open-loop zeroes often reflect in closed-loop poles.

To solve this issue, a CMC can be employed which can provide stability to the system. Some of the recent works on the current-mode control for the high-order power converters include a dual-loop controller for the Luo converter discussed in [17], a two-loop control system for the boost converter with a voltage multiplier cell in [18], and a linear multiloop control of quasi-resonant converters of [19]. In these schemes, a two-loop regulation method is employed in which an inner-loop is based on current feedback and the reference for this is provided by an outer voltage loop based on output voltage feedback. Apart from this, some dual-loop sliding-mode controllers to achieve the voltage regulation in the boost converters are also implemented in the past. For example, in [20] and [22], a constant-frequency PWM-based sliding-mode current controllers are presented for the Cuk converter and quadratic boost converter respectively. The hysteresis-based implementation of this dual-loop sliding-mode control for the quadratic boost converter is addressed in [21]. Even though there has been a considerable amount of work on such indirect control of high-order power topologies, a few issues still need to be resolved to improve the overall quality of a transient response.

Most of the current-mode (CM) and other dual-loop controllers discussed so far for the high-gain topologies use an error signal itself as an integrand. The drawback of this is that when error is large for an initial transient, if a larger integral gain is also employed, the overshoot in the response could increase. The control signal may saturate too. If a saturation block is used to overcome this issue, the control action could be lost and a system starts behaving as an open loop. If a small value of integral gain is used, the speed of the output response becomes lower when parameter variations such as load and input changes are introduced. Because there is a compromise among the overshoot and speed of the responses, tuning the controller gains is therefore a not an easy issue.

In this article, an improved normalized-error based CM control (NECC) scheme for the sixth-order boost-type topology is proposed. The main attribute of the NECC controller is that the integral action operates on an error signal which is normalized and always limited by a user defined constant value. Thus, even in the presence of large errors, integrand does not take very large values which can provide more room for selection of controller gain while avoiding the saturation too. The averaged model of the system is shown and its steady-state values are defined. Also, the thorough stability study of the converter based on the proposed NECC is demonstrated. The main contributions of the paper are: i) the significance of structure and a detailed stability analysis of the normalized-error based CM control for the sixth-order boost converter is shown and ii) a thorough transient performance comparative study of the traditional CM control scheme and an improved normalized-error based control scheme is presented to underline the advantages offered by the later. Notably, this study is provided using both simulation and experimental results.

The article is organized as given. Section II addresses the modeling and steady-state analysis of the system. In section III, the structure of the NECC controller is presented along with the comprehensive stability study of the closed-loop system. In section IV and V, a comparative study involving two controllers is presented using simulation and experimental set-ups respectively. Lastly, section VI is a conclusion.

II. MODELING OF THE SIXTH-ORDER BOOST CONVERTER

The sixth-order dc-dc converter circuit with parasitic resistances is depicted in Fig. 1. The expressions of the component stress values of this topology can be found in [7]. In this Fig 1, E is the input voltage, and R is the load resistance. Also, the two inductors are L_1 and L_2 and capacitors are denoted by C_1, C_2 and C_o respectively. The parasitic resistances values of these capacitors are given by r_C, r_{C_1}, r_{C_2} resp. For initial

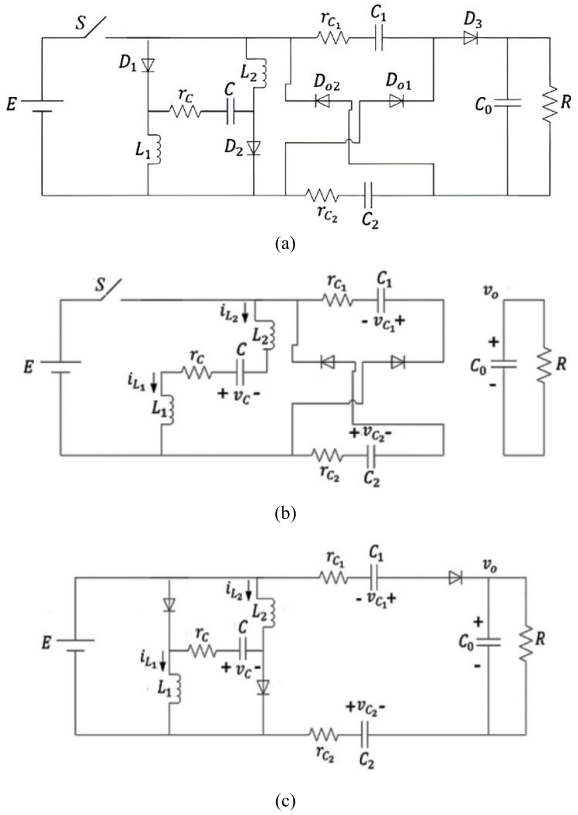

FIGURE 1. Sixth-order power converter: (a) Converter Schematic; (b) semiconductor switch if off state; (c) semiconductor switch if on state.

analysis, the general symbols are used in this section to obtain the model and show the stability analysis. Later, the exact values of these parameters are used for simulation purposes and these values are given in section V. The working of its circuit can be dealt in two phases, "Stage 1" occurs if switch "S" is off state (see Fig. 1(b)) and "Stage 2" occurs when "S" is on state (see Fig. 1(c)), given that the configuration is functioning in continuous mode of conduction.

For simplicity two inductors L_1 and L_2 in the circuit are assumed to be of the same value. Similarly, $C_1 = C_2$ and $r_{C_1} = r_{C_2}$ was used. This allows the dynamics of two currents flowing through L_1 and L_2 to be represented by the same equation. Also, the dynamics of voltages across C_1 and C_2 can be depicted by a single equation. When switch 'S' is turned off (see Fig.1(b)), the differential equations representing this phase of operation are given by:

$$\left(\frac{dx_1}{dt}\right)_{ON} = \frac{r_C + r_{C_1}/2}{2L_1}x_1 + \frac{1}{2L_1}x_2 - \frac{1}{2L_1}x_3 \tag{1a}$$

$$\left(\frac{dx_2}{dt}\right)_{ON} = -\frac{1}{C}x_1 \tag{1b}$$

$$\left(\frac{dx_3}{dt}\right)_{ON} = \frac{1}{2C_1}x_1 \tag{1c}$$

$$\left(\frac{dx_4}{dt}\right)_{ON} = -\frac{1}{RC_o}x_4 \tag{1d}$$

where $x_1 = i_{L_1}$ is inductor L_1's current, and x_2, x_3, and x_4 are the voltages across capacitors C, C_1, and C_o respectively.

Similarly, when switch 'S' is ON, we get,

$$\left(\frac{dx_1}{dt}\right)_{OFF} = \frac{1}{L_1}V_{in} \tag{2a}$$

$$\left(\frac{dx_2}{dt}\right)_{OFF} = -\frac{1}{r_C C}x_2 + \frac{1}{r_C C}V_{in} \tag{2b}$$

$$\left(\frac{dx_3}{dt}\right)_{OFF} = -\frac{1}{r_C C_1}x_3 + \frac{1}{2r_{C_1}C_1}x_4 - \frac{1}{2r_{C_1}C_1}V_{in} \tag{2c}$$

$$\left(\frac{dx_4}{dt}\right)_{OFF} = -\frac{1}{r_{C_1}C_o}x_3 - \left(\frac{1}{RC_o} + \frac{1}{2r_{C_1}C_o}\right)x_4 + \frac{1}{2r_{C_1}C_o}V_{in} \tag{2d}$$

where $V_{in} = E$ is the supply voltage. We can also assume that $\gamma = r_C + r_{C_1}/2$ for simplicity.

The following averaged state-space model is obtained using (1) and (2).

$$\frac{dx_1}{dt} = \left(\frac{r_C + r_{C_1}/2}{2L_1}x_1 + \frac{1}{2L_1}x_2 - \frac{1}{2L_1}x_3\right)d + \frac{1}{L_1}V_{in}\,(1-\mathrm{d}) \tag{3a}$$

$$\frac{dx_2}{dt} = -\left(\frac{1}{C}x_1\right)d - \left(\frac{1}{r_C C}x_2 + \frac{1}{r_C C}V_{in}\right)(1-\mathrm{d}) \tag{3b}$$

$$\frac{dx_3}{dt} = \left(\frac{1}{2C_1}x_1\right)d - \left(\frac{1}{r_C C_1}x_3 + \frac{1}{2r_{C_1}C_1}x_4 - \frac{1}{2r_{C_1}C_1}V_{in}\right)(1-\mathrm{d}) \tag{3c}$$

$$\frac{dx_4}{dt} = -\left(\frac{1}{RC_o}x_4\right)d - \left(\frac{1}{r_{C_1}C_o}x_3 - \left(\frac{1}{RC_o} + \frac{1}{2r_{C_1}C_o}\right)x_4 + \frac{1}{2r_{C_1}C_o}V_{in}\right)(1-\mathrm{d}) \tag{3d}$$

Here, d is a control signal provided dϵ(0, 1) and d$'$= 1 − d. The following equilibrium values can be achieved by keeping (3) to zero.

$$X_1 = \frac{2V_{in}D\,(D+3)}{(1\text{-}D)\left(-RD^2 + RD + 4r_C + 2r_{C_1}\right)},$$

$$X_2 = \frac{V_{in}\left(2r_{C_1} - 2r_c + RD - 2r_cD - RD^2\right)}{\left(-RD^2 + RD + 4r_C + 2r_{C_1}\right)},$$

$$X_3 = \frac{V_{in}\left(2r_{C_1} - 2r_c + RD + r_{C_1}D + RU^2\right)}{\left(-RD^2 + RD + 4r_C + 2r_{C_1}\right)},$$

$$X_4 = \frac{V_{in}RD\,(D+3)}{\left(-RD^2 + RD + 4r_C + 2r_{C_1}\right)} \tag{4}$$

Here, D, X_1, X_2, X_3 and X_4 are nominal values of d, x_1, x_2, x_3 and x_4 respectively.

If we assume $\frac{r_C}{R} \approx 0$ and $\frac{r_{C_1}}{R} \approx 0$, simplified values can be obtained. Therefore, using (4), the approximation of D is:

$$D_a = \frac{V_{ref} - 3V_{in}}{V_{ref} + V_{in}} \tag{5}$$

Here, V_{ref} is the required output reference voltage. Substituting (5) in (4) and assuming $\frac{r_C}{R} \approx 0$ and $\frac{r_{C_1}}{R} \approx 0$ we get:

$$X_{1a} = \frac{V_{ref}(V_{ref} + V_{in})}{2RV_{in}}, X_{2a} = V_{in}, \; X_{3a} = \frac{V_{ref} - V_{in}}{2} \quad (6)$$

where X_{1a} is the approximate value of X_1, X_{2a} is the approximation of X_2 and X_{3a} is the approximations of X_3.

III. DESIGN OF NORMALIZED-ERROR-BASED CURRENT-MODE CONTROL

The strategy of a normalized-error based CM control (NECC) for a given converter topology is covered in this section. To appreciate the significance of this controller, the form of the standard CM control (CMC) for the high-order topology is stated below [27]:

$$d = D_a - M_{Pt}\,(x_1 - X_{1a}) - M_{It}\int_0^t \left(x_4(\tau) - V_{ref}\right) d\tau \quad (7)$$

The system's error actually is the integrand in (7), which is the component on which the integrator functions. This integrand can assume extremely large values such as during transient response, and the controller output may saturate, especially when sufficiently large gain of integration is utilized. For lower control gain values, when there are fluctuations in the load resistance and supply of the converter, the speed of response while reaching the desired reference could be much lower. Thus, we get a tradeoff between the controller response for higher error values and the transient response for changes in system parameters.

Therefore, a NECC is suggested in order to overcome these drawbacks of the conventional CMC. Adaptive control, as covered in [28], uses adaptive rules with normalization. This enhanced controller scheme's form is shown below:

$$d = D_a - M_P\left(x_1 - \hat{X}_{1a}\right) \quad (8)$$

where

$$\hat{X}_{1a} = \frac{V_{ref}\left(V_{ref} + V_{in}\right)}{2\hat{R}_a V_{in}} = \frac{V_{ref}\left(V_{ref} + V_{in}\right)}{2V_{in}}\hat{\vartheta} \quad (9)$$

where $\hat{\vartheta} = 1\Big/\hat{R}_a$. Here, $\hat{R}_a$ is the approximate value of R.

In (9), $\hat{\vartheta}$ is described by:

$$\frac{d\hat{\vartheta}}{dt} = -\frac{2\mu d_m r_4}{1 + \mu^2 r_4^2} \quad (10)$$

Here, r_4 which is equal to $x_4 - V_{ref}$ and two gains μ as well as d_m are fixed values to be tuned by a user. It is worth noting that the integrand $\hat{\vartheta}$ is now based on a normalized value of the error signal. This term is bounded by d_m as shown below. Let,

$$n = -\frac{2\mu d_m r_4}{1 + \mu^2 r_4^2} \quad (11)$$

then

$$\frac{dn}{de_4} = -\frac{2\mu d_m(1 - \mu^2 r_4^2)}{(1 + \mu^2 r_4^2)^2} \quad (12)$$

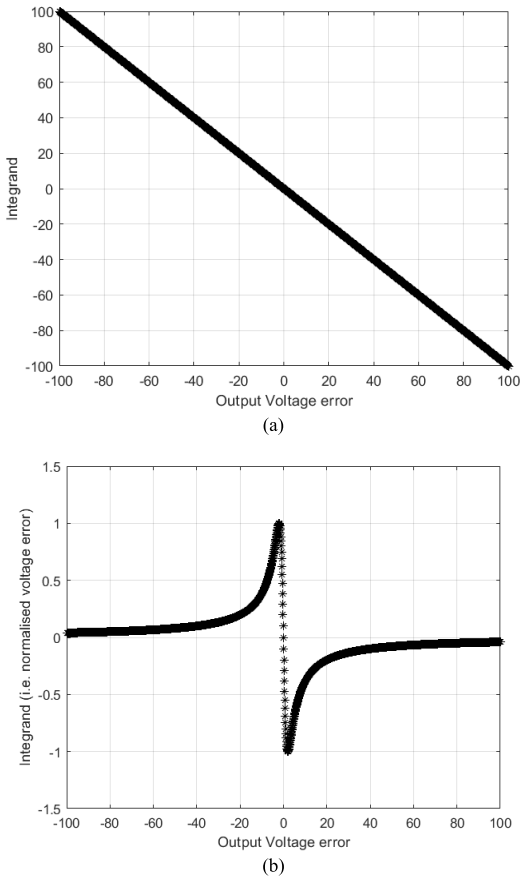

FIGURE 2. Integrand vs error: (a) for the standard CM control (CMC); (b) for the proposed normalized-error current-mode controller (NECC) using $\mu = 0.5$ and $d_m = 1$.

Equating (12) to zero leads to $r_4 = \pm\frac{1}{\mu}$ and putting it in (12) gives $\frac{d\hat{\vartheta}}{dt} = \pm d_m$. Hence, $|\frac{d\hat{\vartheta}}{dt}| \leq d_m$ for all t.

Fig. 2 below shows the graph of integrand vs. error for both the standard CM control of (7) and the proposed NECC of (8) – (10). For (7), the integrand is the error itself and thus, its value is very large when error becomes very large. However, the integrand of the proposed controller is bounded by d_m.

Remark: The overall structure of the proposed controller is given by (8) – (10). It is worth mentioning that eq. (8) and (10) are generic and can be readily applied to other topologies of the recent high-order dc-dc converters such as those used in [29], [30], and [31]. For Eq. (9), it is based on the expression of the steady state inductor current of the dc-dc converter. Thus, for any type of the dc-dc converter, if the expression of the steady-state inductor current is known, the control law can be obtained by replacing the load resistance term by its estimated value such that $\hat{\vartheta} = 1\Big/\hat{R}_a$ and this estimation is in turn calculated using (10).

IV. STABILITY ANALYSIS

Assuming $\frac{r_C}{R} \approx 0$, $\frac{r_{C_1}}{R} \approx 0$ and $R_a \approx R$, a stability study is accomplished to learn more about the CM controlled adaptive

system. The below error terms are used:

$$j_1 = x_1 - X_1, j_2 = x_2 - X_2, j_3 = x_3 - X_3,\ j_4 = x_4 - V_{ref},$$
$$\tilde{\vartheta} = \hat{\vartheta} - \vartheta \tag{13}$$

Now, putting (13), (8) and (9) into (3) yields system dynamics as:

$$\frac{dj_1}{dt} \approx -\frac{\gamma\left(1\text{-}D_a + M_P j_1 - \sigma\tilde{\vartheta}\right)}{2L_1}(x_1) + \frac{1 - D_a + M_P j_1 - \sigma\tilde{\vartheta}}{2L_1}(x_2) - \frac{1 - D_a + M_P j_1 - \sigma\tilde{\vartheta}}{2L_1}(x_3) + \frac{D_a - M_P j_1 + \sigma\tilde{\vartheta}}{L_1}V_{in} \tag{14}$$

$$\frac{dj_2}{dt} \approx -\frac{1 - D_a + M_P j_1 - \sigma\tilde{\vartheta}}{C}(x_1) - \frac{D_a - M_P j_1 + \sigma\tilde{\vartheta}}{r_C C}(x_2) + \frac{D_a - M_P j_1 + \sigma\tilde{\theta}}{r_C C}V_{in} \tag{15}$$

$$\frac{dj_3}{dt} \approx \frac{1 - D_a + M_P j_1 - \sigma\tilde{\vartheta}}{2C_1}(x_1) - \frac{D_a - M_P j_1 + \sigma\tilde{\vartheta}}{r_{C_1} C_1}(x_3) + \frac{D_a - M_P j_1 + \sigma\tilde{\vartheta}}{2r_{C_1} C_1}(x_4) - \frac{D_a - M_P j_1 + \sigma\tilde{\vartheta}}{2r_{C_1} C_1}V_{in} \tag{16}$$

$$\frac{dj_4}{dt} \approx \frac{D_a - M_P j_1 + \sigma\tilde{\vartheta}}{r_{C_1} C_o}(x_3) - \frac{1}{C_o}\left(\frac{1}{R} + \frac{U_a - M_P j_1 + \sigma\tilde{\vartheta}}{2r_{C_1}}\right)(x_4) + \frac{U_a - M_P j_1 + \sigma\tilde{\vartheta}}{2r_{C_1} C_o}V_{in} \tag{17}$$

$$\frac{d\tilde{\vartheta}}{dt} = -\frac{2\mu d_m r_4}{1 + \mu^2 r_4^2} \tag{18}$$

where

$$\sigma = M_P \frac{V_{ref}\left(V_{ref} + V_{in}\right)}{2V_{in}} \tag{19}$$

The required equilibrium values of (14) – (18) is given by $\left(j_{1\infty}, j_{2\infty}, j_{3\infty}, j_{4\infty}, \tilde{\vartheta}_\infty\right) = (0, 0, 0, 0, 0)$. Given the challenge of demonstrating the NECC system's stability, a study utilizing the Lypunov indirect technique is conducted [32]. Linearizing of (14) – (18) about $\left(j_{1\infty}, j_{2\infty}, j_{3\infty}, j_{4\infty}, \tilde{\vartheta}_\infty\right)$ and leads to the linearized system given by:

$$\frac{dk}{dt} \approx Gk \tag{20}$$

where $k = [k_1\ k_2\ k_3\ k_4\ k_5]^T$, $k_1 = j_1 - j_{1\infty}$, $k_2 = j_2 - j_{2\infty}$, $k_3 = j_3 - j_{3\infty}$, $k_4 = j_4 - j_{4\infty}$, $k_5 = \tilde{\vartheta} - \tilde{\vartheta}_\infty$, and the matrix G is given below (see at the bottom of page):

The system (20) is stable only when eigen values for G, i.e., the roots of $p_5(s) = |sI - G| = 0$, where s is a Laplace variable, stay in the LHS of the s-plane. Therefore, given system variables the controller Considering high-order of $p_5(s)$, system stability is analyzed using root locus method [33]. This approach involves holding constant two control gains, such as μ and d_m, fixed and the remaining gain, i.e., K_p is changed till all pole cross the stable region of the s-plane. This is performed to find the values of M_P to ascertain the stability. To guarantee system stability, the ranges of additional controller parameters, such as μ and d_m, may be found using the same process. Let us take into consideration the circuit values provided by (21) as an example.

$$E = 3.3V, V_{ref} = 25V, L_1 = 1\ mH, L_2 = 1\ mH, C = 68\mu F,$$
$$C_1 = 68\mu F, C_2 = 68\mu F, C_0 = 68\mu F, R = 1k\Omega \tag{21}$$
$$r_C = r_{C_1} = r_{C_2} = 0.5\Omega \tag{22}$$

Fig. 3(a) depicts the varying roots $p_5(s)$ when $\mu = 0.25$, $d_m = 1$ and $0 \le M_p \le 5$. The variation of poles with increasing M_P is depicted by an arrow. Similarly, Fig. 3(b) illustrates the varying poles employing $\mu = 0.25$, $M_P = 2$ with $0 \le d_m \le 2$ and Fig. 3(c) displays the pole's plot when $d_m = 1$, $M_P = 2$ and $0 \le \mu \le 0.5$. It is evident that there are bounds to the values of M_P, μ, and d_m in order to maintain system stability. Then next section provides a thorough explanation of how changing controller gains affect the system's transient response. G, as shown in the equation at the bottom of the page.

V. CONTROLLER GAINS' IMPACT ON THE OUTPUT RESPONSE

Several simulations were done using MATLAB Simulink 2023b to examine the impact of the three control system's gains linked to the system's transient output response. This will assist the designer in determining the proper controller gain levels to produce the intended output curve. These simulation outcomes were obtained employing the identical values of converter parameters, as indicated by (21). Initially, a "small" M_p is selected while μ and d_m were fixed to

$$G = \begin{bmatrix} \frac{-\gamma(1\text{-}D_a) - \gamma M_p X_{1a} + M_p V_{Ca} - M_p X_{2a} - 2M_p V_{in}}{2L_1} & \frac{(1\text{-}D_a)}{2L_1} & -\frac{(1\text{-}D_a)}{2L_1} & 0 & \frac{\gamma\sigma X_{1a} - \sigma X_{2a} + \sigma X_{3a} + 2\sigma V_{in}}{2L_1} \\ \frac{-(1\text{-}D_a) r_C - M_p r_C X_{2a} + M_p X_{2a} - M_p V_{in}}{r_C C} & \frac{-D_a}{r_C C} & 0 & 0 & \frac{\sigma X_{1a} r_C - \sigma X_{2a} + \sigma V_{in}}{r_C C} \\ \frac{(1\text{-}D_a) r_{C_1} + M_p r_{C_1} X_{1a} + 2M_p X_{3a} - M_p V_d + M_p V_{in}}{2r_{C_1} C_1} & 0 & \frac{-D_a}{r_{C_1} C_1} & \frac{D_a}{2r_{C_1} C_1} & \frac{-\sigma I_{L_{1a}} r_{C_1} - 2\sigma X_{3a} + \sigma V_{ref} - \sigma V_{in}}{2r_{C_1} C_1} \\ \frac{-2M_p X_{3a} + M_p V_{ref} - M_p V_{in}}{2r_{C_1} C_o} & 0 & \frac{D_a}{r_{C_1} C_o} & \frac{-D_a}{2r_{C_1} C_o} - \frac{1}{RC_o} & \frac{2\sigma X_{3a} - \sigma V_{ref} + \sigma V_{in}}{2r_{C_1} C_o} \\ 0 & 0 & 0 & -2\mu d_m & 0 \end{bmatrix}$$

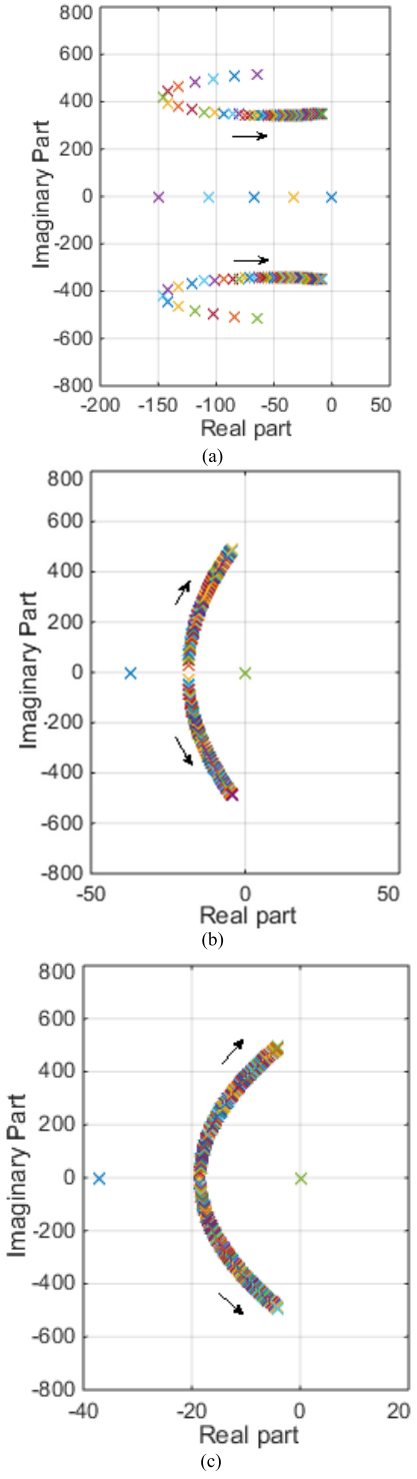

FIGURE 3. Closed loop poles when: (a) when μ is 0.25, d_m is 1 with $0 \leq M_p \leq 5$; (b) when μ is 0.25, M_p is 2 with $0 \leq d_m \leq 2$; (c) when d_m is 1, M_p is 2 with $0 \leq \mu \leq 0.5$.

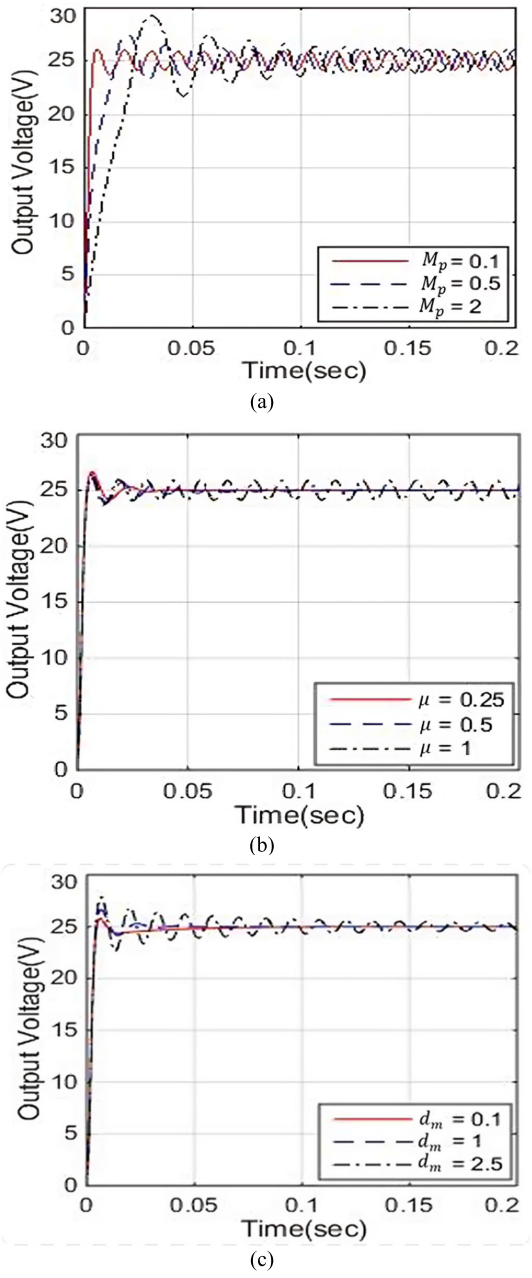

FIGURE 4. System load voltage response: (a) when μ is set to 1, d_m is set to 1 and changing M_p; (b) when M_{pa} is set to 0.1, d_m is set to 1 and changing μ; (c) when M_{pa} is 0.1, μ_a0.25 and changing d_m.

1. Then μ and d_m, are fixed while M_p is varied to fine tune its value to get the low overshoot and settling time. From Fig. 4(a), it is evident that there is an increase in the transient output response's overshoot and speed as M_p increases. In order to get a quick output response with the least amount of overshoot, the proper tiny value of M_p, say M_{pa}, is first selected. Next, in order to get a better response, μ is modified while M_{pa} and d_m remain fixed. As seen by Fig. 4(b), the response's oscillations grow in tandem with an increase in μ. In order to get a good response at steady-state having the fewest oscillations, another gain of the control scheme i.e. μ is adjusted to its ideal, let it be μ_a. After determining the correct values for M_{pa} and d_m, the quality of output curve is further enhanced by varying the gain d_m. The impact of the variable d_m on the converter's response is seen in Fig. 4(c).

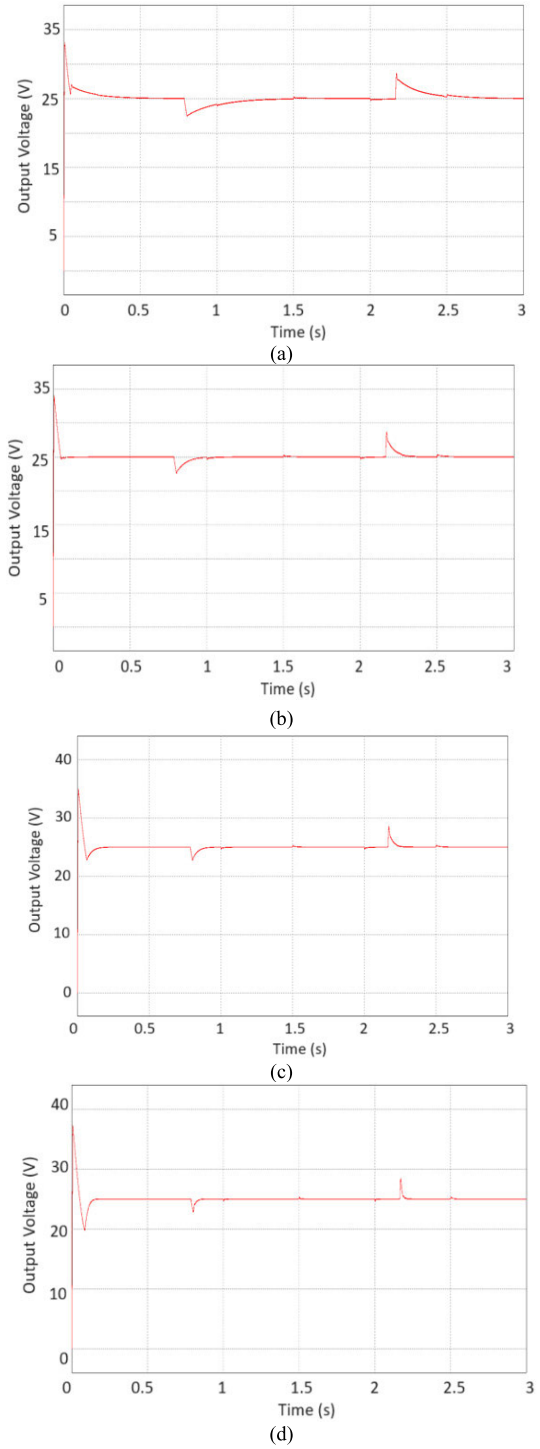

FIGURE 5. Transient and load change response ($1k\Omega$ to $0.66k\Omega$ and again changed to $1k\Omega$) using traditional CMC: (a) for $M_{Pt} = 0.1$ and $M_{It} = 1$; (b) for $M_{Pt} = 0.1$ and $M_{It} = 3$; (c) for $M_{Pt} = 0.1$ and $M_{It} = 5$; (d) for $M_{Pt} = 0.1$ and $M_{It} = 10$.

VI. SIMULATION COMPARATIVE STUDY OF THE TRADITIONAL AND NORMALIZED-ERROR-BASED CURRENT-MODE CONTROLLERS

In this section, a detailed comparative study of the traditional CMC and an improved NECC is illustrated. The converter values as used in (21) were employed to get the outcomes.

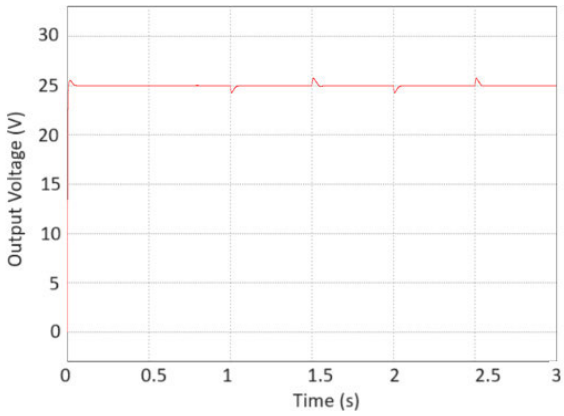

FIGURE 6. Transient and load change response ($1k\Omega$ to $0.66k\Omega$ and again to $1k\Omega$) using proposed NECC.

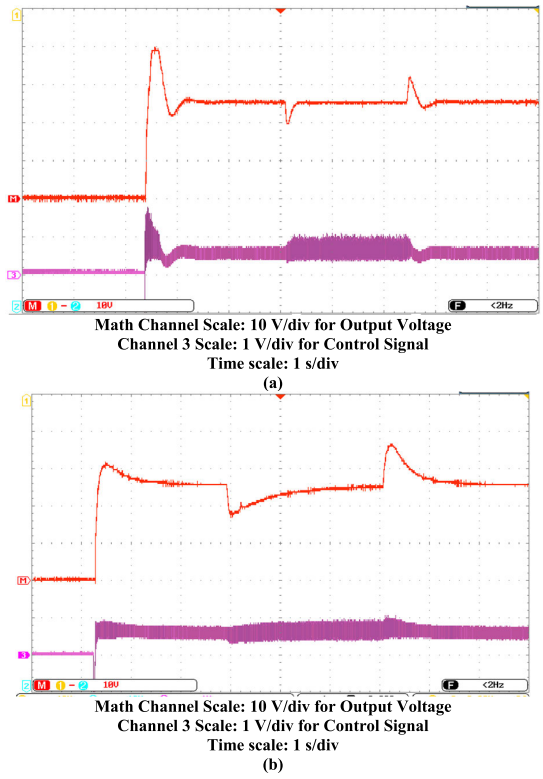

FIGURE 7. Experimental results obtained using typical orthodox CMC of (7) showing transient response from 0V to 25V and load change response when load was changed from 2kΩ to 667Ω obtained using $M_{Pt} = 2$ and: (a) $M_{It} = 5$; (b) $= M_{It} = 0.5$.

A. USING TRADITIONAL CMC

Initially, the traditional CMC given by (7) is applied to obtain the load-side voltage control of the sixth order step-up topology. Fig. 5 shows the output response obtained in PSIM for diverse range of control parameters. Both the transient response and load variation responses are shown and the consequence of changeable control parameters on the waveform is checked. The load is changed from $1k\Omega$ to $0.66k\Omega$ at t $\sim$ 0.75 s and then again to $1k\Omega$ at t $\sim$ 2.2s. Fig. 5(a) shows the load voltage curve obtained using $M_{Pt} = 0.1$ and $M_{It} = 1$. Evidently, the transient curve has an

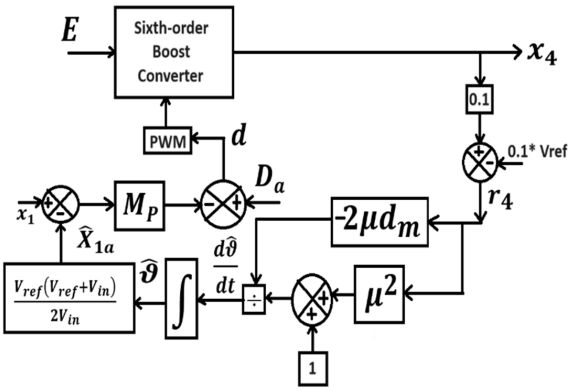

FIGURE 8. Block diagram of NECC controller implementation.

overshoot of ∼30% and load change curve has settling time of ∼500 msec. Similarly, Fig. 5(b-d) shows the load voltage curve using $M_{Pt} = 0.1$ and $M_{It} = 3$, $M_{It} = 5$ and $M_{It} = 10$ respectively. Evdiently, as the value of M_{It} increases, even though the speed of the load variation response improves, the overshoot in the transient response increases. Thus, a trade-off exists between an overall response's overshoot and speed.

B. USING PROPOSED NECC

Next, some simulation results based on improved NECC of the form (8) – (10) are given.

Fig. 6 depicts the output attained using the proposed NECC. Here, $M_P = 1.5$, $d_m = 1$ and $\mu = 1$ was employed. It can be seen that both low overshoot of the transient curve and high speed of the response when load was changed were achieved simultaneously.

VII. EXPERIMENTAL COMPARATIVE STUDY OF THE TRADITIONAL AND NORMALIZED-ERROR-BASED CURRENT-MODE CONTROLLERS

In this part, some experimental findings are shown to support the efficacy of the suggested NECC for the sixth-order converter. The typical CMC of the form (7) and the proposed NECC controller's performance are compared. The converter values used were:

$$E = 3.3V, V_d = 25V, L_1 = 1\ mH, L_2 = 1mH, C = 68\mu F,$$
$$C_1 = 68\mu F, C_2 = 68\ \mu F, C_0 = 68\mu F, R = 2k\Omega$$

A. USING ORTHODOX CMC

The sixth-order topology was initially controlled by the orthodox CMC (7). For realization of (7), a feedback gain of 0.1 was used for implementation. The response of the controller for different values of the controller gains was obtained.

Initially, the transient response of the system was obtained for higher integral gain and it is depicted in Fig. 7(a). The reference was moved from 0V to 25V followed by a change in the load from $2k\Omega$ to 667Ω. Fig. 7(a) was obtained using $M_{Pt} = 2$ and $M_{It} = 5$ and Fig. 7(b) shows the similar response obtained using $M_{Pt} = 2$ and $M_{It} = 0.5$. It is

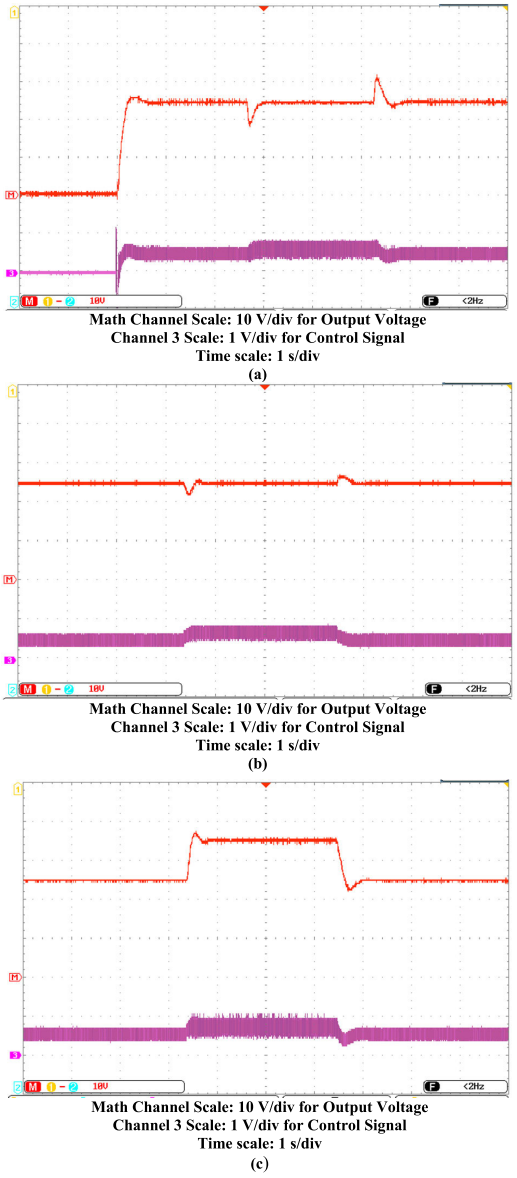

FIGURE 9. Experimental results using proposed NECC (a) Transient response from 0V to 25V and load change response when load was changed from 2kΩ to 667Ω; (b) Line change response when supply changed from 3.3V to 2.5V and again bought back to 3.3V; (c) Nominal voltage changed from 25V to 35V and bought back to 25V.

evident that the overshoot increased for higher integral gain values and later, speed of the response was affected when low integral gain was used. That is, when a typical CMC given by (7) is employed for regulation of the sixth-order converter, there was a compromise between the overshoot and speed of the response.

B. USING PROPOSED NECC

Next, an improved NECC was employed was used to achieve regulation in a sixth-order topology. The controller given by (8) – (10) was employed with a feedback gain of 0.1. Fig. 8 shows the block diagram of the controller implementation. Here, the gains used were: $M_P = 2$, $d_m = 1$ and $\mu = 1$.

TABLE 1. Comparative study of orthodox CMC and proposed NECC.

Parameter	Orthodox CMC with high integral gain =5	Orthodox CMC with low integral gain =0.5	Proposed NECC with normalized-error based integration
Overshoot of transient response for 0 V to 25 V change	15 V	5 V	2 V
Settling time of transient response for 0 V to 25 V change	0.8 s	1.2 s	0.4 s
Overshoot of load change response ($2k\Omega$ to 667Ω and vice-versa)	6 V	11 V	5 V
Settling time of load change response ($2k\Omega$ to 667Ω and vice-versa)	0.6 s	1.5 s	0.5 s

Initially, the transient response from 0V to 25V was obtained, followed by a load change curve when fluctuation in the resistance was from $2k\Omega$ to 667Ω. The response is depicted in Fig. 9(a). It is evident that, in contrast to Fig. 7, a nearly critically damped transient curve with little perceptible overshoot was achieved. Fig. 9(b) shows the output curve when input was changed from 3.3V to 2.5V and again bought back to 3.3V. Also, Fig. 9(c) represents response when nominal voltage changed from 25V to 35V and bought back to 25V. All these results show the improved performance of the proposed NECC as compared to the orthodox CMC. Table 1 below shows the detailed comparison of the transient response parameters when two different controllers are employed.

VIII. CONCLUSION

An improved normalized error-based CM control scheme for the sixth-order dc-dc power converter is presented. The drawbacks of the orthodox current-mode controller which occur due to the integrand being equal to the output voltage errors are shown theoretically as well as practically using some simulation and experimental results. These results validate that there is compromise between the quality of the initial transient response and load change response of the system when this controller is employed. The main feature of the proposed modified current-mode control is that it uses a normalized voltage error as its integrand. This not only offers theoretical advantages such as reduced risk of saturation during high voltage errors but also allows the usage of larger controller gains to achieve the fast load change response. The better performance of this proposed NECC is validated suing simulation and experimental results. Moreover, the stability of the closed-loop system based on the proposed control scheme is proved using the converter's state-space model. Lastly, it is also worth mentioning that the form of the presented NECC is nonspecific to the converter and it can be employed to other topologies of the dc-dc converters as well without any modification.

REFERENCES

[1] N. Subhani, Z. May, M. K. Alam, I. Khan, M. A. Hossain, and S. Mamun, "An improved non-isolated quadratic DC–DC boost converter with ultra high gain ability," *IEEE Access*, vol. 11, pp. 11350–11363, 2023.

[2] A. S. Valarmathy and M. Prabhakar, "High gain interleaved boost-derived DC–DC converters—A review on structural variations, gain extension mechanisms and applications," *e-Prime Adv. Electr. Eng., Electron. Energy*, vol. 8, Jun. 2024, Art. no. 100618, doi: 10.1016/j.prime.2024.100618.

[3] M. Adib and S. Mishra, "Modified high gain non-isolated boost DC–DC converter for electric vehicles," in *Proc. IEEE 3rd Int. Conf. Sustain. Energy Future Electric Transp. (SEFET)*, Aug. 2023.

[4] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[5] G. R. Walker and P. C. Sernia, "Cascaded DC–DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, Jan. 2004.

[6] H. Mahmood and K. Natarajan, "Parasitics and voltage collapse of the DC–DC boost converter," in *Proc. Can. Conf. Electr. Comput. Eng.*, May 2008, pp. 273–278.

[7] A. A. Fardoun and E. H. Ismail, "Ultra step-up DC–DC converter with reduced switch stress," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2025–2034, Sep. 2010.

[8] F. Jiang, P. Wang, Q. Deng, Z. Cheng, L. Tao, and X. Ma, "A novel DC–DC boost converter with high voltage conversion ratio and zero current ripple for fuel cell application," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Nashville, TN, USA, Oct. 2023.

[9] O. Balapanuru, M. M. Lokhande, and M. V. Aware, "Nonisolated integrated boost featured (NIIBF) multi-input ultrahigh gain DC–DC converter," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5682–5694, May 2024.

[10] J. Zeng, W. Qiao, and L. Qu, "A single-switch LCL-resonant isolated DC–DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 5496–5502.

[11] F.L. Luo, and H. Ye, *Advanced DC/DC Converters*. Boca Raton, FL, USA: CRC Press, 2003.

[12] M. Prudente, L. L. Pfitscher, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[13] C. Y. Chan, "Analysis and experimental study of an output feedback controller for a high-order boost DC–DC converter," *IET Power Electron.*, vol. 6, no. 7, pp. 1279–1287, Aug. 2013.

[14] J. C. Rosas-Caro, J. M. Ramirez, and P. M. Garcia-Vite, "Novel DC–DC multilevel boost converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 2146–2151.

[15] H. Matsuo and K. Harada, "The cascade connection of switching regators," *IEEE Trans. Ind. Appl.*, vol. IA-12, no. 2, pp. 192–198, Apr. 1976.

[16] H. Tarzamni, N. V. Kurdkandi, H. S. Gohari, M. Lehtonen, O. Husev, and F. Blaabjerg, "Ultra-high step-up DC–DC converters based on center-tapped inductors," *IEEE Access*, vol. 9, pp. 136373–136383, 2021.

[17] S. H. Chincholkar and C. Chan, "Comparative study of current-mode controllers for the positive output elementary luo converter via state-space and frequency response approaches," *IET Power Electron.*, vol. 8, no. 7, pp. 1137–1145, Jul. 2015.
[18] F. H. Dupont, C. Rech, R. Gules, and J. R. Pinheiro, "Reduced-order model and control approach for the boost converter with a voltage multiplier cell," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3395–3404, Jul. 2013.
[19] I. Cervantes, D. Garcia, and D. Noriega, "Linear multiloop control of quasi-resonant converters," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1194–1201, Sep. 2003.
[20] S.-C. Tan and Y. M. Lai, "Constant-frequency reduced-state sliding-mode current controller for Cuk converters," *IET Power Electron.*, vol. 1, no. 4, pp. 466–477, Dec. 2008.
[21] O. Lopez-Santos, L. Martinez-Salamero, G. Garcia, H. Valderrama-Blavi, and T. Sierra-Polanco, "Robust sliding-mode control design for a voltage regulated quadratic boost converter," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2313–2327, Apr. 2015.
[22] S. H. Chincholkar, W. Jiang, and C.-Y. Chan, "An improved PWM-based sliding-mode controller for a DC–DC cascade boost converter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1639–1643, Nov. 2018.
[23] J. C. Mayo-Maldonado, R. Salas-Cabrera, J. C. Rosas-Caro, J. De Leon-Morales and E. N. Salas-Cabrera, "Modelling and control of a DC–DC multilevel boost converter," *IET Power Electron.*, vol. 4, no. 6, pp. 693–700, Jul. 2011.
[24] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-Inductor structures for getting transformerless hybrid DC–DC PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.
[25] J. A. Morales-Saldaña, R. Loera-Palomo, E. Palacios-Hernández, and J. L. Gonzalez-Martinez, "Modelling and control of a DC–DC quadratic boost converter with R2P2," *IET Power Electron.*, vol. 7, no. 1, pp. 11–22, Jan. 2014.
[26] S. Chincholkar, M. Tariq, and S. Urooj, "Large-signal stability of the quadratic boost converter using a disturbance observer-based sliding-mode control," *Mathematics*, vol. 11, no. 18, p. 3945, Sep. 2023.
[27] S. H. Chincholkar and C. Chan, "Investigation of current-mode controlled cascade boost converter systems: Dynamics and stability issues," *IET Power Electron.*, vol. 9, no. 5, pp. 911–920, Apr. 2016.
[28] P.A. Ioannou, and J. Sun, *Robust Adaptive Control*. Belmont, NJ, USA: Prentice-Hall, 1996.
[29] M. Appikonda and D. Kaliaperumal, "Design of double-integral sliding-mode controller for fourth-order double input DC–DC boost converter with a voltage multiplier cell," *Int. J. Electron.*, vol. 111, no. 1, pp. 42–63, Jan. 2024.
[30] V. K. Gupta, G. Verma, and B. C. Mandi, "Design and implementation of quadratic boost converter for low power applications," in *Proc. 3rd Int. Conf. Power, Control Comput. Technol. (ICPC2T)*, Raipur, India, Jan. 2024, pp. 415–420.
[31] J. C. Rosas-Caro, J. E. Valdez-Resendiz, G. Escobar, and F. Beltran-Carbajal, "Multilevel boost converter with reduced inductor current," *Electronics*, vol. 12, no. 22, pp. 1279–1287, 2023.
[32] H. Khalil, *Nonlinear Systems*. Upper Saddle River, NJ, USA, Pearson, 2000.
[33] K. Ogata, *Modern Control Engineering*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1997.

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