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RESEARCH ARTICLE

Real-Time Implementation of a New Modified 3DSVPWM Control Method for Eliminating Zero-Sequence Circulating Current in Parallel Three-Phase Four-Leg Source Voltage Inverters

ALA ADDIN MOHAMMED AL-DWA[1], ALI CHEBABHI[1], DJAMAL ZIANE[2], SAID BARKAT[1], SYPHAX IHAMMOUCHEN[3], TOUFIK REKIOUA[3], HABIB BENBOUHENNI[4], AND AYMAN ALHEJJI[5]

[1]Electrical Engineering Laboratory, Faculty of Technology, University of M'sila, M'sila 28000, Algeria
[2]IREENA Laboratory, University of Nantes, 44600 Saint-Nazaire, France
[3]Laboratoire de Technologie Industrielle et de l'Information (LTII), Université de Béjaïa, Béjaïa 06000, Algeria
[4]Department of Electrical and Electronics Engineering, Faculty of Engineering and Architecture, Nisantasi University, 34481742 Istanbul, Türkiye
[5]Department of Electrical Engineering, Yanbu Industrial College, Yanbu 46452, Saudi Arabia

Corresponding authors: Ali Chebabhi (ali.chebabhi@univ-msila.dz) and Ayman Alhejji (alhejjia@rcjy.edu.sa)

ABSTRACT Due to its good reliability, high modularity, zero-sequence current (ZSC) path, and lower size and cost, the parallel four-leg source voltage inverter's topology is a perfect choice for many power applications, including renewable power generation-based stand-alone power-supply systems (SAPSSs). However, the major concern associated with this topology is the presence of a zero-sequence circulating current (ZSCC) that circulates between the phase legs of these inverters when the inverters operate under unbalanced current sharing or unbalanced output-filter parameters, which leads to multiple consequences, including output current distortion, power losses, and system stability degradation, as well as impacting the efficiency, reliability, and operational lifespan of the system. The ZSCC model demonstrates that the ZSCC amplitude is linked to the filter inductance and difference between zero-sequence duty ratios or zero-sequence voltages (ZSVs). Considering these facts, we propose a new modified three-dimensional space vector pulse width modulation (3DSVPWM) methodology to suppress ZSCC and its effects on the current quality, efficiency, reliability, and operational lifespan of the parallel system. The suggested strategy aims to eliminate the difference between ZSVs by adjusting the zero-vector duty ratios in each switching period. This adjustment keeps the ZSCC constant at zero with minimal oscillations and switching losses, thereby improving the output current quality, particularly in mitigating the 3rd harmonic and its multiples, and enhancing the system's efficiency, reliability, and operational lifespan. The proposed method offers the advantages of being suitable for suppressing both the ZSCC and ZSC and not impacting the control purposes or the system's output quality. The efficiency and performance of the designed method are validated through various Hardware-in-the-loop (HIL) tests under different conditions using the OPAL-RT-OP5700 real-time simulator.

INDEX TERMS Parallel four-leg source voltage inverter, stand-alone power-supply systems, zero-sequence current, modified three-dimensional space vector pulse width modulation, OPAL-RT-OP5700 real-time simulator.

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I. INTRODUCTION

Three-phase three-leg pulse width modulation (PWM) converters have been widely used in many industrial energy

applications, such as renewable energy (RE) generation-based grid-connected energy distribution systems or stand-alone power-supply systems (SAPSSs) [1]. A high-efficiency device is also considered for such power systems due to its lower current total harmonic distortions (THDs), superior current quality waveforms, and bidirectional power flow [2]. However, nonlinear and unbalanced loading conditions, such as unbalanced single-phase nonlinear loads, are deterministic situations that occur frequently in all power applications, which makes the classical 3-leg PWM converter a non-ideal option [3], [4]. Therefore, the use of 4-leg PWM inverters as energy conversion systems or as SAPSSs is highly recommended. These topologies are suitable for preserving balanced sinusoidal grid currents and voltages under all loading and grid conditions, including unbalanced and other disturbances. So, compared to the split-bus 3-leg 4-wire inverter in which the fourth wire (neutral line) is connected to the midpoint of the DC-bus capacitors, the 4-leg PWM inverter is an advantageous 4-wire inverter and a better choice for perfectly supporting all unbalanced loads. In this topology, not only the capacitor number but also the capacitance value is reduced, and the degree of freedom is enhanced [5], [6]. Furthermore, this approach reduces the DC-bus voltage and increases the output voltage by approximately 15% with a lower volume and weight than those of the split-link 3-leg 4-wire inverter [7], [8]. In addition, the 3-phase 4-leg PWM converter not only achieves the same functions as the classical 3-phase 3-leg PWM converter but also provides a zero-sequence current (ZSC) channel and preserves the ability to handle all unbalanced problems and regulation [9], [10]. However, in high-energy applications, such as distributed energy generation systems and EV charging stations, 4-leg PWM inverters cannot meet certain requirements, such as reliability, power capability, and modularity. To address these limitations, parallel PWM inverter configurations have become common in these types of applications due to their ability to increase system capacity, reduce the thermal stress and current rating limitations of power switches, and increase system stability and reliability [11], [12].

Unfortunately, a zero-sequence circulating current (ZSCC) flow path can be formed in this configuration due to the difference between the zero-sequence voltages (ZSVs) of the parallel inverters, which is generally attributed to mismatches in the inverter filter inductances, unbalanced output current sharing, or unequal switching frequency [13], [14]. The ZSCC is decomposed into high-frequency harmonic components (HFHCs) and low-FHCs (ZSCC-LFHCs). The ZSCC-LFHCs increase the inverter output current distortions due to the presence of LFHCs, especially the third harmonic and its multiples, causing the inverter filter inductances to exhibit abnormal noise and vibrations [15]. In addition, LFHCs increase the output voltage distortions and losses, decrease the system efficiency and reliability, increase electromagnetic interference (EMI), and increase the current stress of power switches [16].

To eliminate ZSCC, several solutions have been proposed in the literature. An inter-phase reactor-based varying impedance method was proposed in [17], which accurately reduced the ZSCC-HFHCs in parallel converters to a suitable level; however, this method was unable to suppress the ZSCC-LFHCs and required high cost and necessarily additional hardware circuits. Other efforts have proposed a series of special PWM techniques. In [18] and [19], a simple harmonic-elimination PWM (HEPWM) method was proposed for ZSCC reduction in parallel PWM inverters by reducing the magnitude of the triple harmonic components. In [20] and [21], a carrier phase shift PWM strategy (CPSPWM) for suppressing the ZSCC in modular interleaved converters was proposed. These methods effectively suppress all the harmonics of ZSCC at a high modulation index, but they cannot successfully suppress the ZSCC-LFHCs at a low modulation index, which degrades the quality of the output voltages and causes extra switching and power losses in high-power applications, impacting the efficiency and reliability of the parallel system, as well as its operational lifespan. Therefore, a series of SVPWM techniques have been suggested for realizing parallel 3-leg PWM converter-based grid connections with an active filter function and a SAPSS with a load voltage imbalance mitigation function. Some efforts include the use of 3-level SVPWM, while others use modified two-level SVPWM. For example, simple and discontinuous three-level SVPWM was suggested to minimize the ZSCC and current undulation [22], [23]. These strategies are used to control parallel PWM converters as if they were single 3-level PWM converters, which can minimize the ZSCC while providing high efficiency and output voltage quality; however, these strategies increase the computational complexity and difficulty of implementation. Additionally, these strategies are becoming increasingly difficult to implement for multiple PWM converters connected in parallel. However, prior efforts [24], [25], [26], [27], [28] proposed an adjusted two-level SVPWM based on the ZSCC-PI regulator to reduce the ZSCC-LFHCs, especially the third harmonic and its multiples; this strategy consists of adjusting or parameterizing the zero vector duty ratios of the SVPWM using a command variable generated by the ZSCC-PI technique. The notable advantages of this technique compared with the above-mentioned command strategies are as follows: (i) it provides a high impedance to the ZSCC-LFHCs and is easy to realize; (ii) it is suitable for multi-parallel PWM converters; (iii) it does not impact the control purposes or the output power quality of the parallel system; and it enhanced the efficiency and reliability of the parallel system, as well as its operational lifespan. However, in the aforementioned methods, the classical 3-leg PWM converter is considered the main device for the parallel system, which means that it cannot control or suppress the ZSCC in parallel 4-leg converters. In contrast to classical parallel 3-leg converters, which require the suppression of only the ZSCC, in parallel 4-leg converters, eliminating not only the ZSCC but also

the ZSC that appears in the fourth leg of each converter is necessary.

Despite these dynamics, there are a few studies on ZSCC suppression dedicated to parallel-connected 4-leg PWM converters. Parallel 4-leg converters with common DC and AC bus topologies are adopted for their ability to provide ZSC regulation and thus avoid voltage fluctuations at the point of common coupling (PCC). The average model of this topology and the equivalent models of the ZSCC were developed and analyzed in [29]. A modified sinusoidal PWM (modified SPWM) method in the dq0 reference frame was proposed in [30] for eliminating the ZSCC in a parallel two 4-leg inverter-based grid connected under unbalanced filter inductors by controlling only the neutral current of the fourth leg of the second inverter. In addition to the high switching power losses and lower DC voltage utilization, this method does not consider the control of the ZSCC, which impacts the performance of the ZSCC suppression and power quality of the output currents under unbalanced conditions such as unbalanced filter parameter and unequal current sharing.

In [31], a sinusoidal PWM with a feedforward control method based on the third harmonic injection in the abc reference frame was proposed to reduce the ZSCC-LFHCs and their impacts on the output currents of the parallel two 4-leg inverters based SAPSS. This method can overcome the output current distortions and effectively reduce the ZSCC-LFHCs under mismatched filter inductors, but it suffers mainly from lower DC voltage utilization and high switching power losses [2]. Furthermore, the task of controlling both the ZSC and ZSV of the parallel inverters using this approach is difficult, which is important in 4-wire systems as these components are not regarded as separate components in the abc reference frame [32].

An adjusting three-level three-dimensional space vector PWM technique was proposed for controlling parallel-connected three-level T-type 4-leg PWM converters in the dq0 reference frame [33]. This method offers effective suppression of both the ZSCC and output current harmonics and enables direct control of the ZSC and ZSV of each converter. Unfortunately, the approach cannot be applied to the parallel-connected two-level 4-leg topology.

An identical ZSV injection-based SPWM technique was proposed for parallel grid-connected two-level three-leg converters [34]. In [35], a modified SPWM based on ZSCC with a PI regulator was proposed for a parallel 4-leg two inverter system-based SAPSS by adjusting one of the two SPWM modulation voltages using the adjusting ZSV offered by the regulation of the ZSCC. The advantage of these techniques is that they are suitable for two-level converter topologies, 3-leg, and 4-leg converters, but they will provide a large ZSCC peak-to-peak value and high output current harmonics, and they also suffer from the SPWM technique issues. Moreover, the utilization of the SPWM technique in these techniques within the abc reference frame inherently limits the ability to directly control the ZSVs of the parallel inverters, resulting in a significant difference between these ZSVs. Thus, a large peak-to-peak value of ZSCC will occur, degrading the efficiency and reliability of the parallel 4-leg inverters.

In this context, this study develops an efficient ZSCC-LFHC and ZSC suppression method based on a modified 3DSVPWM for a parallel connected 4-leg PWM inverter system based SAPSS. The fundamental concept of the proposed technique is to eliminate both the ZSCC and ZSC by eliminating the difference between ZSVs through the adjustment of zero-vector duty ratios of the modified 3DSVPWM method in each switching period. For this purpose, the zero-vector duty ratios of the proposed modified 3DSVPWM method are parameterized by an adjusting variable obtained from the regulation of ZSCC to zero using a ZSCC-PI controller. The proposed modified 3DSVPWM technique offers multiple advantages, including adjustable zero-vector duty ratios for ZSCC suppression, avoiding their effects on the output current quality under unbalanced current sharing or with discrepancies in the output-filter parameters, easy and direct control of the ZSCs and ZSVs, suppressing the difference between the ZSVs, providing high impedance to the ZSCC-LFHCs. The suggested approach is suitable for multi-parallel 4-leg PWM converters, and does not impact the control purposes and the output quality of the parallel system or high input DC voltage utilization. Furthermore, it has the potential to enhance the efficiency, reliability, and operational lifespan of the parallel 4-leg inverter system by optimizing the utilization of power switching devices, minimizing unnecessary losses associated with ZSCC and switching devices, and reducing stress on power switching devices.

The remainder of this paper is organized as follows. Section II describes the basic topology of parallel 4-leg PWM inverters and explains how they can be used for RE generation as an SAPSS. Additionally, the mathematical model of the system in different frames with average equivalent circuits and the ZSCC mechanisms and characteristics are analyzed and presented in this section. The proposed ZSCC suppression technique based on the modified 3DSVPWM technique and ZSCC-PI control loop is described in detail in Section III. To clarify the validity and effectiveness of the suggested technique, comprehensive Hardware-in-the-loop (HIL) simulation (using OPAL-RT-OP5700 real-time simulator) results are shown in Section IV. Section V provides the main conclusions drawn from this work.

II. SYSTEM MODELING AND DESCRIPTION

A. MODELING OF THE PARALLEL SYSTEM

Two parallel connected 4-leg inverters-based SAPSSs are shown in Fig. 1.

The two inverters with common AC and DC buses are connected to a 3-phase load via an LC output filter. The LC filter is utilized to attenuate and avoid high-frequency switching undulations at the parallel system output currents and voltages. For convenience and simplicity, the common

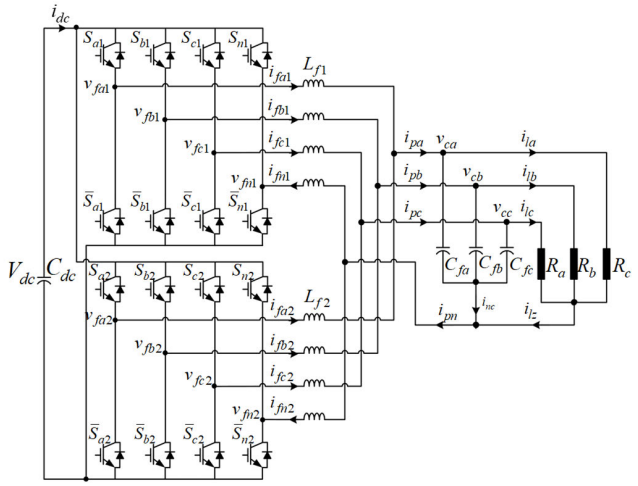

FIGURE 1. Two parallel 4-leg inverter topologies with an output LC filter-based SAPSS.

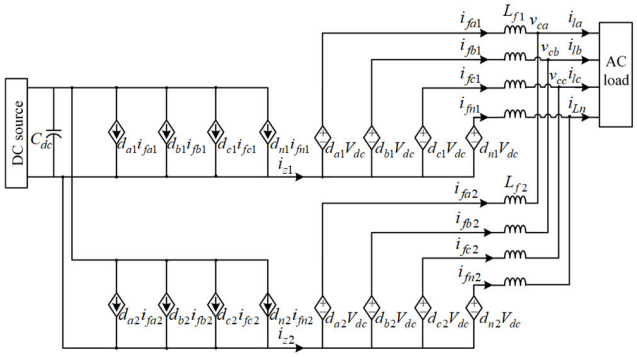

FIGURE 2. Average equivalent circuit model of the two parallel 4-leg inverters in the 3-phase reference frame.

DC-bus is assumed to have a constant voltage, and the duty ratio of the upper switch in phase-leg k (k=a, b, c, and n) of the inverter x(x = 1 and 2) is d_{kx}.

The output voltages of each inverter in the 3-phase reference frame as a function of the DC-bus voltage and average duty ratios are given as follows:

$$\begin{bmatrix} v_{fax} \\ v_{fbx} \\ v_{fcx} \\ v_{fnx} \end{bmatrix} = V_{dc} \begin{bmatrix} d_{ax} \\ d_{bx} \\ d_{cx} \\ d_{nx} \end{bmatrix} \tag{1}$$

By applying Kirchhoff's laws to the equivalent circuit model depicted in Fig. 2, the mathematical model of the parallel system in the 3-phase reference frame as a function of the duty ratio can be obtained by Equations (2) to (5) as follows:

$$\begin{cases} L_{fx}\dfrac{di_{fax}}{dt} = d_{ax}V_{dc} - v_{ca} + L_{fx}\dfrac{di_{fnx}}{dt} \\ L_{fx}\dfrac{di_{fbx}}{dt} = d_{bx}V_{dc} - v_{cb} + L_{fx}\dfrac{di_{fnx}}{dt} \\ L_{fx}\dfrac{di_{fcx}}{dt} = d_{cx}V_{dc} - v_{cc} + L_{fx}\dfrac{di_{fnx}}{dt} \end{cases} \tag{2}$$

$$i_{dc} = d_{a1}i_{fa1} + d_{b1}i_{fb1} + d_{c1}i_{fc1} + d_{n1}i_{fn1} \tag{3}$$

$$\begin{cases} C_f\dfrac{dv_{ca}}{dt} = i_{pa} - i_{la} \\ C_f\dfrac{dv_{cb}}{dt} = i_{pb} - i_{lb} \\ C_f\dfrac{dv_{cc}}{dt} = i_{pc} - i_{lc} \end{cases} \tag{4}$$

$$\begin{cases} C_f\dfrac{dv_{ca}}{dt} = i_{Ca} \\ C_f\dfrac{dv_{cb}}{dt} = i_{Cb} \\ C_f\dfrac{dv_{cc}}{dt} = i_{Cc} \end{cases} \tag{5}$$

where $V_{fx} = [v_{fax}v_{fbx}v_{fcx}v_{fnx}]^{\mathrm{T}}$ and $I_{fx} = [i_{fax}i_{fbx}i_{fcx}i_{fnx}]^{\mathrm{T}}$ are the output voltages and current vectors of inverter x, respectively; $I_{px} = [i_{pa}i_{pb}i_{pc}i_{pn}]^{\mathrm{T}}$ is the parallel system output current vector; $I_L = [i_{la}i_{lb}i_{lc}i_{ln}]^{\mathrm{T}}$ and $V_L = [v_{ca}v_{cb}v_{cc}]^{\mathrm{T}}$ are the load current and voltage vectors, respectively; $I_{Cf} = [i_{Ca}i_{Cb}i_{Cc}]^{\mathrm{T}}$ is the capacitor current vector; and L_{fx} and C_f are the output filter inductances and capacitances of inverter x, respectively.

Equations (2)-(5) demonstrate that the mathematical model of the two parallel connected 4-leg inverter system in the 3-phase reference frame is highly complex, which makes the analysis and control design complicated to implement. For simplicity, a low-complexity average model of this parallel system in the synchronously rotating reference frame (dq0 frame) is obtained as shown in Equations (6) to (7) based on Equations (2) to (5) using Park's transformation.

$$\begin{cases} L_{fx}\dfrac{di_{fdx}}{dt} = d_{dx}V_{dc} - v_{da} + \omega L_{fx}i_{fqx} \\ L_{fx}\dfrac{di_{fqx}}{dt} = d_{qx}V_{dc} - v_{qa} - \omega L_{fx}i_{fdx} \\ 4L_{fx}\dfrac{di_{f0x}}{dt} = d_{dx}V_{dc} \end{cases} \tag{6}$$

$$\begin{cases} C_f\dfrac{dv_{cd}}{dt} = i_{Cd} + \omega C_f v_{cq} \\ C_f\dfrac{dv_{cq}}{dt} = i_{Cq} - \omega C_f v_{cd} \\ C_f\dfrac{dv_{c0}}{dt} = i_{C0} \end{cases} \tag{7}$$

$$\begin{bmatrix} v_{fdx} \\ v_{fqx} \\ v_{f0x} \end{bmatrix} = V_{dc} \begin{bmatrix} d_{dx} \\ d_{qx} \\ d_{0x} \end{bmatrix} \tag{8}$$

where, i_{fdx}, i_{fqx}, i_{f0x} and v_{fdx}, v_{fqx},v_{f0x} are the dq_0-axis output currents and voltages of inverter x, respectively. ω is the load voltage angular frequency. i_{pd}, i_{pq}, i_{p0} and i_{ld}, i_{lq}, i_{l0} are the dq_0-axis output currents of both the inverters and the load currents, respectively.

As mentioned, in parallel 4-leg inverters, in addition to the ZSCC generated under the influence of the filter parameters or unequal output current sharing, a ZSC also appears in the fourth leg of each inverter and needs to be eliminated. According to the average equivalent circuit model

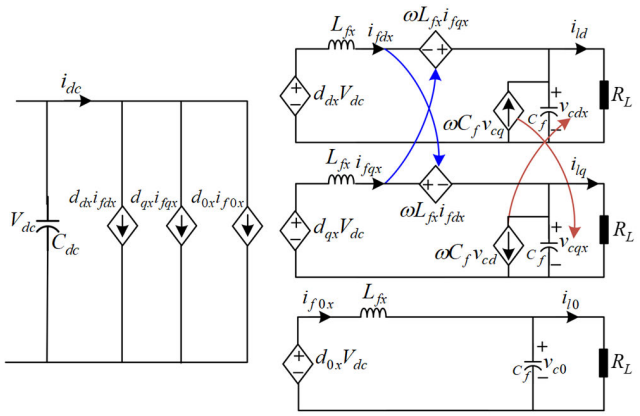

FIGURE 3. Average equivalent circuit model of the two parallel connected 4-leg inverters in the dq0 reference frame.

of the two parallel connected 4-leg inverters in the dq0 frame presented in Fig. 3, the dq-axes are coupled between them by two voltage-controlled current sources and four current-controlled voltage sources, while the 0-axis is decoupled from the dq-axes, which indicates that the zero-sequence component is only present in the 0-axis (and is independent of the d and q components). Therefore, the ZSC can be controlled separately using the control of the neutral current of the fourth leg in each inverter, which contributes to the development of the proposed ZSCC technique and facilitates its implementation.

B. ZSCC MECHANISMS AND CHARACTERISTICS

When inverters are connected in parallel through common AC and DC buses, a difference in the zero-sequence voltages between inverters is induced, which leads to the generation of ZSCCs between these inverter phase legs. These ZSCCs are complicated to model, analyze, and control. To facilitate the realization of these targets, the phase-leg average technique designed in [30] is adopted. The two parallel connected 4-leg inverter average phase-leg models obtained using this method are illustrated in Fig. 2. Thus, the ZSCCs of parallel modules could be derived. According to this figure, the ZSCCs flowing between the two 4-leg inverters have equal magnitudes and opposite phases, as shown in Equations (9) and (10):

$$\begin{cases} i_{z1} = i_{fa1} + i_{fb1} + i_{fc1} + i_{fn1} \\ i_{z2} = i_{fa2} + i_{fb2} + i_{fc2} + i_{fn2} \end{cases} \tag{9}$$

$$i_z = i_{z1} = -i_{z2} \tag{10}$$

Considering Fig. 2, applying Kirchhoff's voltage laws results in:

$$\begin{cases} d_{a1}V_{dc} - L_{f1}\dfrac{di_{fa1}}{dt} = d_{b1}V_{dc} - L_{f1}\dfrac{di_{fb1}}{dt} \\ = d_{c1}V_{dc} - L_{f1}\dfrac{di_{fc1}}{dt} = d_{n1}V_{dc} - L_{f1}\dfrac{di_{fn1}}{dt} \\ d_{a2}V_{dc} - L_{f2}\dfrac{di_{fa2}}{dt} = d_{b2}V_{dc} - L_{f2}\dfrac{di_{fb2}}{dt} \\ = d_{c2}V_{dc} - L_{f2}\dfrac{di_{fc2}}{dt} = d_{n2}V_{dc} - L_{f2}\dfrac{di_{fn2}}{dt} \end{cases} \tag{11}$$

By summing the two equalities of Equation (11), the following equality can be obtained:

$$\sum_{k=a,b,c,n} d_{k1}V_{dc} - L_{f1}\sum_{k=a,b,c,n}\frac{di_{fk1}}{dt} = \sum_{k=a,b,c,n} d_{k2}V_{dc} - L_{f2}\sum_{k=a,b,c,n}\frac{di_{fk2}}{dt} \tag{12}$$

The zero-sequence duty ratio of one 4-leg PWM inverter can be defined as the total of the duty ratios of all phase legs of this inverter and can be expressed by Equation (13) in the two parallel 4-leg inverters as follows:

$$\begin{cases} d_{z1} = \sum_{k=a,b,c,n} d_{k1} = d_{a1} + d_{b1} + d_{c1} + d_{n1} \\ d_{z2} = \sum_{k=a,b,c,n} d_{k2} = d_{a2} + d_{b2} + d_{c2} + d_{n2} \end{cases} \tag{13}$$

By substituting Equations (9) and (13) into Equation (12), a new average model can be obtained as follows:

$$d_{z1}V_{dc} - L_{f1}\frac{di_{z1}}{dt} = d_{z2}V_{dc} - L_{f2}\frac{di_{z2}}{dt} \tag{14}$$

where $d_{z1}V_{dc} = v_{zsv1}$ and $d_{z2}V_{dc} = v_{zsv2}$ are the ZSVs of inverters 1 and 2, respectively, which are expressed as:

$$\begin{cases} v_{zsv1} = (d_{a1} + d_{b1} + d_{c1} + d_{n1})\, V_{dc} \\ v_{zsv2} = (d_{a2} + d_{b2} + d_{c2} + d_{n2})\, V_{dc} \end{cases} \tag{15}$$

From Equations (10) and (14), the ZSCC average model can be rewritten as follows:

$$(L_{f1} + L_{f2})\frac{di_z}{dt} = (d_{z2} - d_{z1})\, V_{dc} \tag{16}$$

Using Equations (15) and (16), the ZSCC average model can be written as a function of the ZSVs as follows:

$$(L_{f1} + L_{f2})\frac{di_z}{dt} = v_{zsv2} - v_{zsv1} \tag{17}$$

Using the Laplace transform of Equation (17), the average model of ZSCC becomes:

$$I_z(s) = \frac{\Delta v_{zsv}(s)}{(L_{f1} + L_{f2})} \tag{18}$$

Equation (18) indicates that the difference between the ZSVs of the two inverters Δv_{zsv} is the main factor involved in generating the ZSCC, which could be the result generally of mismatches in the filter inductances, unbalanced output current sharing, unequal switching devices, etc. If the zero-sequence duty ratios d_{z1} and d_{z2}, i.e., the ZSVs of the two parallel inverters v_{zsv1} and v_{zsv2} are the same, ZSCC will not be generated. Figs. 4a and 4b show the ZSVs of the two inverters (v_{zsv1} and v_{zsv2}) and their difference Δv_{zsv}under both unequal filter inductances and output currents, where the modulation index is 1 and the load voltage frequency is 50 Hz. These ZSVs have a triangular waveform with a frequency equal to 150 Hz (triple load voltage frequency) and equal magnitude but with a phase difference in both cases. Additionally, the Δv_{zsv} waveform observed in both cases is a square wave with a triple load voltage frequency. Theoretically, the ZSCC generated by the difference between ZSVs

has a triangular waveform with the characteristic of a triple load voltage frequency, which was demonstrated in [26] and [27]. Therefore, the ZSCC can be successfully suppressed when Δv_{zsv} is controlled and set to zero.

Based on applying a Fourier series transformation [29] to the data of Figs. 4a and 4b, the ZSV of each inverter (v_{zsvx}) can be approximated as follows:

$$v_{zsvx}(t) = d_{zx} V_{dc} \approx \frac{8V_z}{\pi^2} \sum_{h=1,3,5,..}^{\infty} \frac{(-1)^{(h-1)/2}}{h^2} sin(h\omega_3 t) \quad (19)$$

where $V_z = V_{z1} = V_{z2}$ is the magnitude of the ZSV of each inverter (v_{zsvx}) and $\omega_3 = 3\omega$ is the fundamental frequency of the ZSVs.

Based on this value, when $v_{zsv2}$is shifted from v_{zsv1} by a phase equal to λ, the two ZSVs can be written as:

$$\begin{cases} v_{zsv1}(t) \approx \dfrac{8V_z}{\pi^2} \sum_{h=1,3,5,..}^{\infty} \dfrac{(-1)^{\frac{(h-1)}{2}}}{h^2} sin(h\omega_3 t) \\ v_{zsv2}(t) \approx \dfrac{8V_z}{\pi^2} \sum_{h=1,3,5,..}^{\infty} \dfrac{(-1)^{(h-1)/2}}{h^2} sin(h\omega_3 t - \lambda) \end{cases} \quad (20)$$

From Equation (20), the difference between the ZSVs (Δv_{zsv}) can be expressed as:

$$\Delta v_{zsv} \approx A \sum_{h=1,3,..}^{\infty} \frac{-1^{\frac{(h-1)}{2}}}{h^2} (sin(h\omega_3 t - \lambda) - sin(h\omega_3 t)) \quad (21)$$

where $\boldsymbol{A} = \frac{\boldsymbol{8V_z}}{\boldsymbol{\pi^2}}$

Equation (21) can be rewritten in the following form:

$$\Delta v_{zsv} \approx -2Asin\left(\frac{\lambda}{2}\right) \sum_{h=1,3,..}^{\infty} \frac{(-1)^{\frac{(h-1)}{2}}}{h^2} cos\left(h\omega_3 t - \frac{\lambda}{2}\right) \quad (22)$$

From Equation (18), the ZSCC can be determined by dividing Δv_{zsv} in Equation (22) by its impedance at each harmonic component frequency as follows:

$$i_z(t) \approx \frac{-2Asin\left(\frac{\lambda}{2}\right)}{(L_{f1} + L_{f2})\omega_3} \sum_{h=1,3,..}^{\infty} \frac{(-1)^{\frac{(h-1)}{2}}}{h^2} cos\left(h\omega_3 t - \frac{\lambda}{2}\right) \quad (23)$$

As shown in Equation (23), the ZACC comprises several odd harmonics with a fundamental frequency equal to 150 Hz. These odd harmonics can be written as follows:

$$i_z(t) \approx i_z^{1st}(t) + i_z^{3rd}(t) + i_z^{5rd}(t) + i_z^{7rd}(t) \quad (24)$$

where:

$i_z^{1st}(t) = B\cos(\omega_3 t - \lambda)$, $i_z^{3rd}(t) = B\cos(3\omega_3 t - \lambda)$, $i_z^{5rd}(t) = B\cos(5\omega_3 t - \lambda)$,..... and $B = \frac{-2Asin\left(\frac{\lambda}{2}\right)}{(L_{f1}+L_{f2})\omega_3}$

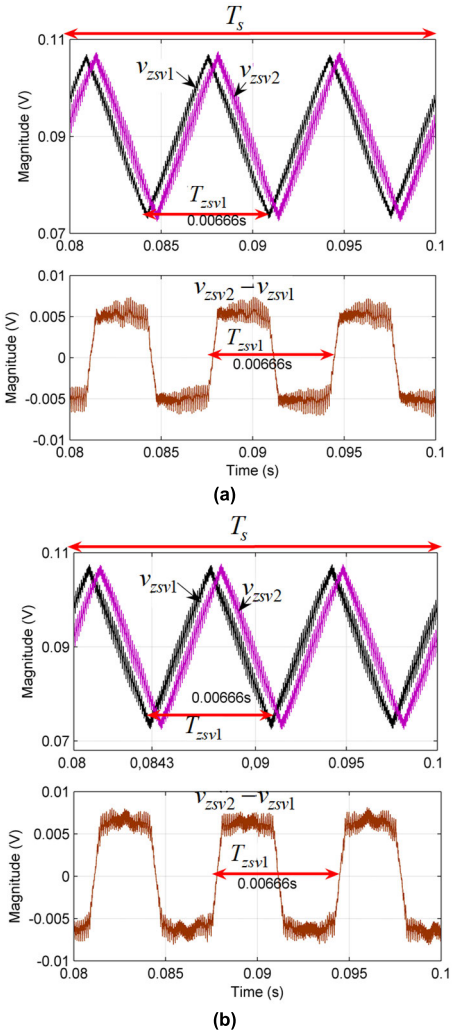

FIGURE 4. Zero-sequence voltages and their differences for parallel 4-leg inverters with m = 1.0 and f = 50 Hz; (a) under unequal filter inductances and (b) unequal output currents.

III. PRINCIPLE OF SUPPRESSING ZSCC USING THE MODIFIED 3DSVPWM METHOD

A. CONVENTIONAL 3DSVPWM

The conventional 3-dimensional SVPWM (C3DSVPWM) technique is widely used to command 4-leg PWM converters due to its advantages, including a constant switching frequency, low AC-side current harmonics, and less DC-bus voltage undulations. This technique can produce symmetrical 4-leg inverter output voltages even under unbalanced conditions [5], [6].

Compared to the 2DSVPWM used to control 3-leg converters, 3DSVPWM has sixteen state vectors ($v_0, v_1 \ldots, v_{16}$), which have fourteen active vectors (AVs) and two zero-vectors (ZVs) distributed in the 3-D space vector diagram (the $\alpha\beta 0$ frame), as presented in Fig. 5a. These state vectors are distributed across five voltages in 2-D space, and the 3-D space vector diagram is decomposed into six prisms. Each prism consists of four tetrahedrons formed by the combination of three AVs and two ZVs, as shown in Figs. 5b

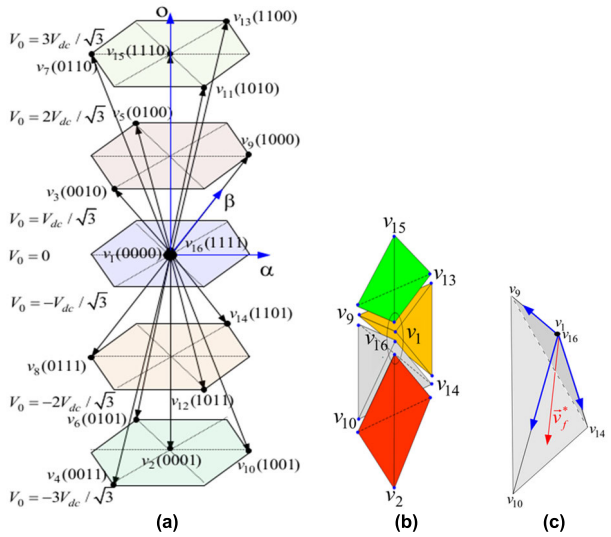

FIGURE 5. Distributions of voltage vectors of the 4-leg inverter; a) 3-D space vector diagram ($\alpha\beta 0$), b) tetrahedrons of prism 1, and c) tetrahedron 1 of prism 1 and their voltage vectors.

and 5c (the first tetrahedron of the first prism is chosen as an example).

In each tetrahedron, it is assumed that the duty ratios of the three AVs inverter x are d_{1x}, d_{2x}, and d_{3x}, respectively, and that the duty ratio of the ZVs is d_{0x}. Then, the reference voltage vector in the first tetrahedron of the first prism can be synthesized in each switching period T_s as in Equation (25):

$$v_{fx}^{*} = \frac{d_{1x}v_9 + d_{2x}v_{10} + d_{3x}v_{14} + d_{0x}\,(v_0 + v_{16})}{T_s} \tag{25}$$

where, the sum of all vector duty ratios satisfies the following constraint:

$$d_{1x} + d_{2x} + d_{3x} + d_{0x} = 1 \tag{26}$$

From Equation (26), the duty ratio of zero vectors d_{0x} can be expressed as:

$$d_{0x} = 1 - d_{1x} - d_{2x} - d_{3x} \tag{27}$$

As presented in Fig. 5c, which assumes that the reference voltage vector of each 3DSVPWM in Equation (25) is located in the first tetrahedron of the first prism as an example, the state vectors and their duty ratios are distributed using a switching sequence of nine segments, as shown in Fig. 6a. The ZVs are orderly distributed with equal duty ratios d_0 at the onset, middle and finish of a switching period, and the AVs are distributed with consideration of the minimal switching states in each switching period or low switching losses.

Based on applying Equation (13) to the data shown in Fig. 6a, the zero-sequence duty ratio d_{zx} of each inverter is linked to the duty ratios of the AVs and ZVs in each switching period by:

$$\begin{aligned} d_{zx} &= d_{ax} + d_{bx} + d_{cx} + d_{nx} \\ &= d_{1x} + 2d_{2x} + 3d_{3x} + 2d_{0x} \end{aligned} \tag{28}$$

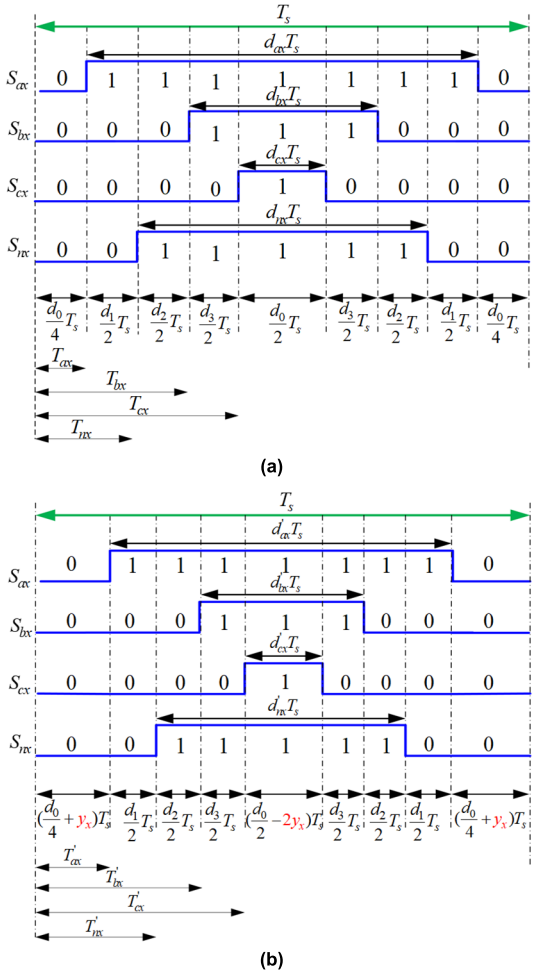

FIGURE 6. Distribution of the state vectors and their duty ratios (e.g., tetrahedron 1 of prism 1); (a) in C3DSVPWM; (b) Proposed modified 3DSVPWM.

Substituting Equation (27) into Equation (28) yields:

$$d_{zx} = -d_{1x} + 2d_{3x} \tag{29}$$

The switching transition times T_{ax}, T_{bx}, T_{cx}, and T_{nx} of the state vectors in each 4-leg inverter are expressed as follows:

$$\begin{cases} T_{ax} = \dfrac{d_{0x}}{4}T_s \\ T_{bx} = T_{ax} + \dfrac{d_{1x}}{2}T_s + \dfrac{d_{2x}}{2}T_s \\ T_{cx} = T_{bx} + \dfrac{d_{3x}}{2}T_s \\ T_{nx} = T_{ax} + \dfrac{d_{1x}}{2}T_s \end{cases} \tag{30}$$

As the C3DSVPWM neglects the modulation of the ZSVs, the ZSCC will exist between the parallel 4-leg inverters. Therefore, the proposed modified 3DSVPWM technique eliminates the effects of the ZSVs, ZSCC, and ZSC.

B. PROPOSED MODIFIED 3DSVPWM

Based on the aforementioned ZSCC analysis and to eliminate the difference between the ZSVs of the two inverters Δv_{zsv}

and the ZSCC, a new modified 3DSVPWM technique is developed in this study, in which the zero-sequence duty ratios are adjusted by introducing an adjusting variable y_x obtained from the ZSCC regulation in each switching period to the duty ratios of the ZVs.

Fig. 6b depicts the distribution of the state vectors and their duty ratios in each switching period of the modified 3DSVPWM technique (the first tetrahedron of the first prism is selected as an example). As depicted, an adjusting variable y_x can be introduced to adjust the zero-sequence duty ratios of ZVs in each switching period to eliminate the zero-sequence duty ratio difference Δd_z between d_{z1} and d_{z2}, in which the duty ratios d_{0x} of the two ZVs v_1 and v_{16} are changed to $(d_{0x}/2-2y_x)$ and $(d_{0x}/2+2y_x)$, respectively. These changes in the duty ratios of the ZVs cannot impact the control purposes or the output energy quality of the parallel system, including the output currents, voltages, and input DC-bus voltage. This Δd_z can be regulated using the control of zero vectors. Theoretically, by setting Δd_z equal to zero, the ZSCC can be eliminated. This purpose can be achieved using the proposed new modified 3DSVPWM technique.

As shown in Fig. 6b, the designed proposed method is satisfactory when the condition $-\frac{d_0}{4} < y_x < \frac{d_0}{4}$ is verified.

Based on Fig. 6b, after adjusting the variable y_x, the new zero-sequence duty ratios d'_{zx} of the proposed new modified 3DSVPWM technique can be calculated using the new duty ratios (d'_{ax},d'_{bx},d'_{cx}, and d'_{nx}) as follows:

$$\begin{aligned} d'_{zx} &= d'_{ax} + d'_{bx} + d'_{cx} + d'_{nx} \\ &= d_{1x} + 2d_{2x} + 3d_{3x} + 2d_{0x} - 8y_x \end{aligned} \tag{31}$$

Substituting Equation (27) into Equation (31), the zero-sequence duty ratio d'_{z2} of the proposed modified 3DSVPWM technique is adjusted by the ZSCC control loop output variable y_2 as follows:

$$d'_{zx} = (-d_{1x} + d_{3x} + 2 - 8y_x) \tag{32}$$

For the two parallel connected 4-leg inverter system, as the ZSCCs in the two inverters have equal magnitudes and opposite signs, if the ZSCC of one inverter is controlled, the ZSCC in the other inverter will be controlled accordingly, which ensures that the ZSCC in one inverter is sufficient to suppress the ZSCC in the whole system. Therefore, the ZSCC is controlled by adjusting the 3DSVPWM of the second inverter using the variable y_2 while the variable y_1 is set to zero (the first inverter is controlled by the C3DSVPWM).

From Equation (32), the difference between the zero-sequence duty ratios of the two inverters Δd_{zx} of the proposed new modified 3DSVPWM technique can be expressed as follows:

$$\begin{aligned} d'_{zx} &= d'_{z2} - d'_{z1} \\ &= d_{11} - d_{12} + d_{32} - d_{31} - 8y_x \end{aligned} \tag{33}$$

Similarly, when the reference voltage vector is situated in other tetrahedrons and prisms, the difference in the zero-sequence duty ratio Δd_{zx} between the two inverters can be determined via the same process.

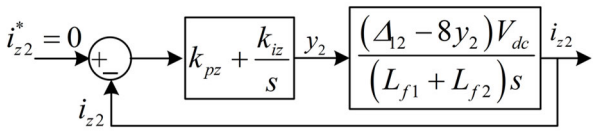

FIGURE 7. Bloc diagram of the PI closed loop of ZSCC command.

Substituting Equation (33) into Equation (18), the new average model of ZSCC can be written as follows:

$$I_z(s) = \frac{d_{11} - d_{12} + d_{32} - d_{31} - 8y_x}{(L_{f1} + L_{f2})} V_{dc} \tag{34}$$

Assuming that $\Delta_{12} = d_{11} - d_{12} + d_{32} - d_{31}$, the new average model of ZSCC becomes:

$$I_z(s) = \frac{\Delta_{12} - 8y_x}{(L_{f1} + L_{f2})} V_{dc} \tag{35}$$

As shown in Fig. 6b and using Equation (30), the new switching transition times of the proposed modified 3DSVPWM are expressed as follows:

$$\begin{cases} T'_{a2} = \dfrac{d_{02}}{4} T_s + y_2 \\ T'_{b2} = T'_{a2} + \dfrac{d_{12}}{2} T_s + \dfrac{d_{22}}{2} T_s \\ T'_{c2} = T'_{b2} + \dfrac{d_{32}}{2} T_s \\ T'_{n2} = T'_{a2} + \dfrac{d_{12}}{2} T_s \end{cases} \tag{36}$$

C. ZSCC REGULATION

The new average model of the ZSCC after adjusting the zero-sequence duty ratio is a first-order model, which enables the design of the closed-loop ZSCC technique. Many linear controllers, including the PI controller [25], PI with feedforward loop controller [26], PI-deadbeat controller [27], and PI-quasi-resonant controller (PIQRC) [28], [29], have been designed for controlling the ZSCC in recent years. Here, a PI controller is used to block the path of the ZSCC harmonics affecting the inverter output harmonic currents, as shown in Fig. 7. The purpose of PI-based ZSCC command is to suppress the difference between the zero-sequence duty ratios of the two inverters Δd_{zx} by acting upon the adjusting variable y_2 as follows:

$$y_2 = (k_{pz} + \frac{k_{iz}}{s})(i^*_z - i_z) \tag{37}$$

where k_{pz} and k_{iz} are the ZSCC-PI controller parameters, which are calculated using the pole placement technique as follows:

$$\begin{cases} k_{pz} = \dfrac{(L_{f1} + L_{f2})\, \xi_z \omega_{cz}}{V_{dc}} \\ k_{iz} = \dfrac{(L_{f1} + L_{f2})\, \omega^2_{cz}}{V_{dc}} \end{cases} \tag{38}$$

where ω_{cz} and ξ_z are the cut off frequency and the damping factor of the ZSCC-PI, respectively.

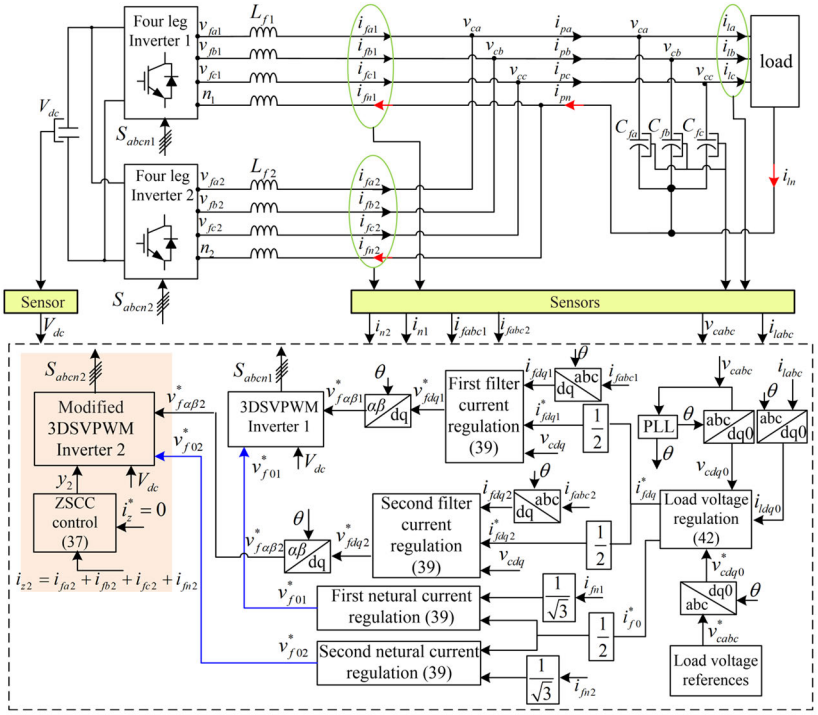

FIGURE 8. Control block diagram of the two parallel connected 4-leg inverter-based SAPSSs, including the designed ZSCC suppression technique.

IV. CONTROL STRATEGY OF THE PARALLEL 4-LEG INVERTER TOPOLOGY FOR AN SAPSS

A diagram of the control block of the parallel connected 4-leg inverter topology-based SAPSS, including the ZSCC regulation and the proposed new modified 3DSVPWM, is shown in Fig. 8. The technique is based on the cascading of load voltages and filter current command loops in the dq0 frame, in which the filter current references are provided from the load voltage control loop. The outer loop is used to regulate the load voltages and mitigate their imbalance, while the inner loop is used to improve the current transient and steady-state performances and to guarantee perfect current sharing between the parallel inverters. Therefore, the ZSCC can be eliminated by the proposed technique while load current sharing is achieved. The reactive power required by the LC filter can be obtained by the two parallel connected inverters, as shown in Fig. 8.

Using PI controllers in the inner current loop, the reference voltages of both 3DSVPWMs in the dq0 frame obtained from this loop can be calculated as follows:

$$\begin{cases} v^*_{fdx} = \left(k_{pid} + \dfrac{k_{iid}}{s}\right)\left(i^*_{fdx} - i_{fdx}\right) + v_{cd} + \omega L_{fx} i_{fqx} \\ v^*_{fqx} = \left(k_{pid} + \dfrac{k_{iid}}{s}\right)\left(i^*_{fqx} - i_{fqx}\right) + v_{cq} - \omega L_{fx} i_{fdx} \\ v^*_{f0x} = \left(k_{pi0} + \dfrac{k_{ii0}}{s}\right)\left(i^*_{f0x} - \dfrac{i_{fnx}}{\sqrt{3}}\right) + v_{c0} \end{cases} \tag{39}$$

where k_{pidq0} and k_{iidq0} are the inner current loop PI controller parameters and can be calculated using the pole placement technique as follows:

$$\begin{cases} k_{pidqx} = 2L_{fx}\xi_i\omega_{ci} \\ k_{iidqx} = L_{fx}\omega^2_{ci} \end{cases} \tag{40}$$

$$\begin{cases} k_{pi0} = \dfrac{8}{\sqrt{3}} L_{fx}\xi_i\omega_{ci} \\ k_{ii0} = \dfrac{4}{\sqrt{3}} L_{fx}\omega^2_{ci} \end{cases} \tag{41}$$

where ω_{ci} and ξ_i are the cut off angular frequency and the damping factor of the inner current loop PI controllers, respectively, and i^*_{fdq0x} denote the filter's current references, which are obtained from the outer load voltage loop as follows:

$$\begin{cases} i^*_{fdx} = \dfrac{\left(k_{pv} + \frac{k_{iv}}{s}\right)\left(v^*_{cd} - v_{cd}\right) + i_{Ld} + \omega C_f v_{cq}}{2} \\ i^*_{fqx} = \dfrac{\left(k_{pv} + \frac{k_{iv}}{s}\right)\left(v^*_{cq} - v_{cq}\right) + i_{Lq} - \omega C_f v_{cd}}{2} \\ i^*_{f0x} = \dfrac{\left(k_{pv} + \frac{k_{iv}}{s}\right)\left(v^*_{c0} - v_{c0}\right) + i_{L0}}{2} \end{cases} \tag{42}$$

where k_{pv} and k_{iv} are the outer loop PI controller parameters and can be calculated using the pole placement technique as follows:

$$\begin{cases} k_{pv} = 2C_f\xi_v\omega_{cv} \\ k_{iv} = C_f\omega^2_{cv} \end{cases} \tag{43}$$

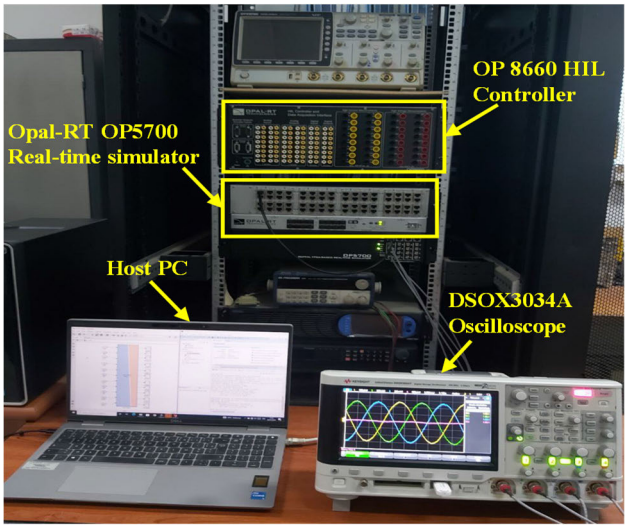

FIGURE 9. Configuration of OPAL-RT OP5700 real-time simulator setup.

TABLE 1. System and HIL simulation parameters.

Symbol	Quantity	Value
V_c	Grid voltage (RMS)	220 V
f	Load voltage frequency	50 Hz
U_{dc}	DC-link voltage	600 V
L_{f1},L_{f2}	Filters inductances	10 mH, 5 mH
C_f	Filter capacitor	60 uF
R	Load resistance	10 Ω
f_s	Switching frequency	8 kHz
T_s	Sampling time	10 us

where, $\boldsymbol{\omega_{cv}}$ and $\boldsymbol{\xi_v}$ are the cut off angular frequency and the damping factor of the outer loop PI regulators, respectively.

V. HIL SIMULATION RESULTS DISCUSSION

To evaluate the viability and effectiveness of the designed ZSCC suppression technique and the overall system behavior, multiple HIL simulation tests were conducted using the OPAL-RT OP5700 real-time simulator executing in a MATLAB environment. In this section, the characteristic of the designed ZSCC suppression technique is compared with those of the conventional 3DSVPWM, identical ZSV injection-based SPWM technique designed in [34], and the modified SPWM based on ZSCC with PI regulator designed in [35].

The characteristics of the three techniques are compared in the following five scenarios:

Scenario 1: unbalanced filter inductances (UFIs) with equal output current sharing under a balanced 3-phase load;

Scenario 2: unbalanced output current sharing (UOCS) and equal filter inductances under a balanced 3-phase load;

Scenario 3: UOCS with UFIs under a balanced 3-phase load;

Scenario 4: UOCS with UFIs under an unbalanced three-phase load;

Scenario 5: UFIs with equal output current sharing under unbalanced nonlinear single-phase loads.

TABLE 2. PI controllers' parameters.

Symbol	Quantity	Value
ω_{ci}	Cut off angular frequency of PI inner loop controllers	3500
ξ_i	Damping factor of PI inner loop controllers	0.707
ω_{cv}	Cut off angular frequency of PI outer loop controllers	800
ξ_v	Damping factor of PI outer loop controllers	0.707
ω_{cz}	Cut off angular frequency of PI ZSCC controller	700
ξ_z	Damping factor of PI ZSCC controller	0.707

The corresponding setup of the experiment platform is depicted in Fig. 9, which is an integral part of the LTII laboratory's energy converter platform. The system, HIL simulation platform, and PI regulator parameters are listed in Tables 1 and 2.

To obtain immunity against the ZSCC and harmonic voltages and currents, the PI controllers have the damping factors and the cut off angular frequencies listed in Table 2.

A. SCENARIO 1: UNBALANCED FILTER INDUCTANCES

In this case, the output current sharing is balanced, and the filter inductances are unbalanced, where $L_{f1} = 10$ mH, $L_{f2} = 5$ mH, and $i_{fdq01} = i_{fdq02} = 50\%$ of i_{fdq0}. To evaluate the characteristic of the proposed method, the HIL simulation results of all techniques are presented in Figs. 10a to 10c.

Fig. 10a shows that a very large ZSCC is generated with a peak-to-peak value of approximately 8A due to the difference between the ZSVs of the two inverters created under the unbalanced filter inductances. This ZSCC circulates among the inverters with triple the load voltage fundamental frequency (150 Hz), and as can be observed, it causes high distortion and asymmetry of both inverter output currents as well as a large magnitude of the 3rd harmonic, as shown in the FFT analysis of these output currents illustrated in Fig. 11a. The THDs of i_{fa1} and i_{fa2} are 6.71% and 6.59%, respectively, which do not fit the IEEE Std 519 standard for current distortion limits. In this case, the output current harmonics with high magnitudes are mainly 3rd harmonics.

Figs. 10 and 11 show the results of this test with the identical ZSV injection-based SPWM technique, the modified SPWM technique, and the proposed modified 3D SVPWM technique. Both the identical ZSV injection-based SPWM and the modified SPWM techniques achieve the poorest results in terms of ZSCC suppression performance and inverter output current THD reductions. The identical ZSV injection-based SPWM technique results in a ZSCC with a peak-to-peak value of approximately 2.4 A (Fig. 10b) and the THD values of both i_{fa1} and i_{fa2} are equal to 3.82% and 4.37%, respectively (Fig. 11b). While the modified SPWM technique produces a ZSCC with a peak-to-peak value of about 1.6 A (Fig. 10c) and the THD values are equal to 2.37% and 3.68% for both i_{fa1} and i_{fa2},respectively (Fig. 11c).

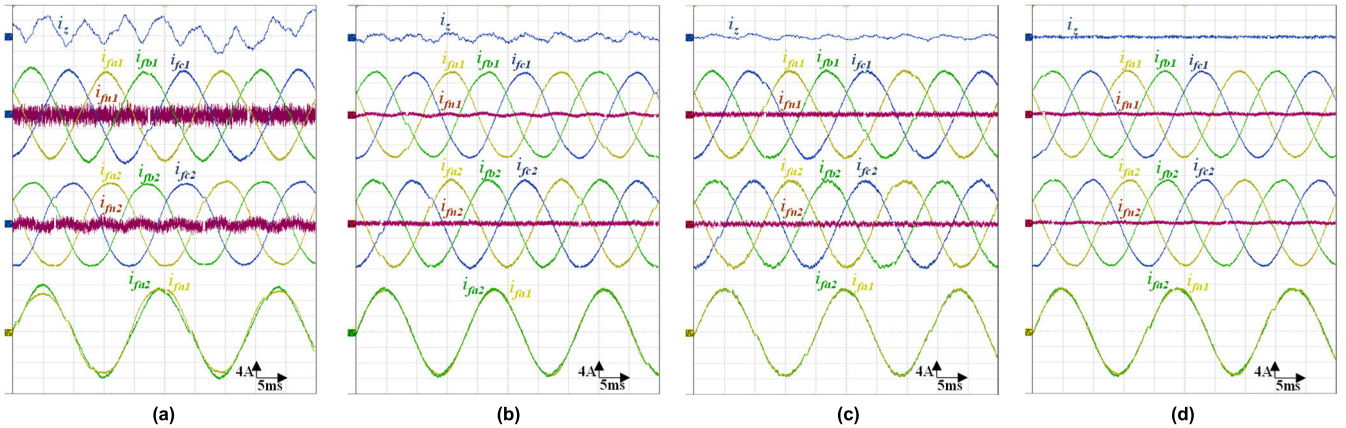

FIGURE 10. Results of parallel connected 4-leg inverters under unequal filter inductances and balanced output current sharing when the three-phase load is balanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

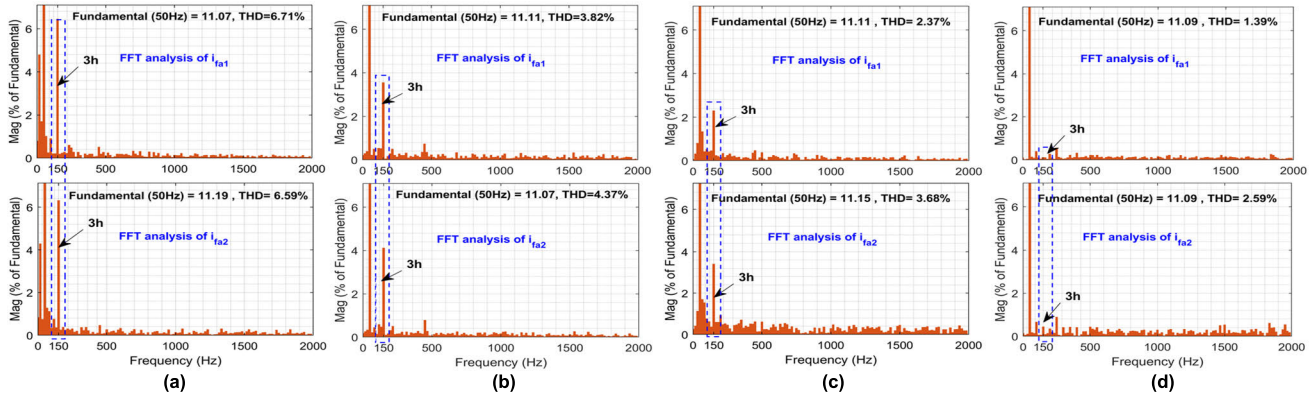

FIGURE 11. The spectra of both inverter output currents under unequal filter inductances and balanced output current sharing when the three-phase load is balanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

Figs. 10d and 11d show the obtained results when the proposed modified 3DSVPWM technique is adopted. By comparing these waveforms with those obtained using both the identical ZSV injection-based SPWM and the modified SPWM technique based on PI-ZSCC control methods, as shown in Figs. 10b and 10c, the ZSCC is demonstrated to be completely suppressed. Fig. 10d demonstrates that both inverter output currents become sinusoidal, balanced, and identical, and the problems of distortion and asymmetry in Fig. 10a are mitigated efficiently, indicating that perfect sinusoidal current sharing accuracy between parallel 4-leg inverters can be achieved using the designed technique. The maximum neutral current oscillations in the two inverters are also clearly reduced.

Fig. 11d shows the FFT analysis of the inverter output currents i_{fa1} and i_{fa2}. The THDs of these currents are further minimized to small values (1.29% and 2.59%), which is in concordance with IEEE Std. Consequently, the inverter output current distortions are almost mitigated, and as expected, the magnitude of the 3rd harmonic is perfectly minimized in both inverter output currents. This observation validates that the designed modified 3DSVPWM can perfectly suppress the ZSCC generated under unbalanced filter inductances and can mitigate the impact of ZSCC on the parallel system better than the modified SPWM technique can.

B. SCENARIO 2: UNEQUAL OUTPUT CURRENT SHARING

In this case, the filter inductances are equal, and the reference output currents are unequal, where $L_{f1} = L_{f2} = 10$ mH with $i_{fdq01} = 70\%$ of i_{fdq0} and $i_{fdq02} = 30\%$ of i_{fdq0}. Figs. 12 and 13 show the results of the three control methods, respectively.

As shown in Fig. 12a, a large ZSCC is generated with a peak-to-peak value of approximately 13.4 A because of the difference between the ZSVs of the two inverters caused by the unequal reference output currents, which seriously distorts both inverter output currents. The THDs of i_{fa1} and i_{fa2} are 6.15% and 14.27%, respectively, as shown in Fig. 13a, which do not fit the IEEE Std 519 for current distortion limits. These high THDs are mainly due to the high magnitude of the 3rd harmonic component.

Figs. 12b and 12c show the results of the modified SPWM technique and the identical ZSV injection-based SPWM technique, respectively. Figs. 13b and 13c display the output current THDs of both ZSCC suppression techniques. The

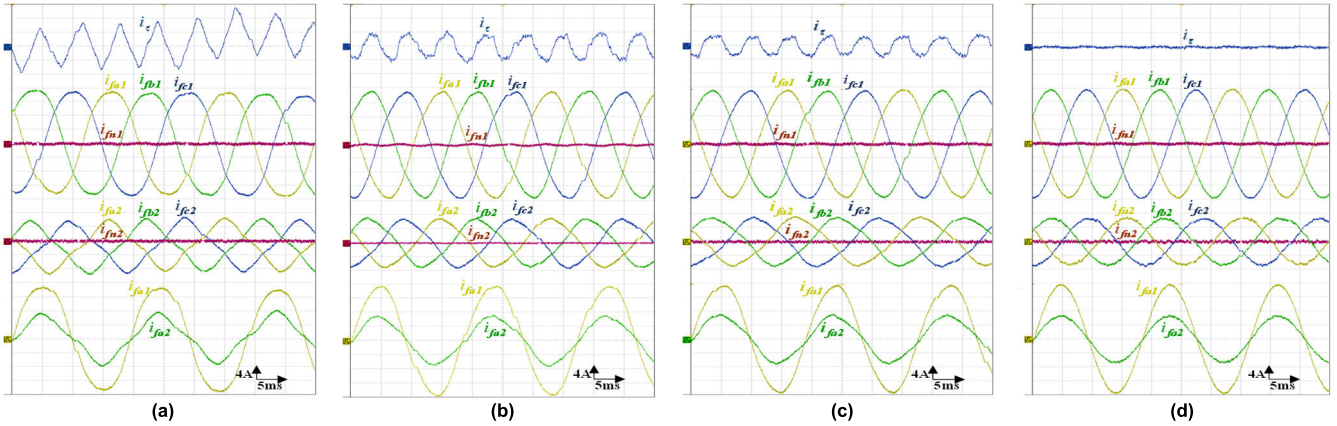

FIGURE 12. Results of parallel connected 4-leg inverters under unequal output current sharing and balanced filter inductances when the three-phase load is balanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

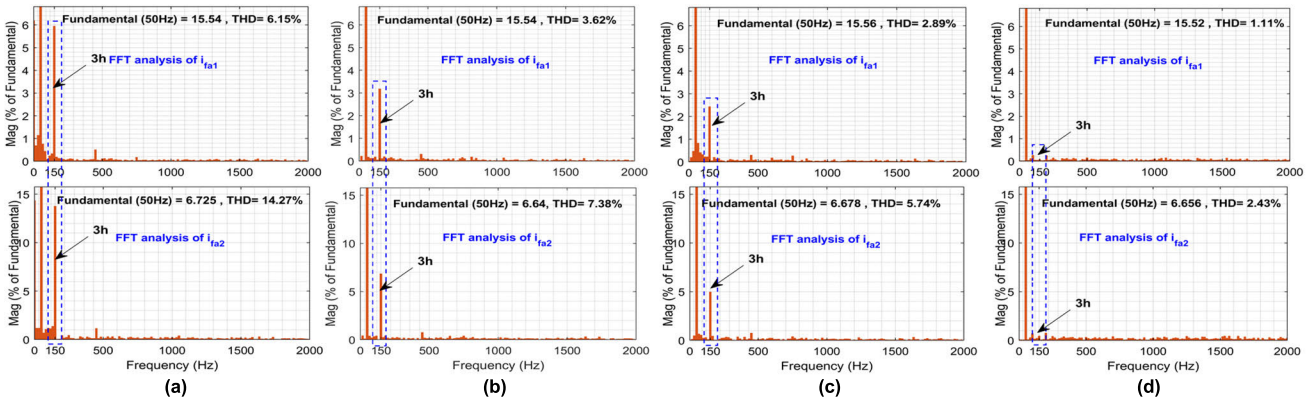

FIGURE 13. The spectra of both inverter output currents under unequal output current sharing and balanced filter inductances when the three-phase load is balanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

TABLE 3. Comparison of the peak-peak values of the ZSCC, output current quality, output current THD, and 3rd harmonic component in the output currents for the three ZSCC control methods.

Scenario	Unbalanced filters inductances				Unbalanced output current sharing			
Method	Without ZSCC control	Method in [34]	Method in [35]	Proposed method	Without ZSCC control	Method in [34]	Method in [35]	Proposed method
Peak-to-peak value of ZSCC (A)	8	2.4A	1.6A	0.6A	13.4A	7.6A	5.6A	0.6A
THD of i_{f1} (%)	6.71	3.82	2.37	1.39	6.15	3.62	2.89	1.11
THD of i_{f2} (%)	6.59	4.37	3.68	2.59	14.27	7.38	5.74	2.43
3rd harmonic in i_{f1} (%)	6.4	3.7	2.25	0.04	5.95	3.28	2.4	0.05
3rd harmonic in i_{f2} (%)	6.15	4.1	3.15	0.4	13.7	6.8	5	0.4
Output currents quality	Distorted and asymmetrical	Accept	Accept	High	Distorted and asymmetrical	Poor	Poor	High

data shown in these figures demonstrates that both ZSCC suppression techniques have the worst performance. The identical ZSV injection-based SPWM technique provides a ZSCC peak-to-peak value of 7.6 A (Fig. 12b), along with a THD of 3.62% for i_{fa1} and 7.38% for i_{fa2}(Fig. 13b), while the modified SPWM technique has a peak-to-peak ZSCC of 5.6 A (Fig. 12c) with a THD of 2.89% for i_{fa1} and 5.74% for i_{fa2}(Fig. 13c).

By using the designed modified 3DSVPWM, excellent ZSCC suppression is achieved, as shown in Fig. 12d. As expected, the inverter output current waveforms are sinusoidal and balanced, and the problems of distortion and asymmetry in Fig. 12a are efficiently eliminated. The maximum neutral current oscillations in the two inverters are also perfectly reduced. In addition, Fig. 13d shows that the THDs of the output currents i_{fa1} and i_{fa2} are minimized to

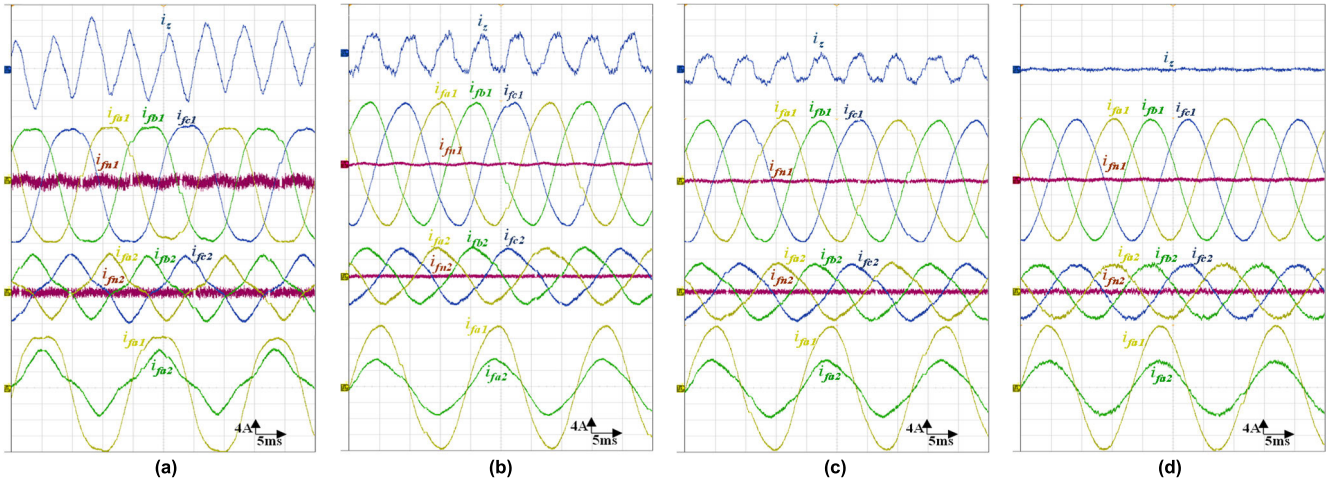

FIGURE 14. Results of the parallel connected 4-leg inverters under both unbalanced output current sharing and filter inductances when the three-phase load is balanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

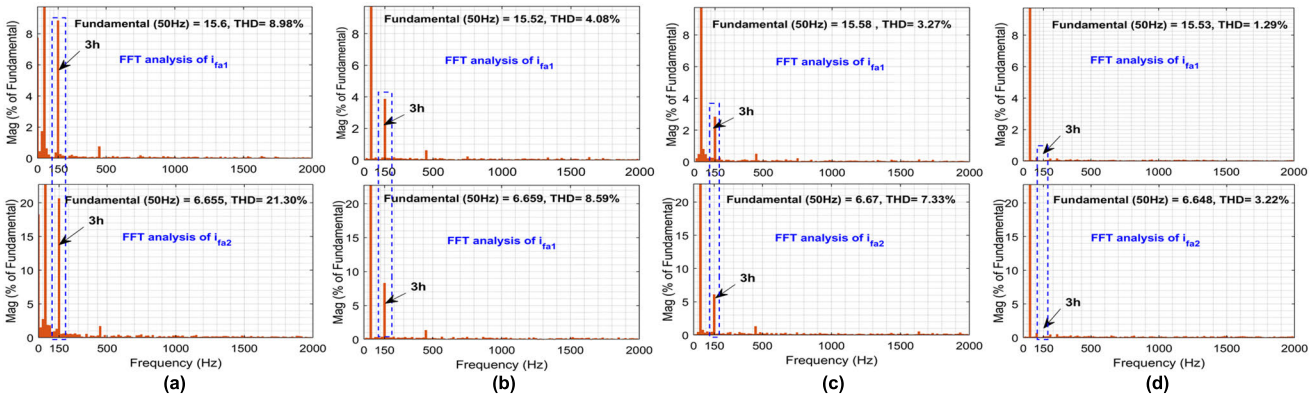

FIGURE 15. The spectra of both inverter output currents under both unbalanced output current sharing and filter inductances when the three-phase load is balanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

1.11% and 2.43%, respectively, using the proposed modified 3DSVPWM technique. This indicates that a very low 3rd harmonic component is included in both inverter output currents. These findings confirm that the designed modified 3DSVPWM can efficiently suppress the ZSCC and its impact on the parallel system is also suppressed even under unbalanced output current sharing.

Table 3 presents a qualitative comparison between the proposed modified 3DSVPWM technique and the other three techniques. The peak-to-peak values of ZSCC, the output currents THDs, the 3rd harmonic component in the output currents, and the output current quality demonstrate the full dominance of the designed modified 3DSVPWM technique.

C. SCENARIO 3: UNBALANCED FILTER INDUCTANCES AND OUTPUT CURRENT SHARING

To further test the proposed ZSCC technique, both the filter inductance and reference output currents are unequal, where, $L_{f1} = 10$ mH, $L_{f2} = 5$ mH, $i_{fdq01} = 70\%$ of i_{fdq0}, and $i_{fdq02} = 30\%$ of i_{fdq0}. The results for this case are presented in Figs. 14 and 15. Based on Fig. 14a, a ZSCC is generated with a peak-to-peak value of 18 A, and the inverter output currents are both seriously distorted due to the presence of a large ZSCC peak-to-peak value.

Figs. 14b, 14c, 15b, and 15c illustrate the results of using both the identical ZSV injection-based SPWM and modified SPWM techniques under unequal filter inductance and output current references. Similar to scenarios 1 and 2, these two techniques perform the poorest in terms of ZSCC suppression performance and output current quality. Figs. 14b and 14c show that the identical ZSV injection-based SPWM technique reduces the ZSCC peak-to-peak value from 18 A to about8.8 A, while the modified SPWM technique reduces it to 7.2 A. The identical ZSV injection-based SPWM technique reduces the output current THD value from 8.98% to 4.08% for i_{fa1} and from 21.30% to 8.59% for i_{fa2}, as depicted in Fig. 15b, while the modified SPWM technique, as shown in Fig. 15c, reduces it to 3.27% for i_{fa1} and 7.33% for i_{fa2}, as depicted in Fig. 15c.

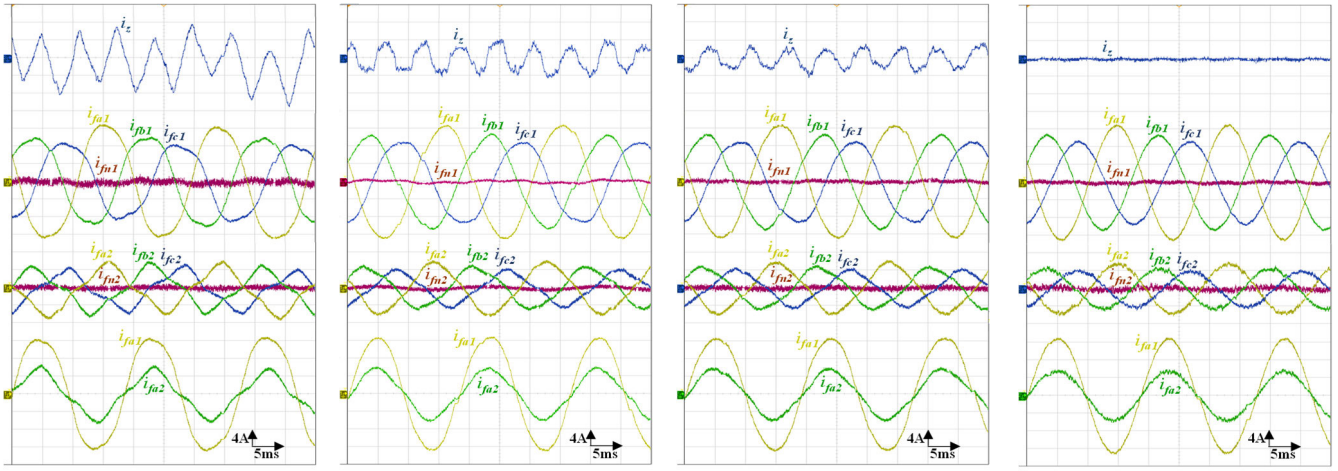

FIGURE 16. Results of the parallel connected 4-leg inverters under both filter inductances and unbalanced output current sharing when the three-phase load is unbalanced. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

TABLE 4. Comparison of the output current THD values of both inverters with their corresponding 3rd harmonic components for the three ZSCC techniques under unbalanced filter inductances, output current sharing, and three-phase linear loads.

Method	Without ZSCC suppression			Method in [34]			Method in [35]			Proposed Method		
Phase current	i_{fa}	i_{fb}	i_{fc}	i_{fa}	i_{fb}	i_{fc}	i_{fa}	i_{fb}	i_{fc}	i_{fa}	i_{fb}	i_{fc}
THD values of the inverter 1 currents (%)	7.2	9.5	10.95	3.22	3.92	4.35	3.05	3.81	4.21	1.45	1.95	2.3
THD values of the inverter 2 currents (%)	18.11	20.09	22.19	7.04	7.21	8.59	6.97	6.74	10.15	3.65	3.87	4.13
3rd harmonic in currents of inverter 1 (%)	6.7	8.8	10.5	2.76	3.45	3.8	2.55	3.22	3.55	0.42	0.59	0.66
3rd harmonic in currents of inverter 2 (%)	17.2	19.1	21	5.81	7.13	8.21	5.11	6.4	7.8	0.98	1.12	1.27

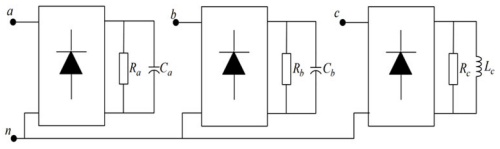

FIGURE 17. Topology of the unbalanced single-phase nonlinear loads considered in this work.

In contrast, the designed modified 3DSVPWM technique produces a much lower peak-to-peak value for the ZSCC (0.3 A), as well as sinusoidal, symmetrical, and balanced output currents; moreover, the problems of distortion and asymmetry in Fig. 14c are effectively mitigated, as shown in Fig. 14c. The oscillations in both neutral currents are also considerably reduced, and the THDs of the output currents are minimized to 1.29% for i_{fa1} and 3.22% for i_{fa2} with a reduced 3rd harmonic component using the designed modified 3DSVPWM technique, as shown in Fig. 15c.

D. SCENARIO 4: UNBALANCED FILTER INDUCTANCES, OUTPUT CURRENT SHARING, AND THREE-PHASE LINEAR LOADS

To evaluate the characteristics of the suggested modified 3DSVPWM technique under critical operating conditions, a scenario of unbalanced three-phase resistive loads ($R_a = 10\ \Omega$, $R_b = 15\ \Omega$, and $R_c = 20\ \Omega$) is considered. Fig. 16 shows the characteristics of the two parallel inverters with the three ZSCC methods. Fig. 16a clearly shows that the peak-to-peak value of the ZSCC is approximately 14A. Due to the ZSCCs, the output currents of both inverters are asymmetrical and distorted with high oscillations in the fourth leg currents, as shown in Figs. 16a and 17a. At this time, the ZSCC suppression characteristic and output current quality of both the identical ZSV injection-based SPWM and modified SPWM techniques are weak, as shown in Figs. 16b, 16c, 17b, and 17c. Compared with these techniques, the proposed modified 3DSVPWM technique has better performance in suppressing the ZSCC and improving the output current quality, as shown in Figs. 16d and 17d. The peak-to-peak value of ZSCC decreases from 16A, 8A, and 6.8 A to approximately 0.4 A. In Fig. 16d, the asymmetry in both inverter output currents is suppressed, and the output harmonic currents and fourth leg current oscillations are perfectly mitigated. The THDs of the output currents of both inverters with their 3rd harmonic components in this case are listed in Table 4. The results in Table 4 demonstrate that the proposed modified 3DSVPWM technique-based parallel 4-leg inverter system can provide good THDs values for the output currents with a very small 3rd harmonic component percentage when

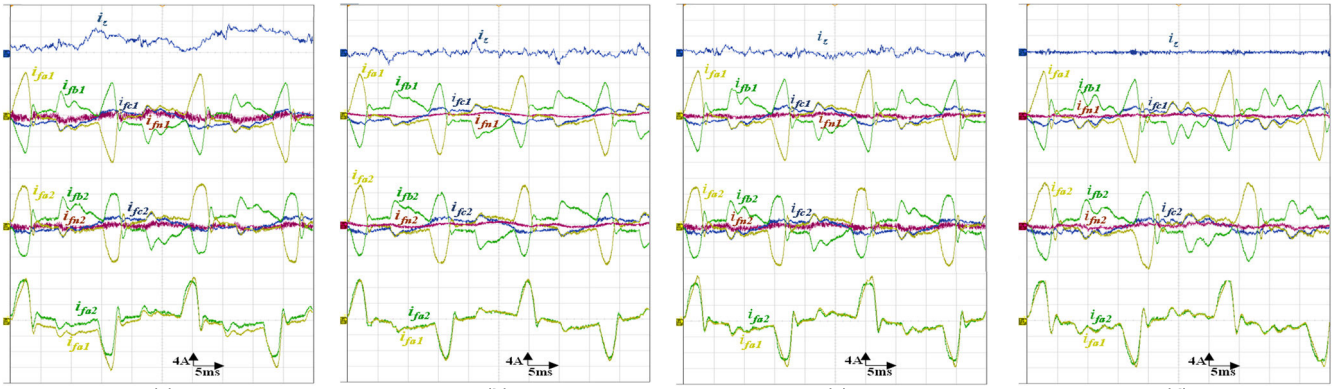

FIGURE 18. Results of the parallel connected 4-leg inverters under unbalanced single-phase nonlinear loads and unbalanced filter inductances. (a) Without ZSCC suppression. (b) Method in [34]. (c) Method in [35]. (d) Proposed modified 3D SVPWM method.

TABLE 5. Comparison of the proposed modified 3DSVPWM technique with the existing PWM techniques.

Ref.	[20, 21]	[22-28]	[30]	[31]	[33]	[34]	[35]	Prop.
Suitability	Yes	No	Yes	Yes	No	Yes	Yes	Yes
Peak value of ZSCC	Large	-----	Large	Large	-----	Large	Large	Very smaller
Output current quality	Poor	-----	Poor	Poor	-----	Poor	Poor	Better
Switching power losses	High	-----	High	High	-----	High	High	Lower
Controllability of ZSVs	No	-----	No	No	-----	No	No	Yes
DC voltage utilization	Lower	-----	Lower	Lower	-----	Lower	Lower	High
System efficiency	Lower	-----	Lower	Lower	-----	Lower	Lower	High
System reliability	Lower	-----	Lower	Lower	-----	Lower	Lower	High
Inverter's operational lifespan	Lower	-----	Lower	Lower	-----	Lower	Lower	Large
Complexity	Lower	-----	Lower	Lower	-----	Lower	Lower	Complex

the parallel inverter system is operating under unbalanced 3-phase loads, filter inductances, and output current sharing conditions.

Based on the results of these tests, the proposed modified 3DSVPWM technique can effectively suppress the ZSCC, fourth leg current oscillations, and output current harmonics, especially the 3rd harmonic component, with good steady-state performance under both balanced and unbalanced three-phase linear loads. These results verify the viability of the theoretical analysis and the efficiency of the designed modified 3DSVPWM technique for regulating two parallel connected 4-leg PWM inverter-based SAPSSs in terms of ZSCC suppression, sharing of output currents, and elimination of 4-leg inverter output current harmonics, especially low-frequency harmonics under an unbalanced filter and unequal output currents when the three-phase linear load is balanced or unbalanced.

E. SCENARIO 5: UNBALANCED FILTER INDUCTANCES AND SINGLE-PHASE NONLINEAR LOADS

Finally, to investigate the characteristic of the suggested modified 3D SVPWM in terms of ZSCC mitigation under unbalanced single-phase nonlinear loads, three single-phase diode rectifiers, depicted in Fig. 17, are considered in this section as three-phase unbalanced nonlinear loads [36], [37]. The parameters of these loads are $R_a = 80\ \Omega$; $C_a = 1100\ \mu$ F, $R_b = 20\ \Omega$; $C_b = 500\ \mu$F, and $R_c = 100\ \Omega$; $L_c = 30$ mH. The results obtained in this test using the three methods are shown in Figs. 18a to 18d. In this evaluation, the output current THD is not considered a comparison factor because nonlinear loads generate naturally high current harmonics.

These results demonstrate that the updated modified 3D SVPWM technique works more steadily under unbalanced nonlinear single-phase loads than do the other techniques, and the proposed technique remains capable of providing suitable ZSCC peak-to-peak values and fourth leg current oscillations.

Table 5 presents the ZSCC, output current quality, switching power losses, controllability of ZSCs, DC-bus voltage utilization, system efficiency and reliability, and parallel 4-leg inverters operational lifespan of the proposed modified 3DSVPWM technique and other existing PWM techniques they are suitable for parallel connected 4-leg inverters system control [20], [21], [30], [31], [34], [35]. Similar parameters of system and control algorithms are used for comparison including loads, switching frequency, DC-bus voltage, filter inductors and capacitors, PLL, and PI controllers. The comparison results show the superiority of the proposed modified 3DSVPWM technique in terms of ZSCC and ZSC control and suppressions, output current quality enhancement, lower switching power losses, high DC-bus voltage utilization, high

efficiency and reliability of the parallel system, and large operational lifespan of the parallel system. These gains somehow dampen the implementation complexity of the proposed technique.

VI. CONCLUSION

In this paper, a new ZSCC suppression technique for parallel connected four-leg inverter-based stand-alone power supplies under different imbalance conditions is presented. The proposed technique mainly eliminates the difference between the zero-sequence duty voltages of the parallel inverter system by using a newly modified 3DSVPWM in which the zero-vector duty ratios are adjusted by an appropriate factor provided by a ZSCC-PI command loop. This operational strategy has a significant impact on the ZSCC. The resulting control system is able not only to suppress the ZSCC but also to compensate for the fourth leg currents and mitigate the 3rd harmonic component of the output currents.

To evaluate the performance of the designed ZSCC suppression technique, comprehensive real-time simulations in which OPAL-RT5700 is used are performed under various unbalanced conditions. Compared with existing ZSCC suppression methods in parallel four-leg inverters, the proposed modified 3DSVPWM technique has the lowest ZSCC peak-to-peak value. This peak value does not exceed 0.6 A when the filter inductance and sharing current are unbalanced under balanced and unbalanced 3-phase linear loads. Additionally, the proposed technique has lower output current harmonics when compared to the other existing PWM techniques because the 3rd harmonic component is reduced to very small values in all cases of linear 3-phase loading. This result corroborates that the problems of distortion and asymmetry caused by the ZSCC under unbalanced filter inductances and unequal current sharing under both balanced and unbalanced 3-phase loads are efficiently mitigated using the suggested technique. In addition, this approach does not require any additional hardware, which makes it affordable. Furthermore, the HIL simulation results verify that the suggested control can suitably suppress the ZSCC when these parallel inverter-based standalone power supply systems supply unbalanced nonlinear loads. In future work, a simplified and generalized 3DSVPWM for multi-parallel 4-leg PWM inverters will be designed.

NOMENCLATURE

SAPSS	Stand-alone power-supply system
ZSCC	Zero sequence circulating current
ZSC	Zero sequence current
ZSV	Zero sequence voltage
C3DSVPWM	Conventional three-dimensional space vector pulse width modulation
SPWM	Sinusoidal pulse width modulation
PCC	Point of common coupling
LFHCS	Low frequency harmonic components
HFHCs	High frequency harmonic components
HEPWM	Harmonic elimination PWM method
CPSPWM	Carrier phase shift PWM method
PI	Proportional-integral controller
PIQRC	Proportional-integral quasi resonant controller
3HIPWM	Third harmonic injection PWM method
dq0	The synchronous rotating reference frame
$\alpha\beta 0$	Stationary reference frame
AVs	Active vectors
ZVs	Zero vectors
DC	Direct current
AC	Alternative current

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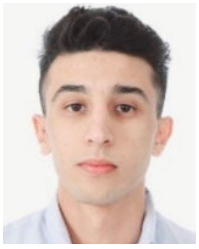
ALA ADDIN MOHAMMED AL-DWA received the master's degree in electrical engineering from the University Mohamed El Bachir El Ibrahimi, Bordj Bou Arréridj, Algeria, in 2019. He is currently pursuing the Ph.D. degree with the University of M'sila, Algeria. His current research interests include advanced and sensorless control of electrical power converters and renewable energy power systems.

ALI CHEBABHI was born in M'sila, Algeria, in 1985. He received the Engineer degree in electrical power engineering from the University of M'sila, Algeria, in 2009, and the M.Sc. degree in power electronics and the Ph.D. degree in power electronics from the University of Sidi-bel-Abbes, in 2011. He has been a Full Professor with the Department of Electrical Engineering, University of M'sila, since 2023. His research interests include advanced and sensorless control of electrical power converters and renewable energy power systems.

DJAMAL ZIANE received the Ph.D. degree in electrical engineering from the University of Abderrahmane Mira, Béjaïa, in 2010. Currently, he is an Associate Professor with the IREENA Laboratory, Department of Electrical Engineering, University of Nantes. His current research interests include advanced and sensorless control of electrical power converters, renewable energy power systems, and microgrids.

SAID BARKAT received the Ph.D. degree in electrical engineering from the National Polytechnic School of Algiers, El Harrach, Algeria, in 2008. In 2000, he joined with the Faculty of Technology, University of M'sila, M'sila, Algeria, where he is currently a Full Professor with the Department of Electrical Engineering. His research interests include renewable energy conversion, power electronics, and advanced control theory and applications.



SYPHAX IHAMMOUCHEN received the master's degree in electrical power engineering from the University of Abderrahmane Mira, Béjaïa, Algeria, in 2020, where he is currently pursuing the Ph.D. degree. His current research interests include advanced and sensorless control of control of electrical drives, renewable energy power systems, and microgrids.

TOUFIK REKIOUA received the Engineer degree from the National Polytechnic Institute of Algiers and the Ph.D. degree from I.N.P.L, Nancy, France, in 1991. He has been a Full Professor with the Department of Electrical Engineering, University of Béjaïa, Algeria, since 1992. His research interests include control of electrical drives, modelling, wind turbines, photovoltaic, and control in ac machines

HABIB BENBOUHENNI was born in Chlef, Algeria. He received the M.A. degree in automatic and industrial informatics, in 2017, and the Ph.D. degree in electrical engineering from ENPO-MA, Oran, Algeria. He is currently a Professor with Nisantasi University, Türkiye. He is an Editor of seven books and more than 200 papers in scientific fields related to electrical engineering. In recent years, he has served as a Committee Member of several scientific conferences such as ECAI-2024 and ECA-2023. He is also a Committee Member of Symmetry and EPCS journals. His research interests include the application of robust control in wind turbine power systems, active power filtering, and microgrids.

AYMAN ALHEJJI received the B.S. degree in electrical power engineering from Riyadh College of Technology, in 2007, the M.Sc. degree in engineering technology from Wayne State University, MI, USA, in 2010, and the Ph.D. degree in electrical and computer engineering from Southern Illinois University, Carbondale, IL, USA, in August 2014. Since October 2014, he has been with the Department of Electrical Engineering, Yanbu Industrial College, Saudi Arabia. He is currently an Associate Professor. His research interests include adaptive and optimal control and renewable energy power system modeling and control.