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RESEARCH ARTICLE

A Single Phase Five Level Switched Capacitor Inverter With Common Ground Configuration

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ABSTRACT In the energy sector, the application of renewable energy sources especially solar photovoltaics (PV), is expanding exponentially. Inverters find application in converting DC power from solar PV generating arrays to AC power and feeding it to grid. This study proposes a 5-level switched-capacitor multilevel inverter (SCMLI) that can be used for solar PV applications. The problem of leakage current was mitigated with the use of common ground configuration. Based on various performance parameters a comparison with recently proposed SCMLI's has been carried out. The proposed SCMLI achieves an efficiency of 95.03% under a 2-kW load. It utilizes one input DC power source, 7 switches, and 2 capacitors only. The experimental results of the proposed inverter show better harmonic profile with reduced Total Harmonic Distortion (THD). The performance of the proposed MLI topology is validated through MATLAB/SIMULINK. Moreover, loss analysis has been carried out on PLECS platform. The hardware implementation is done on a power converter test bed.

INDEX TERMS Single phase, switched capacitor, multilevel inverter, common ground.

I. INTRODUCTION

The use of renewable energy sources, namely small-scale Multilevel inverters represent a transformative advancement in power electronics, offering enhanced voltage and power capabilities compared to traditional two-level inverters. By employing multiple levels of voltage output, they effectively mitigate harmonic distortion, reduce switching losses, and improve the overall efficiency of power conversion systems. With their ability to generate high-quality AC waveforms, multilevel inverters have found widespread applications in renewable energy systems, motor drives, and grid-connected power supplies, driving innovation towards more efficient and reliable electrical infrastructure. More recently, Switched Capacitor Multilevel Inverters (SCMLI) employing a combination of switched capacitors to generate multiple voltage levels, enabling precise control over output waveforms while minimizing component count and complexity has been introduced. With their ability to achieve high-voltage outputs with reduced semiconductor requirements, SCMLIs present a promising solution for applications requiring high efficiency, reduced size, and improved reliability, thus paving the way for advancements in renewable energy systems, electric vehicles, and grid-connected power supplies. Common-Ground Switched-Capacitor Transformer less (CGSC-TL) inverters minimize the leakage current of the circuit. In order to provide different output voltage levels and achieve higher voltage gain, [1] presents a generic

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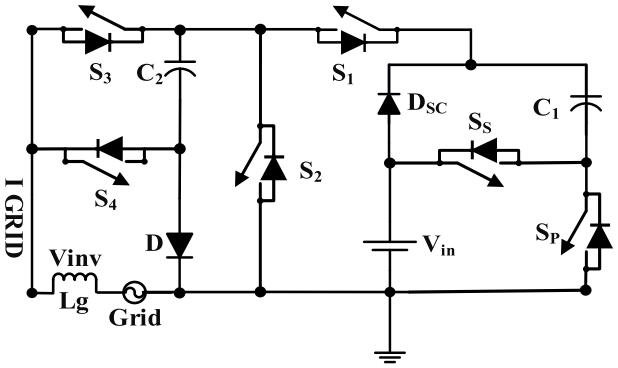

FIGURE 1. 5 level inverter topology presented in [4].

circuit layout for such converters. The first proposal describes a simple five-level (5L) CGSC-TL inverter that uses two self-balanced DC-link capacitors and eight power switches. With a double voltage enhancing function, the 5L-CGSC-TL inverter described in the study has the potential to perform quadratic boosting. Reference [2] also proposes a switched capacitor multilevel inverter (SCMLI) with boost voltage up to six times.

A transformer-less inverter requires careful consideration of factors such as isolation methods and proper grounding to ensure the safety and reliability of the overall system. A five-level common ground type (5L-CGT) transformer-less inverter topology with dual voltage boosting is introduced in [3]. The efficiency of the proposed inverter, which has eight switches arranged in a row and two capacitors charged at the input voltage level is evaluated. The research clearly proves the efficacy and feasibility of the suggested inverter design through comparisons and experimental results. A single-stage inverter, sometimes referred to as a single-stage conversion inverter, is a type of electronic device that quickly and directly transforms direct current (DC) power to alternating current (AC) power. The transformer-less grid-connected design of photovoltaic (PV) string inverters makes them a popular choice for solar energy conversion because of their economical and user-friendly features. Reference [4] presents a novel circuit design for these inverters by converting a switched-capacitor (SC) cell to series-parallel switching which is shown in figure 1. There are six unidirectional power switches with a common-grounded (CG) characteristic in the suggested structure. Compared to conventional two-level inverters, the multilevel topology has the benefit of being able to dissipate voltage stress among several components, hence reducing stress on individual sections.

A dual-mode five level common grounded type (5L-DM-CGT) was proposed in, [5] with an input range of 200-400 volt. Owing to its dual mode operation, it can be used in both the boost and buck mode of operation. The proposed inverter topology is transformerless, which makes it inexpensive and small in size. Some advantages, compared to similar 5-level topologies, include a smaller number of switches and diodes, low voltage drop across various components, and high-power density. The hardware prototype shows an efficiency of more than 97% for both modes of operation. To reduce leakage current, [6] presents a half-bridge inverter that makes use of a common ground. This is accomplished by combining a switched capacitor network with the half-bridge architecture. In [7], a sensor less voltage control is proposed for a packed U-cell containing 5 levels in the output waveforms. This control is responsible for maintaining low harmonic content in the output waveform and keeping all the 5 levels symmetric to each other by keeping the capacitor voltage (DC) fixed to half the value of input DC voltage, minimizing the complexity of the control system. An external voltage/current controller circuit is needed in grid-connected mode only. Reference [8] presents a five-level common-ground-type inverter with integrated boosting capability that is space-efficient. Because of the common ground feature, which eliminates leakage current, it is especially well-suited for solar photovoltaic applications. Two switching capacitors with self-voltage balancing capabilities that are each rated for just half of the output voltage make up the topology. This reduces the inverter's size, cost, and intricacy while also providing lower total standing voltage, a lower component count, low dv/dt, and a lower voltage in the capacitor. The grid-dependent photovoltaic (PV) inverter with transformer less (TL) and common-ground (CG) circuit topology is introduced in [9]. In the two different boost and buck operation phases, the DMSC5L-TL inverter can provide five distinct output voltage levels based on the switches' series-parallel switching transformation. The method maintains a fixed switching frequency while managing the interchange of both active and reactive power with a simple dead-beat continuous current controller (DB3C) modulation mechanism. Figure 2 illustrates a five-level (5L) single-phase common-ground inverter. This inverter employs a single-stage energy conversion setup and is capable of operating across a wide input voltage range, as introduced in [10]. The integrated SB module uses two self-balanced capacitors and one boost inductor to generate a 5L final voltage spectrum with dynamic voltage conversion capabilities. The suggested design is expanded by adding a second diode-capacitor-inductor network to the SB module and using the same SFC cell in order to obtain a quadratic voltage conversion gain.

One kind of multilevel inverter arrangement is the T-type multilevel inverter. They are compact variants of multilevel inverters that are neutral-point-clamped (NPC). Each phase in the T-type design consists of one bidirectional switching device and two conventional switching devices.

When used in the moderate switching frequency range, or between 6 and 30 kHz, T-type inverters are known for their efficiency. It features a 20% reduction in the converter's weight and dimensions, which could make it lighter and more portable than earlier models. In the T-type architecture, the series connection of many switches lowers the voltage drop for every switch. This can contribute to improved efficiency and performance in the inverter. Because of this feature, they are appropriate for high-voltage and high-wattage uses where

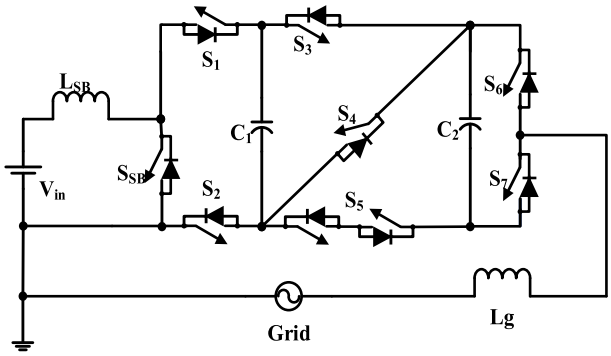

FIGURE 2. Topology of inverter presented in [10].

minimizing losses is essential. A unique 5-level inverter design with a shared AC and DC ground is demonstrated in [11]. Because of its special construction, common mode voltage issues are successfully resolved, leakage currents are avoided, and the input current in PV systems is consistently maintained. The switch triggering is controlled via a PWM approach. This design's most attractive feature is its significant voltage gain improvement, which makes gain adjustment easy to achieve by varying the modulation index. Reference [12] discusses two novel 5-level active neutral point-clamped (ANPC) inverters. For each phase, a half bridge is used to generate all 5 voltage levels of AC waveform symmetrical to each other. Balancing of voltages of DC-link capacitors is also implemented, which reduces 2 switches in each phase eliminating the need for voltage balancing controllers and sensors, which are present in conventional ANPC inverters. The efficiency of the proposed converter is claimed to be 97%. A conventional two-stage 5-level Active Neutral Point Clamped (ANPC) topology has been significantly modified in [13]. These changes include removing the use of voltage balancing controllers and sensors, the addition of cross clamping between split DC link middle points and capacitors, and the elimination of the flying capacitor. Voltage gain is one area where the improved topology is useful. Furthermore, the modifications lead to reduced voltage stress on capacitors and inverters, which improves overall performance. The integration of simulation & experimentation offers a strong basis for comprehending the performance gains resulting from the suggested modifications to the ANPC architecture.

Reference [14] presents a 5-level active Neutral Point Clamped (NPC) inverter designed for electric aircraft propulsion drive systems. In order to enhance the overall efficiency, two Silicon Carbide (SiC) switches have been used. The rest of the switches are silicon IGBTs. Furthermore, to reduce losses, Synchronous Optimal Pulse Width Modulation (SOPWM) is implemented as a modulation technique. Reference [15] discusses the reduction of ground leakage current in a 60-kW 5-level T-type ($5LT^2$) transformer less Sic photovoltaic (PV) inverter. When compared to a 3-level T-type ($3LT^2$) inverter, the resultant high frequency common mode voltage (CMV) in the $5LT^2$ inverter shows an 86% reduction. Additionally, the research explores the analysis of neutral point (NP) voltage oscillation-induced low frequency CMV. The 60-kW prototype's experimental findings demonstrate CMV's consistency with the analysis and modelling results.

Multilevel inverters employ a variety of control strategies to regulate the semiconductor device switching process. One particular technique is Pulse Width Modulation (PWM), which involves varying the pulse widths in the modulating stream in order to control the output voltage. Other popular modulation methods include Level Shifted Pulse Width Modulation (LSPWM) and Nearest Level Control (NLC). The article [16] presents a single-phase step-up multi-winding transformer-based nine-level multilevel inverter (MWTMLI) optimized for minimal device count. It employs level-shifted pulse width modulation (LSPWM) to generate levels on the load side. The proposed converters have been compared based on transformer requirements, PWM control methods, switch count, voltage stress, and gate driver requirements. The MWTMLI demonstrates satisfactory performance in both steady-state and dynamic-state scenarios. Emerging as a sophisticated tactic, Model Predictive Control (MPC) makes use of a mathematical model of the entire system to forecast future behavior and maximize control signals. Multilevel inverters have successfully used MPC to improve overall performance. The paper [17] offers a thorough analysis of a nonlinear model predictive control technique that can be used to a wide range of power electronics application. By using this strategic method, the computing effort is significantly less than with the traditional finite control set model predictive control (FCS-MPC). Notably, the recorded total harmonic distortion (THD) is demonstrated to be lower than that achieved with the MP-NLC method, thereby validating the intended enhancements. Reference [18] compares metaheuristic-based selective harmonic elimination and mitigation (SHE and SHM) with sine-triangular pulse width modulation techniques used for multilevel inverters. Also, an eight-band hysteresis control is designed to guarantee unity power factor and sinusoidal load current. Papers [19] and [20] explore the application of model predictive control (MPC) in two areas: flexible output impedance shaping for inverters in weak grids and enhanced inverter management in electric vehicle (EV) charging. Paper [19] proposes a virtual MPC-based method to improve system stability and mitigate harmonics, validated through simulations and experiments. Paper [20] introduces an efficient MPC approach for EV charging, using a discrete-time system model to ensure high-quality output voltage. Both studies demonstrate MPC's versatility and effectiveness in enhancing inverter performance, stability, and voltage quality.

Highlights of the proposed topology:

1. 5-level inverter with common ground configuration.
2. 7 switches and 2 capacitors employed in the circuit.
3. High efficiency of 96.7% at 50W of load.
4. Level-shifted PWM scheme implemented for the proposed CGSCMLI.

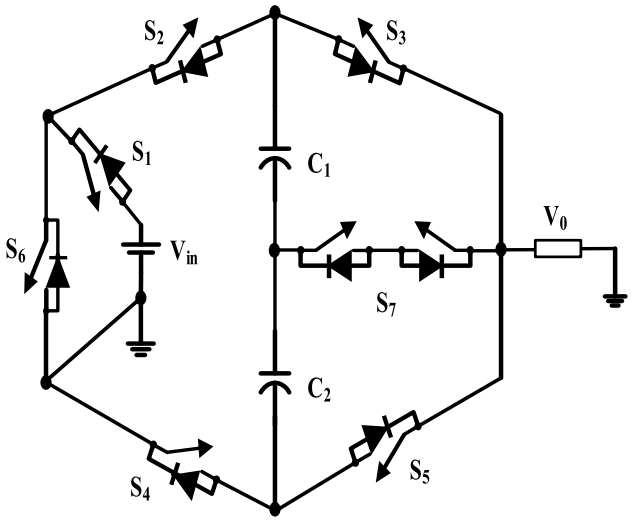

FIGURE 3. Proposed 5 level 7 switch common ground inverter (5L7SCGI).

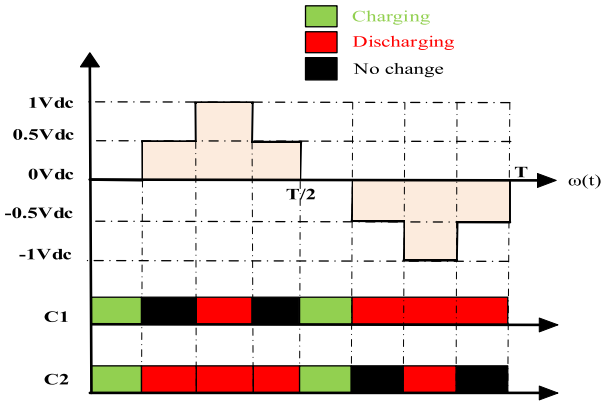

FIGURE 4. Staircase output with capacitor voltage pattern.

The paper is organized as follows: Section II delves into the design and analysis of the proposed topology. Power loss analysis, encompassing both conduction and switching losses, is detailed in Section III. Section IV provides a comparative analysis of the proposed topology with five-level inverters. Sections V and VI showcase simulation and hardware/experimental results respectively. Finally, Section VII draws conclusions based on the findings presented.

II. PROPOSED COMMON GROUND SWITCHED CAPACITOR TOPOLOGY (5L7SCGI)

The design and evaluation of the suggested 5-level Switched Capacitor Multilevel Inverter (SCMLI) are covered in this part. Figure 3 shows the proposed 5-level inverter structure. The six unidirectional switches (S_1, S_2, S_3, S_4, S_5, and S_6) and one bi-directional switch (S_7) constitute the fundamental components of the proposed Multilevel Inverter (MLI). An individual DC that naturally balance at $V_{dc/2}$. Across the load, the generated voltage waveform encompasses voltage levels of *0,* $\pm V_{dc}/2$, *&* $\pm V_{dc}$. To prevent a short circuit, it is crucial to make sure that all of the switches are not being switched on at the same time.

A. LEVEL DESCRIPTION

A thorough explanation of the working principles of the suggested 5-level Switched-Capacitor Multilevel Inverter (SCMLI) is provided in this section. TABLE 1 and figures 5A–E provide a complete overview of the conduction profiles related to each switching situation. The on as well as off states of the corresponding switches are shown by the entries correspond to the capacitors' charging, discharging, and no change states, respectively as shown in figure 4. The suggested voltage values for the topology's each and every level are shown in figures 5A–E, where conduction channels are indicated by blue lines and non-conducting paths by grey lines.

B. TOPOLOGY OPERATION ACROSS MULTIPLE VOLTAGE LEVEL STATES

This section outlines the operational principles that are proposed for the SCMLI. To obtain the numerous positive and negative output voltages, the subsequent procedures are implemented:

1) LEVEL 0: 0 V_{DC}

The four switches (S_1, S_2, S_4, and S_5) in this scenario, which is shown in figure 5A, are in a conducting condition, which corresponds to state number 3 in TABLE 1. As a result, there is no voltage generated across the load. When both C_1 as well as C_2 are being charged by Vin, this happens. Understanding this behavior can be achieved by using the given relation ($V_o = V_{in} - V_{C1} - V_{c2}$).

2) LEVEL 1: 0.5 V_{DC}

As shown by state number 2 in TABLE 1, this state's output voltage level is $V_{dc}/2$, and it can be reached by turning on three switches: S_4, and S_7. figure 5B shows the conduction diagram that represents this level. While C_2 discharges through the load, C_1 is inert during this condition and neither charges nor discharges.

3) LEVEL 2: V_{DC}

The necessary switches (S_3 and S_4) are turned on in response to the switching state number 1 shown in TABLE 1, using the energy accumulated in capacitors C_1 and C_2 to produce this specific voltage level. As seen in figure 5C, the resulting voltage for this mode of operation is V_{dc}. Both capacitors C_1 and C_2 keep discharging in this state. This state can be understood by the expression $Vo = Vc_1 + Vc_2$.

4) LEVEL 3: - 0.5 V_{DC}

In accordance with the fourth transitioning state listed in TABLE 1, switches S_2, S_6, and S_7 are engaged to generate the -0.5 V_{dc} level, as illustrated in the conduction diagram in figure 5D. In this condition, the energy stored within

TABLE 1. Switching scheme of the proposed SCMLI.

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_O	C_1	C_2
1	0	0	1	1	0	0	0	$1V_{dc}$	DIS	DIS
2	0	0	0	1	0	0	1	$0.5V_{dc}$	NCH	DIS
3	1	1	0	1	1	0	0	0	CHG	CHG
4	0	1	0	0	0	1	1	$-0.5V_{dc}$	DIS	NCH
5	0	1	0	0	1	1	0	$-1V_{dc}$	DIS	DIS

capacitor C_1 is utilized to supply the load terminals with the required amount of power.

5) LEVEL 4: - V_{DC}

The production of a voltage level whereby the final voltage across the load is $-V_{dc}$ is shown by the conduction diagram in figure 5E. As indicated in state number 5 of the TABLE 1, this state is attained by turning on switches S_2, S_5, and S_6,and making use of the energy that is stored in capacitors C_1 and C_2.

C. CONTROL SCHEME OF THE PROPOSED CGSCMLI

The control scheme used for the proposed inverter is LSPWM. To generate five levels, LSPWM primarily manipulates reference waveform levels. Precise phase correction of the reference signal for every inverter arm is necessary for the application of LSPWM.

This change introduces the phase shift that is required to achieve appropriate output voltage levels. The function is generated with the help of the circuit as shown in figure 6. The logic is implemented using sine and triangular wave as inputs and comparing these signals through relational operators. The block A represents the function generated. Figure 7 shows the level comparison of the proposed CGSCMLI with a reference value using a relational operator. Each switch receives the individual generated voltage levels and constitutes towards producing 5 level stepped output voltage waveform, shown in figure 4.

III. POWER LOSS ANALYSIS

Current is necessary for the circuit's components to operate properly and produces heat in the system. The heat produced also adds to total losses, which are primarily caused by conduction losses when electrically powered semiconductor devices conduct current and switching losses that occur when these devices switch between the ON and OFF states. To increase the effectiveness and performance of inverters, it is imperative to reduce these losses. Adopting advanced modulation techniques, choosing devices meticulously managing heat effectively, and utilizing effective control algorithms are all necessary to achieve the aforementioned objective.

A. CONDUCTION LOSSES (P_{CON})

Conduction losses are affected by the on-state resistance of the devices and the magnitude of the current flowing through them, which fluctuates based on the load. As the load increases, more current is drawn from the voltage source, resulting in higher losses and reduced efficiency. For the given CGSC MLI the total conduction loss $P_{CON_{TOTAL}}$ which depends on rms and average load current denoted by I_{RMS} and I_{AVG} respectively can be written as following

$$P_{CON\_n} = x(V_{SW\_ON} \times I_{AVG} + R_S \times I_{RMS}^2) \quad (1)$$

where, n represents individual level, & x represents the quantities of switches, while R_s stand for the resistances of switches.

$$P_{CON\_0} = 4(V_{SW\_ON} \times I_{AVG} + R_S \times I_{RMS}^2) \quad (2)$$

$$P_{CON\_1} = 3(V_{SW\_ON} \times I_{AVG} + R_S \times I_{RMS}^2) \quad (3)$$

$$P_{CON\_2} = 2(V_{SW\_ON} \times I_{AVG} + R_S \times I_{RMS}^2) \quad (4)$$

$$P_{CON\_3} = 4(V_{SW\_ON} \times I_{AVG} + R_S \times I_{RMS}^2) \quad (5)$$

$$P_{CON\_4} = 3(V_{SW\_ON} \times I_{AVG} + R_S \times I_{RMS}^2) \quad (6)$$

The equation illustrates that the sum of the conduction losses at each level yields the total conduction losses.

$$P_{CON_{TOTAL}} = P_{CON\_0} + P_{CON\_1} + P_{CON\_2} + P_{CON\_3} + P_{CON\_4} \quad (7)$$

where, $P_{CON_{TOTAL}}$ represents sum of conduction losses of all levels of the SCMLI.

Figure 8 illustrates the distribution of conduction and switching losses as a percentage across each switch. As indicated in TABLE 1, the battery is utilized solely

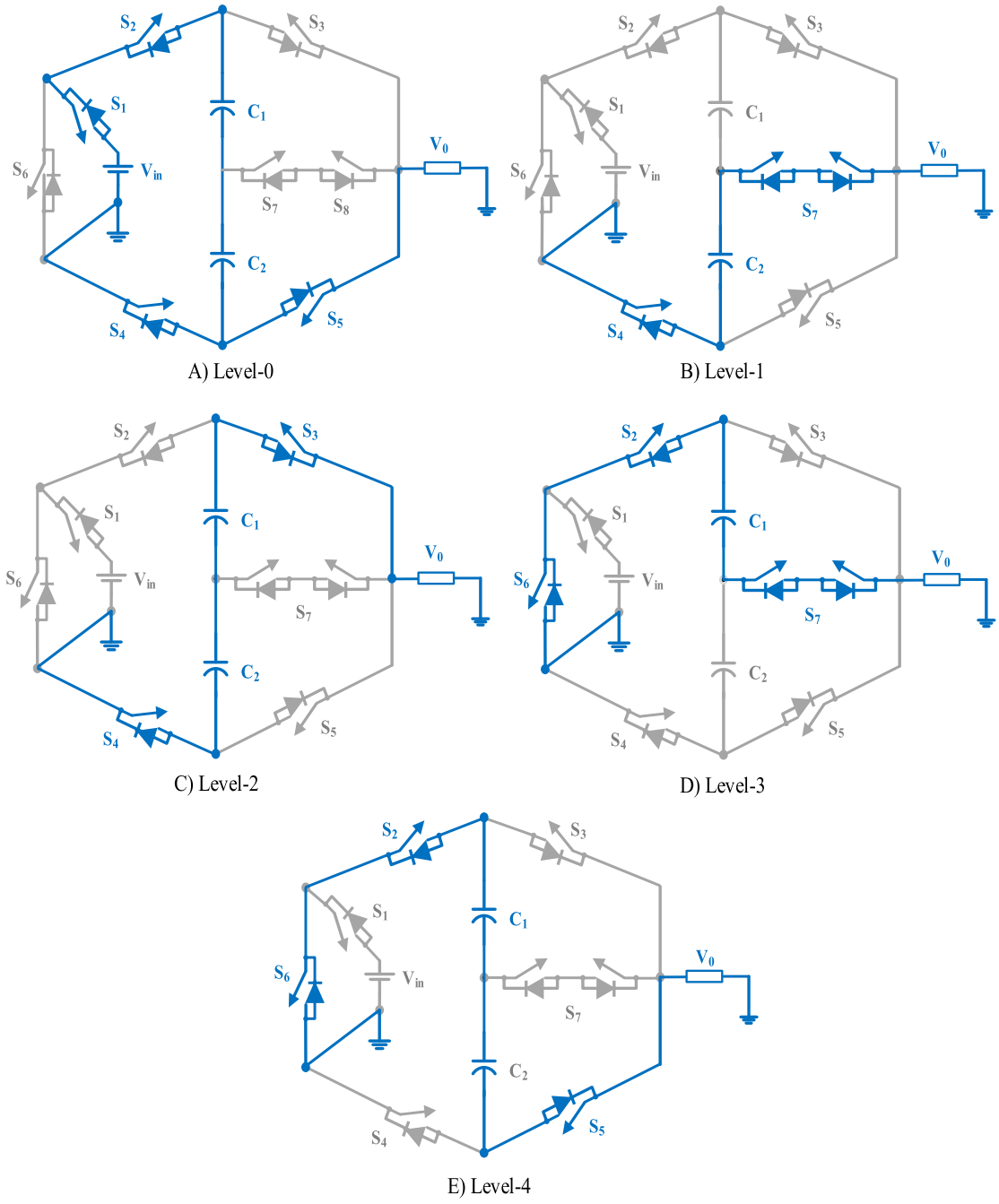

FIGURE 5. Conduction diagram of the proposed CGSCMLI.

during state 3 for both charging the capacitor and supplying current to the load. The primary factor contributing to the highest conduction loss observed in switch 1 is its engagement in the conduction mode during the third state.

B. SWITCHING LOSSES (P_{SW})

The duration required for the switch to activate and deactivate is represented by T_{ON} and T_{OFF}, respectively. Throughout these periods, the switch is in a transitional state where the current from the source is not yet reaching the load; instead, it is consumed by the switches to alter their operational states. In these transitional phases, there is a voltage drop across the switches, which adds to the switching losses. During ON state the current across the switch is I_{SW_ON} and it takes time T_{ON} to attain the voltage V_{SW_ON}.

Losses during this state are denoted by P_{SW_ON}, which is shown in the expression (8). Also T_T represents the total time of the switch ($T_{ON} + T_{OPERATING} + T_{OFF}$). Similarly, the voltage and current during the time T_{OFF} are V_{SW_OFF}

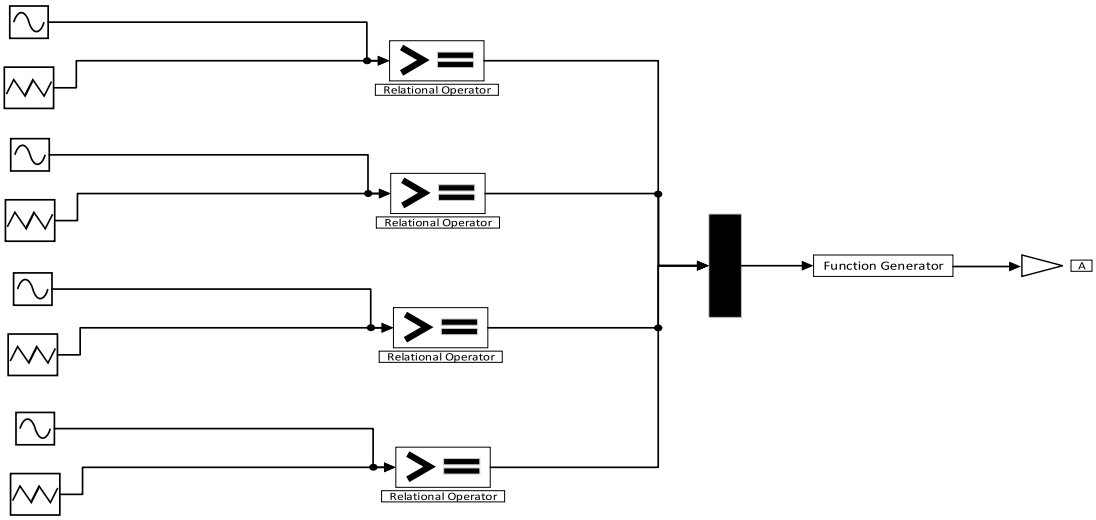

FIGURE 6. Block diagram of the function generator.

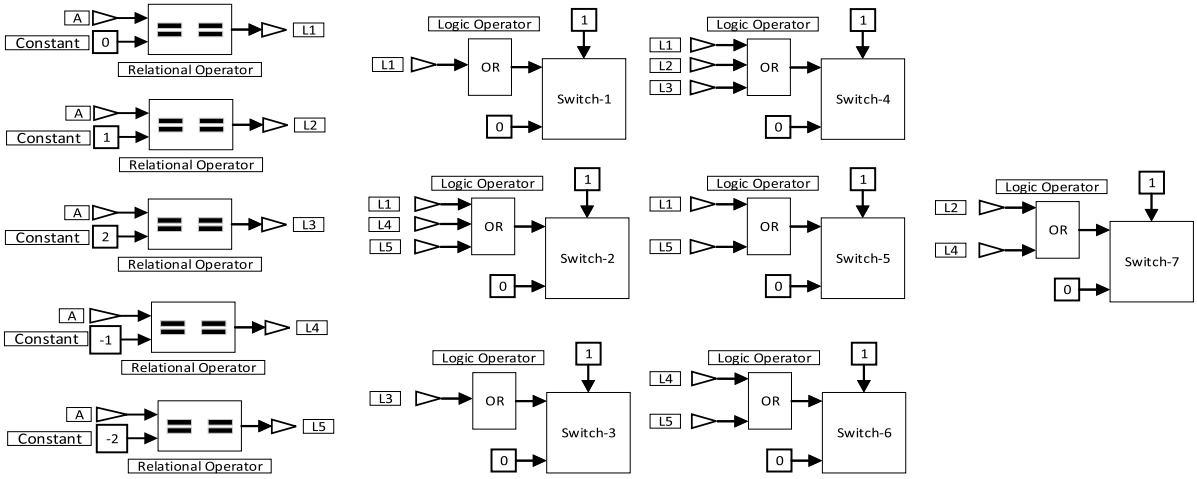

FIGURE 7. Control scheme if the proposed CGSCMLI.

and I_{SW_OFF} respectively and the power loss, $P_{SW_{OFF}}$ which is depicted in equation (9).

$$\begin{aligned} P_{SW_{ON}} &= f_{cf} \int_0^{T_{ON}} V_{SW_{OFF}} i(t) dt \\ &= f_{cf} \int_0^{TON} \frac{V_{SW_{OFF}}}{T_{ON}} (T_T - T_{ON}) \left(\frac{I_{SW_{ON}}}{T_{ON}} \right) dt \\ &= \frac{1}{6} f_{cf} \times V_{SW_{OFF}} \times I_{SW_{ON}} \times T_{ON} \end{aligned} \tag{8}$$

Similarly,

$$P_{SW_{OFF}} = \frac{1}{6} f_{cf} \times V_{SW_{OFF}} \times I_{SW_{ON}} \times T_{ON} \tag{9}$$

The number of switches in ON state and OFF state can be calculated using equation (10), where N_{ON} & N_{OFF} are the number of switches in ON and OFF states in one cycle respectively. f_{cf} and f_{mf} are the carrier frequency and modulating frequency.

$$N_{ON} = N_{OFF} = \frac{f_{cf}}{f_{mf}} \tag{10}$$

The cumulative turn-on & turn-off losses of every individual switch are summed up to get the overall switching losses for all switches using equation (11).

$$P_{SWITCHING} = \sum_{i=1}^{N_{ST}} \left(\sum_{j=1}^{N_{ON}} P_{SW_{ON}}(ij) \sum_{j=1}^{N_{OFF}} P_{SW_{OFF}}(ij) \right) \tag{11}$$

The overall efficiency of the proposed CGSC MLI is given by Efficiency,

$$\eta = \left(\frac{P_{IN} - P_{SW\_TOTAL}}{P_{IN}} \right) \times 100 \tag{12}$$

$$\eta = \left(\frac{V_{dc} \times I_{dc} - P_{LVL\_TOTAL} - P_{SW\_TOTAL}}{V_{dc} \times I_{dc}} \right) \times 100 \tag{13}$$

Figure 9 shows the efficiency of the proposed 5L7SCGI for different loads.

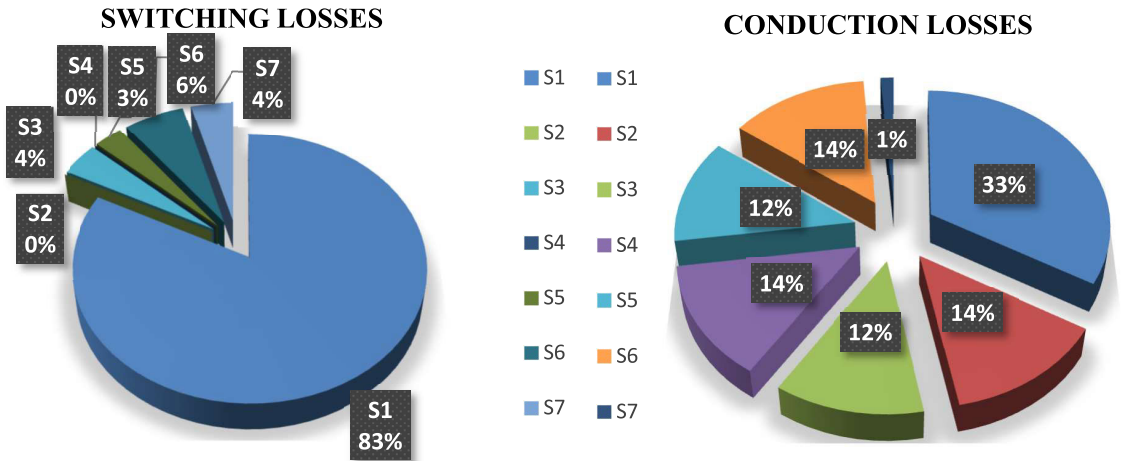

FIGURE 8. Switching and conduction losses in various switches at 50W load.

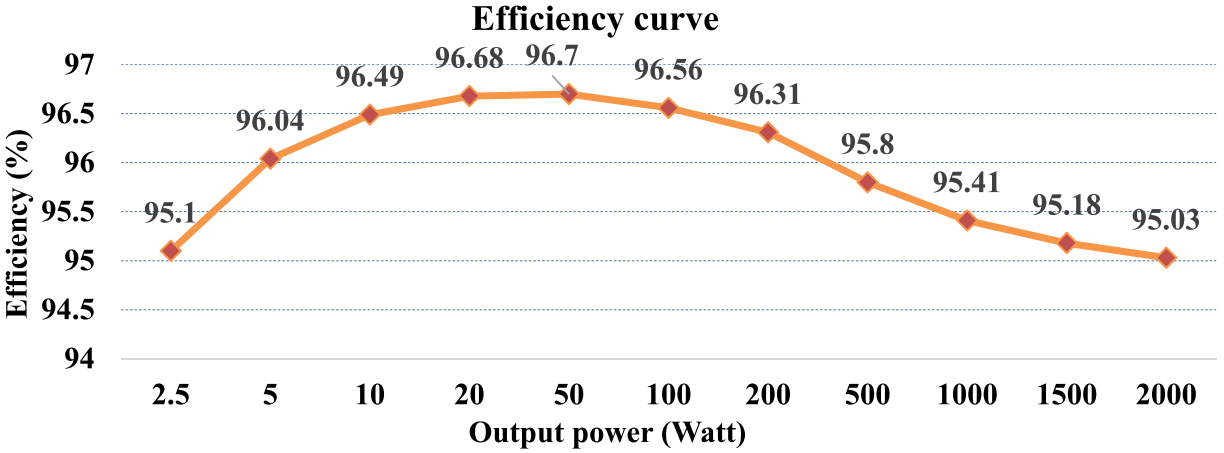

FIGURE 9. Efficiency curve for different loads.

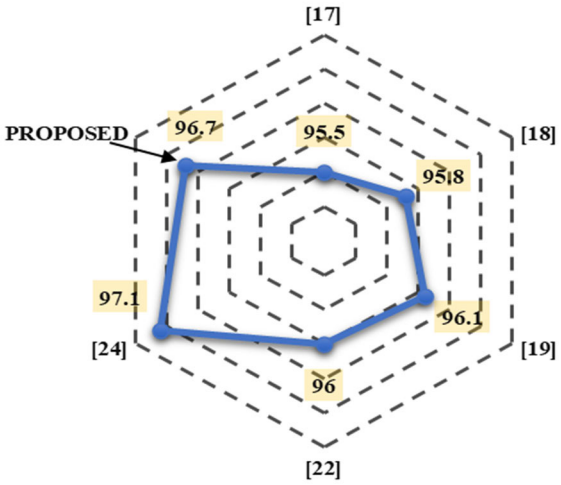

FIGURE 10. Efficiency curve for different loads.

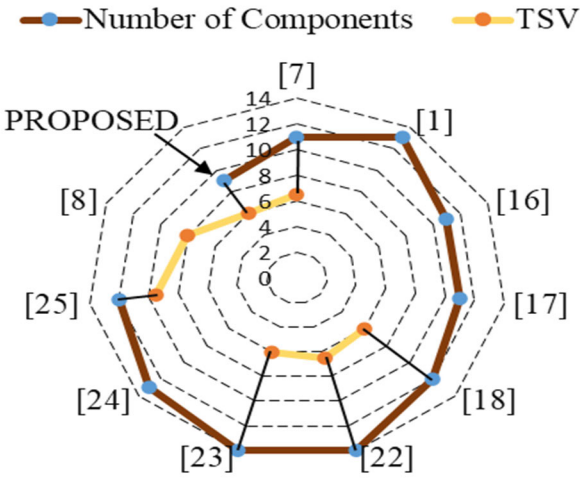

FIGURE 11. Comparison of total components and TSV of different topologies with proposed SCMLI.

IV. COMPARISON WITH OTHER TOPOLOGIES

This section looks at reported 5-level configurations to give an in-depth examination among the 5-level inverter and current topologies. TABLE 2 provides a comprehensive analysis based on a variety of factors, such as the total number

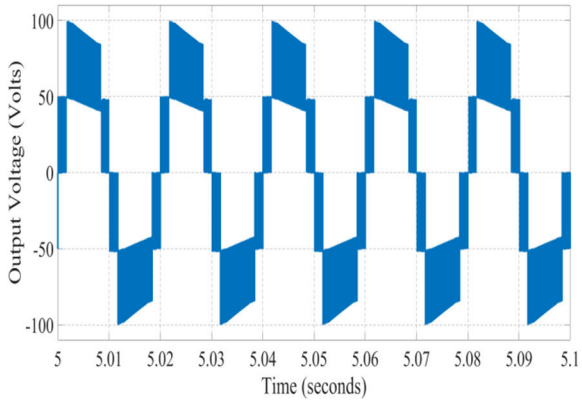

FIGURE 12. Waveform of output voltage with purely resistive load. (R = 50 Ω).

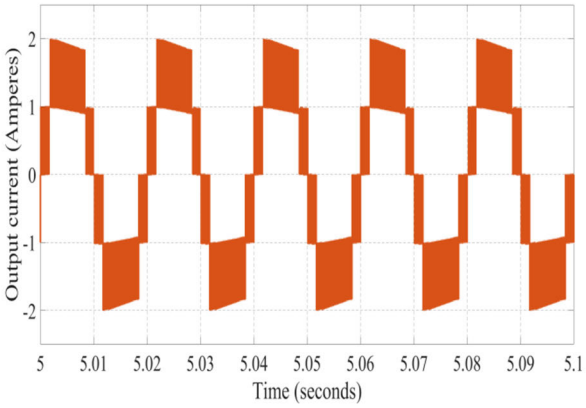

FIGURE 13. Waveform of the simulated output current using a resistive load only. (R = 50 Ω).

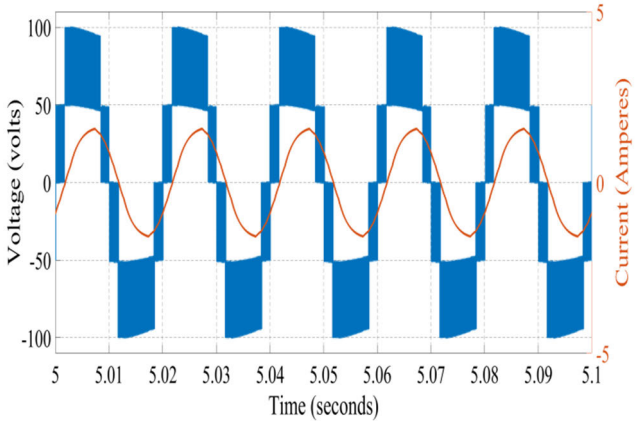

FIGURE 14. Simulated waveform of output voltage and current with RL load. (R = 50 Ω, L = 100 mH).

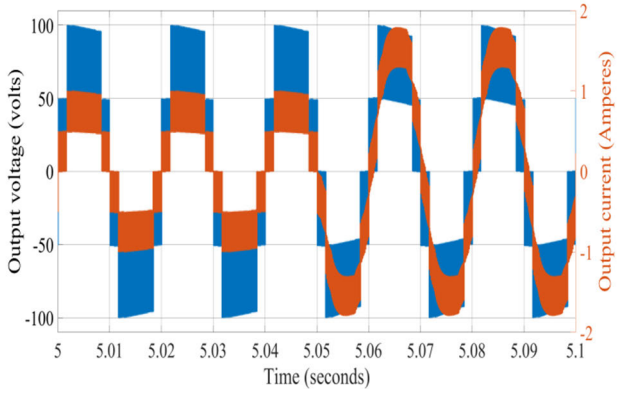

FIGURE 15. Simulated waveform of output voltage and current during the transition from R to RL load. (R = 50 Ω, L = 100 mH).

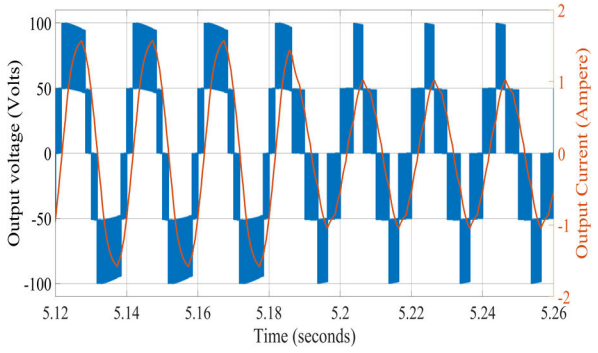

FIGURE 16. Simulated voltage and current waveforms for the suggested SCMLI system while varying the modulation index from 2-1.1.

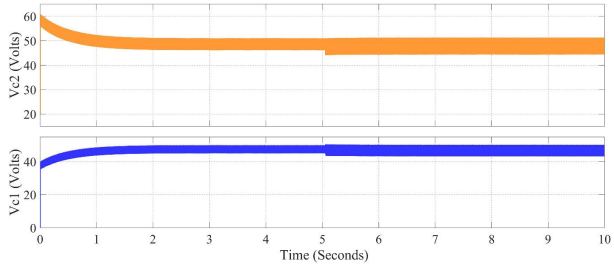

FIGURE 17. Simulated waveform of the capacitor voltage.

of components, inverter voltage gain, efficiency, quantity of switches (S), diodes (D), inductors (L) and capacitors (C), as well as the total standing voltage (TSV) in per unit (p.u.). Voltage values for the switches within the topology are influenced by total standing voltage (TSV), which is defined as the total of all peak voltage strains across the switches. The proportion of TSV compared to the maximum value corresponding to the AC voltage that is generated is expressed as TSV (p.u.). TABLE 2 elaborates on the topologies' comparative features and sheds light on these factors. TABLE 2 shows that all of the topologies that are illustrated demands a greater number of components than the design that has been proposed in order to achieve a 5-level output voltage. It is worth noting, nevertheless, that some topologies show a voltage gain that is greater than the suggested one.

A variety of inverter types have been considered in addition to the multilevel Common Ground based Transformer less (CG-based TL) inverters in order to perform

TABLE 2. Comparison with other topologies.

Topology	S	D	C	L	Total components	Gain	TSV(p.u)	Efficiency (%)
[8],**2023**	7	2	2	-	11	2	6.5	97.59
[1],**2021**	8	0	3	2	13	2	5.5	98.3
[22],**2020**	6	1	3	1	11	1	5	95.8
[23],**2021**	7	0	3	1	11	1	5	95.5
[24],**2020**	7	1	3	1	12	2	6	95.8
[4], [25], [26] **,2020 & 2021**	6	2	3	1	12	2	4.5	96.1
[27],**2021**	8	0	4	2	14	1	6.5	96
[28],**2020**	8	1	3	2	14	1	6	96.8
[9],**2021**	9	2	3	-	14	2	8	96.76
[29],**2023**	6	3	3	-	12	2.5	9.5	96.87
Proposed	7	0	2	0	9	1	6	96.7

a comprehensive and fair comparison. Numerous modern Active-Boost-Neutral Point Clamp (ABNPC)-TL inverters that use the Sinusoidal Pulse Width Modulation (SPWM) approach for multilayer output voltage production are among them, as is the 5LH8-TL inverter that is evaluated as in [27]. TL inverters based on ABNPC technology notably use the mid-point clamping method in place of the CG-based idea. Consequently, the aforementioned inverters do not fully address the challenge of leakage current, in contrast to the suggested network topology and their associated CG-based counterparts. Additionally, these inverters have limited static voltage gain and have a maximum output voltage limit of a certain value. Series-parallel switching is used by the 5LH8-TL inverter variant's Integrated Sinusoidal Pulse Width Modulation (SPWM) cell, as described in [27]. Leakage current is still a problem even though the inverter can restrict its common-mode voltage to half the input DC source value.

Achieving a wider range of voltage levels while reducing the overall number of components is the primary goal of practical inverters. TABLE 2 shows that the recommended inverter has the fewest components compared to the other topologies that are being investigated. The total number of both active and passive components used in network [26] and the associated TSV rating are larger since the configuration makes use of a greater number of switches compared with the suggested one. Moreover, [26] uses additional DC-link capacitors to produce a 5L output voltage than the suggested one, and its dc voltage use is also higher. Although some of the 5LCG-based topologies in this case might have fewer power switches than the one that is suggested, they frequently require more power diodes or face difficulties because of significant input voltage demand and complicated charging procedures. The DC-linked input capacitor intended for solar power applications and the suggested output filter is described in [1]. A comparison of the total number of components of different topologies with the proposed SCMLI

TABLE 3. Simulation parameters of the proposed SCMLI.

Parameters	Values
DC source voltage	100 volts
Peak output voltage	100 volts
Inductance of load	100 mH
Load resistance	50 Ω
Capacitors	2200 μF
Frequency	50 Hz

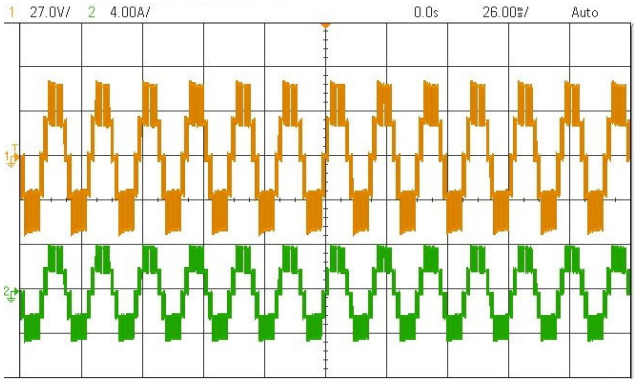

FIGURE 18. Waveform of output voltage and current waveforms with purely resistive load (R = 10 Ω).

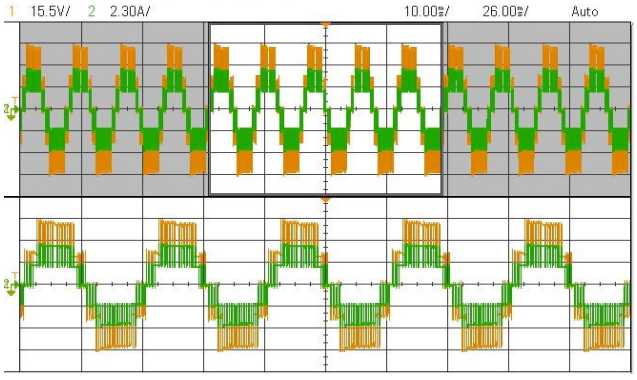

FIGURE 19. Magnified waveform of output voltage and current waveforms with purely resistive load (R = 10 Ω.

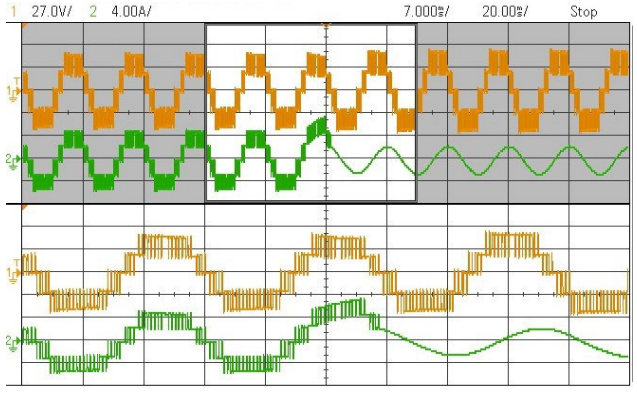

FIGURE 20. Magnified voltage and current waveforms for the output during the transition from R to RL load. (R = 10Ω, L = 100 mH).

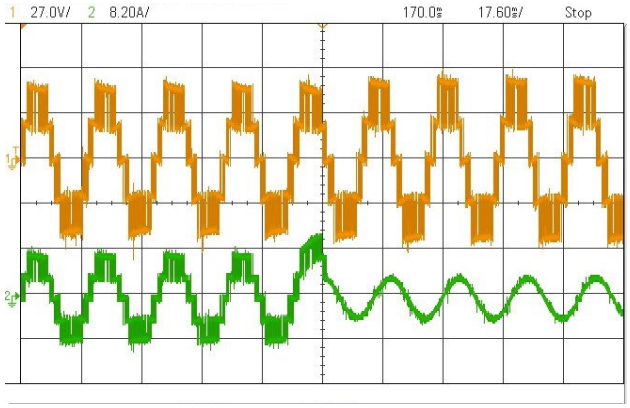

FIGURE 21. Voltage and current waveforms for the output during the transition from R to RL load. (R = 10 Ω, L = 100 mH).

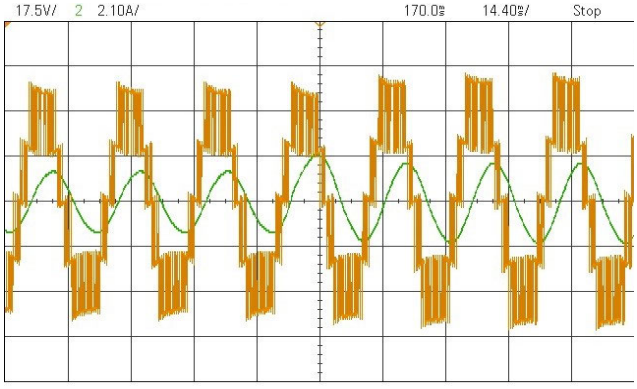

FIGURE 22. Waveform of output voltage and current with RL load. (R = 10Ω, L = 100 mH).

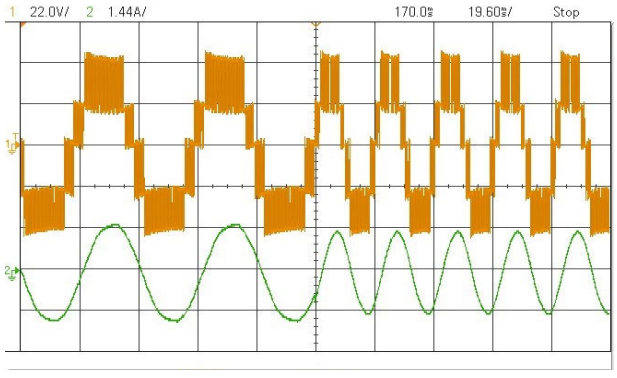

FIGURE 23. Voltage and current waveforms for a proposed SCMLI when the frequency is doubled.

is shown in figure 11. In comparison to the recommended architecture, the result shows a reduced Total Switching Loss (TSV) and requires the use of more switches, but it still offers a gain of 2. In comparison to the suggested inverter, [23] and [27] likewise have the same TSV value, but at the expense of utilizing more diodes and inductors. An overall comparison for TSV of different topologies has been shown in figure 11.

Figure 10 illustrates a comparison of the efficiency of various 5-level inverter topologies under a 1 kW load. Among these, the proposed SCMLI stands out with the maximum efficiency, reaching 96.7%. Remarkably, this superior performance is achieved with a minimal number of components, highlighting the efficiency and simplicity of the SCMLI design.

V. SIMULATION RESULTS AND ANALYSIS

The simulation results for the proposed 5-level inverter topology pursuant to various loading conditions are presented

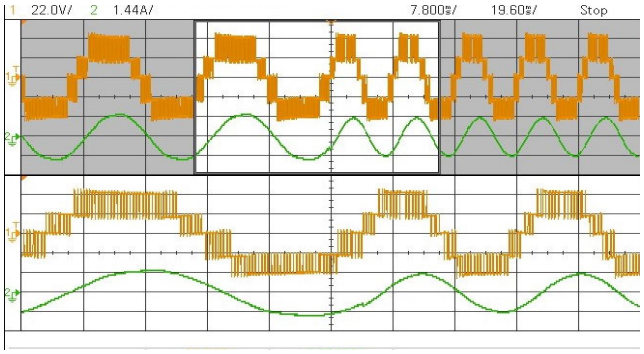

FIGURE 24. Voltage and current waveforms for a proposed SCMLI system when the frequency is doubled.

TABLE 4. Experimental parameters of the proposed 5L7SCGI.

Parameters	Values
DC source voltage	40 volts
Inductance of load	100 mH
Load resistance	10 Ω
Capacitors	2200 µF
Switches	IKW75N60H3
Frequency	50 Hz

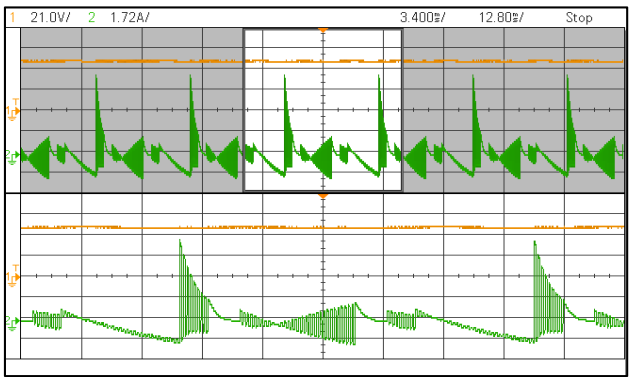

FIGURE 25. Capacitor voltage and current waveform of the proposed inverter.

in this section. MATLAB/Simulink software is utilized to simulate the proposed topology for a five-level setup. A variety of simulation results achieved for the 5-level SCMLI configuration are shown in figure 12 to figure 16. The output voltage and current waveforms of the suggested 5-level inverter for a solely resistive load (R = 50 Ω) are shown

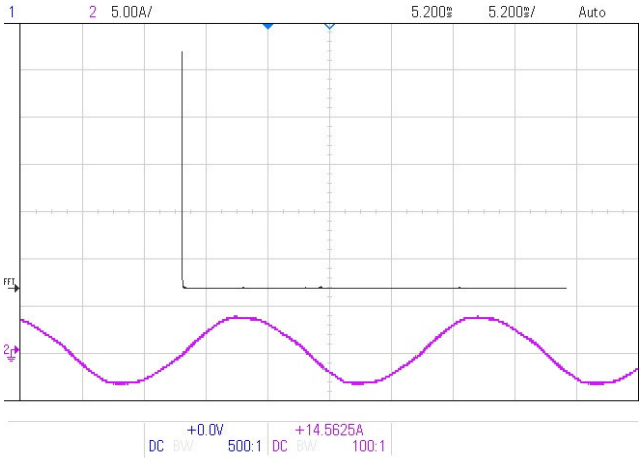

FIGURE 26. Harmonic profile of the current (THD in current is 1.2%) of the proposed inverter in RL load. ($R = 10\Omega$, $L = 100$ mH).

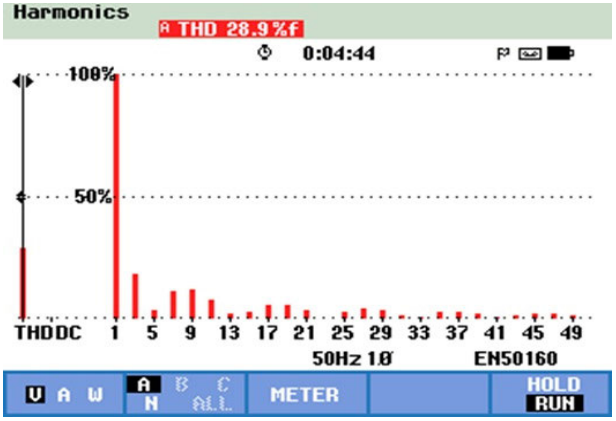

FIGURE 27. THD waveform of the hardware test bed for the proposed 5L7SCGI.

in figure 12 and figure 13 respectively. The generated voltage waveform produced by the SCMLI shows five levels, each of which corresponds to a different voltage magnitude, as seen in figure 12. Figure 14 illustrates the voltage and current waveforms corresponding to an RL load consisting of a resistance (R) of 50 Ω and an inductance (L) of 100 mH. Because of the inductive characteristics of the load, there is a phase shift between the voltage and current waveforms. The voltage waveform's frequency and inductance value both affect how much of a phase shift occurs. Notably, the current waveform exhibits lesser harmonic distortion than the voltage waveform and closely resembles a sine wave at precisely the same frequency as the waveform of the output voltage.

The voltage and current waveforms at the time of the dynamic load transitioning from a load resistance of 50 Ω to a load resistance of 100 Ω, together with a load inductance of 100 mH, are shown in figure 15. The circuit dynamics are affected when a load is changed from being solely resistive (R-load) to being both resistive and inductance (RL load). An R-load has a power factor of 1 because the load current is

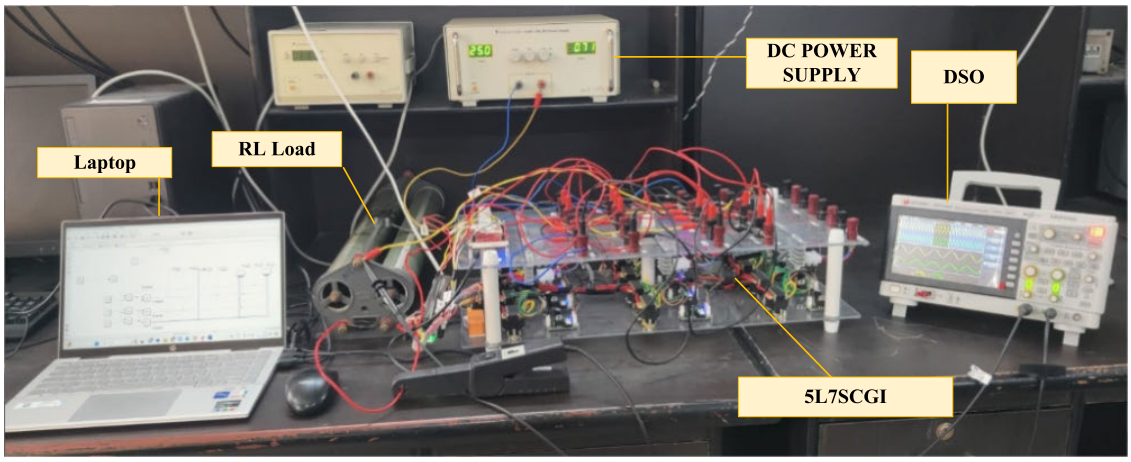

FIGURE 28. Hardware test bed for the proposed 5L7SCGI.

precisely proportional to the voltage. But for an RL load, the load current falls behind the voltage, which reduces the power factor. The SCMLI may need to modify its control strategy in order to maintain effective and stable performance as a result of this change in load impedance. In particular, as a consequence to the modification of load characteristics, the inverter's duty cycle and switching frequency may need to be adjusted in order to maintain a desired output voltage range and reduce harmonic distortion. The effects of changing the modulation index from M = 2.0 to M = 1.1 on the overall system are shown in figure 16. The output levels remain unchanged as the index of modulation moves from 2.0 to 1.1, but the peak intensities of the voltage and current waveforms vary in proportion. Thus, a commensurate modification is experienced by the output power. Despite these variations in amplitude, it is critical to keep in mind that the contour of the waveform and the phase relationship between the current and voltage waveforms remain unaltered. The simulated waveforms of the capacitor voltages are shown in figure 17. TABLE 3 provides a detailed presentation of various characteristics relevant to simulations, offering comprehensive information on key aspects and parameters involved in the simulated scenarios or experiments.

VI. EXPERIMENTAL RESULTS

The experimental parameters have been listed in TABLE 4 and the setup of the proposed 5L7SCGI. The hardware results of the proposed prototype are shown in figure 18 to figure 28. Waveforms of 5-level output voltage and current for R = 10 Ω are shown in figures 18 and 19. Modifications in load from R to RL is shown in figures 20 & 21. A power factor of one indicates that the phases of voltage and current are perfectly aligned in purely resistive loads. Nevertheless, a phase shift between the current and voltage may happen when resistive loads with inductance are added (RL loads), which will lower the power factor. Reactance is also introduced by the inductance, which alters the impedance characteristics of the load in comparison to purely resistive loads. Because of this phase shift and the reactive power present, both current and voltage waveforms may become distorted. This could have an impact on system performance, especially in applications where waveform integrity is crucial. The waveform of voltage and current for RL load has been depicted in figure 22. Figures 23 & 24, illustrate the response of the output voltage and current to variations in the modulation frequency, which alters the impedance characteristics of the load in comparison to purely resistive loads. Because of this phase shift and the reactive power present, both current and voltage waveforms get distorted. This could have an impact on modulating frequency.

The data depicted in figures 23 and 24 is derived by doubling the modulating frequency. Figure 25 shows the waveform of the capacitor voltage (V_{c1}) and capacitor current (I_{c1}) on hardware test bed of the proposed 5L7SCGI. A frequency is said to be harmonic if it is an integral multiple of the fundamental frequency. Non-linear burdens, switching devices, or errors in the system are some of the possible causes of these extra frequencies. To avoid challenges like greater losses, equipment overheating, and interference with delicate electronics, power systems must effectively manage harmonics.

Harmonic distortion is a prevalent problem that multilevel inverters have to be addressed to ensure efficient and reliable performance. Typical techniques include encompass filtering, harmonic mitigation initiatives, and standard compliance. Figures 26 and 27 illustrates the harmonic profile of the proposed inverter, with a vertical line highlighting the first harmonic. Harmonics beyond the first are also present within the graph, albeit with magnitudes that are notably smaller in comparison. The hardware test bed of the proposed converter in the figure 28. The proposed inverter has been realized on a generalized converter test bed with high IGBT ratings. If a prototype of the inverter is developed then lower rating IGBT will be sufficient for it. For practical realization same has been selected with IGBT IKW75N60H3 (600V/75A) configuration which has nearly same parameters for performance of topology.

VII. CONCLUSION

The novel 5-level Common Ground Switched Capacitor Multilevel Inverter (CGSCMLI) structure presented in this paper has been created particularly for solar PV applications. The suggested arrangement makes use of a single DC-source setup with 1 bidirectional and 6 unidirectional switches. A detailed comparison with recent studies is done to analyze its benefits. Additionally, the circuit's capacitors are entirely self-balancing, which reduces complex control issues. LSPWM, a simple modulation technique, is used to generate gating pulses for IGBTs. Using a prototype, experimental verification of the suggested 5-level SCMLI is done in a variety of operational environments. The proposed 5L7SCGI shows the maximum efficiency of 96.7% at supply voltage of 100 volts and load of 50 Watts, which can be used in energy storage systems, electric vehicles, and renewable energy sources like wind and solar power. Further developments in components and materials could lead to the creation of more complex SCMLI topologies with higher efficiency and low conduction and switching losses.

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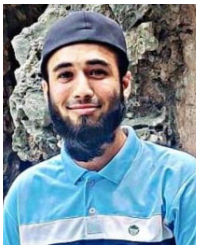

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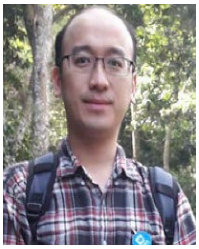

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