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RESEARCH ARTICLE

Analysis and Design of a Single-Phase Half-Bridge Rectifier With an Active DC Bus

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ABSTRACT This paper introduces the concept of an active DC. The active DC bus consists of a reduced passive DC bus and an Active Resonant Voltage Balancer (ARVB). The ARVB, operating as a series resonant converter, reduces the DC bus current ripple by injecting balancing current into the DC bus mid-point. This injected current effectively counteracts the fundamental component of the current flowing to the mid-point of the DC bus, resulting in a significant reduction in both the gravimetric and volumetric volume of the DC bus. The proposed concept is thoroughly analyzed through a case study involving a single-phase half-bridge rectifier application. Through theoretical analysis and experimental validation, the usefulness and feasibility of the proposed concept are demonstrated, showing in the presented case study a reduction of the DC bus volume by a factor of 4 at the expense of an increase in losses. The concept represents a viable option in power conversation applications where volume and weight reduction and optimization are required.

INDEX TERMS Rectifiers, resonant converters, DC bus.

I. INTRODUCTION

Three-phase induction motors have been the most popular motors in electric drive applications since the days of Tesla [1], [2], [3], [4], [5]. The three-phase induction motors are more efficient, less expensive, last longer and have better torque/speed characteristics than single-phase motors. However, the three-phase public grid is often not available, especially in rural areas where it may not be economical to install a three-phase distribution network. Therefore, conversion from single-phase to three-phase is necessary. Single-phase to three-phase conversion cannot be achieved with passive devices such as transformers. For these applications, more complex conversion systems, such as rotary converters (motor-generator sets) or solid-state power converters are used. The first solution has no practical value in the era of advanced power converters. Solid state single-phase to three-phase [6], [7], [8] and three-phase to single-phase [9] power converters are only alternative.

Traditionally, the single-phase converter (rectifier/inverter) is a full bridge pulse width modulated (PWM) converter. A well-known issue with this type of single-phase full bridge system is the power ripple at twice the grid frequency. This has a direct impact on the design of the converter DC bus. The DC bus must be designed to keep the DC bus voltage ripple below the limit and to sustain large 2^{nd} harmonic current ripple [10], [11], [12], [13], [14], [15], [16].

In some cases, a half bridge rectifier with voltage booster is used [6], [7]. Typical applications are: 400/230V variable speed drives (VSD) operating on 230/110V mains, FIGURE 1 (a) or three-phase UPS operating on single phase load [9] (b).

In this case, the DC bus current is comprised dominantly by fundamental frequency (the 1^{st} harmonic) current. As the

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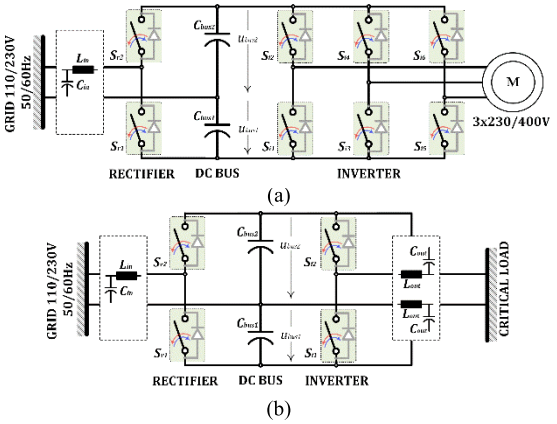

FIGURE 1. Typical applications of single-phase half bridge rectifier. a) Single-phase to three-phase Variable Speed Drive (VSD), b) Single-phase to single-phase UPS.

consequence, the DC bus must be significantly larger than in case of a full bridge configuration.

Traditionally electrolytic capacitors are used to build a bulky DC bus capacitor bank.

This is an issue when compact design is required. To reduce the size of the bulky DC bus, several active solutions have been proposed [11], [12], [13], [14], [15], [16], [17], [18], [19], [20].

The main difference, between the state of the art and the proposed solution in this paper, is that the existing solutions propose to compensate the low frequency voltage ripple, while the proposed solution, proposes to compensate the low frequency current ripple instead. The compensation of the lower frequency voltage ripple requires a more elaborate controller, while the proposed method is based on the open loop control which is self-regulating.

In this paper, an active balancing circuit is proposed, analyzed and test results are presented. The active balancing circuit injects a balancing current into a mid-point of the DC bus. The solution is based on a resonant converter that eliminates the fundamental frequency current from the DC bus in the single-phase half bridge application. Compared to a conventional single-phase half-bridge application, the total DC bus volume including the active balancing circuit is reduced by nearly a factor of 4 compared to the passive bulky DC bus.

A. BRIEF ANALYSIS OF AN ORDINARY RECTIFIER DC BUS CAPACITOR CURRENT

Circuit diagram of an conventional half-bridge rectifier is depicted in FIGURE 2. The rectifier consists of an input (boost) inductor L_{in}, two bidirectional switches S_{r1}, S_{r2} and spilt DC bus capacitor C_{bus1}, C_{bus2}. The rectifier input is the grid denoted as an ideal voltage source $u_{in}(t)$, while the load is designated as DC LOAD.

Let's the rectifier input current $i_{in}(t)$ and voltage $u_{in}(t)$ be:

$$\begin{aligned} i_{in}(t) &= \sqrt{2} I_{in} sin(\omega t + \varphi) \\ u_{in}(t) &= \sqrt{2} U_{in} sin(\omega t) \end{aligned} \tag{1}$$

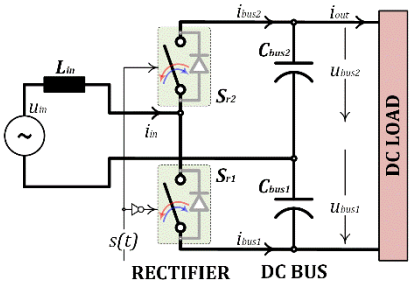

FIGURE 2. Single-phase half-bridge rectifier.

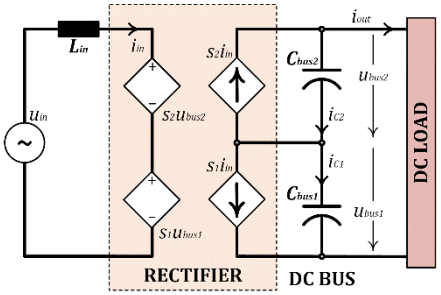

FIGURE 3. Switching mode model of single-phase half-bridge rectifier.

where U_{in} is the grid rated RMS voltage, I_{in} is the rectifier rated RMS current and φ is the current phase displacement.

For generality of the analysis, the current displacement φ can be any in a range between $\pi - /2$ and $\pi/2$. The rectifier efficiency is assumed close to unity.

The rectifier modulation index is defined as

$$m = \frac{1}{2}\left(1 + M_0 sin(\omega t)\right) \text{ and } M_0 = \frac{2\sqrt{2}U_{in}}{U_{out}} \tag{2}$$

where M_0 is the rectifier modulation depth.

B. THE DC BUS CAPACITOR CURRENT STRESS

The DC bus capacitors current can be computed using an equivalent model depicted in FIGURE 3. The DC bus capacitor current is given by the following equation.

$$\begin{aligned} i_{C2}(t) &= s_2(t)\, i_{in}(t) - i_{out}(t) = s(t)\, i_{in}(t) - i_{out}(t) \\ i_{C1}(t) &= -s_1(t)\, i_{in}(t) - i_{out}(t) \\ &= -\left(1 - s(t)\right) i_{in}(t) - i_{out}(t) \end{aligned} \tag{3}$$

where $i_{out}(t)$ is the dc side load current and $s(t)$ is the rectifier switching function [20], [21], [22].

Generally speaking, the capacitors current (3) can be decomposed in two different frequency ranges: namely low frequency current $i_{LF}(t)$ and high frequency current $i_{HF}(t)$.

The low frequency current $i_{LF}(t)$ is mainly fundamental frequency and its harmonics. The high frequency current $i_{HF}(t)$ is the switching frequency current and the related harmonics. In the analysis that follows, the total RMS and low frequency RMS current will be computed. Then, high frequency component will be computed from the total and the low frequency component.

1) TOTAL RMS CURRENT

Let $x(t)$ be a multi-periodic variable with sub-period of T_{sw} and fundamental period of T. It could be proven that total RMS value of the variable $x(t)$ is

$$X_{(rms)} = \sqrt{\frac{1}{T}\int_0^T \left\langle x_{(rms)}\right\rangle^2(t)dt} = \sqrt{\frac{1}{T}\frac{1}{T_{sw}}\int_0^T\int_t^{t+T_{sw}} x^2(\tau)\,d\tau dt}, \tag{4}$$

where $\left\langle x_{(rms)}\right\rangle(t)$ is one cycle RMS value.

$$\left\langle x_{(rms)}\right\rangle(t) = \sqrt{\frac{1}{T_{sw}}\int_t^{t+T_{sw}} x^2(\tau)\,d\tau} \tag{5}$$

Substituting (1)-(3) into (4) and (5) yields the capacitor one-cycle (moving) RMS $\left\langle i_{C(rms)}\right\rangle(t)$

$$\left\langle i_{C(rms)}\right\rangle(t) = \sqrt{m(t)i_{in}^2(t) - 2I_{out}m(t)i_{in}(t) + I_{out}^2} \tag{6}$$

Total RMS current $I_{C(rms)}$ is computed from (6) as

$$I_{C(rms)} = \sqrt{\frac{1}{T_0}\int_0^{T_0}\left\langle i_{C(rms)}\right\rangle^2(t)\,dt} = I_{in}\sqrt{\frac{1}{2} - \left(\frac{U_{in}}{U_{out}}cos\varphi\right)^2} \tag{7}$$

2) LOW FREQUENCY CURRENT

To calculate low frequency RMS current, we can use two methods: 1) Frequency decomposition and 2) One cycle averaging. The frequency decomposition method is the Fourier analysis, applied on (3). Such approach can be complicated and not practical. The one-cycle averaging method [20], [21], [22] is basically filtering of high frequency component of the current. The filtered current (one-cycle average) is remaining low frequency component. This method will be used to calculate the capacitor low frequency RMS current.

Applying moving averaging technique [19], [20], [21], [22], on (3), yields the DC bus capacitor current averaged over one switching cycle T_{sw}

$$i_{C1(2)} = \pm\frac{\sqrt{2}}{2}I_{in}sin(\omega t + \varphi) - I_{in}\left(\frac{U_{in}}{U_{out}}\right)cos\,(2\omega t + \varphi) \tag{8}$$

where U_{out} is the rectifier DC bus (output) voltage respectively.

Please notice from (8) the DC bus capacitor current $i_{C1(2)}$ consists of two main components: Fundamental frequency (the 1^{st} harmonic), and the 2^{nd} harmonic. The RMS value of fundamental frequency and the 2^{nd} harmonic are respectively:

$$I_{C(rms)}\big|_{50Hz} = \frac{1}{2}I_{in}$$
$$I_{C(rms)}\big|_{100Hz} = \frac{1}{\sqrt{2}}I_{in}\left(\frac{U_{in}}{U_{out}}\right) \tag{9}$$

3) SWITCHING FREQUENCY RMS CURRENT

The switching frequency RMS current can be computed from the Parseval theorem [21], [23] as

$$I_{HF(rms)} = \sqrt{I_{C(rms)}^2 - \left(I_{C(rms)}^2\big|_{50Hz} + I_{C(rms)}^2\big|_{100Hz}\right)}. \tag{10}$$

Substituting (7) and (9) into (10) yields the capacitors HF RMS current

$$I_{HF(rms)} = I_{in}\sqrt{\frac{1}{4} - \left(\frac{U_n}{U_{out}}\right)^2\left(\frac{1}{2} + cos^2\varphi\right)} \tag{11}$$

C. DC BUS CAPACITORS LOSSES

For generality of the analysis, let's assume the DC bus capacitor current is a periodic function defined as

$$i_C(t) = \sum_{n=1}^{\infty}\sqrt{2}I_n sin\,(n\omega t + \varphi_n)\,. \tag{12}$$

The capacitor internal resistance *ESR* is frequency dependent resistance [21], [24]. The voltage across equivalent series resistance ESR can also be expanded in a Fourier series.

$$u_{esr}(t) = \sum_{n=0}^{+\infty}R_{C0}(n\omega)\sqrt{2}I_{C(n)}sin\,(n\omega t + \varphi_n) \tag{13}$$

where $R_{C0}(n\omega)$ is the frequency dependent *ESR* [21], [24]. From (12) and (13) we have instantaneous power

$$p(t) = \sum_{n=0}^{+\infty}\sqrt{2}I_{C(n)}sin\,(n\omega t + \varphi_n) \times \sum_{n=0}^{+\infty}R_{C0}(n\omega)\sqrt{2}I_{C(n)}sin\,(n\omega t + \varphi_n) \tag{14}$$

Average power is computed from (14) as described in [21],

$$P_C = \sum_{n=0}^{+\infty}R_{C0}(n\omega_0)\,I_{C(n)}^2. \tag{15}$$

DC bus capacitor losses can also be computed as

$$P_C = R_{C0(100Hz)}I_{eq(rms)}^2 \tag{16}$$

where $R_{C0(100Hz)}$ is the capacitor *ESR* at the base frequency of 100Hz. $I_{eq(rms)}$ is the capacitor equivalent RMS current defined by (17).

$$I_{eq(rms)} = \sqrt{\sum_{n=1}^{\infty}\frac{I_n^2}{k_n}}, \tag{17}$$

where k_n is the capacitor current-to-frequency scaling factor [21], [24]. Typical k_n function is depicted in FIGURE 4.

Substituting (9) and (11) into (17) yields the total equivalent capacitor RMS current (18), as shown at the bottom of the next page, where k_{50} and k_{HF} are the current scaling factors at 50Hz and the switching frequency.

FIGURE 5 shows the DC bus capacitor currents versus the input RMS voltage U_{in}. The DC bus voltage and power are $U_{out} = 700V$ and $P_{out} = 3300W$ respectively.

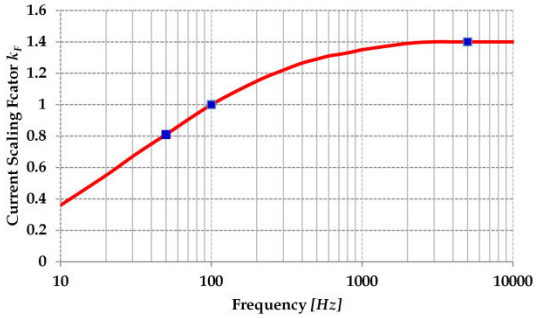

FIGURE 4. Typical characteristics of a large electrolytic capacitors; the ESR versus frequency [24].

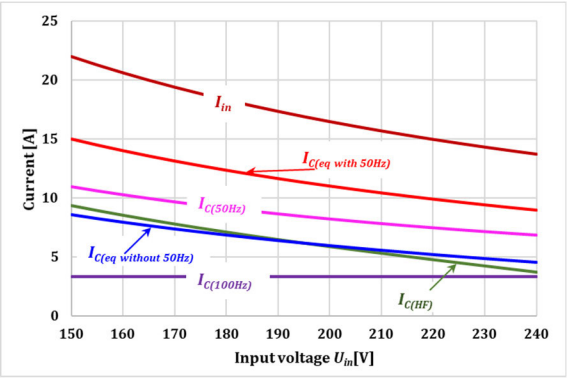

FIGURE 5. The DC bus Capacitor current stress versus input voltage. The DC bus voltage $U_{out} = 700V$ and power $P_{out} = 3300W$.

D. THE CAPACITORS VOLTAGE RIPPLE

Another important design parameter is the DC bus voltage ripple. In case of half bridge rectifier configuration, we can distinguish partial DC bus voltages u_{bus1}, u_{bus2} and the total DC bus voltage u_{out}.

The capacitors instantaneous voltages $u_{bus1}(t)$ and $u_{bus2}(t)$ are computed from (8) and given by (19), as shown at the bottom of the page. Fundamental frequency voltage ripple is given by (20), as shown at the bottom of the page. The total DC bus instantaneous voltage and voltage ripple are given by (21), as shown at the bottom of the next page and (22) respectively.

$$\Delta u_{out} \cong \frac{U_{in}}{U_{out}} \frac{I_{in}}{\omega C_{bus}} = \frac{P_{in}}{U_{out}} \frac{1}{\omega C_{bus}} \tag{22}$$

where C_{bus} is the DC bus equivalent capacitance given by (23).

$$C_{bus} = \frac{C_{bus1} C_{bus2}}{C_{bus1} + C_{bus2}}. \tag{23}$$

Please notice the DC bus voltage ripple (21) consists of 50Hz and 100Hz component, where 50Hz component is a function of the capacitance deviation of the DC bus capacitors ($\Delta C_{bus2} = C_{bus1} - C_{bus2}$). Normally, if the capacitors are well balanced ($C_{bus1} \cong C_{bus2}$), the DC bus voltage ripple consists only of 100Hz component, (22).

II. DC BUS CAPACITOR WITH AN ACTIVE VOLTAGE BALANCER (AVB)

As discussed in section I-A, the fundamental frequency capacitor current has strong impact on the capacitor losses, size, life-time and cost. Therefore, in order to optimize the system design (size and cost), fundamental frequency current has to be reduced as much as possible. An Active Voltage Balancer (AVB) able to eliminate fundamental frequency current has been proposed and analysed in this paper.

A. ACTIVE VOLTAGE BALANCER

A generalized block diagram of an active voltage balancer is depicted in FIGURE 6. The active voltage balancer is connected to the rectifier PLUS DC BUS, MINUS DC BUS and MID POINT. The main role of the AVB is to inject current $i_b(t)$ in the DC bus mid-point in order to compensate

$$I_{eq(rms)} = I_{in} \frac{1}{\sqrt{2}} \frac{U_{in}}{U_{out}} \sqrt{1 + \underbrace{\frac{1}{k_{50}} \frac{1}{8} \left(\frac{U_{out}}{U_{in}}\right)^2}_{50Hz} + \underbrace{\frac{1}{k_{HF}} \frac{1}{8} \left(\frac{7}{16} \left(\frac{U_{out}}{U_{in}}\right)^2 - \frac{1}{2} - cos^2\varphi\right)^2}_{HF}} \tag{18}$$

$$u_{bus1}(t) = \underbrace{\frac{U_{out}}{2}}_{DC} - \underbrace{\frac{\sqrt{2}}{4} \frac{I_{in}}{\omega C_{bus1}} cos(\omega t + \varphi)}_{50\ Hz} - \underbrace{\frac{U_{in}}{U_{out}} \frac{I_{in}}{2\omega C_{bus1}} sin(2\omega t + \varphi)}_{100\ Hz}$$

$$u_{bus2}(t) = \underbrace{\frac{U_{out}}{2}}_{DC} + \underbrace{\frac{\sqrt{2}}{4} \frac{I_{in}}{\omega C_{bus2}} cos(\omega t + \varphi)}_{50\ Hz} - \underbrace{\frac{U_{in}}{U_{out}} \frac{I_{in}}{2\omega C_{bus2}} sin(2\omega t + \varphi)}_{100\ Hz} \tag{19}$$

$$\Delta u_{bus1(50Hz)} = \frac{\sqrt{2}}{2} \frac{I_{in}}{\omega C_{bus1}} \ and \ \Delta u_{bus2(50Hz)} = \frac{\sqrt{2}}{2} \frac{I_{in}}{\omega C_{bus2}} \tag{20}$$

$$u_{out}(t) = \underbrace{\frac{U_{out}}{DC}}_{DC} + \underbrace{\frac{\sqrt{2}}{4} I_{in} \left(\frac{1}{C_{bus2}} - \frac{1}{C_{bus1}}\right) \frac{1}{\omega} cos(\omega t + \varphi)}_{50\ Hz} - \underbrace{\frac{U_{in}}{U_{out}} \frac{I_{in}}{2\omega C_{bus}} sin(2\omega t + \varphi)}_{100\ Hz} \tag{21}$$

the current $i_0(t)$ being injected from the rectifier into the capacitors mid-point.

1) THE AVB CONFIGURATIONS

Let's assume the AVB is a two-terminal device, having an input and an output terminal. We can distinguish two possible configurations of the DC bus and AVB. FIGURE 7 (a) shows asymmetrical configuration, where the AVBC input is connected across top (or bottom) DC bus capacitor, while the output is connected across the total DC bus. The 2^{nd} configuration is depicted in FIGURE 7 (b). The AVB input is connected across the top capacitor C_{bus2} while the output is connected across the bottom capacitor C_{bus1}. Which one is better one? The selection criterion is power rating of the AVB.

2) THE AVB POWER RATING

Power rating of the AVB depends on the configuration. The AVB power rating is computed as an average power as given by (24), (25).

$$P_{AVB}^{(1)} = \frac{U_{out}}{2}\left(\frac{1}{T}\int_0^T |i_b(t)|\,dt\right) = U_{out}\frac{\sqrt{2}}{\pi}I_{in} \tag{24}$$

$$P_{AVB}^{(2)} = \frac{U_{out}}{2}\left(\frac{1}{T}\int_0^T \frac{|i_b(t)|}{2}dt\right) = \frac{1}{2}\left[U_{out}\frac{\sqrt{2}}{\pi}I_{in}\right] \tag{25}$$

From the analysis above it is obvious the configuration 2, depicted in FIGURE 7 (b), is a preferred solution.

III. ACTIVE RESONANT VOLTAGE BALANCER (ARVB)

As already mentioned in section II, the role of the Active Voltage Balancer (AVB) is to compensate the DC bus mid-point current $i_b(t)$ and balance the voltages $u_{bus1}(t)$ and $u_{bus2}(t)$.

Symmetrical configuration, FIGURE 7 (b) is a preferred solution because minimum power rating. The solution proposed in this paper is an Active Resonant Voltage Balancer (ARVB). Simplified circuit diagram is depicted in FIGURE 8.

As discussed in [25], the balancing converter is nothing more than a variant of a switched capacitor converter [26], [27], [28]. A switch leg S_1S_2 is connected across the capacitor C_{bus1} while switch leg S_3S_4 is connected across the capacitor C_{bus2}. The capacitor C_r is the main switched-resonant capacitor that transfers the energy from C_{bus2} to C_{bus1} and vice versa. The inductor L_r is an auxiliary resonant inductor used to reduce conduction losses and ensure zero current switching (ZCS) condition [27]. The switch pairs S_1S_3 and S_2S_4 are driven with complementary control signals at period T_{sw}. The duty cycle d is constant, around 50%.

A. BRIEF ANALYSIS

For simplicity of the analysis, one can assume that the capacitors C_{bus1} to C_{bus2} are large enough to maintain the voltages $u_{bus1}(t)$ and $u_{bus2}(t)$ constant over one switching cycle T_{sw}. Also, the mid-point current $i_b(t)$ is assumed to be positive in respect to the direction given in FIGURE 9. The switches and diodes are modelled by constant voltage drop U_{sw} and

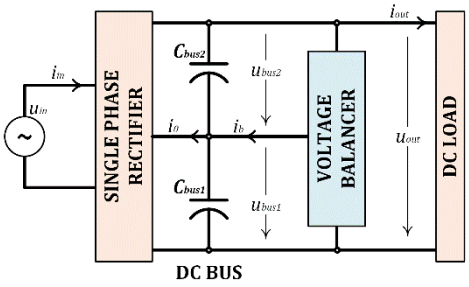

FIGURE 6. Single phase half-bridge rectifier with a voltage balancer.

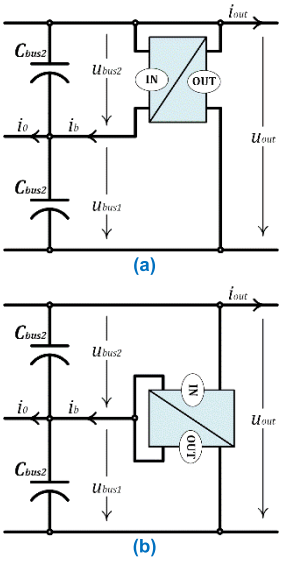

FIGURE 7. Possible arrangements of the AVB. a) Asymmetric, b) Symmetric configuration.

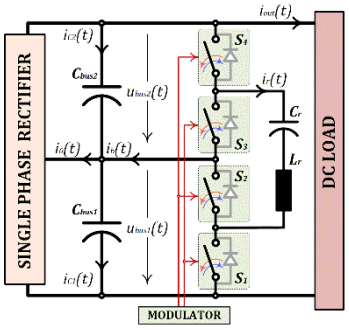

FIGURE 8. Series resonant converter as an active voltage balancer.

U_d. One complete cycle T_{sw} can be divided into four stages, namely stage A to stage D.

Stage A: Switches S_2 and S_4 are closed at the instant $t = 0$. The capacitor C_r is charged from $u_{bus2}(t)$ via the switch S_4, the inductor L_r and switch S_2.The current $i_r(t)$ increases toward the peak I_{r0}. Once the current reaches the maximum, the current starts decreasing towards zero (L_rC_r resonance).

Stage B: The current $i_r(t)$ reaches zero the moment $t = 0, 5T_0$. The switches S_2 and S_4 are switched off and the current remains zero until the next switch-pair (S_1S_3) is switched on. This period is dead time denoted as DT.

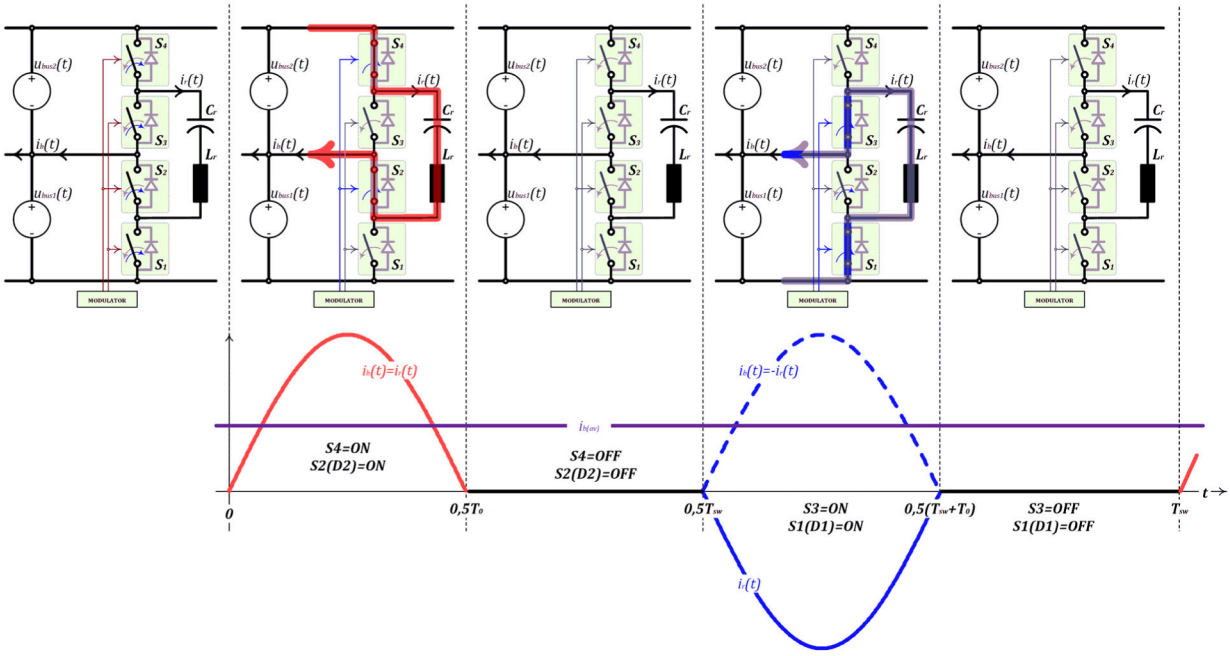

FIGURE 9. Operation of the resonant active voltage balancer.

Stage C: Switches S_1 and S_3 are closed at the moment $t = 0,5T_{sw}$. The capacitor C_r is discharged into $u_{bus1}(t)$ via the switch S_1, inductor L_r and switch S_3. The current $i_r(t)$ increases in negative direction in respect to the direction in FIGURE 9. After reaching the maximum I_{r0}, the current starts decreasing towards zero (L_rC_r resonance).

Stage D: The current $i_r(t)$ reaches at the moment $t = 0,5T_{sw}+0,5T_0$. The current remains zero until the next commutation of the switch-pair (S_2S_4) at the moment $t = T_{sw}$. One switching cycle T_{sw} is finished.

B. THE DC BUS CAPACITOR CURRENT STRESS AND VOLTAGE RIPPLE

1) THE CAPACITOR CURRENT STRESS

The capacitors instantaneous currents are

$$\begin{aligned} i_{C2}(t) &= s(t)\, i_{in}(t) - \frac{1}{2} i_{in}(t) - I_{out} \\ i_{C1}(t) &= -(1 - s(t))\, i_{in}(t) + \frac{1}{2} i_{in}(t) - I_{out} \end{aligned} \tag{26}$$

Applying moving averaging technique [20], [21], [22] on (26), yields the DC bus capacitor current averaged over one switching period T_{sw}

$$\begin{aligned} \langle i_{C1} \rangle (t) &= -I_{in} \frac{U_{in}}{U_{out}} cos(2\omega t + \varphi) = i_{C1(LF)}(t), \\ \langle i_{C2} \rangle (t) &= I_{in} \frac{U_{in}}{U_{out}} cos(2\omega t + \varphi) = i_{C2(LF)}(t). \end{aligned} \tag{27}$$

It could be proven the current (27) is nothing else than low frequency component of the DC bus capacitors current. High frequency current stress can be assumed same as in the case of an conventional rectifier (11).

The total equivalent capacitor RMS current $I_{eq(rms)}$ (28) is computed from (11), (27) and the Parseval theorem [21], [22], [23]

$$I_{eq(rms)} = \frac{1}{\sqrt{2}} \frac{I_{in} U_{in}}{U_{out}} \times \sqrt{1 + \underbrace{\frac{1}{k_{HF}} \frac{1}{8} \left(\frac{7}{16} \left(\frac{U_{out}}{U_{in}} \right)^2 - \frac{1}{2} - cos^2 \varphi \right)}_{HF}}^2 \tag{28}$$

2) THE DC BUS VOLTAGE RIPPLE

The capacitors instantaneous voltage is computed from (27) as

$$\begin{aligned} u_{bus1}(t) &= \frac{U_{out}}{2} + \frac{I_{in}}{\omega C_{bus1}} \frac{U_{in}}{U_{out}} sin(2\omega t + \varphi) \\ u_{bus2}(t) &= \frac{U_{out}}{2} + \frac{I_{in}}{\omega C_{bus2}} \frac{U_{in}}{U_{out}} sin(2\omega t + \varphi) \end{aligned} \tag{29}$$

Total DC bus instantaneous voltage is

$$\begin{aligned} u_{out}(t) &= u_{bus1}(t) + u_{bus2}(t) \\ &= \underbrace{U_{out}}_{DC} + \underbrace{\frac{1}{\omega C_{bus}} I_{in} \frac{2U_{in}}{U_{out}} sin(2\omega t + \varphi)}_{100\ Hz} \end{aligned} \tag{30}$$

where C_{bus} is total DC bus capacitance.

$$C_{bus} = \frac{C_{bus1} C_{bus2}}{C_{bus1} + C_{bus2}}. \tag{31}$$

Please notice the DC bus voltage ripple (30) contents only 100Hz component (the 2^{nd} harmonic).

C. THE VOLTAGE BALANCING CAPABILITY

The balancing converter (FIGURE 8) is a series resonant converter that operates in discontinuous conduction mode (DCM), mode 1 [25], [26], [27], [28]. The input is voltage u_{bus1} while the output is voltage u_{bus2}. The input-to-output voltage ratio (gain) of a series resonant converter operating in DCM, mode 1 is unity regardless on the load.

$$\frac{u_{bus1} + (U_{sw} + U_d)}{u_{bus2} - (U_{sw} + U_d)} = 1 \tag{32}$$

where U_{sw} and U_d are the switch and the diode voltage droop.

Partial DC bus capacitor voltages are computed from (32) as

$$u_{bus1} = \frac{U_{out}}{2} - sgn\,(i_b)\,(U_{sw} + U_d)$$
$$u_{bus2} = \frac{U_{out}}{2} + sgn\,(i_b)\,(U_{sw} + U_d) \tag{33}$$
$$\Delta u_{bus} = u_{bus2} - u_{bus1} = sgn\,(i_b)\,2\,(U_{sw} + U_d) \tag{34}$$

Please notice from (33) and (34), the bottom to the top capacitor voltage ratio is constant regardless on the current i_b. Hence, the voltages are self-balanced and there is no need for direct measurement and closed loop control of the voltage distribution.

D. DETAILED ANALYSIS AND DESIGN OF THE RESONANT VOLTAGE BALANCING CIRCUIT

1) CURRENT STRESS

For sake of simplicity, it will be assumed that the DC bus capacitor voltages are perfectly balanced. This is quite reasonable assumption especially if the ARVB switches are low voltage MOSFET devices. Under such an assumption, the one cycle average compensation current $i_b(t)$ can calculate by (35)

$$i_b(t) = i_{in}(t) = \sqrt{2} I_{in} sin\,(\omega t + \varphi) \tag{35}$$

As described in [25], the resonant current $i_r\,(t)$ is given by (36), The resonant current magnitude $I_{r0}\,(t)$ is given by (37) where T_0 is the resonant period, and DT is dead time [25].

$$\begin{aligned} i_r\,(t) &= (-1)^k\,|i_{in}\,(t)|\,\frac{\pi}{2}\left(\frac{T_0 + 2DT}{T_0}\right) sin\omega_0 t \\ \text{when } k\frac{T_0 + 2DT}{2} &< t \\ &\le \frac{k\,(T_0 + 2DT) + T_0}{2} \\ i_r\,(t) &= 0 \\ \text{when } \frac{k\,(T_0 + 2DT) + T_0}{2} &< t \\ &\le (k+1)\,\frac{T_0 + 2DT}{2} \end{aligned} \tag{36}$$

$$\begin{aligned} I_{r0}\,(t) &= |i_{in}\,(t)|\,\frac{\pi}{2}\left(\frac{T_0 + 2DT}{T_0}\right) \\ &= \sqrt{2}\frac{\pi}{2} I_{in}\left(\frac{T_0 + 2DT}{T_0}\right)|sin\,(\omega t + \varphi)| \end{aligned} \tag{37}$$

$$\begin{aligned} \left\langle i_{sw(av)}\right\rangle(t) &= \frac{I_{r0}\,(t)}{\pi} = \frac{\sqrt{2}}{2} I_{in}\,|sin\,(\omega t + \varphi)| \\ \left\langle i_{sw(rms)}\right\rangle(t) &= \left(\frac{\pi}{2\sqrt{2}}\sqrt{\frac{T_0 + 2DT}{T_0}}\right) \\ &\quad \times I_{in}\,|sin\,(\omega t + \varphi)| \end{aligned} \tag{38}$$

The switches/diodes moving RMS and average currents (38) are computed from (36) and moving average and RMS operator [21], [22].

The circuit resonant frequency ω_0 and the integer k are defined as

$$\omega_0 = \frac{2\pi}{T_0} = \frac{1}{\sqrt{L_R C_R}}\ and\ k = INT\left(\frac{2t}{T_0 + 2DT}\right). \tag{39}$$

The resonant circuit moving RMS current (40) is computed in the same way as the switch RMS current,

$$\left\langle i_{r(rms)}\right\rangle(t) = \left(\frac{\pi}{2}\sqrt{\frac{T_0 + 2DT}{T_0}}\right) I_{in}\,|sin\,(\omega t + \varphi)|\,. \tag{40}$$

Total RMS current of the resonant LC circuit is

$$I_{r(rms)} = I_{in}\frac{\pi}{2\sqrt{2}}\sqrt{\frac{T_0 + 2DT}{T_0}}. \tag{41}$$

2) THE SWITCH VOLTAGE RATING

In a general case switch voltage rating is

$$U_{sw(n)} = \frac{U_{out}}{2} + \frac{1}{\omega C_{bus2}} I_{in}\frac{U_{in}}{U_{out}} + \Delta U_{sw} \tag{42}$$

where ΔU_{sw} is the switch transient over-voltage [21], [29]. Since the resonant voltage balancer operates close to Zero Current (ZC) condition, the transient over-voltage ΔU_{sw} can be neglected.

3) THE SWITCH CONDUCTION LOSSES

Conduction loss of one switch is

$$\begin{aligned} P_{sw(con)} &= \frac{1}{T}\int_0^T p_{sw}\,(t)\,dt \\ &= \frac{1}{T}\int_0^T \left(U_{sw(0)}\left\langle i_{sw(av)}\right\rangle(t) + r_{sw}\left\langle i_{sw(rms)}\right\rangle^2(t)\right) dt \end{aligned} \tag{43}$$

where $U_{sw(0)}$ and r_{sw} are the switch voltage knee and dynamic resistance respectively. Substituting moving average and RMS current (38) into (43) yields (44).

$$P_{sw(con)} = U_{sw(0)}\left(\frac{\sqrt{2}}{\pi} I_{in}\right) + r_{sw}\frac{\pi^2}{16}\left(\frac{T_0 + 2DT}{T_0}\right) I_{in}^2. \tag{44}$$

4) SWITCHING LOSSES

Since the converter operates close to zero current (ZC) turn-off, the switching loses can be neglect. However, if the switching frequency is high and large die unipolar switches are used, such as low resistance SJ MOSFET, it may happen

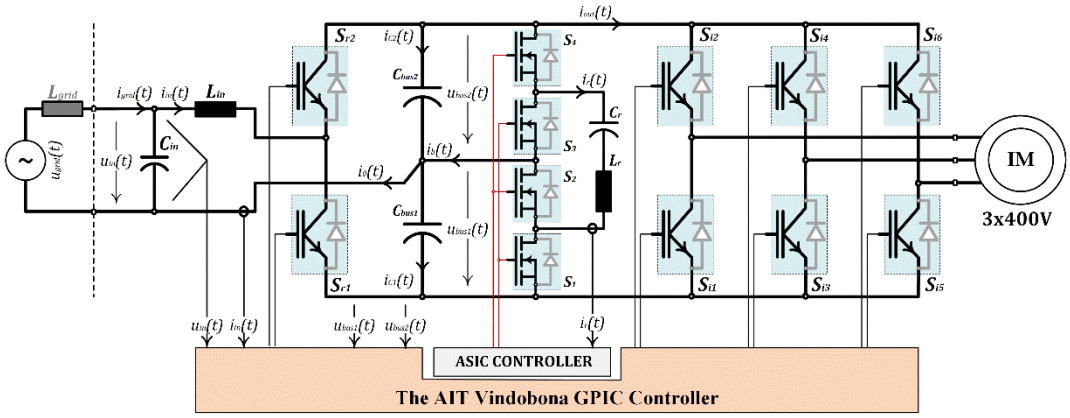

FIGURE 10. The proof-of-concept prototype circuit diagram.

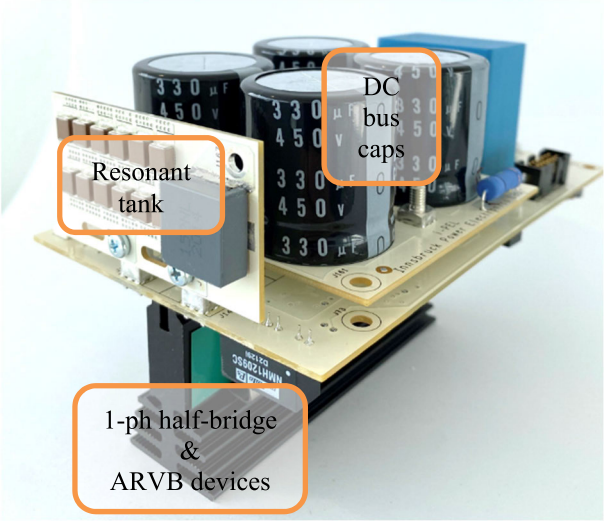

FIGURE 11. Experimental prototype of the single-phase half-bridge rectifier with an active resonant voltage balancer.

the turn-on discharge losses are significant. If this is a case, switching losses can be approximated by

$$P_{sw(sw)} = \frac{1}{2}\left(\frac{U_{out}}{2}\right)^2 C_{oss} f_{sw}, \tag{45}$$

where C_{oss} is the switch output capacitance and f_{sw} is the converter switching frequency.

IV. DESIGN EXAMPLE

A. SPECIFICATION

To illustrate the advantages and disadvantages of the solution presented in this paper, a 3.3 kW single-phase half-bridge rectifier with an active resonant voltage balancer was designed and experimentally validated. The design specifications and constrains are given in Table 1

Simplified circuit diagram of the proof-of-concept power conversion application is depicted FIGURE 10. Details of the design are given hereafter. The experimental prototype of

TABLE 1. Proof of concept prototype specification.

Rated Power [W]	3300
Input (Phase-to-Neutral) Voltage [V]	230
Input Current [A]	14,4
Output (Phase-to-Phase) Voltage [V]	3x400
Total DC bus Voltage [V]	700
Total DC bus voltage ripple [V]	50
Partial DC bus voltage ripple [V]	25
Life Time [h]	30000

the single-phase half-bridge rectifier with the active resonant voltage balancer (ARVB) is shown in FIGURE 11.

The DC bus capacitors C_{bus1} and C_{bus2} were selected to meet the current stress and the voltage ripple requirements (20) and (22), Table 1. and II. For both cases LGW2W331MELC35 Nichicon 330μF 450V electrolytic capacitors were used. The DC bus sizing is discussed in the next paragraph. The rectifier input LC filter is designed to satisfy harmonics requirements and AC current ripple better than 20% in all operating conditions. The inductor L_{in} is made of Hitachi Metals Metglas AMCC50 cores and litz wire with inductance of 400 μH. The input filter capacitor C_{in} is EPCOS class X2 6.8μF 330V.

The active resonant voltage balancer resonant tank is built with high voltage ceramic capacitor and off-the-shelf power SMT inductor. The resonant capacitor $\mu C_r = 24\text{F}/450\text{V}$ was built with 24 parallel connected MLCC C5750 $\times$ 7.2W105M250KA (1μF/450V). The resonant inductor $\mu L_r = 1,5\text{H}/47\text{A}$ was Pulse Electronics PA4344.152NLT.

The control algorithm, PWM signals, signal processing and protections were implemented on the AIT's Vindobona GPIC controller [31].

The single-phase half-bridge rectifier is driven with the bipolar PWM modulation technique at the switching frequency $f_{r(sw)} = 20kHz$. The active resonant voltage balancer is driven with a complementary pair of PWM signals and fixed equal duty cycle, approx. 50%. The switching frequency

TABLE 2. Comparison.

	Conventional Rectifier	Rectifier with the Active Voltage Balancing
Rectifier current [A]	14,4	14,4
DC bus 50Hz Current [A]	7,17	0
DC bus 100Hz Current [A]	3,3	3,3
DC bus HF RMS Current [A]	4,25	4,25
DC bus Equivalent RMS Current [A]	9,40	4,90
DC bus DESIGN		
Selected Capacitors	NichiconLGW2W331MELC35 330µF/450V 16 cells in parallel/series	Nichicon LGW2W331MELC35 330µF/450V 4 cells in parallel/series
DC bus losses [W]	22	8
Resonant Active Voltage Balancing Device Design		
Resonant Balancing Circuit		$C_r \cong 8\mu F$ @ 350V: C5750X7T2W105M250KA (24 in parallel) $L_r = 1{,}5\mu H$: Pulse Electronics PA4344.152NLT Switches: IPP65R041CFD7XKSA1
Resonant Balancing Circuit Losses [W]		47,81
Resonant Balancing Circuit Volume [cm^3]		22,40
Comparison		
Total Losses [W]	171,36 (100%)	219,17 (127%)
Total DC bus Cubical Volume [cm^3]	850,176 (100%)	234,94 (27,63%)

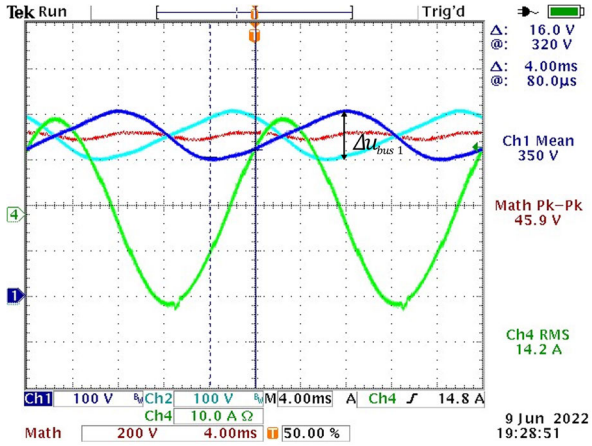

FIGURE 12. DC bus waveforms rectifier only without ARVB, Ch1 DC bus voltage upper side, Ch2 DC bus voltage lower side, Ch4 input current, Math Total DC bus voltage ripple.

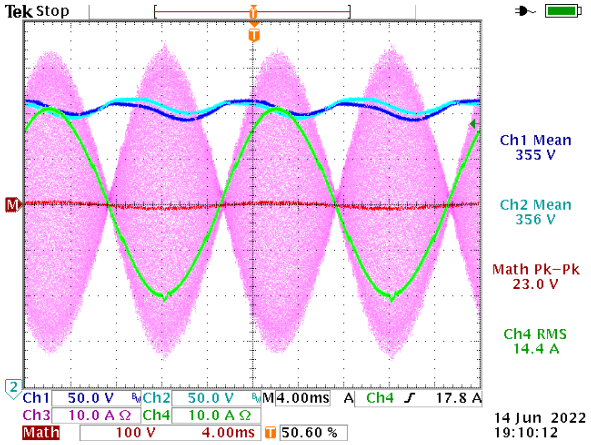

FIGURE 13. DC bus waveforms rectifier with AVRB, Ch1 DC bus voltage upper side, Ch2 DC bus voltage lower side, Ch3 resonant current, Ch4 input current, Math half DC bus voltages difference.

is selected to ensure zero voltage switching of MOSFET devices for given resonant frequency of the resonant tank, C_r and L_r for given operating DC bus voltage. The resonant frequency for the actual design is $f_0 \cong 45\ kHz$. Please notice the resonant capacitor is a multilayer ceramic capacitor having strong voltage-to-capacitance nonlinear characteristic [21], [29], [30]. The actual resonant capacitance is $\mu C_r \cong$ 8F@350V.

V. COMPARISON AND DISCUSSION

To clearly illustrate the benefits of using an active resonant voltage to reduce voltage ripple, the single-phase half-bridge rectifier is experimentally tested with and without an active resonant voltage balancer, FIGURE 11.

As shown in FIGURE 12, when the DC bus consists of only 4 capacitors, the conventional single-phase half-bridge rectifier exhibits significant partial DC bus voltage ripple, $\Delta u_{bus1} \cong 104V$. This corresponds to the analytical estimate of $\Delta u_{bus1} \cong 102,4V$ (20). The large voltage ripple is due to the fundamental frequency current flowing into a mid-point of the DC bus capacitors (9) and (20). The partial DC bus voltage ripple has an impact on the controllability of the input current and the minimal operating DC bus voltage, and it should be contained within specified limits. The resulting equivalent DC bus capacitors current stress, according to Table 1. and (18) is $I_{eq(rms)} = 9,4A$. To meet this requirement, as well as to meet the partial DC bus voltage ripple requirement $\Delta u_{bus1(max)} = 25V$, at least 16 capacitors of the selected capacitors should be used to build the DC bus. This results in a significant increase in the volume and weight of the DC bus.

On the contrary with the addition of an active resonant voltage balancer FIGURE 13 and TABLE 2., the balancer compensates the fundamental current flowing into a

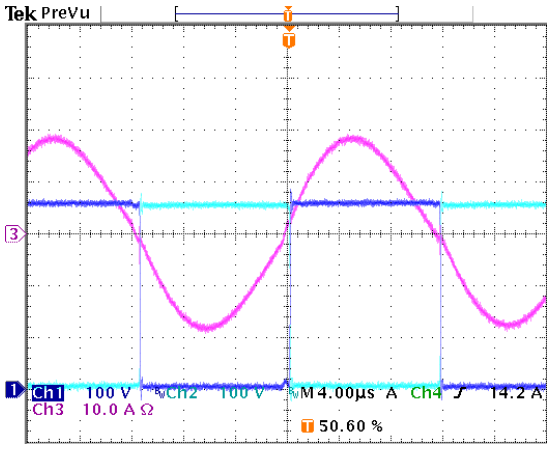

FIGURE 14. Experimental waveforms with ARVB, Ch1 voltage across drain source of M4, Ch2 voltage across drain source M1, Ch3 resonant current, Ch4 input current (trigger only).

mid-point of the DC bus and the equivalent current stress on the DC bus is reduced by approximately 52,17%, and the volume is reduced to only 27,63 %, or almost by factor of 4. Also, the half DC bus voltage ripple is $\Delta u_{bus1} \cong 23V$.

Therefore, the DC bus design with only 4 capacitors as shown in FIGURE 11 is feasible. It should also be mentioned that the elimination of the fundamental current increases the life-time of the DC bus. Also, the total DC bus with and without the balancer is not significantly affected.

The balancing resonant current magnitude and total RMS values slightly exceed the output current at fundamental. This is necessary to compensate the ripple at the fundamental frequency, at the expense of additional balancer losses. The total RMS current of the balancer according to (41), and experimental measurements, FIGURE 13 is $I_{r(rms)} = 16,4$A.

The balancer losses are mostly due to conduction losses through ARVB devices, M_1 to M_4, and a resonant tank, C_r to L_r. The switching losses may be neglected as zero voltage switching is achieved, FIGURE 14.

Experimentally determined total incremental losses due to the balancer in this design example is 48W, TABLE 2., while according to ARVB loss model, (44) and (45), 39.7 W. This is a close estimate of the actual losses. The difference is probably due to some switching losses and the conduction losses of the resonant tank. The total increase in power dissipation is 27%, which means that the cooling effort is increased. In this case, this has not increased the volume of the heatsink because the same heatsink has been reused for the single-phase half-bridge rectifier and balancer semiconductor devices, FIGURE 11. The losses could have been reduced by paralleling MOSFETs, but the aim of this paper is to demonstrate the benefits of the volume and size reduction of a DC bus.

The approach of using ARVB in a passive DC bus can be called an active DC bus, as highlighted in the title of this paper.

VI. CONCLUSION

A detailed analysis, design, and experimental validation of a single-phase half-bridge rectifier with an active resonant voltage balancer, as well as a DC bus optimization design procedure, are presented in this paper. It's shown that by using an active resonant voltage balancer, significant volume and weight reduction of the DC bus can be achieved. In the presented design example, the volume is reduced by a factor of 4, TABLE 2. This is achieved at the expense of increased losses, which should be considered when designing the cooling system. Also, given increased complexity of the proposed solution, a potential cost-benefit analysis should be conducted depending on the application specifics and applicability of the proposed solution.

Thus, the proposed solution may represent a viable option in power conversation applications where volume and weight reduction and optimization are required. The active DC bus concept or the use of an active resonant voltage balancer to reduce the DC bus current can be extended to the three-phase applications and especially for multi-level multi-cell topologies where there are multiple voltage levels and DC bus mid points.

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