IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 28 June 2024, accepted 8 July 2024, date of publication 16 July 2024, date of current version 26 July 2024.

*Digital Object Identifier 10.1109/ACCESS.2024.3429378*

RESEARCH ARTICLE

# Empowered Virtual Synchronous Generator Based Control Scheme for Improved Transient Response and Reduced Nuisance Tripping in Stable Microgrids

**MANDARAPU SRIKANTH[1], Y. V. PAVAN KUMAR[1], (Senior Member, IEEE), CH. PRADEEP REDDY[2], (Member, IEEE), AND RAMMOHAN MALLIPEDDI[3,4], (Senior Member, IEEE)**

[1]School of Electronics Engineering, VIT-AP University, Amaravati Andhra Pradesh 522237, India
[2]School of Computer Science and Engineering, VIT-AP University, Amaravati, Andhra Pradesh 522237, India
[3]Department of Artificial Intelligence, School of Electronics Engineering, Kyungpook National University, Daegu 37224, Republic of Korea
[4]Smart Agriculture Innovation Center, Kyungpook National University, Daegu 41566, Republic of Korea

Corresponding authors: Y. V. Pavan Kumar (pavankumar.yv@vitap.ac.in) and Rammohan Mallipeddi (mallipeddi.ram@gmail.com)

This work was supported by the Korea Agency for Infrastructure Technology Advancement (KAIA) Grant funded by the Ministry of Land, Infrastructure and Transport, under Grant RS-2023-00251002.

**ABSTRACT** Multiloop voltage-controlled virtual synchronous generator (VSG) based control scheme is recently popular in forming stable microgrids. This scheme deploys traditional VSG (TVSG) control for power controllers in the outermost loop and proportional-integral synchronous reference frame-based voltage-current (PIVA) controllers in the inner loop (named TVSG-PIVA scheme). But, this scheme usually exhibits larger deviations and longer settling times in transient response under large active power demands. This poor transient response would further lead to unnecessary tripping which is referred to as nuisance tripping in the literature. This hampers the system's stability even though there is no genuine fault. Thus, to address this problem, this paper proposes a modified VSG (MVSG) power controller based on adjusting the gain constant of the speed governor in the TVSG through an equalizing factor. From simulations, it is found that this MVSG supported by PIVA controllers (named MVSG-PIVA scheme) successfully avoided undesired trips under large active power demands, but, is susceptible to nuisance tripping under large reactive power demands. Thus, to effectively improve transient response and reduce the chances of nuisance trips under both large active/reactive power loads, this paper proposes a hybrid control scheme by deploying the MVSG power controller and internal model control-based VA controllers (named MVSG-IMCVA scheme). The efficacy of the proposed MVSG-IMCVA scheme is compared with the MVSG-PIVA scheme and conventional TVSG-PIVA scheme under different power factor loadings. From the results, it is proved that the proposed scheme improved the transient response and reduced unnecessary trips. Thus, the proposed modifications demonstrate the empowerment of the multiloop voltage-controlled VSG scheme, thereby ensuring system stability during dominant load changes.

**INDEX TERMS** Internal model control, microgrids, nuisance tripping, transient response, virtual inertia, virtual synchronous generator.

## NOMENCLATURE

APL =Active Power Loop.
DGS =Distributed Generating Station.
IMC =Internal Model Control.
PID =Proportional-Integral-Derivative.
RPL =Reactive Power Loop.
T80 =Transient at time of 80$^{th}$ sec.
T100 =Transient at time of 100$^{th}$ sec.

The associate editor coordinating the review of this manuscript and approving it for publication was Wencong Su.

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VA =Voltage and Current.
VSG =Virtual Synchronous Generator.
TVSG =Traditional VSG.
MVSG =Modified VSG.

*Conventional Control Scheme:*

TVSG-PIVA =TVSG-based Power Controller and PI-based VA Controllers.

*Proposed Control Schemes:*

MVSG-PIVA =MVSG-based Power Controller and PI-based VA Controllers.
MVSG-IMCVA =MVSG-based Power Controller and IMC-based VA Controllers.

## I. INTRODUCTION

To address the environmental concerns and rapid depletion of fossil fuels and to cut short the cost involved in erecting conventional power plants, renewable energy-based DGSs are set up near load centers. Since the capacity of these DGSs is typically less, these plants are named "microgrids" [1]. These plants use power electronic converters as an interface between the source and load, which are regulated by suitable control structures. The conventional structure is a multiloop control scheme with VA controllers in the inner loops and a power controller in the outer loop. Generally, these controllers are tuned independently to influence the transient performance of the microgrid.

The synchronous generator-based conventional power plants possess sufficient inertia that ensures system stability during transient conditions. However, this advantage is hardly seen with microgrids because of their limited capacity and use of power electronic converters. This issue became more complicated with the increasing penetration of DGSs-based microgrids into the utility grid [2]. This motivates the evolution of several virtual inertia emulation mechanisms in microgrids through their power controllers, by mimicking the behavior of conventional synchronous generators, which are known as VSGs. These virtual inertia emulation schemes are classified into three categories [3], namely, (i) synchronverter, (ii) multiloop current-controlled VSG, and (iii) multiloop voltage-current-controlled VSG (also referred to as multiloop voltage-controlled VSG), which are briefly discussed as follows.

Inertia emulation through a synchronverter that is designed based on the mathematical model of the synchronous generator is discussed in [4] and [5]. The structure of this scheme is simple and provides a better scope for inertia emulation. However, the absence of VA controllers restricts its ability to mitigate the disturbances and limit the current. Inertia emulation through multiloop current-controlled VSG that includes a VSG-based power controller and a current controller is discussed in [6] and [7]. This scheme limits the output current and regulates the active and reactive powers delivered to the load satisfactorily during the grid-connected mode. However, this scheme can't maintain voltage and frequency during the islanded mode.

Thus, to address various issues of the aforesaid schemes, a multiloop voltage-controlled VSG scheme is developed as a potential alternative. This scheme includes a VSG-based power controller and PI-based VA controllers as shown in Fig. 1 to establish a closed-loop control operation in the microgrid. Further, the VSG control includes an active power loop (APL) and a reactive power loop (RPL). APL and RPL provide frequency and voltage references respectively. In this scheme, VA controllers provide support to maintain voltage and frequency while delivering the required active and reactive powers. Thus, this holistic scheme that can exhibit better transient response in islanded mode is used as a basis for the proposed work in this paper.

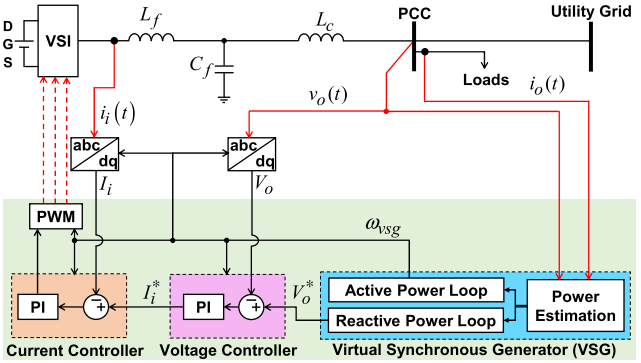



**FIGURE 1.** Microgrid schematic with multiloop voltage-controlled VSG.

### A. REVIEW OF MULTILOOP VOLTAGE-CONTROLLED VSG SCHEME AND PROBLEM STATEMENT

A review of literature related to the VSG power controllers and VA controllers of microgrids is presented as follows. Based on this, the need for improving the conventional multiloop voltage-controlled VSG scheme to address the problem of transient response and nuisance tripping is stated.

Key designs of power controllers for multiloop voltage-controlled VSG schemes to enhance stability through inertia emulation are (i) droop control-based VSG [8], [9] and (ii) traditional swing equation-based VSG (TVSG) [10], [11].

The development related to droop control as a source of inertia emulation, thereby stability enhancement is discussed as follows. Inertia emulation by fixed droop-based VSG control depending on the inherent time lag associated with the power measurement is discussed in [8]. However, a narrow range of allowable time lag puts a limitation on the inertia emulated by this scheme. Further, inertia emulation based on the adjustment of the variable droop coefficient is discussed in [12]. However, due to droop value constraints, the scope of inertia emulation is limited.

The development related to TVSG as a source of inertia emulation is discussed as follows. Small signal modelling-based stability analysis against parameter variations which helps to understand their role in the stability

of TVSG, is discussed in [13] and [14]. Based on this analysis, it is suggested in these works that adjusting inertia and damping coefficients can contribute to improvement in stability. Further, some recent developments in VSG design based on artificial intelligence and optimization to adjust the inertia coefficient are discussed in [15], [16], [17], [18], and [19]. The main disadvantage of these methods is increased computational time and burden.

Even though tuning of inertia and damping coefficients can help to achieve enhancement in stability, the chances of improvement in transient response through this will be minimal. Moreover, a reduction in settling time which could avoid unnecessary tripping of DGS cannot be achieved. To address these issues, [20] suggested that adjusting the gain constant of the speed governor in the TVSG scheme will provide better chances of improved transient response and reduced settling time. However, a procedure or description for fixing this gain constant is not discussed.

Comparing droop and TVSG schemes, it can be stated that, following a transient situation even though TVSG control provides better stability, it takes comparatively longer settling time than droop control. However, based on the equivalence between droop and TVSG control, [21], [22] have suggested that the control performance of TVSG is better than droop control. This means that high chances are available for reducing the settling time with TVSG through appropriate control. Therefore, in view of better stability and control performance, TVSG is hereafter considered for power controller in a multiloop voltage-controlled VSG scheme. The following discussion reviews the possibility of getting further support from VA controllers for enhancing the transient response and reducing the settling time. Since PIVA are considered as the base VA controllers in this work, this scheme will be hereafter referred to as the ''conventional TVSG-PIVA scheme''.

Conventional TVSG-PIVA scheme helps improve the microgrid's stability when subjected to sudden changes in active power demands. However, this scheme cannot reduce the settling time when subjected to resistively dominant load switchings which could lead to unnecessary tripping. The TVSG power controller mainly dictates the stability margin while the disturbance rejection is mainly regulated by inner VA controllers. It is therefore understood that the role of VA controllers is significant in improving the transient response and reducing the settling time. However, achieving better transient response and reduced settling time through the tuning of PIVA controllers is relatively complex and not effective. Thus, some modifications to conventional PIVA controllers of the TVSG-PIVA scheme are presented [23], [24], [25], [26]. Here, [23] and [24] presented improved disturbance rejection through compensators, and [25] and [26] presented extensions to existing PIVA controllers. High computational burden and need for complex mathematical knowledge are the major disadvantages of these schemes. Moreover, commonly in all these works, the impact of inductively dominant loads on the transient response of the microgrid is neglected.

To the best of the authors' knowledge, a comprehensive study to enhance the capability of the conventional TVSG-PIVA scheme aiming to avoid the chances of nuisance tripping by reducing the settling time when subjected to resistively dominant as well as inductively dominant loads is lacking. Therefore, it is essential to modify both VSG and VA controllers to improve the transient response in microgrids and to reduce the settling time.

### B. PAPER CONTRIBUTION AND ORGANIZATION

The problem of nuisance tripping in VSG control along with the conditions that are considered in this work to verify the occurrence of nuisance tripping is given in Appendix. This work focuses on enhancing the merit of the conventional TVSG-PIVA scheme such that it can improve transient response and satisfactorily work under the constraint of an acceptable/lower clearing time to avoid nuisance tripping problem in stable microgrids. So, this paper proposes the necessary modifications to the conventional TVSG-PIVA scheme in two steps. In step-1, which is an intermediate stage, this paper proposes an MVSG-PIVA scheme to avoid nuisance tripping under large active power demands. In step-2, this paper proposes the MVSG-IMCVA scheme as an effective solution to avoid nuisance tripping under both large active/reactive power demands.

The remaining sections of the paper are organized as follows. Section II proposes a solution to enhance the merit of the VSG with the necessary justification for using IMC-based VA controllers. Section III describes the tuning procedure of the proposed/conventional microgrid's power, voltage, and current controllers. Section IV analyzes the simulation results of the conventional/proposed schemes at various load conditions. In Section V, the conclusion of the proposed work is presented. Further, it notes the limitations of the proposed work and its future research directions.

## II. PROPOSED SOLUTION AND JUSTIFICATION

For the power controller, an MVSG controller is proposed based on adjusting the gain constant of the speed governor in the VSG through an equalizing factor. This proposed MVSG improves the transient response under sudden changes in active power demands (resistively dominant loads). Besides, to reduce the chances of nuisance tripping under large reactive power demands (inductively dominant loads), MVSG needs to be supported with advanced type of VA controllers. Considering the limitations of conventional PI-based VA controllers, the design of the advanced VA controllers should be less complex and more effective. In such a case, IMC-based VA controllers which offer less design complexity and yet are effective are a favourable choice [27], [28], [29]. Thus, to take benefit of IMC-based control, the proposed control scheme in this paper suggests an MVSG controller supported by IMC-based VA controllers. The conceptual model of

the conventional/proposed multiloop voltage-controlled VSG schemes is shown in Fig. 2.

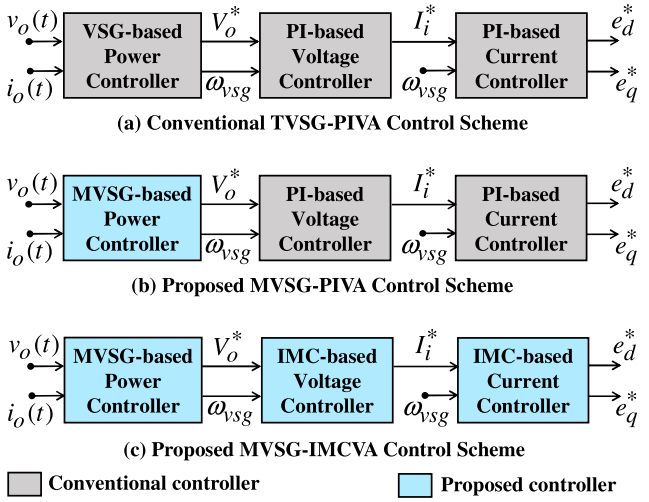



**FIGURE 2.** Conceptual model of conventional/proposed control scheme.

This helps to easily identify the modifications that are proposed to the conventional TVSG-PIVA scheme that is shown in Fig. 2(a). These modifications are evolved in two stages. In stage-1, the MVSG-PIVA scheme is proposed as shown in Fig. 2(b) to avoid nuisance tripping under large active power loads. In stage-2, the MVSG-IMCVA scheme is proposed as shown in Fig. 2(c) to avoid nuisance tripping under both large active and reactive power loads.

### A. RATIONALE OF THE PROPOSED SOLUTION

Eigenvalue analysis is performed in this paper to justify the importance of IMC-based VA controllers as an effective support to power controllers over conventional PI-based VA controllers in enhancing the transient response in microgrids. For this purpose, the small signal model of the system that is expressed as $\dot{X} = AX + BU$ and $Y = CX + DU$ is required, where $A$ is the system matrix whose eigenvalues are the roots of the characteristic equation. The locus of these roots on the s-plane indicates the stability and quality of the transient response of the microgrid when subjected to parametric variations. The small signal model of an autonomous microgrid with PI-based VA controllers is presented in [30]. In similar lines, the small signal model of the microgrid with IMC-based VA controllers is discussed in [27]. However, the superiority of the IMC-based VA controllers under dynamic load conditions that majorly affect the microgrid's transient response has not been studied in the literature. With this motivation, this paper performs the following analysis.

In autonomous microgrids, the equivalent inductance ($L_c$) that is used in small signal modelling can be treated as the combination of variable load inductance and fixed line inductance. So, '$L_c$' is an influential parameter that affects the transient response under large dynamic reactive loadings. In view of this, the locus of dominant eigenvalues belonging to the system matrix $A$ with PI-based VA controllers and with IMC-based VA controllers when subjected to incremental and decremental variations of $L_c$ are plotted and compared as shown in Fig. 3. In these plots, an effect of incremental variations of $L_c$ in 10 steps from 1pu to 6.5pu and decremental variations of $L_c$ in 10 steps from 1pu to 0.001pu is recorded. From these results, the following observations are made.

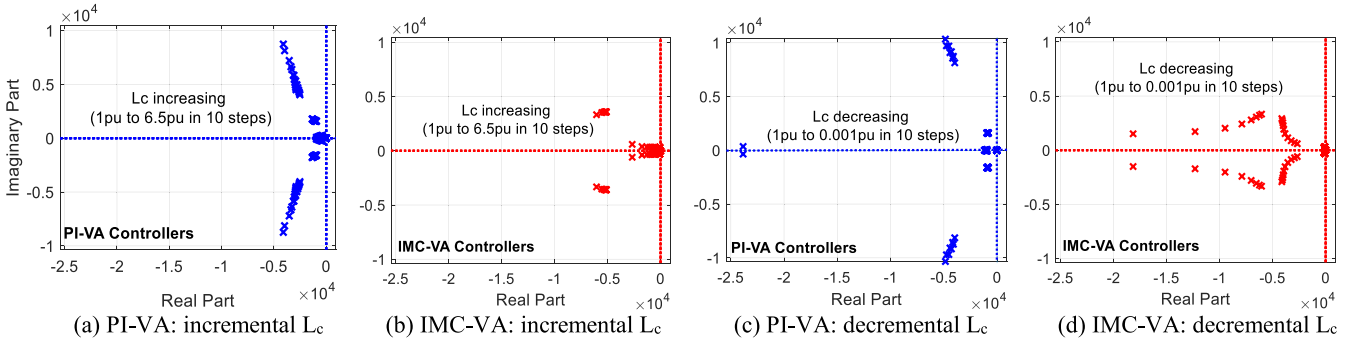
- In case of the PI-based VA controllers (either incremental $L_c$ given in Fig. 3(a) or with decremental $L_c$ given in Fig. 3(c)), the eigenvalues have a large imaginary part, thus positioning them at a farther distance from the real axis. This makes the system more sensitive to transients.
- In the case of the IMC-based VA controllers (either with incremental $L_c$ given in Fig. 3(b) or with decremental $L_c$ given in Fig. 3(d)), the eigenvalues have small imaginary parts, thus positioning them nearer to the real axis. This helps the system to exhibit better transient response.

This justification has provided the necessary motivation to replace the existing conventional PI-based VA controllers with IMC-based VA controllers for better transient response under dynamic loading conditions. Thus, IMC-based VA controllers are used in this paper to support the proposed MVSG power controller to achieve the desired objectives of improved transient response and reduced nuisance tripping.

## III. DESIGN OF THE MICROGRID CONTROLLERS

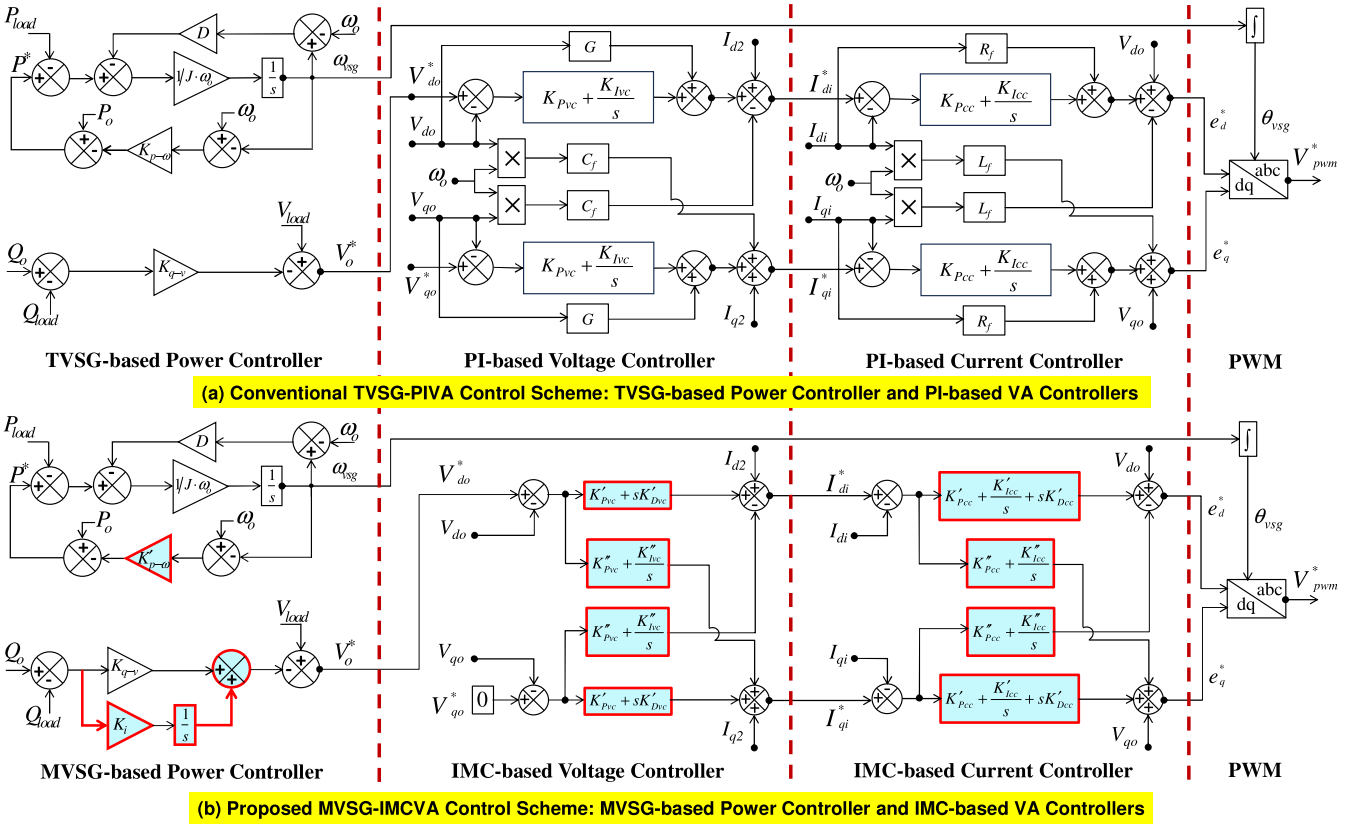
The design of power, voltage, and current controllers for both conventional (TVSG-PIVA) and proposed (MVSG-PIVA and MVSG-IMCVA) schemes are discussed in this section. The conceptual models given in Fig. 2 are detailed as shown in Fig. 4., where Fig. 4(a) refers to the TVSG-PIVA control scheme and Fig. 4(b) refers to the MVSG-IMCVA control scheme. However, the detailed MVSG-PIVA control scheme is not shown in Fig. 4., as it is an intermediate stage that can be understood in Fig. 2. The following modifications are made to the proposed MVSG-IMCVA scheme in comparison with the conventional TVSG-PIVA scheme. All these are highlighted in the proposed control scheme shown in Fig. 4.

- *Power controller*:
  - APL: The gain constant of the speed governor in the case of TVSG is $K_{p-\omega}$, which is fixed based on the VSG parameters. However, this value for MVSG is $K'_{p-\omega}$ that is obtained by tuning it using an equalizing constant.
  - RPL: To ensure stability while handling parallel R-L loads, a modified RPL with PI controller is implemented in the MVSG scheme. Whereas, the conventional TVSG generally uses a P controller. Thus, to maintain the generality during all test cases, the RPLs of both TVSG and MVSG are designed with PI controllers.
- *Voltage controller*:
  - Forward paths: PD controllers are used in the proposed scheme, while, PI controllers are used in the conventional scheme.




(a) PI-VA: incremental $L_c$ (b) IMC-VA: incremental $L_c$ (c) PI-VA: decremental $L_c$ (d) IMC-VA: decremental $L_c$

**FIGURE 3.** Locus of dominant eigenvalues plotted for a microgrid with PI-based VA controller and IMC-based VA controller.




(a) Conventional TVSG-PIVA Control Scheme: TVSG-based Power Controller and PI-based VA Controllers

(b) Proposed MVSG-IMCVA Control Scheme: MVSG-based Power Controller and IMC-based VA Controllers

**FIGURE 4.** Detailed models of conventional TVSG-PIVA and proposed MVSG-IMCVA control schemes for microgrids.

  - Cross-coupling paths: PI controllers are used in the proposed scheme, while, a fixed gain of $C_f$ is used in the conventional scheme.

- *Current controller*:

  - Forward paths: PID controllers are used in the proposed scheme, while, PI controllers are used in the conventional scheme.
  - Cross-coupling paths: PI controllers are used in the proposed scheme, while, a fixed gain of $L_f$ is used in the conventional scheme.

The following subsections give the modelling and design of key parts of the conventional/proposed control schemes namely TVSG, MVSG, PIVA, and IMCVA controllers.

### A. TRADITIONAL VIRTUAL SYNCHRONOUS GENERATOR (TVSG)

TVSG is designed to mimic the behavior of a conventional synchronous generator by emulating virtual inertia. For this purpose, the swing equation which characterizes the behavior of the conventional synchronous generator as shown in (1) is adopted to develop the APL of TVSG [31]. Under sudden changes in power demands, the inertia delays the sudden

changes in frequency to ensure system stability.

$$P^* - P_{load} = J\omega_0 \frac{d\omega_{vsg}}{dt} + D(\omega_{vsg} - \omega_0) \tag{1}$$

$$where,\ P^* = P_0 - K_{p-\omega}(\omega_{vsg} - \omega_0) \tag{2}$$

$$P_0 - P_{load} = J\omega_0 \frac{d\omega_{vsg}}{dt} + K_{p-\omega}(\omega_{vsg} - \omega_0) + D(\omega_{vsg} - \omega_0) \tag{3}$$

$$v_0^* = v_{load} - K_{q-v}\,(Q_0 - Q_{load}) \tag{4}$$

where $P^*$ is the equivalent of reference mechanical power input, $P_{load}$ is the electrical power output, $J$ is the equivalent of rotor inertia, $D$ is damping constant, $\omega_0$ is the nominal angular frequency corresponding to 50Hz and $\omega_{vsg}$ is the rotor speed estimated by the VSG.

The speed governor provides the necessary mechanical power input reference $P^*$ to the synchronous generator. The coordination between the speed governor and synchronous generator is described in the literature with active power-frequency ($P$-$\omega$) droop control as shown in (2). $P_0$ is the nominal active power and $K_{P-\omega}$ is the governor's proportional gain coefficient. Equating $P^*$ of (1) and (2), the resulting equation which describes the APL is shown in (3). In similar lines, RPL is designed based on the relationship between reactive power output and voltage in conventional synchronous generator i.e., (Q-$v$) droop characteristics. The corresponding control equation expressing this behavior is shown in (4). $v_0$ and $v_{load}$ are the reference voltage to the voltage controller and voltage measured at the load terminals respectively; $Q_0$ and $Q_{load}$ are the nominal value of reactive power and reactive power measured at the load terminals respectively and $K_{q-v}$ is the droop gain coefficient of RPL. The representation of the APL based on (3) and the RPL based on (4) is shown in Fig. 5.

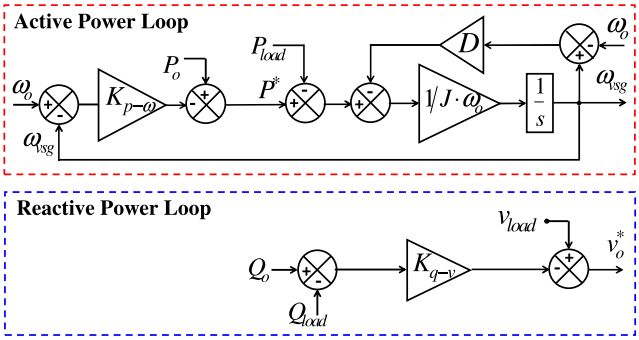



**FIGURE 5.** Active and reactive power loops of the TVSG.

### B. PROPOSED MODIFIED VIRTUAL SYNCHRONOUS GENERATOR (MVSG) – DESIGN EXAMPLE

The active and reactive power loops in the proposed MVSG are designed by considering the TVSG parameters and procedures that are defined in [20], [21], and [22] and Fig. 5 as basis. This design procedure is derived as follows.

With an equivalent rotor inertia value of $J$=56.3 kg-m$^2$, nominal frequency of 50Hz, and $\omega_0 = 2\pi \times 50$ rad/s, the gain in the forward path of the active power loop is shown in (5). With a maximum allowable active power variation ($\Delta P_{max}$) of $62.8\times10^3$W and a maximum allowable frequency deviation of 2%, the value of the $P$-$\omega$ droop coefficient is calculated in (6). Similarly, with a maximum allowable reactive power variation ($\Delta Q_{\max}$) of $21.02 \times 10^3$ Var and the maximum allowable voltage deviation of 10% for a nominal voltage of 220V, the value of $Q - v$ droop coefficient is calculated as given in (7).

$$\frac{1}{J\omega_0} = 5.6567 \times 10^{-5} \tag{5}$$

$$D_p = \frac{\Delta P_{\max}}{\Delta \omega_{\max}} = \frac{62.8 \times 10^3}{(2 \times \pi \times 50) \times 2\%} = 1 \times 10^{-4} \tag{6}$$

$$D_q = \frac{\Delta Q_{\max}}{\Delta V_{\max}} = \frac{21.02 \times 10^3}{\left(220 \times \sqrt{2}\right) \times 10\%} = 1.48 \times 10^{-3} \tag{7}$$

The base value of the apparent power is obtained in (8).

$$\left.\begin{aligned} S_{base} &= \sqrt{(\Delta P_{\max})^2 + (\Delta Q_{\max})^2} \\ &= \sqrt{\left(62.8 \times 10^3\right)^2 + \left(21.02 \times 10^3\right)^2} = 66.224 \times 10^3 \text{VA} \end{aligned}\right\} \tag{8}$$

Through the comparison between active power loops of droop control and VSG control, [21] identifies the relation between the speed governor proportional gain constant and $P - \omega$ droop coefficient as "$K_{P-\omega} = 1/D_P$". It is identified in [22] that by adjusting $J$ and $D$ alone, satisfactory performance cannot be achieved. Further, it points out that the relation "$K_{P-\omega} = 1/D_P$" should not be maintained strictly and $K_{P-\omega}$ should be adjusted for better performance. From this research direction, for an active power loop (APL) gain of $K_{P-\omega} = 20$pu, its equivalent value is obtained by solving (9).

$$K'_{p-\omega} = 20pu = 20 \times \frac{S_{base}}{\omega_0} = [a] \times \left[\frac{1}{D_p}\right] \tag{9}$$

where '$a$' is an equalizing constant whose value is obtained by solving (10). This value of '$a$' when substituted in (9), the equivalent value of $K_{P-\omega}$ is thus obtained as shown in (11). Similarly, for $D = 17$pu, its equivalent value is calculated as shown in (12).

$$20 \times \frac{66.224 \times 10^3}{314.7} = [a] \times \left[\frac{1}{1 \times 10^{-4}}\right] \Rightarrow a = 2.3759 \tag{10}$$

$$K'_{p-\omega} = [2.3759] \times \left[\frac{1}{1 \times 10^{-4}}\right] \tag{11}$$

$$D = 17pu = 17 \times \frac{S_{base}}{\omega_0} = 17 \times \frac{66.224 \times 10^3}{314.7} = 3577.4 \tag{12}$$

This concludes the design of APL of the proposed MVSG. Similarly, for the design of reactive power loop (RPL), the equivalent value of loop gain $K_{q-v}$ is estimated from $D_q$ as shown in (13). It has been verified that the RPL in Fig. 5 can handle R (resistive) and series RL (resistive-inductive) types of loads but fails to remain stable when parallel RL types of loads are applied. Thus, to address this, a modification to the RPL of TVSG is considered by adding an integral gain as shown in (14), in the design of RPL in MVSG [30]. Thus, the APL and RPL of the proposed MVSG are shown in Fig. 6, which can effectively handle parallel RL-type of load as well.

$$K_{q-v} = D_q = 1.48 \times 10^{-3} \tag{13}$$

$$V_0^* = V_{load} - \left[ K_{q-v}\,(Q_0 - Q_{load}) + \frac{K_i}{s}\,(Q_0 - Q_{load}) \right] \tag{14}$$

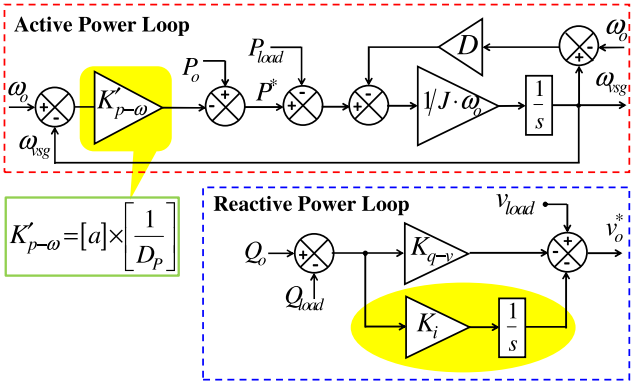



**FIGURE 6.** Active and reactive power loops of MVSG.

### C. PI-BASED VA (PIVA) CONTROLLERS

This section describes the necessary details for the implementation of the PI-based VA controllers for the conventional multiloop voltage-controlled VSG scheme. A typical schematic of the cascaded structure for conventional PI-based VA controllers is shown in Fig. 7. The voltage controller receives $v_{d0}$, $v_{q0}$, and $\omega_{vsg}$ as reference signals from VSG. $V_{d0}^*$ and $V_{q0}^*$ are compared with the output load voltages $V_{d0}$ and $V_{q0}$ and the error signal is processed through PI controllers in the forward paths whose proportional and integral gain constants are represented with $K_{Pvc}$ and $K_{Ivc}$ respectively. The conductance ($G$) of the filter capacitance ($C_f$) is typically assumed zero. For better disturbance rejection, the output of the PI controllers is added with $I_{d0}$ and $I_{q0}$ which are d-q components of load current in their respective paths. To this sum, the $\omega_{vsg}C_f V_{q0}$ is subtracted from the d-axis result, and $\omega_{vsg}C_f V_{d0}$ is added to the q-axis result to eliminate the coupling between the d and axis.

The final outcome of the voltage controller is fed as reference current inputs $I_{di}^*$ and $I_{qi}^*$ to the current controller. These are compared with $I_{di}$ and $I_{qi}$ which are the $d$-$q$ components of the inverter output current flowing through the filter inductance ($L_f$). The error signal is processed through PI controllers in the forward paths whose proportional and integral gain constants are represented with $K_{Pcc}$ and $K_{Icc}$ respectively. With $R_f$ as the intrinsic resistance of $L_f$, the outcome of the PI controller is added with $I_{dq}R_f$ to their respective axes. For better disturbance rejection, the output of the PI controllers is further added with $V_{d0}$ and $V_{q0}$. Lastly to this sum, the $\omega_{vsg}L_f I_{qi}$ is subtracted from $d$-axis result and $\omega_{vsg}L_f I_{di}$ is added to the $q$-axis result to eliminate the coupling between $d$ and $q$ axes.

The output of the current controller ($e_{dq}^*$) is the reference signal that is provided to the pulse width modulation unit. The process involved in tuning the proportional and integral gain constants of PIVA controllers is given in [32], [33], and [34].

#### 1) TUNING OF PI-BASED CURRENT CONTROLLER

Since the current control loop is the innermost of all, its tuning is done first. The closed loop block diagram of the PI-based current controller is shown in Fig. 8.

From this, the open loop transfer function of the current control loop is expressed as shown in (15). Where $T_P$ is the time delay of PWM which is dependent on the switching frequency ($f_s$) and $\tau_f$ which is the time constant of filter inductance defined by (16). The technique used for the tuning of the PI-based current controller is based on the criterion of modulus optimum. In this procedure, the time constant of the PI controller is adjusted to a suitable value such that a pole cancellation occurs in (15). Accordingly, the values for $K_{Pcc}$ and $K_{Icc}$ are fixed whose formulas are shown in (17) where $\omega_{base}$ is the base angular frequency.

$$H_{cc-ol}(s) = \underbrace{\left(\frac{sK_{Pcc} + K_{Icc}}{s}\right)}_{K_A(s)} \cdot \underbrace{\left(\frac{1}{1+sT_P}\right) \cdot \left(\frac{1}{1+s\tau_f}\right)}_{G_{sA}(s)} \tag{15}$$

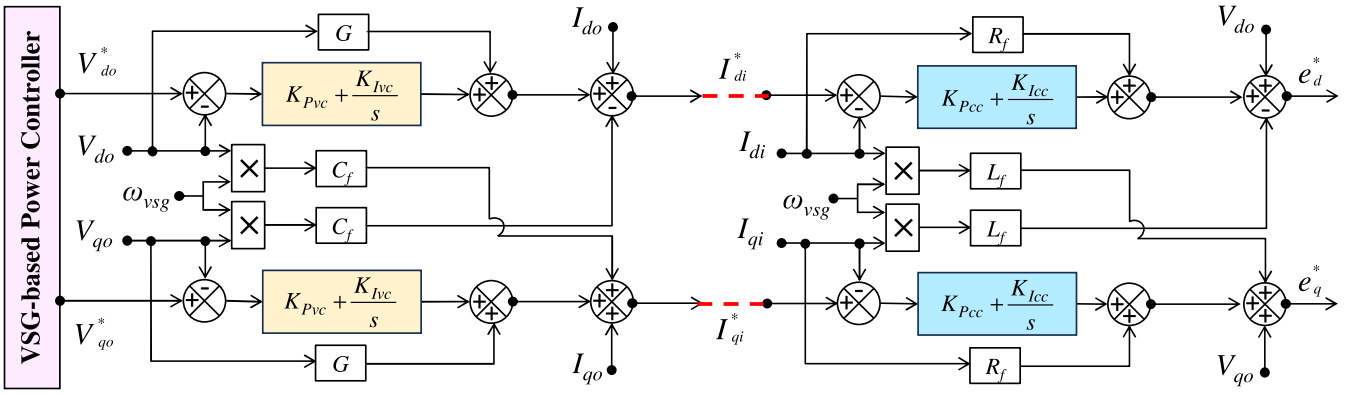
$$\tau_f = \frac{L_f}{R_f} \; and \; T_P = \frac{1}{2f_s} \tag{16}$$

$$K_{Pcc} = \frac{L_f}{2 \cdot T_P \cdot \omega_{base}} \; and \; K_{Icc} = \frac{R_f}{2 \cdot T_P} \tag{17}$$

#### 2) TUNING OF PI-BASED VOLTAGE CONTROLLER

After the tuning process of the current controller is completed, the dynamics of this current controller are approximated with its closed-loop transfer function '$G_{cc}$(s)', with $\tau_{cc}$ as the corresponding time constant. This is used for tuning of voltage control loop. The closed-loop model of the PI-based voltage controller is shown in Fig. 9.

From this figure, the open-loop transfer function of the voltage control loop is expressed as shown in (18). The formulas for calculating $\tau_{cc}$ are given through (19). The technique used for the tuning of the PI-based voltage controller




(a) Conventional PI-based voltage control module (b) Conventional PI-based current control module

**FIGURE 7.** Typical schematic of the PI-based VA control modules.

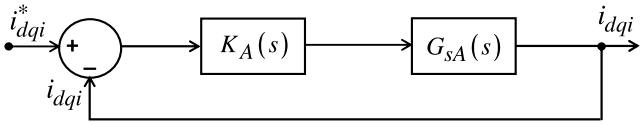



**FIGURE 8.** Block diagram for design of PI-based current controller.

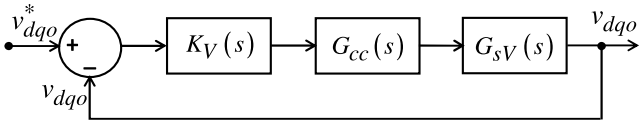



**FIGURE 9.** Block diagram for design of PI-based voltage controller.

is based on applying the criterion of symmetrical optimum to (18). Accordingly, the values for $K_{Pvc}$ and $K_{Ivc}$ are fixed, and the corresponding formulas are shown in (20). Where '$m$' is a design parameter given by $m = 2\xi + 1$ to ensure a safe gap between the bandwidths of voltage and current control loops and $\xi$ is the damping factor.

$$H_{vc-ol}(s) = \underbrace{\left(\frac{sK_{Pvc} + K_{Ivc}}{s}\right)}_{K_V(s)} \cdot \underbrace{\left(\frac{1}{1+s\tau_{cc}}\right)}_{G_{cc}(s)} \cdot \underbrace{\left(\frac{1}{sC_f}\right)}_{G_{sV}(s)} \quad (18)$$

$$\tau_{cc} = 2T_P \quad (19)$$

$$K_{Pvc} = \frac{C_f}{m \times \tau_{cc}} and K_{Ivc} = \frac{C_f}{m^3 \times \tau_{cc}^2} \quad (20)$$

### D. IMC-BASED VA (IMCVA) CONTROLLERS

This section describes the necessary details for the implementation of the IMC-based VA controllers for the proposed multiloop voltage-controlled VSG scheme. A typical schematic of the cascaded structure of IMC-based VA control modules is shown in Fig. 10.

#### 1) TUNING OF IMC-BASED CURRENT CONTROLLER

The modification to the generic IMC structure as suggested in [28] is applied to the design of the current controller as shown in Fig. 11.

$G_{sA}(s)$ as identified from (15) is the complex transfer function of the inverter, whose simplified form is shown in (21) where, $\tau_f = L_f/R_f$ and $K = 1/R_f$.

$$G_{sA}(s) = \frac{K}{1 + (s + j\omega)\tau_f} \quad (21)$$

To make the model exactly track the actual plant $G_{sA}$, the dynamics of PWM are also included in the design of $\tilde{G}_{sA}$ given in (22). In this, $j\omega * T_P$ indicates the time constant associated with the PWM model.

$$\tilde{G}_{sA}(s) = \frac{K}{\left[1 + (s + j\omega)\tau_f\right]\left[1 + (s + j\omega)T_P\right]} \quad (22)$$

$G_{cA}(s)$ is the transfer function of the controller that is expressed as (23). This is a product of the inverse of the invertible part of $G_{sA}(s)$ which is represented as $\tilde{G}^-_{sA}(s)^{-1}$ and a low pass filter $G_{lpf}(s)$ to improve robustness against any model mismatches. Where $\lambda_A$ is the only parameter in the IMC design of the current controller which requires tuning and '$n$' is the order of the low pass filter.

$$G_{cA}(s) = \tilde{G}^-_{sA}(s)^{-1} \times G_{lpf}(s) = \tilde{G}^-_{sA}(s)^{-1} \times \frac{1}{(1 + s\lambda_A)^n} \quad (23)$$

Applying the classical block diagram reduction techniques, the feedback controller $K_A(s)$ as seen in Fig. 11, is obtained as shown in (24). After substituting the necessary terms into (24), the $K_A(s)$ is obtained as shown in (25).

$$K_A(s) = \frac{G_{cA}(s)}{1 - G_{cA}(s)\tilde{G}_{sA}(s)} \quad (24)$$

$$K_A(s) = \frac{\left[1 + (s + j\omega)\tau_{cc}\right]\left[1 + (s + j\omega)T_P\right]}{s\lambda_A K} \quad (25)$$

After segregating the real and imaginary terms, the appearance of $K_A(s)$ in its generic form is shown in (26). The terms separated from the real part belong to the controller in the forward path, while those separated from the imaginary part belong to the controller in the coupling path. The terms

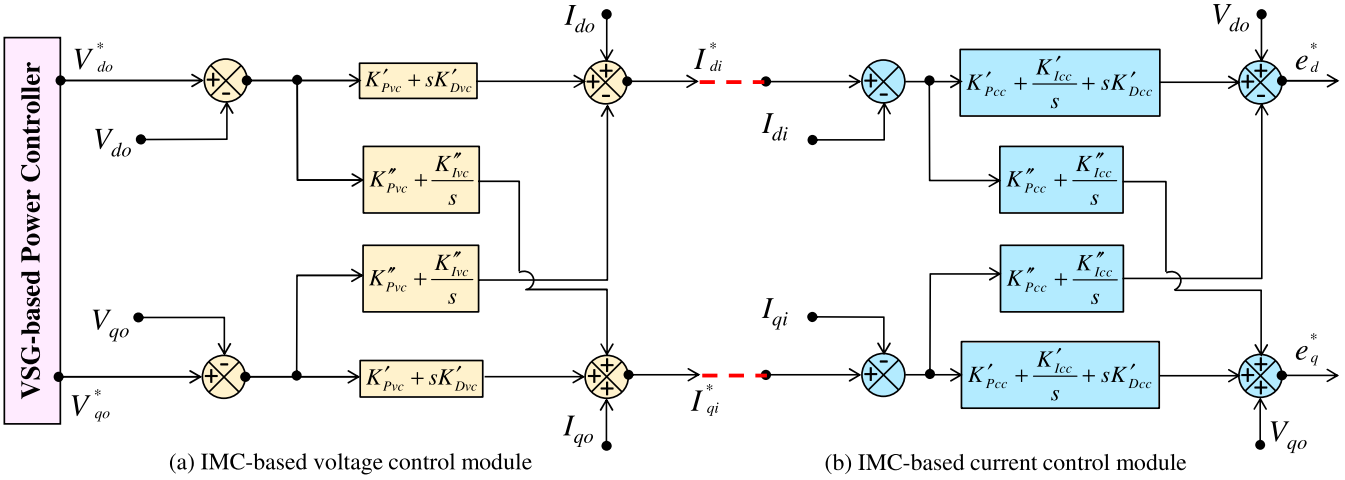



**FIGURE 10.** Typical schematic of the IMC-based VA control modules.

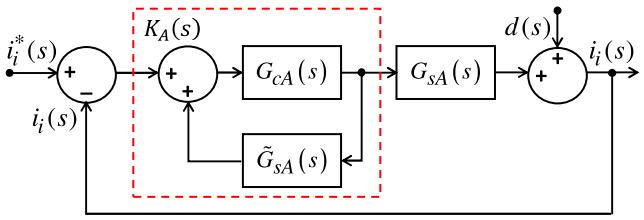



**FIGURE 11.** Block diagram for design of IMC-based current controller.

represented in (26) are derived from the equations shown in (27) and (28).

$$K_A(s) = \left(K'_{Pcc} + \frac{K'_{Icc}}{s} + sK'_{Dcc}\right) + j\left(K''_{Pcc} + \frac{K''_{Icc}}{s}\right) \tag{26}$$

$$K'_{Pcc} = \frac{L_f + T_P R_f}{\lambda_A};\ K'_{Icc} = \frac{T_P L_f \omega_0^2 + R_f}{\lambda_A};\ K'_{Dcc} = \frac{T_P L_f}{\lambda_A} \Big\} \tag{27}$$

$$K''_{Pcc} = \frac{2\omega_0 L_f T_P}{\lambda_A};\ K''_{Icc} = \frac{2T_P R_f + 2L_f}{\lambda_A} \Big\} \tag{28}$$

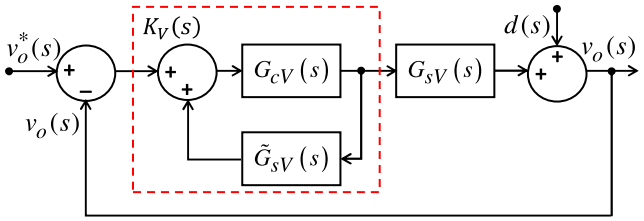



**FIGURE 12.** Block diagram for design of IMC-based voltage controller.

### 2) TUNING OF IMC-BASED VOLTAGE CONTROLLER

In this section, the voltage controller is designed with the IMC principle [29]. For this purpose, the modified IMC structure is applied to design the voltage controller as shown in Fig. 12.

$G_{sV}(s)$ as identified from (18) is the complex transfer function of the load dynamics, whose simplified form is shown in (29). The $j\omega$ term represents the coupling between the d and q axes. The procedure of designing the voltage controller is similar to the current controller design.

$$G_{sV}(s) = \frac{K}{C_f(s + j\omega)} \tag{29}$$

As shown in Fig. 9, the closed-loop transfer function of the current controller needs to be included while designing the voltage controller. With this, the transfer function of the plant model is shown in (30).

$$\tilde{G}_{sV}(s) = \frac{1}{C_f(s + j\omega)(1 + s\tau_{cc})} \tag{30}$$

$G_{cV}(s)$ is the transfer function of the controller that is expressed as shown in (31). This involves a product of the inverse of the invertible part of $G_{sV}(s)$ which is represented as $\tilde{G}^-_{sV}(s)^{-1}$ and a low pass filter $G_{lpf}(s)$ to improve robustness against any model mismatches. Where $\lambda_V$ is the only parameter that requires tuning in the IMC design of the voltage controller and '$n$' is the order of the low pass filter whose value is considered as 1. After substituting the necessary terms into (32), $K_V(s)$ is obtained as shown in (33).

$$G_{cV}(s) = \tilde{G}^-_{sV}(s)^{-1} \times G_{lpf}(s) = \tilde{G}^-_{sV}(s)^{-1} \times \frac{1}{(1 + s\lambda_V)^n} \tag{31}$$

$$K_V(s) = \frac{G_{cV}(s)}{1 - G_{cV}(s)\tilde{G}_{sV}(s)} \tag{32}$$

$$K_V(s) = \frac{C_f(s + j\omega)(1 + s\tau_{cc})}{s\lambda_V} \tag{33}$$

After rearranging the real and imaginary terms, the appearance of $K_V(s)$ in its generic form is shown in (34). Real part terms determine the coefficients of the controller in the forward path and imaginary terms determine the coefficients

of the controller in the coupling path. The terms shown in this (34) are calculated from (35) and (36).

$$K_V(s) = \left(K'_{Pvc} + sK'_{Dvc}\right) + j\left(K''_{Pvc} + \frac{K''_{Ivc}}{s}\right) \tag{34}$$

$$K'_{Pvc} = \frac{C_f}{\lambda_V} \text{ and } K'_{Dvc} = \frac{C_f \tau_{cc}}{\lambda_V} \tag{35}$$

$$K''_{PV} = \frac{C_f \omega_0 \tau_{cc}}{\lambda_V} \text{ and } K''_{IV} = \frac{2C_f \omega_0}{\lambda_V} \tag{36}$$

## IV. RESULTS AND DISCUSSION

A single DGS-based system feeding a three-phase load with a nominal voltage and frequency of 440V and 50 Hz is considered as microgrid in this study. The rated capacity of the DGS is 25kW+j25kVar. The rated input DC voltage to the inverter is 540V. The output of the inverter is processed through an LC filter whose values are $R_f = 0.1$ mΩ, $L_f = 1$ mH, and $C_f = 5$ $\mu$F. The parameters of the load line (the line connecting to the load) are $R = 12.7$ mΩ/km, $L_c = 0.933$ mH/km. The output of the inverter is regulated by a cascaded power-voltage-current controller. The three control schemes (conventional TVSG-PIVA, proposed MVSG-PIVA, and proposed MVSG-IMCVA) are implemented for the transient response analysis of the system. The control parameters and ratings of the study microgrid are shown in Table 1. The performance of the control schemes is studied under grid-connected and islanded modes of operation of the study microgrid.

**TABLE 1. System Control Parameters and Ratings**

| Parameter | Description | Value |
|---|---|---|
| $J$ | Equivalent rotor inertia (kg-m$^2$) | 56.3 |
| $\omega_o$ | Nominal angular frequency (rad/s) | 314.7 |
| $K_{p-\omega}$ | Active power loop gain (pu) | 20 |
| $D$ | Damping coefficient (pu) | 17 |
| $K_{q-v}$ | Reactive power loop gain | 1.48x10$^{-3}$ |
| $K_{Pvc}$ | Proportional coefficient of the voltage controller | 0.004 |
| $K_{Ivc}$ | Integral coefficient of the voltage controller | 0.2487 |
| $K_{Pcc}$ | Proportional coefficient of the current controller | 0.0032 |
| $K_{Icc}$ | Integral coefficient of the current controller | 0.1 |
| $K'_{Pvc}$ | Proportional coefficient of the PD controller in the forward path of the voltage controller | 25 |
| $K'_{Dvc}$ | Derivative coefficient of the PD controller in the forward path of the voltage controller | 0.05 |
| $K''_{Pvc}$ | Proportional coefficient of the PI controller in the cross-coupling path of voltage controller | 15.7 |
| $K''_{Ivc}$ | Integral coefficient of the PI controller in the cross-coupling path of the voltage controller | 7.85x10$^3$ |
| $K'_{Pcc}$ | Proportional coefficient of the PID controller in the forward path of the current controller | 100 |
| $K'_{Icc}$ | Integral coefficient of the PID controller in the forward path of the current controller | 4.94x10$^3$ |
| $K'_{Dcc}$ | Derivative coefficient of PID controller in the forward path of the current controller | 0.05 |

### A. GRID CONNECTED MODE OF OPERATION

Here, an IEEE 9 bus system whose single line diagram is shown in Fig. 13 is used to create a realistic multi-machine model-based grid. The modeling of the IEEE 9 bus system and the values of its corresponding parameters is done as per the IEEE standard discussed in [35]. The connection and disconnection of the microgrid with the existing grid is done by closing/opening SW. In this section, the performance of various control schemes is assessed based on their response during grid-connected mode of operation. For this assessment, load changes are made to the microgrid's local load (MG Load) that is connected to the "Load bus".

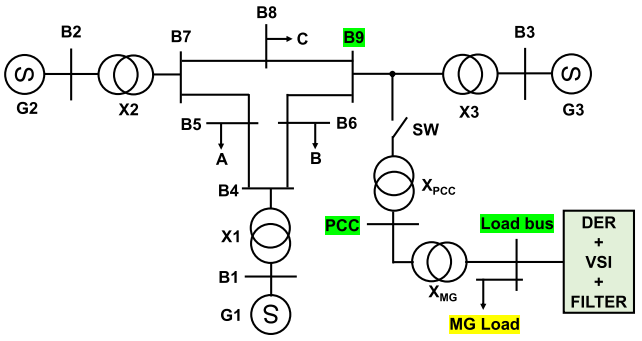



**FIGURE 13. Power system layout comprising of the microgrid connected to IEEE 9 bus system.**

MG load comprises of two separate loads namely Load-1 and Load-2. Load-1 is a fixed and continuous type of series R-L load with resistive loading of 1.2kW and inductive loading of 0.3kVar and Load-2 is a momentary load. It is verified that the IEEE 9 bus system takes around 36 sec to reach a steady state after startup. Therefore, to avoid overlap in dynamics, the microgrid under study is connected to grid by closing SW at t = 40 sec. Next, Load-2 which is designed for a resistive loading of 10kW and inductive loading of 12kVar is applied during 50 to 60 secs. The impact of these load changes on the frequency profile is studied at three different locations viz., load bus, PCC, and B9. Among the three locations, the frequency at B9 is considered as the grid frequency. The corresponding frequency profiles at load bus, PCC, and B9 are shown in Fig. 14(a), Fig. 15(a), and Fig. 16(a) respectively. The respective zoomed aspects of these frequency profiles are shown in Fig. 14(b), Fig. 15(b), and Fig. 16(b). As the existing grid is more powerful than the microgrid, the existing grid determines the frequency in grid-connected mode. This feature is observed in Fig. 14(b), Fig. 15(b), and Fig. 16(b), where the responses of all three methods are similar with no noticeable differences during the grid-connected mode of operation. However, among the three the frequency profile at MG load bus is coarser among all. While that at B9 is smooth, and at MG load bus falls in the middle.

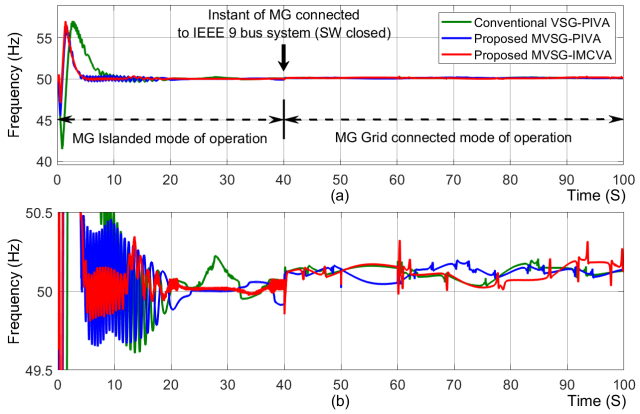



**FIGURE 14.** Frequency results at MG load bus.

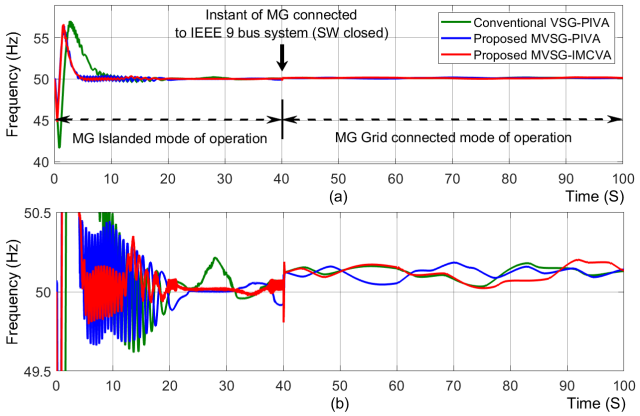



**FIGURE 15.** Frequency results at PCC.

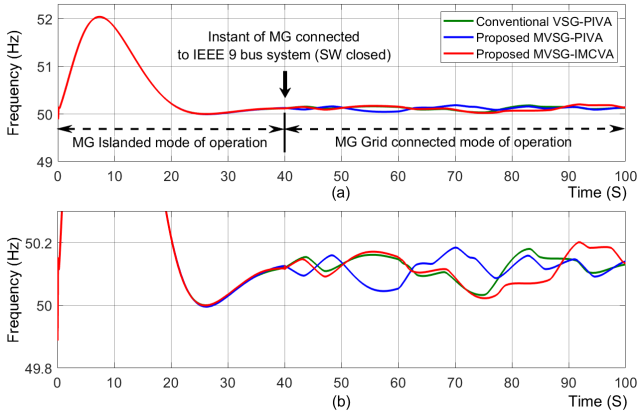



**FIGURE 16.** Frequency results at B9.

In summary, the performance of the studied control schemes cannot be assessed in grid-connected mode of operation. Hence their performance is verified in the islanded mode of operation, where the grid support will not exist.

### *B. ISLANDED MODE OF OPERATION*

Here, the performance of the control schemes is studied based on the performance of the microgrid in the islanded mode of operation during load changes on MG load. The summary of the loads of MG load under various test cases is shown in Table 2. The entire load is segregated into two parts (Load-1 and Load-2). Load-1 is a fixed and continuous type of series R-L load with resistive loading of 1200W and inductive loading of 300Var. Load-2 is a momentary load that remains active from 80 to 100 secs. Also, the value and the type of load-2 are varied in different test cases to test the system under a wide range of power factors. In test case 1, the values of resistive and inductive load parts of load-2 are carefully adjusted to ensure resistively dominant load power factor conditions. Examples of large inductively dominant loads are HVAC systems which generally operate at power factors of less than 0.5, induction motors at power factors of 0.2 under light load conditions, and some reactive power compensation coils at power factors close to zero. Keeping in view of these load conditions, the values of resistive and inductive load parts of load-2 in test case 2 and test case 3 are carefully adjusted to come under a wide operating power factor range of 0.1-0.5.

**TABLE 2.** Summary of load configurations used in various test cases.

| Test Case | | Overall load power factor (approx., lagging) | Load-1 | | Load-2 | | |
|---|---|---|---|---|---|---|---|
| | | | R-load (W) | L-Load (Var) | R-load (W) | L-Load (Var) | Load Type |
| 1 | (a) | 0.90 | 1200 | 300 | 2000 | 700 | R load |
| | (b) | 0.99 | 1200 | 300 | 5000 | 700 | |
| 2 | (a) | 0.50 | 1200 | 300 | 300 | 3000 | Series R-L load |
| | (b) | 0.30 | 1200 | 300 | 300 | 5000 | |
| | (c) | 0.10 | 1200 | 300 | 300 | 10000 | |
| 3 | (a) | 0.50 | 1200 | 300 | 300 | 3000 | Parallel R-L load |
| | (b) | 0.30 | 1200 | 300 | 300 | 5000 | |
| | (c) | 0.10 | 1200 | 300 | 300 | 10000 | |

From Fig. 17 to Fig. 32 correspond to the results of test cases 1, 2, and 3 as per Table 2, it is identified that when VSG is deployed for the power controller, the system's frequency has returned to 50Hz when subjected to load changes. This confirms the merit of the VSG in ensuring the system's stability during the steady state. The results of active power, reactive power, and voltage are also included to investigate the effectiveness of the three control schemes.

To emphasize the effect of the loading, frequency results under all test cases are presented. However, the results of voltage, active power, and reactive power are presented only for test cases 1(b), 2(c), and 3(c) as these cases correspond to the highest loading of test case-1, test case-2, and test case-3. In the present study, transients due to the sudden introduction of load-2 at the time instant of 80 sec (referred to as T80), and the sudden removal of load-2 at 100 sec (referred to as T100) are implemented.

#### 1) OBSERVATIONS OF TEST CASE-1

The concept of VSG control is primarily introduced in the literature to limit the rate of change of frequency when subjected to sudden changes in active power demands. Thus,

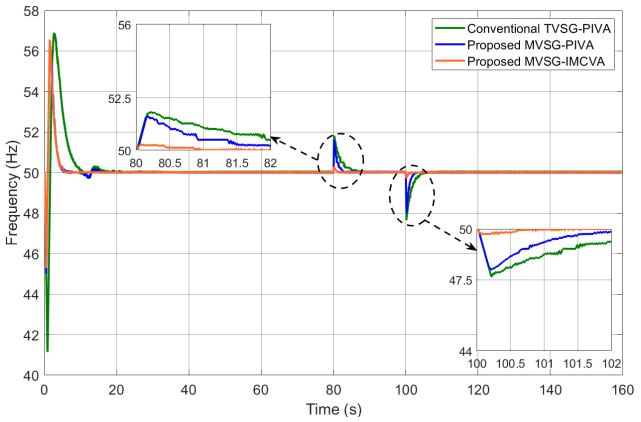



**FIGURE 17.** Frequency results of test case 1(a).

all three schemes are tested with dominantly resistive (active) power factor loads. The corresponding test cases 1(a) and 1(b) are implemented as described in Table 2 and their simulation results are shown in Fig. 17 to Fig. 20.

In test case 1(a), corresponding to T80, the instantaneous frequency value with any of the three schemes has not crossed the upper limit, thus, there is no chance of tripping. Further, corresponding to T100, the instantaneous frequency with any of the three schemes has not crossed the lower limit, thus, there is no chance of tripping. Therefore, under both T80 and T100, the system is stable with all three schemes. As seen from the zoomed aspect of T80 and T100 in Fig. 17, the TVSG-PIVA scheme is inferior to the other two schemes as it produces the largest overshoot and longest settling time.

The response of the MVSG-PIVA scheme shows moderate performance with almost the same magnitude of overshoot/undershoot as like TVSG-PIVA scheme but with lesser settling time. However, the proposed MVSG-IMCVA scheme provided the best response with the least overshoot/undershoot and settling time. The performance of all three schemes under test case 1(b) is analyzed from the zoomed aspects of T80 and T100 from frequency results shown in Fig. 18. In case of the TVSG-PIVA scheme, corresponding to T80, the overshoot in frequency with a deviation of 3.78Hz had crossed the upper limit of 52.5Hz and took 1.18sec to return. This is greater than the set clearing time of 1sec and therefore tripping occurs. In the case of the MVSG-PIVA scheme, the overshoot with a deviation of 3.17Hz has crossed the upper limit but returned to safe limits within 0.43 sec, which means nuisance tripping is avoided. Similarly, corresponding to T100, the undershoot in frequency with the TVSG-PIVA scheme has shown a deviation of $-5.5$Hz, thus crossing the lower limit of 47.5Hz and taking 1.36 sec to return, which leads to tripping. Further, with the MVSG-PIVA scheme, the overshoot with a deviation of 3.17Hz has crossed the upper limit but returned to the safe limit within 0.63sec, which means tripping is avoided. These observations confirm that by replacing the conventional TVSG with the proposed MVSG, the chances of nuisance tripping against dominant resistive loading can be reduced.

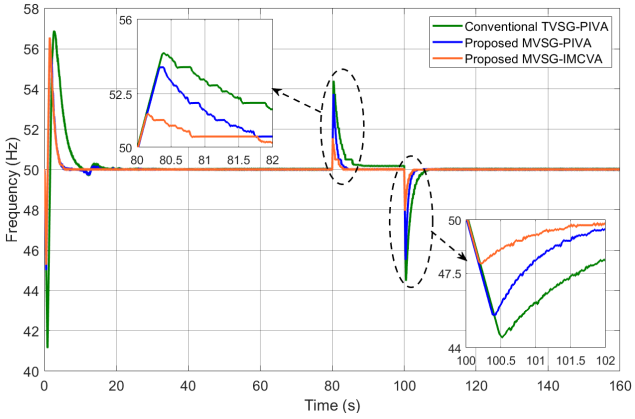



**FIGURE 18.** Frequency results of test case 1(b).

With the proposed MVSG-IMCVA scheme, Under T80, the deviation in overshoot is 1.16Hz, and under T100, the deviation in undershoot is $-2$Hz. This means that in either situation, the crossing of either upper limit or lower limit has not occurred, thereby the tripping action won't be triggered. Hence, the proposed MVSG-IMCVA scheme is superior in avoiding nuisance tripping under resistively dominant load switching when compared to the other schemes.

The results of the voltage in this test case 1(b) are shown in Fig. 19. From the zoomed portions of Fig. 19, it is noticed that for transient at T80, the conventional TVSG-PIVA scheme (Fig. 19(a)) shows a voltage deviation of 8.64% with a settling time of 1.1sec leading to tripping. With the MVSG-PIVA (Fig. 19(b)), even though the deviation is 8.64%, as the settling time is 0.7sec, tripping is avoided. With the proposed MVSG-IMCVA scheme (Fig. 19(c)), as the deviation is 2.95%, there is no chance of tripping. Corresponding to the transient at T100, the conventional TVSG-PIVA scheme (Fig. 19(a)) shows a voltage deviation of $-12.5\%$ with a settling time of 1.3sec leading to tripping. With the MVSG-PIVA (Fig. 19(b)), even though the deviation is $-12.5\%$, as the settling time is 0.7sec, tripping is avoided. With the proposed MVSG-IMCVA scheme (Fig. 19(c)), as the deviation is $-4.55\%$, there is no chance of tripping. Under both T80 and T100, the proposed MVSG-IMCVA scheme had shown deviation indicating crossing of $\pm 5\%$ limit which indicates no tripping action is triggered by the voltage relay. Further, it is identified that the transient response of the proposed MVSG-IMCVA scheme is superior, followed by MVSG-PIVA and TVSG-PIVA schemes respectively. The results of the active power in this test case 1(b) are shown in Fig. 20. Longer settling time is noticed with the conventional TVSG-PIVA scheme than with the proposed schemes.

### 2) OBSERVATIONS OF TEST CASE-2

In test case-1, the superiority of the proposed MVSG is validated with respect to active power loading. Now, this

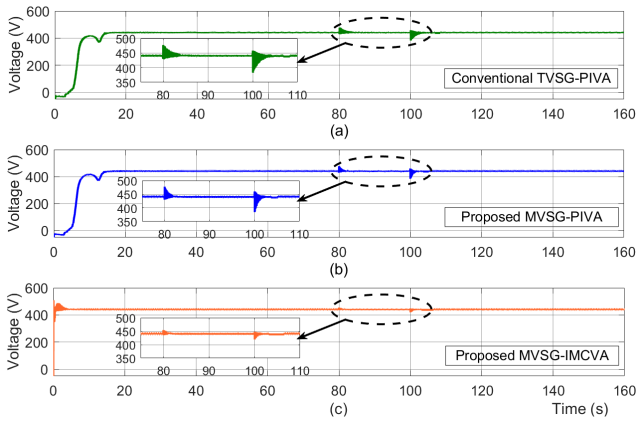



**FIGURE 19.** Voltage results of test case 1(b).

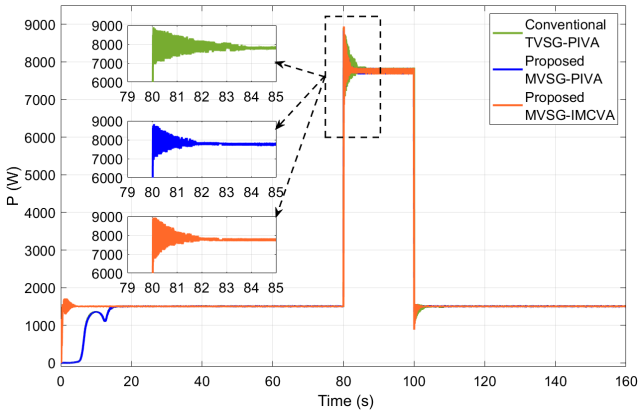



**FIGURE 20.** Active power results of test case 1(b).

section presents the results of test case-2, where all three schemes are tested with series R-L load. The testing is conducted in three stages with the resistive part of the load is fixed and the inductive element is varied. These are referred to as test cases 2(a), 2(b), and 2(c). The corresponding results of these test cases are shown in Fig. 21 to Fig. 26.

In test case 2(a), from Fig. 21, corresponding to T80, the undershoot in frequency with TVSG-PIVA, MVSG-PIVA, and MVSG-IMCVA schemes have deviations of −1.91Hz, −1.7Hz, and −0.65Hz respectively. Thus, there is no chance of tripping with any of the schemes. Corresponding to T100, the overshoot in frequency with TVSG-PIVA and MVSG-PIVA schemes has deviations of 2.4Hz and 2.08Hz respectively. Whereas, the MVSG-IMCVA scheme shows an undershoot with a deviation of −0.65Hz. Since none of these values has crossed safe limits, thereby there is no chance of tripping with any of the schemes. Moreover, these values indicate that under both T80 and T100, the transient response of the TVSG-PIVA scheme is inferior to the other two schemes. This can be justified by the largest overshoot and longest settling time. The response of the MVSG-PIVA scheme shows moderate performance and the proposed MVSG-IMCVA scheme shows the best performance.

In test case 2(b), from Fig. 22, corresponding to T80, the undershoot in frequency with TVSG-PIVA and MVSG-PIVA schemes has deviations of −3.05Hz and −2.6Hz respectively. These values indicate the triggering of the tripping process. However, since the corresponding settling times of these schemes are 0.29sec and 0.03sec respectively, the tripping is avoided. While the deviation is only −1.17Hz with the proposed MVSG-IMCVA scheme, the tripping process is not initiated. Therefore, there is no chance of tripping in this test case under T80 with any of the schemes. Corresponding to T100, the overshoot in frequency with TVSG-PIVA and MVSG-PIVA schemes has deviations of 4.05Hz and 3.38Hz respectively which indicate the initiation of the tripping process. However, since the corresponding settling times of these schemes are 0.46sec and 0.12sec respectively, the tripping is avoided. While the deviation with the proposed MVSG-IMCVA scheme is only −0.64Hz, the tripping process is not initiated. Thus, the chances of tripping in this test case under T100 with any of the schemes are avoided. Further, similar to test case 2(a), it is observed that the proposed MVSG-IMCVA scheme shows superior transient response under test case 2(b) as well.

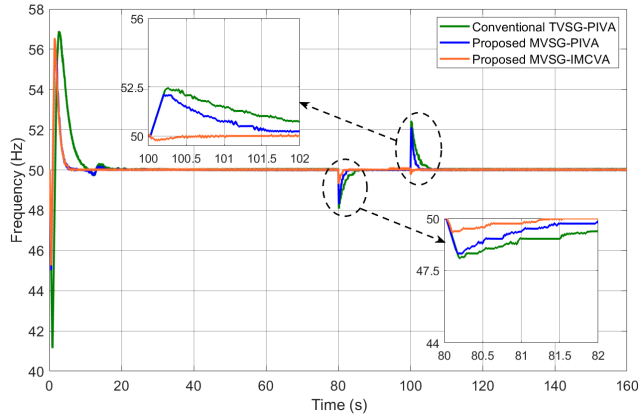



**FIGURE 21.** Frequency results of test case 2(a).

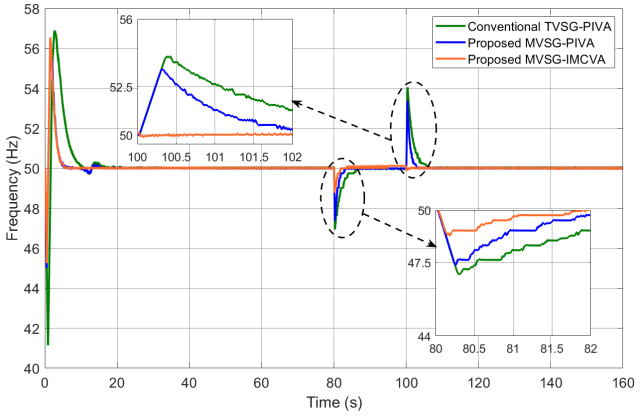



**FIGURE 22.** Frequency results of test case 2(b).

The frequency results of the test case 2(c) are shown in Fig. 23. In this, corresponding to T80, the conventional TVSG-PIVA scheme with a frequency deviation of −5Hz and with a settling time of 1.46sec leads to tripping. MVSG-PIVA even though has a −4.3Hz deviation, its settling time is 0.62sec. Therefore, the tripping action is suspended. With the proposed MVSG-IMCVA scheme, as the deviation is −2.3Hz only, tripping is completely avoided. Corresponding to T100, the conventional TVSG-PIVA scheme shows a frequency deviation of 6.9Hz with a settling time of 1.83sec and the MVSG-PIVA scheme shows a frequency deviation of 5.4Hz with a settling time of 1.2sec. Therefore, nuisance tripping occurs with either of these schemes. But, as the deviation in frequency with the proposed MVSG-IMCVA scheme is only −0.64Hz, tripping with respect to frequency is avoided.

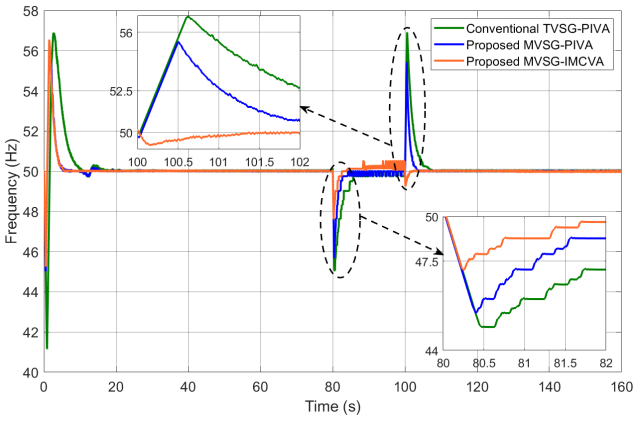



**FIGURE 23.** Frequency results of test case 2(c).

The results of the voltage in this test case 2(c) are shown in Fig. 24. From the zoomed portions of Fig. 24, it is noticed that for transient at T80, the conventional TVSG-PIVA scheme (Fig. 24(a)) shows a voltage deviation of −14.77% with a settling time of 2.3sec leading to tripping. The MVSG-PIVA (Fig. 24(b)), shows a deviation of −14.77% with a settling time of 1.2sec leading to tripping. With the proposed MVSG-IMCVA scheme (Fig. 24(c)), even though the deviation is −6.82%, as the settling time is 0.4sec, tripping is avoided.

Corresponding to the transient at T100, the conventional TVSG-PIVA scheme (Fig. 24(a)) shows a voltage deviation of 14.77% with a settling time of 2.0sec leading to tripping. The MVSG-PIVA (Fig. 24(b)), shows a voltage deviation of 14.77% with a settling time of 1.1sec leading to tripping. With the proposed MVSG-IMCVA scheme (Fig. 24(c)), as the deviation is 1.14%, there is no chance of tripping. Under both T80 and T100, the proposed MVSG-IMCVA scheme avoided tripping by the voltage relay. Moreover, it is identified that the transient response of the proposed MVSG-IMCVA scheme is superior, followed by MVSG-PIVA and TVSG-PIVA schemes respectively.

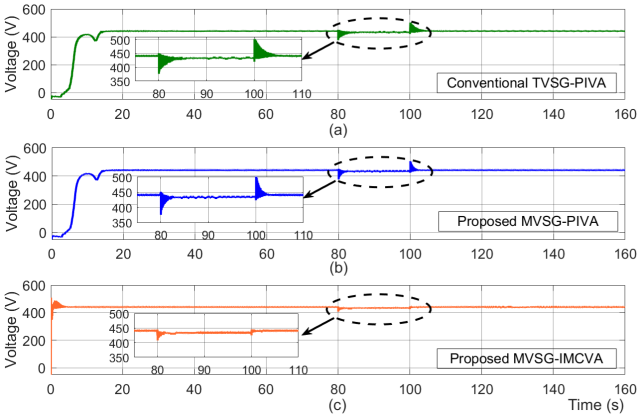



**FIGURE 24.** Voltage results of test case 2(c).

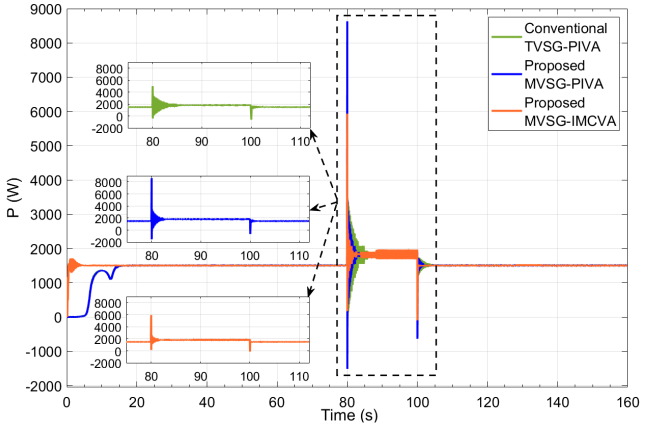



**FIGURE 25.** Active power results of test case 2(c).

The active and reactive power results in test case 2(c) are shown in Fig. 25 and Fig. 26 respectively. From the zoomed portion of Fig. 25, it is noticed that the application of a large inductive load has caused a surge in active power immediately after T80. Even though the surge in conventional TVSG-PIVA is minimal, it suffers from longer settling time. On the other hand, even though there is a little higher surge observed with the proposed MVSG-IMCVA scheme, the surge settling time is very less. This indicates an improved transient response with the proposed MVSG-IMCVA scheme.

The zoomed portion of Fig. 26 shows that the conventional TVSG-PIVA scheme produces a little lower surge in reactive power than the proposed MVSG-IMCVA scheme. However, there is no advantage of the TVSG-PIVA scheme as it suffered from nuisance tripping, thus failed to maintain frequency stability, as per the above explanation referring to Fig. 23. Moreover, the VSG should draw extra active power from the reserve capacity to maintain the frequency within the limits. In this aspect, conventional TVSG failed to maintain the task while MVSG successfully tried to extract more active power from the source. Therefore, better frequency regulation

and stability are achieved through the MVSG-based scheme.

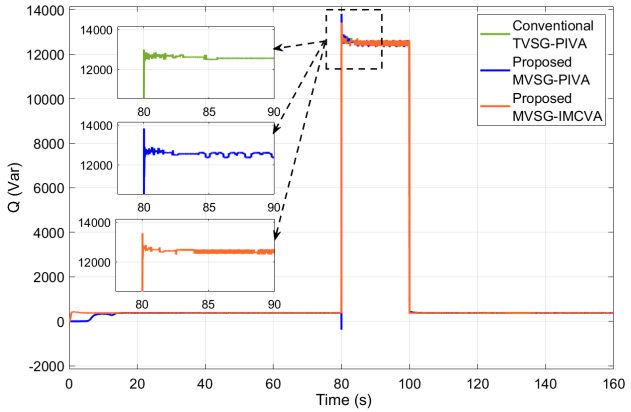



**FIGURE 26.** Reactive power results of test case 2(c).

### 3) OBSERVATIONS OF TEST CASE-3

In test case-3, the performance of all three schemes is observed when a parallel R-L load is deployed. The corresponding results are shown in Fig. 27 to Fig. 32.

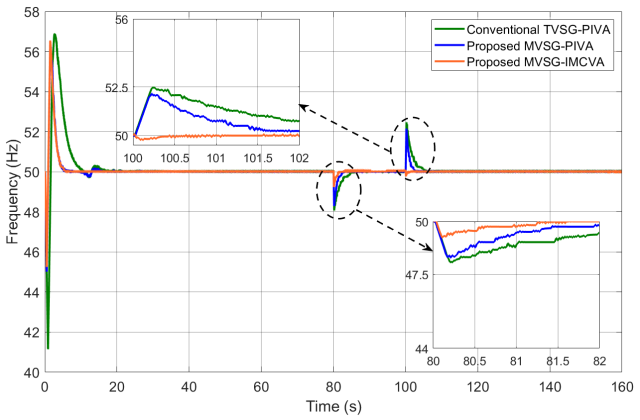



**FIGURE 27.** Frequency results of test case 3(a).

In test case 3(a), from Fig. 27, corresponding to T80, the undershoot in frequency with TVSG-PIVA, MVSG-PIVA, and MVSG-IMCVA schemes have deviations of −1.92Hz, −1.71Hz, and −0.76Hz respectively. Thus, there is no chance of tripping in this test case with any of the schemes. Also, corresponding to T100, the overshoot in frequency with TVSG-PIVA and MVSG-PIVA schemes has deviations of 2.5Hz and 2.2Hz respectively. While the MVSG-IMCVA scheme shows an undershoot with a deviation of −0.21Hz. Since none of these values has crossed safe limits, there is no chance of tripping. Moreover, these values under both T80 and T100 indicate that the proposed MVSG-IMCVA scheme leads to a superior transient response than the other schemes.

In test case 3(b), from Fig. 28, corresponding to T80, the undershoot in frequency with TVSG-PIVA and MVSG-PIVA schemes has deviations of −3.06Hz and −2.64Hz

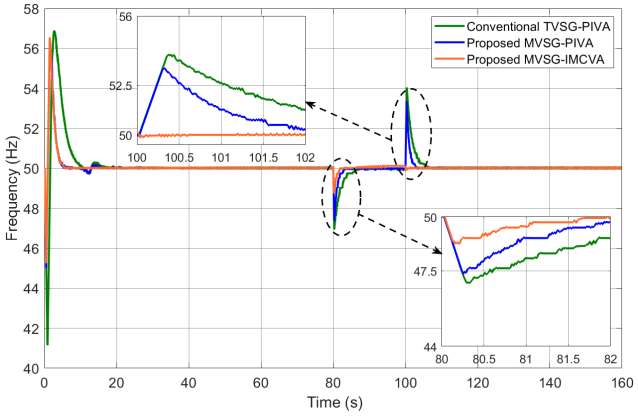



**FIGURE 28.** Frequency results of test case 3(b).

respectively. These values indicate the triggering of the tripping process. However, as the corresponding settling time of these schemes are 0.32sec and 0.06sec respectively, which are within safe limits, the tripping is avoided. While the deviation is only −1.25Hz with the proposed MVSG-IMCVA scheme, the tripping process is not initiated. Therefore, there is no chance of tripping in this test case under T80 with any of the schemes. Corresponding to T100, the overshoot in frequency with TVSG-PIVA and MVSG-PIVA schemes has deviations of 4.03Hz and 3.34Hz respectively that indicate the initiation of the tripping process. However, since the corresponding settling times of these schemes are 0.85sec and 0.29sec respectively, the tripping is avoided. While the deviation with the proposed MVSG-IMCVA scheme is only −0.58Hz, the tripping process is not initiated. Thus, there is no chance of tripping in this test case under T100 with any of the schemes.

In test case 3(c), the zoomed aspects of T80 and T100 in Fig. 29 help for the following analysis. Corresponding to T80, the TVSG-PIVA scheme with a frequency deviation of −5.1Hz and with a settling time of 1.57sec leads to tripping. While, with the MVSG-PIVA scheme, even though there is a deviation of −4.35Hz, its settling time is 0.64sec. Thus, the tripping action is suspended. With the proposed MVSG-IMCVA scheme, since the deviation is −2.34Hz only, tripping is completely avoided. Corresponding to T100, the TVSG-PIVA scheme shows a frequency deviation of 6.87Hz with a settling time of 1.86sec will cause tripping. The MVSG-PIVA scheme shows a frequency deviation of 5.52Hz with a settling time of 0.81sec avoids nuisance tripping based on frequency. However, since the deviation in frequency with the proposed MVSG-IMCVA scheme is only −0.73Hz, tripping with respect to frequency is completely avoided.

The results of the voltage in this test case 3(c) are shown in Fig. 30. From the zoomed portions of Fig. 30, it is noticed that for transient at T80, the conventional TVSG-PIVA scheme (Fig. 30(a)) shows a voltage deviation of −14.77% with a settling time of 2.5sec leading to tripping. The MVSG-PIVA (Fig. 30(b)), shows a deviation of −14.77%

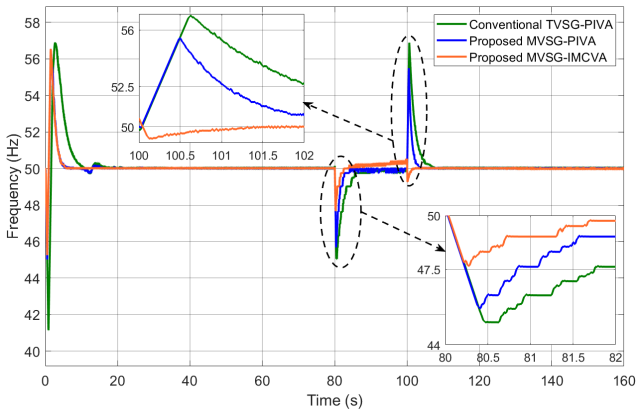



**FIGURE 29.** Frequency results of test case 3(c).

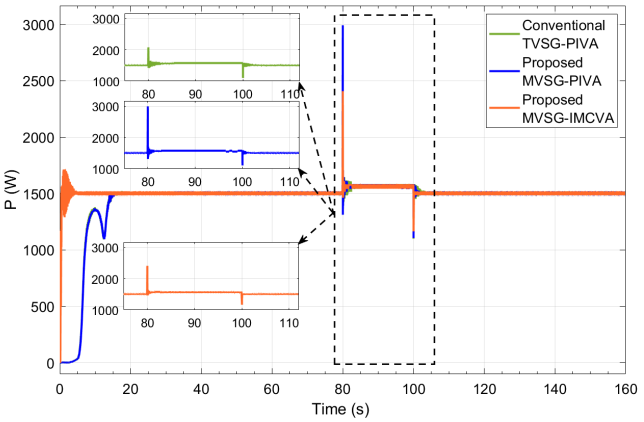



**FIGURE 31.** Active power results of test case 3(c).

with a settling time of 1.4sec leading to tripping. With the proposed MVSG-IMCVA scheme (Fig. 30(c)), even though the deviation is −7.95%, as the settling time is 0.5sec, tripping is avoided. Corresponding to the transient at T100, the conventional TVSG-PIVA scheme (Fig. 30(a)) shows a voltage deviation of 14.77% with a settling time of 2.2sec leading to tripping. The MVSG-PIVA (Fig. 30(b)), shows a voltage deviation of 14.77% with a settling time of 1.1sec leading to tripping. With the proposed MVSG-IMCVA scheme (Fig. 30(c)), as the deviation is 1.14%, there is no chance of tripping. Under both T80 and T100, the proposed MVSG-IMCVA scheme avoided tripping by the voltage relay. In this test case, it is found that the transient response of the proposed MVSG-IMCVA scheme is superior.

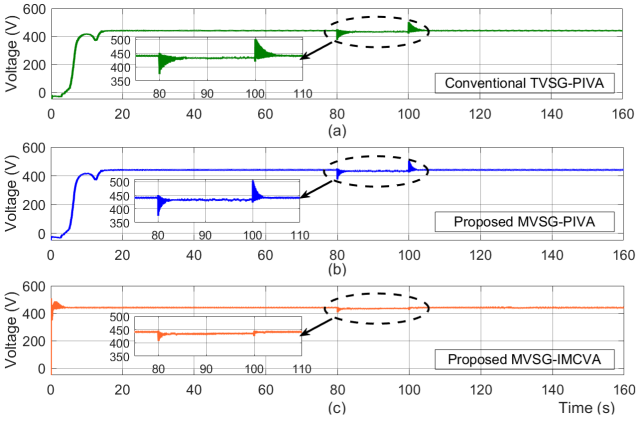



**FIGURE 30.** Voltage results of test case 3(c).

The active and reactive power results in test case 3(c) are shown in Fig. 31 and Fig. 32, respectively. From the zoomed portion of Fig. 31, it is noticed that the application of a large inductive load caused a surge in active power immediately after T80. Even though the surge in conventional TVSG-PIVA is minimal, it suffers from longer settling time.

On the other hand, even though there is a little higher surge observed with the proposed MVSG-IMCVA scheme,

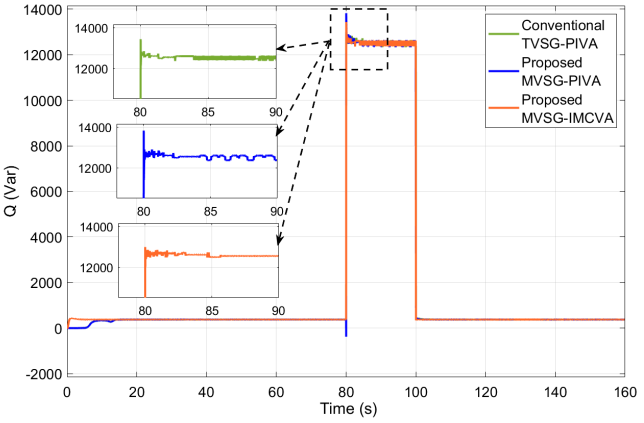



**FIGURE 32.** Reactive power results of test case 3(c).

the surge settling time is very less. This indicates an improved transient response with the proposed MVSG-IMCVA scheme. Similarly, from the zoomed portion of Fig. 32, it is observed that the deviation and settling time are less with the proposed MVSG-IMCVA scheme than with the conventional TVSG-PIVA scheme.

A cumulative comparison in terms of frequency and voltage transient response metrics of the conventional and proposed schemes under different test cases is presented in Table 3. From this, the chances of tripping can be analyzed as follows.

- All the highlighted values indicate a violation of the allowed limits (either magnitude or settling time).
- The values with * as superscript in frequency/voltage characteristics indicate the violation of magnitude limits. This may lead to the tripping of the corresponding relay, which is confirmed by their settling time condition.
- The values with ** as superscript in frequency/voltage characteristics indicate that the settling time of the magnitude deviations is greater than the set clearing time of the relays, which indicates the violation of the time limits. Thus, leading to tripping.

**TABLE 3.** Transient response comparison of frequency and voltage under T80 (load switch on) and T100 (load switch off).

| Performance Parameter | Test Case | Under T80 (Load Switch ON) | | | Under T100 (Load Switch OFF) | | |
|---|---|---|---|---|---|---|---|
| | | Conventional TVSG-PIVA [21] | Proposed MVSG-PIVA | Proposed MVSG-IMCVA | Conventional TVSG-PIVA [21] | Proposed MVSG-PIVA | Proposed MVSG-IMCVA |
| **Frequency Characteristics** | | | | | | | |
| **Transient Frequency Deviation (Hz)** ▪ Nominal value = 50 Hz ▪ Desired deviation ≤ 2.5Hz (±5% of 50 Hz) +ve indicates overshoot -ve indicates undershoot | 1(a) | 1.83 | 1.61 | 0.28 | **-2.36*** | -2.00 | -0.30 |
| | 1(b) | **3.78*** | **3.17*** | 1.16 | **-5.50*** | **-4.50*** | -2.00 |
| | 2(a) | -1.91 | -1.70 | -0.65 | 2.40 | 2.08 | -0.20 |
| | 2(b) | **-3.05*** | **-2.60*** | -1.17 | **4.05*** | **3.38*** | -0.08 |
| | 2(c) | **-5.01*** | **-4.30*** | -2.30 | **6.90*** | **5.40*** | -0.64 |
| | 3(a) | -1.92 | -1.71 | -0.76 | **2.50*** | 2.20 | -0.21 |
| | 3(b) | **-3.06*** | **-2.64*** | -1.25 | **4.03*** | **3.34*** | -0.58 |
| | 3(c) | **-5.10*** | **-4.35*** | -2.34 | **6.87*** | **5.52*** | -0.73 |
| **Transient Frequency Overshoot/Undershoot Settling Time (sec)** ▪ Desired value ≤ 1 sec | 1(a) | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1(b) | **1.18** (trip)** | 0.43 | 0 | **1.36** (trip)** | 0.63 | 0 |
| | 2(a) | 0 | 0 | 0 | 0 | 0 | 0 |
| | 2(b) | 0.29 | 0.03 | 0 | 0.46 | 0.12 | 0 |
| | 2(c) | **1.46** (trip)** | 0.62 | 0 | **1.83** (trip)** | **1.20** (trip)** | 0 |
| | 3(a) | 0 | 0 | 0 | 0 | 0 | 0 |
| | 3(b) | 0.32 | 0.06 | 0 | 0.85 | 0.29 | 0 |
| | 3(c) | **1.57** (trip)** | 0.64 | 0 | **1.86** (trip)** | 0.81 | 0 |
| **Voltage Characteristics** | | | | | | | |
| **Transient Voltage Deviation (%)** ▪ Desired deviation ≤ ±5% +ve indicates overshoot -ve indicates undershoot | 1(a) | 3.41 | 3.41 | 0.00 | -4.55 | -4.55 | 0.00 |
| | 1(b) | **8.64*** | **8.64*** | 2.95 | **-12.50*** | **-12.50*** | -4.55 |
| | 2(a) | -4.55 | -3.86 | -2.05 | **5.23*** | **5.23*** | 0.68 |
| | 2(b) | **-7.95*** | **-7.95*** | -3.41 | **7.95*** | **7.95*** | 0.68 |
| | 2(c) | **-14.77*** | **-14.77*** | **-6.82*** | **14.77*** | **14.77*** | 1.14 |
| | 3(a) | -4.32 | -4.32 | -1.82 | **5.23*** | **5.23*** | 0.68 |
| | 3(b) | **-7.95*** | **-7.95*** | -4.09 | **7.95*** | **7.95*** | 0.68 |
| | 3(c) | **-14.77*** | **-14.77*** | **-7.95*** | **14.77*** | **14.77*** | 1.14 |
| **Transient Voltage Settling Time (sec)** ▪ Desired value ≤ 1 sec | 1(a) | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1(b) | **1.1** (trip)** | 0.7 | 0 | **1.3** (trip)** | 0.7 | 0 |
| | 2(a) | 0 | 0 | 0 | 0.2 | 0.1 | 0 |
| | 2(b) | 0.5 | 0.2 | 0 | **1.1** (trip)** | 0.5 | 0 |
| | 2(c) | **2.3** (trip)** | **1.2** (trip)** | 0.4 | **2** (trip)** | **1.1** (trip)** | 0 |
| | 3(a) | 0 | 0 | 0 | 0.2 | 0.1 | 0 |
| | 3(b) | 0.9 | 0.4 | 0 | **1.2** (trip)** | 0.6 | 0 |
| | 3(c) | **2.5** (trip)** | **1.4** (trip)** | 0.5 | **2.2** (trip)** | **1.1** (trip)** | 0 |

Therefore, when both the values of magnitude and settling time limits are violated (the values with ** superscript indication), nuisance tripping will occur.

The effect of dominant reactive power loading on the active power characteristics is shown in Table 4. From this, it is observed that under T80, even though the conventional TVSG-PIVA scheme produces the lowest deviation, it leads to a large settling time when compared to the proposed MVSG-PIVA and MVSG-IMCVA schemes. Further, under T100, the proposed MVSG-IMCVA scheme produces the lowest deviation as well as the settling time when compared to the conventional TVSG-PIVA scheme.

## V. CONCLUSION

This paper compares the transient response of conventional TVSG-PIVA and proposed MVSG-PIVA/MVSG-IMCVA control schemes. All the schemes are examined under three different test cases, namely resistively dominant load switchings, inductively dominant series RL load switchings, and inductively dominant parallel RL load switchings. The effectiveness of these schemes is analyzed by considering standard tolerances of voltage and frequency magnitudes, and their settling times. From the summary of outcomes given in Table 3, the salient observations from these studies are given as follows.

- ***Dominant Resistive Loading:*** Under both T80 and T100, the TVSG-PIVA scheme leads to tripping in test case 1(b) due to frequency and voltage deviation. However, no tripping occurred when MVSG-PIVA or MVSG-IMCVA were used. This observation confirms that by replacing the conventional TVSG with the proposed MVSG control, the chances of nuisance tripping against dominant resistive load switching can be reduced.
- ***Dominant Reactive Loading (Series R-L Load):*** In test case 2(b), under T100, voltage deviations are the cause of tripping with the TVSG-PIVA scheme. In test case 2(c), under T80 and T100, both frequency and voltage deviations are the cause of tripping with the TVSG-PIVA scheme. Under T80, voltage deviations are the cause of tripping with the MVSG-PIVA scheme, and under T100, both frequency and voltage deviations are the cause of tripping. However, either under T80 or T100, neither frequency nor voltage response has caused tripping when the MVSG-IMCVA scheme is used. This justifies the need to retain the MVSG for the power

controller and replace the PI-based VA controllers with IMC-based VA controllers to avoid nuisance tripping in case of inductively dominant series RL types of loads.

- ***Dominant Reactive Loading (Parallel R-L Load):*** In test case 3(b), under T100, voltage deviations are the cause of tripping with the TVSG-PIVA scheme. In test case 3(c), under T80 and T100, both frequency and voltage deviations are the cause of tripping with the TVSG-PIVA scheme. Under T80 and T100, voltage deviations are the cause of tripping with the MVSG-PIVA scheme. Thus, the MVSG-PIVA scheme could avoid nuisance tripping with respect to frequency response but is susceptible to nuisance tripping due to voltage response. However, in any of the test cases, no tripping is observed when the MVSG-IMCVA scheme is used.

Further, from Table 4, it is confirmed that the effect of transient reactive loading on active power results is faithfully improved with the proposed MVSG-IMCVA scheme.

Therefore, from all the above-mentioned observations, it is concluded that the proposed MVSG-IMCVA control scheme addresses the issue of nuisance tripping by improving the response of the system under transient loading conditions. This empowers the merit of the VSG-based control scheme in stable microgrids.

### A. SCOPE/LIMITATION OF THE PROPOSED SCHEME

- The concept of nuisance tripping is considered under stable operating conditions of the microgrids during the occurrence of transient loadings. Thus, the proposed schemes and the analysis that is presented in this paper assume a stable microgrid test system. The system behavior under real faults that leads to instability is not within the scope of this work.
- The objective of the paper is mainly to study the impact of the load variations on the effectiveness of the proposed control scheme. For this purpose, a large range of power factor (0.9 to 0.1) loading is applied and their impact on the efficacy of the conventional and proposed schemes is studied. So, in this paper, the other variations such as inertia and time constants of low pass filters in VSG are not implemented.

### B. FUTURE RESEARCH ASPECT

The outcomes of this research confirm that the design of the equalizing coefficient in APL of the proposed MVSG, (discussed in Section III-B) empowers the merit of the TVSG. So, to further enhance the capability of the TVSGs, this equalizing coefficient can be adaptively changed with respect to dynamic loading conditions.

## APPENDIX
## DESCRIPTION OF NUISANCE TRIPPING ISSUE

The merit of deploying VSG control is its capability to enhance system stability when compared to droop control. By emulating virtual inertia, the VSG controllers improve frequency stability in both transient and steady-state conditions through the regulation of the rate of change of frequency. However, even though the stability of frequency is guaranteed during the steady state, the response during the transient state may take a longer time to settle. Such transient conditions, where the peak overshoot/undershoot observed in the frequency/voltage that are sustained above the predefined relay's clearing time are treated as a serious deviation by the corresponding relays. Hence, the protective relays may inaccurately interpret these transients as a loss of stability, prompting unnecessary tripping of the connected DGSs, which is referred to as nuisance tripping.

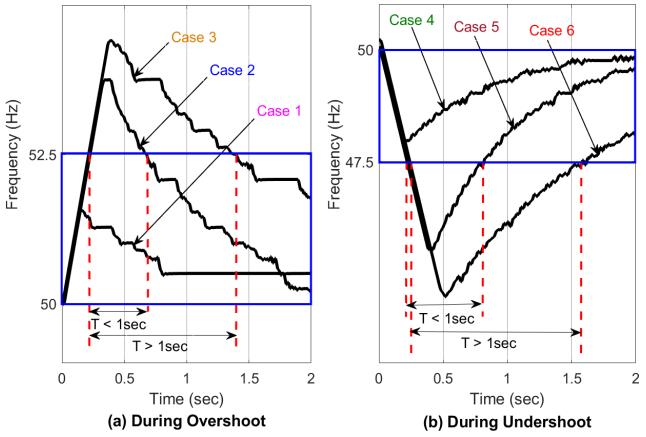



**FIGURE 33. Typical frequency deviation plots to understand the tripping chances in different cases based on magnitude and time conditions.**

One way of avoiding nuisance tripping is by increasing the time setting of the relay. Thus, the manufacturers of frequency and voltage relays normally provide an adjustable range (0-10sec) of clearing time, in which a suitable value will be fixed by the user to avoid nuisance tripping [36]. But, the setting of longer clearing time affects the microgrid's safety in case of a real fault, where tripping is necessary.

Thus, from the above discussion, the merit of the VSG control can be enhanced if it can address the demerit of large overshoot/undershoot and/or longer settling time during transient conditions.

The phenomenon of nuisance tripping considered in this work includes the magnitude condition (upper and lower limits) and the time condition (clearing time). These conditions refer to the permissible limits of voltage and frequency. In this work, for both voltage and frequency, the magnitude condition is defined as $\pm 5\%$ and the time condition as 1sec based on the recommendation of IEEE1547 standard [37], [38], [39]. The condition of nuisance tripping is demonstrated using an assumed frequency characteristics shown in Fig. 33. The same is applicable even for the voltage.

As mentioned above, corresponding to $\pm 5\%$ of 50 Hz, the upper and lower limits of frequency are 52.5 Hz and 47.5 Hz respectively. Thus, the permissible ranges are 50-52.5 Hz for overshoot (as highlighted in Fig. 33(a)) and 47.5-50 Hz for undershoot (as highlighted in Fig. 33(b)). In case of a

**TABLE 4.** Effect of low power factor loading on active power transient response under T80 (load switch on) and T100 (load switch off).

| Performance Parameter | Test Case | Under T80 (Load Switch ON) | | | | Under T100 (Load Switch OFF) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Conventional TVSG-PIVA [21] | Proposed MVSG-PIVA | Proposed MVSG-IMCVA | Best Scheme | Conventional TVSG-PIVA [21] | Proposed MVSG-PIVA | Proposed MVSG-IMCVA | Best Scheme |
| | | (I) | (II) | (III) | (I/II/III) | (I) | (II) | (III) | (I/II/III) |
| **Active Power Deviation (W)** | 2(a) | 709 | 1754 | 1005 | I | -559 | -559 | -468 | III |
| | 2(b) | 1344 | 3197 | 1861 | I | -1188 | -1194 | -843 | III |
| ▪ Desired deviation = Low | 2(c) | 3124 | 6756 | 4061 | I | -2085 | -2129 | -1596 | III |
| +ve indicates overshoot | 3(a) | 125 | 409 | 224 | I | -109 | -97 | -94 | III |
| -ve indicates undershoot | 3(b) | 215 | 704 | 375 | I | -169 | -182 | -161 | III |
| | 3(c) | 502 | 1416 | 833 | I | -400 | -390 | -335 | III |
| **Settling Time (sec)** | 2(a) | 2.88 | 1.47 | 0.61 | III | 2.30 | 1.44 | 0 | III |
| | 2(b) | 3.90 | 1.87 | 1.02 | III | 3.30 | 1.54 | 0 | III |
| ▪ Desired value = Low | 2(c) | 5.66 | 2.55 | 1.65 | III | 4.18 | 1.86 | 0 | III |
| | 3(a) | 2.82 | 1.74 | 0.79 | III | 1.07 | 0.60 | 0 | III |
| | 3(b) | 1.83 | 1.23 | 0.30 | III | 2.03 | 0.97 | 0 | III |
| | 3(c) | 1.60 | 1.15 | 0.56 | III | 3.07 | 1.48 | 0 | III |

transient that leads to an overshoot/undershoot in frequency, the situation can fall into any of the six cases shown in Fig. 33. The phenomena of nuisance tripping can happen based on the occurrence of any of these six cases explained as follows. The description of cases 1, 2, and 3 are based on Fig. 33(a) while those of cases 4, 5, and 6 refer to Fig. 33(b).

- Case-1: Here, the overshoot magnitude is lesser than the upper limit, thereby lying within the acceptable region of ±5% of 50 Hz. Therefore, the relay will not be activated in this case, thus there will be no chance of tripping.
- Case-2: Here, the overshoot magnitude is higher than the upper limit, thus it does not lie within the acceptable region of ±5% of 50 Hz, which initiates the tripping process. But this overshoot is suppressed within the permissible time of 1 sec, and the occurrence of tripping is prevented.
- Case-3: Here, similar to case-2, the characteristic does not lie within the acceptable region of ±5% of 50 Hz, which initiates the tripping process. Further, this overshoot is not suppressed to safe limits within the permissible time of 1 sec, thereby the nuisance trip will occur.
- Case-4: Here, the undershoot magnitude is higher than the lower limit, thereby lying within the acceptable region of ±5% of 50 Hz. Therefore, the relay will not be activated in this case, thus there will be no chance of tripping.
- Case-5: Here, the undershoot magnitude is lower than the lower limit, thus it does not lie within the acceptable region of ±5% of 50 Hz, which initiates the tripping process. But this undershoot is suppressed within the permissible time of 1 sec, and the occurrence of tripping is prevented.
- Case-6: Here, similar to case-5, the characteristic does not lie within the acceptable region of ±5% of 50 Hz, which initiates the tripping process. Further, this undershoot is not suppressed to safe limits within the permissible time of 1 sec, thereby the nuisance trip will occur.

## DATA AVAILABILITY STATEMENT

Not applicable.

## CONFLICTS OF INTEREST

The authors declare no conflict of interest.

## REFERENCES

[1] S. N. V. B. Rao, Y. V. P. Kumar, M. Amir, and F. Ahmad, "An adaptive neuro-fuzzy control strategy for improved power quality in multi-microgrid clusters," *IEEE Access*, vol. 10, pp. 128007–128021, 2022, doi: 10.1109/ACCESS.2022.3226670.

[2] Y. V. Pavan Kumar and R. Bhimasingu, "Electrical machines based DC/AC energy conversion schemes for the improvement of power quality and resiliency in renewable energy microgrids," *Int. J. Electr. Power Energy Syst.*, vol. 90, pp. 10–26, Sep. 2017, doi: 10.1016/j.ijepes.2017.01.015.

[3] E. Unamuno, J. A. Suul, M. Molinas, and J. A. Barrena, "Comparative eigenvalue analysis of synchronous machine emulations and synchronous machines," in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, vol. 1. Lisbon, Portugal, Oct. 2019, pp. 3863–3870, doi: 10.1109/IECON.2019.8927826.

[4] Q.-C. Zhong, P.-L. Nguyen, Z. Ma, and W. Sheng, "Self-synchronized synchronverters: Inverters without a dedicated synchronization unit," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 617–630, Feb. 2014, doi: 10.1109/TPEL.2013.2258684.

[5] S. Dong and Y. C. Chen, "Adjusting synchronverter dynamic response speed via damping correction loop," *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 608–619, Jun. 2017, doi: 10.1109/TEC.2016.2645450.

[6] P. F. Frack, P. E. Mercado, and M. G. Molina, "Extending the VISMA concept to improve the frequency stability in microgrids," in *Proc. 18th Int. Conf. Intell. Syst. Appl. Power Syst. (ISAP)*, Porto, Portugal, Sep. 2015, pp. 1–6, doi: 10.1109/ISAP.2015.7325530.

[7] O. Mo, S. D'Arco, and J. A. Suul, "Evaluation of virtual synchronous machines with dynamic or quasi-stationary machine models," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5952–5962, Jul. 2017, doi: 10.1109/TIE.2016.2638810.

[8] N. Soni, S. Doolla, and M. C. Chandorkar, "Improvement of transient response in microgrids using virtual inertia," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1830–1838, Jul. 2013, doi: 10.1109/TPWRD.2013.2264738.

[9] Y. V. P. Kumar and R. Bhimasingu, "Fuzzy logic based adaptive virtual inertia in droop control operation of the microgrid for improved transient response," in *Proc. IEEE PES Asia–Pacific Power Energy Eng. Conf. (APPEEC)*, Bengaluru, India, Nov. 2017, pp. 1–6, doi: 10.1109/APPEEC.2017.8309006.

[10] S. D'Arco, J. A. Suul, and O. B. Fosso, "A virtual synchronous machine implementation for distributed control of power converters in SmartGrids," *Electr. Power Syst. Res.*, vol. 122, pp. 180–197, May 2015, doi: 10.1016/j.epsr.2015.01.001.

[11] H. Zhao, Q. Yang, and H. Zeng, "Multi-loop virtual synchronous generator control of inverter-based DGs under microgrid dynamics," *IET Gener., Transmiss. Distrib.*, vol. 11, no. 3, pp. 795–803, Feb. 2017, doi: 10.1049/iet-gtd.2016.0645.

[12] M. Srikanth and Y. Venkata Pavan Kumar, "A state machine-based droop control method aided with droop coefficients tuning through in-feasible range detection for improved transient performance of microgrids," *Symmetry*, vol. 15, no. 1, p. 1, Dec. 2022, doi: 10.3390/sym15010001.

[13] C. Hu, K. Chen, S. Luo, B. Zhou, and L. Ding, "Small signal modeling and stability analysis of virtual synchronous generators," in *Proc. 20th Int. Conf. Electr. Mach. Syst. (ICEMS)*. Sydney, NSW, Australia: IEEE, Aug. 2017, pp. 1–5, doi: 10.1109/ICEMS.2017.8056115.

[14] Z. Song, J. Zhang, F. Tang, M. Wu, Z. Lv, L. Sun, and T. Zhao, "Small signal modeling and parameter design of virtual synchronous generator to weak grid," in *Proc. 13th IEEE Conf. Ind. Electron. Appl. (ICIEA)*, May 2018, pp. 2618–2624, doi: 10.1109/ICIEA.2018.8398153.

[15] X. Hou, Y. Sun, X. Zhang, J. Lu, P. Wang, and J. M. Guerrero, "Improvement of frequency regulation in VSG-based AC microgrid via adaptive virtual inertia," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1589–1602, Feb. 2020, doi: 10.1109/TPEL.2019.2923734.

[16] T. H. Mohamed, M. A. M. Alamin, and A. M. Hassan, "A novel adaptive load frequency control in single and interconnected power systems," *Ain Shams Eng. J.*, vol. 12, no. 2, pp. 1763–1773, Jun. 2021, doi: 10.1016/j.asej.2020.08.024.

[17] H. Ur Rehman, X. Yan, M. A. Abdelbaky, M. Ullah Jan, and S. Iqbal, "An advanced virtual synchronous generator control technique for frequency regulation of grid-connected PV system," *Int. J. Electr. Power Energy Syst.*, vol. 125, Feb. 2021, Art. no. 106440, doi: 10.1016/j.ijepes.2020.106440.

[18] B. Long, Y. Liao, K. T. Chong, J. Rodríguez, and J. M. Guerrero, "Enhancement of frequency regulation in AC microgrid: A fuzzy-MPC controlled virtual synchronous generator," *IEEE Trans. Smart Grid*, vol. 12, no. 4, pp. 3138–3149, Jul. 2021, doi: 10.1109/TSG.2021.3060780.

[19] L. Zhang, X. Wang, Z. Zhang, Y. Cui, L. Ling, and G. Cai, "An adaptative control strategy for interfacing converter of hybrid microgrid based on improved virtual synchronous generator," *IET Renew. Power Gener.*, vol. 16, no. 2, pp. 261–273, Feb. 2022, doi: 10.1049/rpg2.12293.

[20] X. Meng, J. Liu, and Z. Liu, "A generalized droop control for grid-supporting inverter based on comparison between traditional droop control and virtual synchronous generator control," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5416–5438, Jun. 2019, doi: 10.1109/TPEL.2018.2868722.

[21] H. Wu, X. Ruan, D. Yang, X. Chen, W. Zhao, Z. Lv, and Q.-C. Zhong, "Small-signal modeling and parameters design for virtual synchronous generators," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4292–4303, Jul. 2016, doi: 10.1109/TIE.2016.2543181.

[22] J. Liu, Y. Miura, and T. Ise, "Comparison of dynamic characteristics between virtual synchronous generator and droop control in inverter-based distributed generators," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3600–3611, May 2016, doi: 10.1109/TPEL.2015.2465852.

[23] C. Andalib-Bin-Karim, X. Liang, and H. Zhang, "Fuzzy-secondary-controller-based virtual synchronous generator control scheme for interfacing inverters of renewable distributed generation in microgrids," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1047–1061, Mar. 2018, doi: 10.1109/TIA.2017.2773432.

[24] W. Ma, Y. Guan, and B. Zhang, "Active disturbance rejection control based control strategy for virtual synchronous generators," *IEEE Trans. Energy Convers.*, vol. 35, no. 4, pp. 1747–1761, Dec. 2020, doi: 10.1109/TEC.2020.2991737.

[25] Y. Wang, D. Wang, Z. Huang, and Y. Li, "Hybrid voltage and current control strategy for virtual synchronous generator under unbalanced voltage conditions," *IET Renew. Power Gener.*, early access, pp. 1–10, Jun. 2022, doi: 10.1049/rpg2.12497.

[26] Y. Zhu, H. Wang, and Z. Zhu, "Improved VSG control strategy based on the combined power generation system with hydrogen fuel cells and super capacitors," *Energy Rep.*, vol. 7, pp. 6820–6832, Nov. 2021, doi: 10.1016/j.egyr.2021.10.056.

[27] S. Leitner, M. Yazdanian, A. Mehrizi-Sani, and A. Muetze, "Small-signal stability analysis of an inverter-based microgrid with internal model-based controllers," *IEEE Trans. Smart Grid*, vol. 9, no. 5, pp. 5393–5402, Sep. 2018, doi: 10.1109/TSG.2017.2688481.

[28] M. Yazdanian and A. Mehrizi-Sani, "Internal model-based current control of the RL filter-based voltage-sourced converter," *IEEE Trans. Energy Convers.*, vol. 29, no. 4, pp. 873–881, Dec. 2014, doi: 10.1109/TEC.2014.2353035.

[29] M. Yazdanian and A. Mehrizi-Sani, "Case studies on cascade voltage control of islanded microgrids based on the internal model control," *IFAC-PapersOnLine*, vol. 48, no. 30, pp. 578–582, 2015, doi: 10.1016/j.ifacol.2015.12.442.

[30] C.-T. Lee, C.-C. Chu, and P.-T. Cheng, "A new droop control method for the autonomous operation of distributed energy resource interface converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1980–1993, Apr. 2013, doi: 10.1109/TPEL.2012.2205944.

[31] M. A. Torres L., L. A. C. Lopes, L. A. Morán T., and J. R. Espinoza C., "Self-tuning virtual synchronous machine: A control strategy for energy storage systems to support dynamic frequency control," *IEEE Trans. Energy Convers.*, vol. 29, no. 4, pp. 833–840, Dec. 2014, doi: 10.1109/TEC.2014.2362577.

[32] J. A. Suul, M. Molinas, L. Norum, and T. Undeland, "Tuning of control loops for grid connected voltage source converters," in *Proc. IEEE 2nd Int. Power Energy Conf.* Johor Bahru, Malaysia: IEEE, Dec. 2008, pp. 797–802, doi: 10.1109/PECON.2008.4762584.

[33] S. D'Arco, J. A. Suul, and O. B. Fosso, "Automatic tuning of cascaded controllers for power converters using eigenvalue parametric sensitivities," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1743–1753, Mar. 2015, doi: 10.1109/TIA.2014.2354732.

[34] Y. V. P. Kumar and R. Bhimasingu, "Design of voltage and current controller parameters using small signal model-based polezero cancellation method for improved transient response in microgrids," *SN Appl. Sci.*, vol. 3, no. 11, p. 836, Nov. 2021, doi: 10.1007/s42452-021-04815-x.

[35] L. Djilali, E. N. Sanchez, F. Ornelas-Tellez, A. Avalos, and M. Belkheiri, "Improving microgrid low-voltage ride-through capacity using neural control," *IEEE Syst. J.*, vol. 14, no. 2, pp. 2825–2836, Jun. 2020, doi: 10.1109/JSYST.2019.2947840.

[36] *Combined Under/Over Voltage & Under/Over Frequency Relay*. Accessed: Jul. 14, 2024. [Online]. Available: https://rishabh.co.in/products/download/Combined_Under-Over_Voltage_Under-Over_Frequency_Relay.pdf

[37] J. C. M. Vieira, W. Freitas, W. Xu, and A. Morelato, "Performance of frequency relays for distributed generation protection," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1120–1127, Jul. 2006, doi: 10.1109/TPWRD.2005.858751.

[38] Z. Wang, J. Xiong, and X. Wang, "Investigation of frequency oscillation caused false trips for biomass distributed generation," *IEEE Trans. Smart Grid*, vol. 10, no. 6, pp. 6092–6101, Nov. 2019, doi: 10.1109/TSG.2019.2896480.

[39] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources With Associated Electric Power Systems Interfaces*, IEEE Standard 1547-2018, (Revision IEEE Standard 1547-2003), Apr. 2018, pp. 1–138, doi: 10.1109/IEEESTD.2018.8332112.

**MANDARAPU SRIKANTH** was born in Vizianagaram, Andhra Pradesh, India, in 1983. He received the B.Tech. degree in electrical and electronics engineering from JNT University, Hyderabad, Telangana, India, in 2005, and the M.Tech. degree in power electronics and drives from GIET University, Gunupur, Odisha, India, in 2012. He is currently pursuing the Ph.D. degree with the School of Electronics Engineering, VIT-AP University, Andhra Pradesh, India.

From 2005 to 2009, he was an Electrical Engineer with Walchandnagar Industries Ltd., Pune, Maharashtra, India. From 2009 to 2017, he was an Assistant Professor with Pydah Educational Institutions, Visakhapatnam, Andhra Pradesh. From 2017 to 2020, he was an Assistant Professor with the Raghu Engineering College, Visakhapatnam. His research interests include microgrids, smart grids, advanced control systems, and artificial intelligence.

**Y. V. PAVAN KUMAR** (Senior Member, IEEE) was born in Tenali, Andhra Pradesh, India, in 1985. He received the B.Tech. degree in electrical and electronics engineering from JNT University, Hyderabad, Telangana, India, in 2007, the M.Tech. degree in instrumentation and control systems from the University College of Engineering, JNTUK University, Kakinada, Andhra Pradesh, in 2011, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology Hyderabad (IITH), Telangana, in 2018.

From 2007 to 2009, he was an Assistant Professor with the Sir C. R. Reddy College of Engineering, Eluru, Andhra Pradesh. From 2011 to 2014, he was an Engineer with Honeywell Technology Solutions Laboratory Pvt. Ltd., Hyderabad. Since 2017, he has been an Associate Professor with the School of Electronics Engineering, VIT-AP University, Amaravati, Andhra Pradesh. He was a recipient of the SERB SIRE Fellowship and the SERB SRG Sponsored Project Grant, from 2019 to 2023. He is the author of three books, 130 papers, and 26 patents. His research interests include microgrids, smart grids (data analytics and communications), electric vehicles, power quality, advanced control, and power converters.

Dr. Pavan Kumar was a Nominated Member of the Electronics and Information Technology Department (LITD 27 Internet of Things and related technologies sectional committee), Bureau of Indian Standards (BIS), India; and a member of ISO/IEC JTC 1/SC 41 Internet of Things and Digital Twin.

**CH. PRADEEP REDDY** (Member, IEEE) is currently a Professor and the Dean with the School of Computer Science and Engineering, VIT-AP University, Andhra Pradesh, India. He has over 18 years of experience in the field of computer science and engineering in both teaching and research. He has published several papers in international refereed journals and conferences. He has successfully guided six research scholars toward their Ph.D. degrees and currently works with two more, demonstrating his ability to mentor and lead research teams. His research interests include the IoT, sensor networks, wireless systems, artificial intelligence, and machine learning, indicating his strong passion for advancing scientific research in these fields. He served as a technical program committee member and a guest editor for several reputable international conferences and journals.

**RAMMOHAN MALLIPEDDI** (Senior Member, IEEE) received the master's and Ph.D. degrees in computer control and automation from Nanyang Technological University, Singapore, in 2007 and 2010, respectively.

Currently, he is a Professor with the Department of Artificial Intelligence, School of Electronics Engineering, Kyungpook National University, Daegu, South Korea. He has co-authored articles in IEEE TRANSACTIONS ON EVOLUTIONARY COMPUTATION. His research interests include evolutionary computing, artificial intelligence, image processing, digital signal processing, robotics, and control engineering. He regularly reviews articles for journals, including IEEE TRANSACTIONS ON EVOLUTIONARY COMPUTATION and IEEE TRANSACTIONS ON CYBERNETICS. He serves as an Associate Editor for *Swarm and Evolutionary Computation*, an international journal by Elsevier.