

RESEARCH ARTICLE

Assessment of Performance of One-Turn Inductors in Series Configuration Through a Transmission-Line Modeling Approach

GERMÁN ALVAREZ-BOTERO¹, (Senior Member, IEEE),
EDUARDO MOCTEZUMA-PASCUAL²,
MIGUEL A. G. LASO¹, (Fellow, IEEE),
AND REYZEL TORRES-TORRES³, (Senior Member, IEEE)

¹Department of Electrical, Electronic and Communications Engineering, Public University of Navarre, 31006 Pamplona, Spain

²Intel Guadalajara, Zapopan 45017, Mexico

³Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Puebla 72840, Mexico

Corresponding author: Germán Alvarez-Botero (germanandres.alvarez@unavarra.es)

The work of Germán Alvarez-Botero was supported in part by the Spanish Ministerio de Ciencia e Innovación—Agencia Estatal de Investigación (MCIN/AEI/10.13039/501100011033) under Project PID2020-112545RB-C53; and in part by the Government of Navarre, Spain, through the Andia Fellowship. The work of Miguel A. G. Laso was supported by the Spanish Ministerio de Ciencia e Innovación—Agencia Estatal de Investigación (MCIN/AEI/10.13039/501100011033) under Project PID2020-112545RB-C53.

ABSTRACT In this paper, transmission-line theory is applied to implement a physical model for compact one-turn inductors, which simultaneously incorporates the frequency-dependent effects introduced by the conductor skin effect and the loss originated by the coupling with the ground plane. For this purpose, S-parameter measurements are processed to extract the associated parameters, which exhibit scalability with the turn radius. This allows the model to be used for interpolation and extrapolation analyses. In this regard, the device performance is assessed for one-turn inductors in series connection, for different load impedances, and when the turn is narrowed. To validate the proposal, agreement between the model and the experimental transmission line RLGC parameters, the return loss, and the Q-factor is obtained up to 20 GHz.

INDEX TERMS Integrated inductor, transmission-line model, S-parameters.

I. INTRODUCTION

Currently, passive components and interconnects occupy valuable space on integrated circuits (ICs) operating at microwave frequencies [1]. Hence, alternatives to reduce the size of these devices, such as using one-turn inductors, either alone or as part of more complex devices [2], [3], have been proposed. Nonetheless, to exploit the advantages of these structures, it is necessary to understand the potential and limitations of single metal turns for achieving inductance of practical values [4], [5], [6]. For this reason, the physical modeling of such structures is essential to

The associate editor coordinating the review of this manuscript and approving it for publication was Photos Vryonides.

systematically analyze their corresponding electrical performance under actual operating conditions, ultimately enabling their application in the implementation of more complex devices.

In addition to accurately predicting the intrinsic inductance achievable with single metal turns, understanding the associated quality (Q) factor is crucial for IC designers. In this regard, there are several approaches to compute this parameter. For simplicity, some of the proposals assume that the inductor is a one-port device [7], which provides enough information for the case when shunt connection to ground is considered. Nonetheless, a more rigorous assessment for the Q-factor is required when the inductor is connected in series configuration [8], [9]. In this case, it is necessary to take into

account that the parasitics associated with the device input and output ports may substantially impact performance at microwave frequencies. Furthermore, an additional challenge arises in this latter case since the Q-factor depends on the load at which the device is terminated [10].

Moreover, in addition to requiring the description of an inductor as a two-port device to achieve useful representations for RF ICs, it is necessary to predict the conditions under which the device parasitics dominate the intrinsic inductive behavior. In fact, these conditions also depend on frequency, the device size, and the load impedance terminating the output port. Nonetheless, even when inductors are used to compensate for microwave degradation of other devices [11], [12], there is little information regarding the boundaries within which an inductor remains useful.

Hence, the aim of this paper is to propose a systematic modeling and parameter extraction methodology for one-turn inductors. Furthermore, to demonstrate the utility of this approach, it is applied to analyze how performance depends on the device size and the magnitude of the terminating load. In terms of modeling, leveraging the similarity between single-turn inductors of practical size and transmission lines, the proposed approach is based on an *RLGC* representation that enables separate modeling of the device's series and shunt parasitics. This also allows for the straightforward extraction of physically meaningful parameters, while carefully adhering to the conditions under which practical one-turn inductors can be analyzed using transmission line theory. Besides, the resulting two-port equivalent circuit makes possible the representation in either series or parallel configuration, which can also be interpolated and extrapolated to different sizes, and for analyzing the impact of shifting the load impedance from the reference impedance used during the experiments. Furthermore, the proposal is employed to inspect the advantage of using two traces in parallel rather than a single trace for implementing the inductor's turn. Based on the built models, several plots of the Q-factor and the reflection coefficient are used to thoroughly assess the performance of different inductors under various operating conditions.

II. PROTOTYPES AND EXPERIMENTS

To illustrate the modeling methodology proposed here for analyzing the performance of one-turn inductors, test structures on a semiconductor wafer were thoroughly measured. This prototype was fabricated on a p-type Si substrate with a resistivity of $20 \Omega\cdot\text{cm}$, and includes inductors exhibiting the layout depicted in Fig. 1(a). Notice that rather than using a single circular trace to implement the device, two short-circuited concentric traces are used to reduce the metal series resistance; this results in an improvement of up to 20% in the Q-factor over a single turn inductor [4]. This improvement is achieved while respecting the maximum trace width established by layout design rules. Thus, for the implemented structures, the equivalent width of the inductor, as defined in

Fig. 1(a), is $w = 15 \mu\text{m}$. Additionally, a pattern ground shield was included to avoid undesired coupling between the inductors and the semiconductor substrate. This shield is directly connected to the ground pads at both sides of the device and is depicted in Fig. 1(b), as well as the metal fills that are needed to maintain the metal density of the wafer. In this regard, these fills were avoided below the metal traces to reduce additional parasitic effects. Within the prototype, three inductors are included, exhibiting radius $r = 100 \mu\text{m}$, $150 \mu\text{m}$, and $200 \mu\text{m}$.

Regarding the electrical measurements, the vector network analyzer (VNA) setup shown in Fig. 1(c) was used to measure the two-port S-parameters of the three inductors up to 20 GHz with the aid of ground-signal-ground (GSG) microprobes with a pitch of $100 \mu\text{m}$. For this purpose, the setup was calibrated up to the probe tips by using a line-reflect-reflect-match (LRRM) algorithm and an impedance standard substrate. Furthermore, once the S-parameters were measured, a two-step de-embedding was carried out to remove the effect of the pads and the feeding interconnects from the inductor experimental data [13]. Hence, measurements performed to 'open' and 'short' dummy structures included within the prototype were employed.

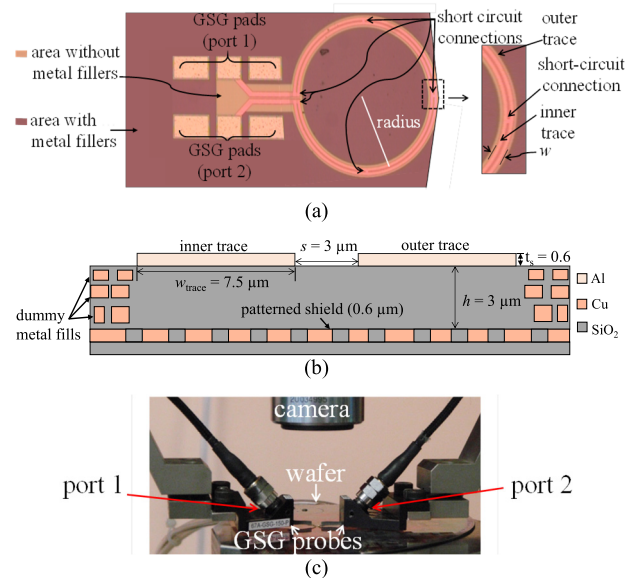


FIGURE 1. Description of the prototyped devices: a) photograph of the inductor with a radius of $200 \mu\text{m}$, b) sketch showing the device cross section the level of the traces that form the turn, and c) photograph of the two-port measurement of one device.

Finally, it is assumed in this paper that the one-turn inductors can be represented by means of a transmission-line model consisting of the cascaded connection of frequency-dependent RLGC parameters. These parameters are separately obtained for each one of the inductors from the de-embedded S-parameters as explained in [14], and are used throughout the parameter extraction procedure described hereafter.

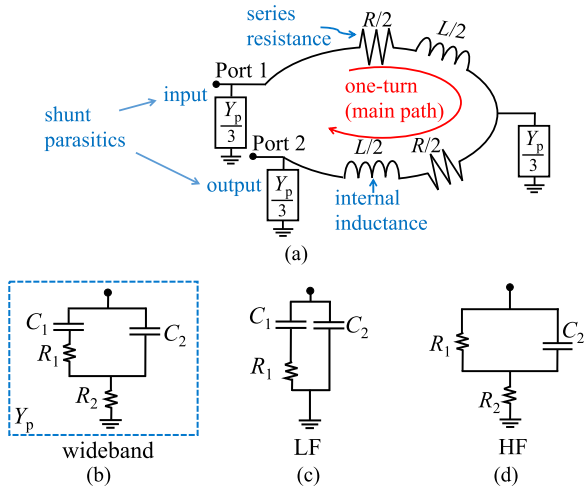


FIGURE 2. Equivalent circuit model for the inductors: a) two-port representation, b) wideband model for Y_p , c) low-frequency model for Y_p , and d) high-frequency model for Y_p .

III. CIRCUIT MODELING AND PARAMETER EXTRACTION

The first step to analyze the performance of a one-turn inductor is defining an equivalent circuit that allows for the wideband representation of its electrical behavior. In this regard, the perimeter of the largest prototyped device is $p_{max} = 2\pi \times (200 \mu m) \approx 1.2 \text{ mm}$, whereas the wavelength at the maximum frequency considered here is $\lambda_{min} = c/[\sqrt{\epsilon_r} \times (20 \text{ GHz})] \approx 7.6 \text{ mm}$, where c is the speed of light in vacuum and $\epsilon_r \approx 3.9$ is assumed as the relative permittivity of the field oxide. Hence, since a criterion to determine the minimum number of stages (n) in cascade connection for an equivalent circuit to represent a device of a given length dictates that $p_{max}/n \leq \lambda_{min}/10$ [15], a two-stage circuit (i.e., $n = 2$) as the one shown in Fig. 2 (a) is used in this paper.

For representing R and L as functions of frequency (f) in the circuit shown in Fig. 2 (a), the skin effect occurring within the conductor traces is considered using the following equation models:

$$R = R_0 + k_s \sqrt{f} \quad (1)$$

$$L = L_\infty + k_s / (2\pi \sqrt{f}) \quad (2)$$

where R_0 represents the low frequency resistance exhibited by the inductor, k_s is the skin effect coefficient for a conductor with smooth surface, and L_∞ is the external inductance, which is dominant at high frequencies [16].

In order to determine these parameters, a linear regression is firstly applied to the experimental R versus \sqrt{f} data. This allows for the extraction of k_s and R_0 from the corresponding slope and intercept with the ordinates, respectively. Afterwards, the experimental L is plotted versus $1/\sqrt{f}$ for obtaining L_∞ from the intercept with the ordinates of the associated linear regression. Observe in Fig. 3 that after extracting the parameters, (1) and (2) accurately reproduce both R and L for the prototyped inductors.

Regarding the inductor parasitic shunt admittance (Y_p), it can be represented by means of the wideband model shown

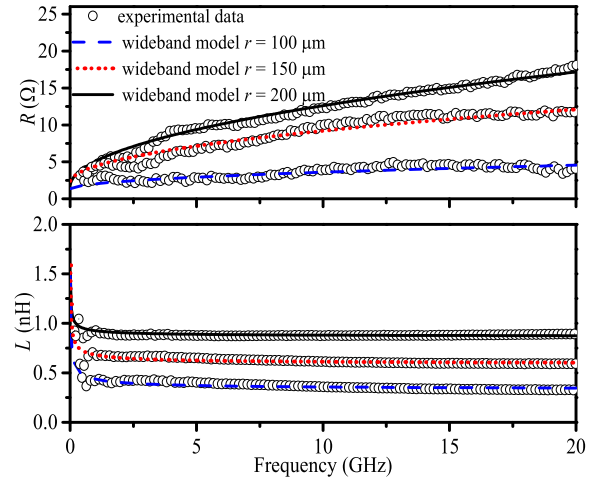


FIGURE 3. Model-experiment correlation for R and L for the three inductors.

in Fig. 2(b), which consists of two resistances (R_1 and R_2) and two capacitances (C_1 and C_2). This circuit not only allows for a distributed representation of the capacitive coupling between the inductor and the ground plane, but also considers the loss occurring due to transverse polarization currents and also currents within the pattern structure. In fact, the validity of this representation has been previously verified in microstrip structures [17]; thus, the model application is extended here by carefully associating the corresponding elements to effects occurring in an on-chip inductor. For this purpose, the resistance to ground (i.e., R_2) is used to increase the model bandwidth of validity while maintaining causality as explained in [18]. So, the problem now is to determine the four unknown parameters from the experimental Y_p given by:

$$Y_p = G + j2\pi fC \quad (3)$$

To simplify this problem, rather than expressing Y_p in terms of R_1 , R_2 , C_1 , and C_2 , by directly using the wideband model, it is firstly assumed that, at low frequencies, this admittance can be represented by means of the circuit shown in Fig. 2(c). In this case, and considering (3), it is possible to write:

$$Re(Y_p)|_{LF} = G|_{LF} \approx \frac{(\omega C_1)^2 R_1}{1 + (\omega C_1 R_1)^2} \quad (4)$$

where $\omega = 2\pi f$, and the subscript LF indicates that the approximation is valid at low frequencies. Notice also that rearranging (4), it is possible to define the following auxiliary variable:

$$U = \frac{\omega^2}{G}|_{LF} \approx R_1 \omega^2 + \frac{1}{C_1^2 R_1} \quad (5)$$

Therefore, in accordance with (5), when performing a linear regression to experimental U versus ω^2 data, R_1 and C_1 can easily be obtained from the corresponding slope and intercept with the ordinates. In this regard, good linearity in the data determined from (5) is achieved considering that the upper LF limit is about 2 GHz.

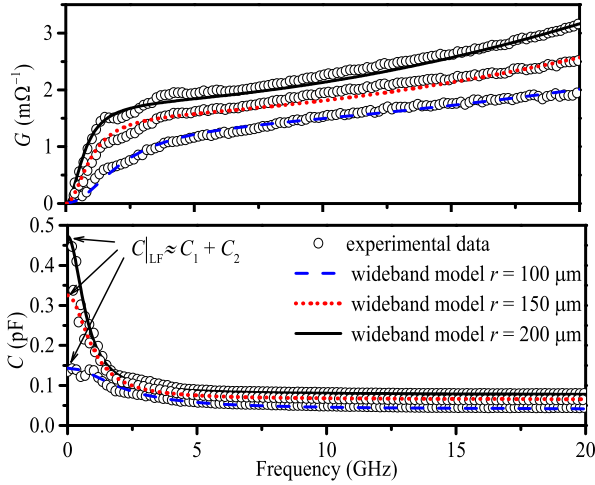


FIGURE 4. Model-experiment correlation for G and C for the three inductors.

On the other hand, at high frequencies the wideband model for Y_p can be simplified to the circuit shown in Fig. 2(d), which allows one to write the following equation:

$$Z_p|_{HF} = \frac{1}{G + j\omega C}|_{HF} \approx \frac{R_1}{1 + (\omega R_1 C_2)^2} + R_2 - \frac{j\omega R_1^2 C_2}{1 + (\omega R_1 C_2)^2} \quad (6)$$

where $Z_p = 1/Y_p$, and HF indicates that the approximation is valid at high frequencies. Now, from (6) it is possible to define a new additional auxiliary variable as:

$$V = -\frac{\omega}{\text{Im}(Z_p)}|_{HF} \approx C_2 \omega^2 + \frac{1}{R_1 C_2} \quad (7)$$

With the aid of (7), C_2 can be obtained from the slope of the linear regression performed to V versus ω^2 data. Afterwards, once R_1 , C_1 , and C_2 are known, the remaining parameter is determined by solving the real part of Z_p in (6) for R_2 ; this yields:

$$R_2 = \text{Re}(Z_p)|_{HF} - \frac{R_1}{1 + (\omega R_1 C_2)^2} \quad (8)$$

Now, it is possible to correlate in Fig. 4 the model for Y_p with the experimental G and C curves for the different inductors. Excellent agreement is achieved within the measured frequency range.

Fig. 5(a) shows that the parameters related to the series resistance (i.e., R_0 and k_s) are approximately proportional to the effective length of the traces that form the inductors. In other words, R increases with the perimeter of the devices. A similar and physically expected trend is also observed in this figure for the capacitances C_1 and C_2 , that account for the parasitic coupling of the inductor's traces with the return path. On the other hand, since the part of the shunt loss is due to the electric polarization occurring between the inductor trace to the ground plane, the associated currents are expected to increase with the perimeter. This increase in the parasitic shunt currents is interpreted as a reduction in R_1 and R_2 ,

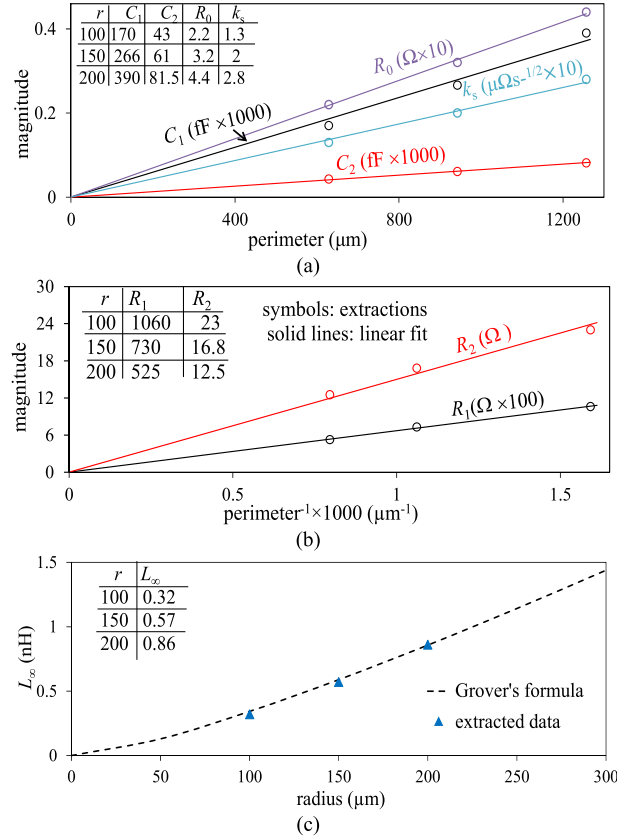


FIGURE 5. Extracted model parameters for the different inductors: **a)** parameters that show proportionality with the perimeter, **b)** parameters that show proportionality with the inverse of the perimeter, and **c)** external component of the intrinsic inductance versus radius.

which clearly shows a linear trend when plotted versus the inverse of the perimeter in Fig. 5(b).

For the case of the effective inductance of the device, k_s extracted for R allows for modeling the frequency-dependent term in (2). On the other hand, to represent the dependence of L_∞ on geometry, Grover's formula for a one-turn inductor is employed, which is expressed by [19]:

$$L_\infty = \mu_0 \cdot r \left(\frac{1}{2} \left(1 + \frac{1}{6} a^2 \right) \cdot \ln \left(\frac{8}{a^2} \right) - 0.848 + 0.204 a^2 \right) \quad (9)$$

where $\mu_0 = 4\pi \times 10^{-7} \text{ T}\cdot\text{m}\cdot\text{A}^{-1}$ is the permeability of free space, and $a = w/2r$. Fig. 5 (c) shows the agreement between (9) and the extracted data, which enables the provision of a model for L_∞ for both interpolation and extrapolation purposes.

IV. ASSESSMENT OF PERFORMANCE

Once the model for the inductors has been implemented, the simulated curves for the reflection parameter S_{11} are compared to experimental data. Fig. 6(a) shows the corresponding agreement achieved for the three fabricated devices. In addition, notice that using data extrapolations as illustrated in Fig. 5, the simulated curve for an inductor presenting a radius of $300 \mu\text{m}$ is also obtained. This also allows for illustrating the trend in the Q-factor as the radius is increased

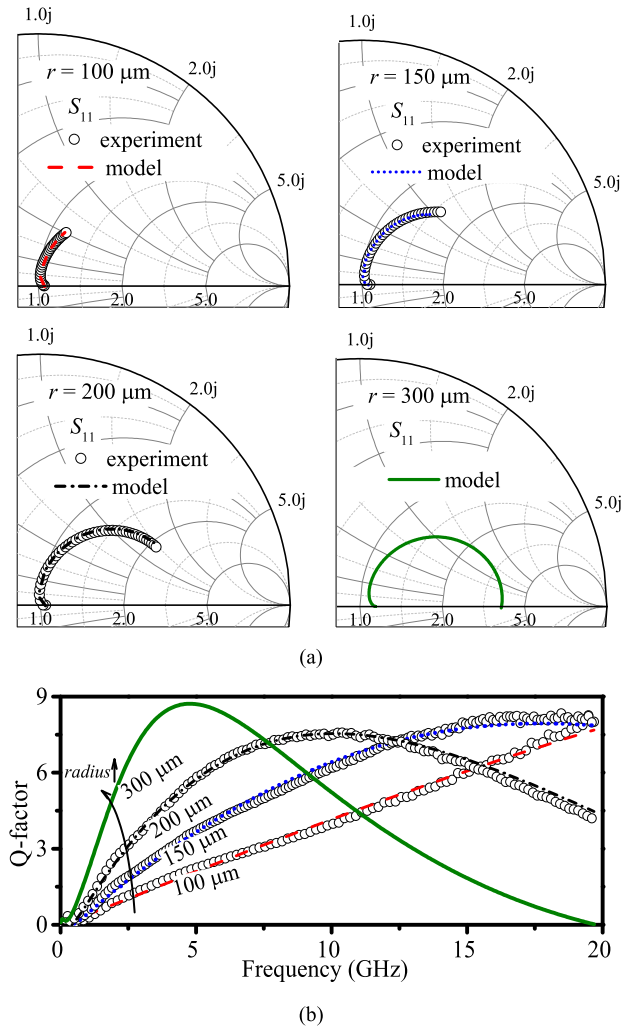


FIGURE 6. Model–experiment correlation up to 20 GHz and assuming $Z_L = 50 \Omega$ for: a) S_{11} , and b) the quality factor. The simulated curve corresponding to an inductor with $r = 300 \mu\text{m}$ is also included; this curve was obtained through the extrapolation of the model parameters.

in Fig. 6 (b). Observe in this figure that, as expected, the peak of the Q-factor occurs at lower frequencies as the size of the inductor is increased since the parasitics also increase with the radius. This points out the usefulness of the proposal within a design cycle for estimating the performance of an inductor of a given radius.

A. IMPACT OF LOAD CONDITIONS

An important aspect to be considered when using an on-chip inductor under actual conditions is the fact that it is typically connected in series configuration. Actually, the device output port might even be terminated at a load of large magnitude [8]. For this reason, it is necessary to analyze the impact of the load impedance on the performance of the inductor. In this regard, considering that the two-stage transmission-line circuit shown in Fig. 2 (a) is used, it is possible to re-draw it in the form presented in Fig. 7. Hence, it is clear that the current flowing through the main path is reduced as the load impedance (Z_L) is increased. This undesired effect introduces a larger deviation of the device operation from

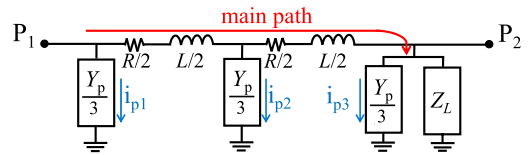


FIGURE 7. Illustration of the input parasitic path and the main path.

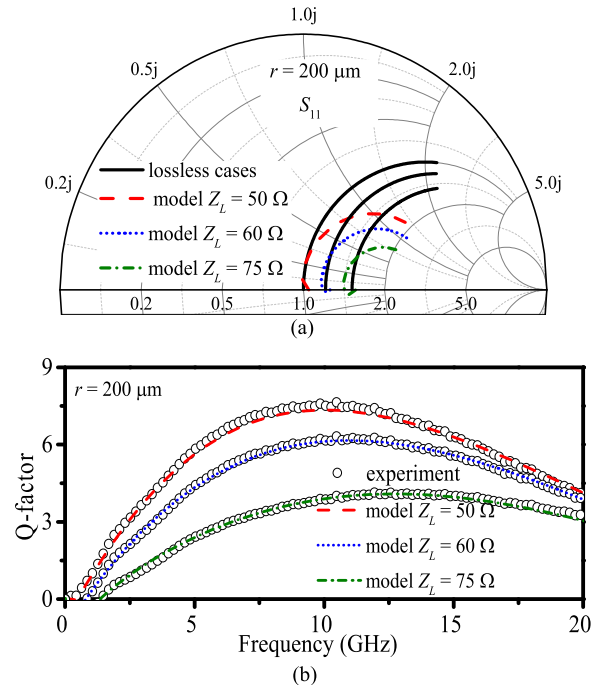


FIGURE 8. Performance degradation as the load impedance is increased: a) S_{11} up to 20 GHz for an ideal inductor with no parasitics against the simulated curves for $r = 200 \mu\text{m}$, and b) Q-factor curves for the same cases.

the ideal behavior expected from a lossless inductor. This is graphically illustrated in Fig. 8(a), where the length of the S_{11} plot is not only shortened as Z_L increases, but also more curvature is exhibited since more proportion of current is flowing through the device shunt parasitics. Furthermore, observe in Fig. 8(b) the significant reduction of the Q-factor as the load impedance is increased. This reduction is also accurately predicted by the proposed transmission line model.

B. PERFORMANCE ENHANCEMENT WHEN USING TWO PARALLEL TRACES

As previously mentioned, using two parallel traces to implement one-turn inductors reduces the series resistance without significantly affecting the magnitude of the inductance. Here, it is quantified the improvement in the Q-factor by employing this technique. For this purpose, the performance of the two-trace inductor practically implemented with radius $r = 200 \mu\text{m}$ is compared to the one corresponding to an inductor of the same internal radius but using only one trace. In this case, in accordance with Grover’s formula [21], considering that the cross section through which the current is flowing is reduced to half the size of the two-trace inductor, the inductance is increased from 0.86 nH to 1.2 nH. Nevertheless, this change in the cross section also doubles the series resistive

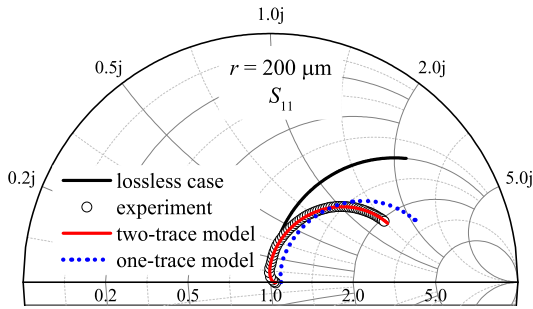


FIGURE 9. Upper part of smith chart comparing S_{11} up to 20 GHz for an ideal inductor with no parasitics against the experimental case, and the case when the turn of the inductor is implemented with only one trace. The curves are obtained assuming $Z_L = 50 \Omega$.

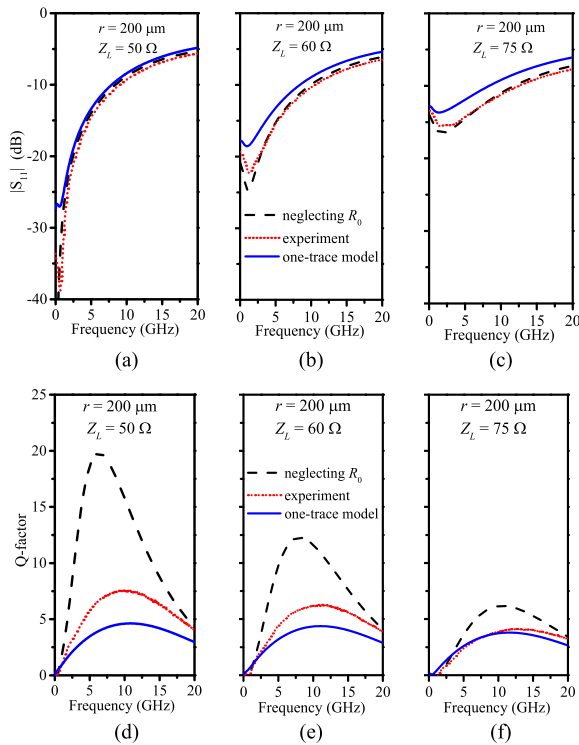


FIGURE 10. Performance degradation as the magnitude of the load impedance increases. The plots on top show the return loss for: a) $Z_L = 50 \Omega$, b) $Z_L = 60 \Omega$, and c) $Z_L = 75 \Omega$. The plots at the bottom present the comparison of the Q-factor for the experimental case, for the case where the parasitic series resistance is ignored, and also assuming that the turn of the inductor is implemented with one trace: a) $Z_L = 50 \Omega$, b) $Z_L = 60 \Omega$, and d) $Z_L = 75 \Omega$.

components. Now, to obtain the shunt capacitive components in the transmission line model, Schneider's formula can be applied [20]. This formula dictates that, for a microstrip trace, the capacitance is approximately given by:

$$C = 0.225\epsilon_{eff} \left[\frac{w}{h} + 2.42 - 0.44 \frac{h}{w} + \left(1 - \frac{h}{w} \right)^6 \right] \quad (10)$$

where ϵ_{eff} is the effective permittivity of the surrounding media, which can be calculated as described in [20] considering the relative permittivity of the silicon dioxide as $\epsilon_r = 3.9$. So, when calculating the capacitance of the two-trace inductor and that of the one-trace inductor using (10), a reduction of 32% is obtained in the latter case.

At this point, the model for the one trace inductor can be straightforwardly implemented considering the equivalent circuit given in Fig. 2 (a). In Fig. 9, the corresponding S_{11} curve is compared to the ideal lossless case and to the curves corresponding to the two-trace case and a noticeable difference is observed. Furthermore, this difference is more clearly seen in the magnitude curves with different load impedances shown in Figs. 10(a), (b), and (c), where the curves for the one-trace and the ones for the two-trace inductors are compared to the case where the series resistance is ignored. In fact, observe in Figs. 10(d), (e), and (f) that, as the magnitude of Z_L is closer to the reference impedance (i.e., 50Ω), the Q-factor corresponding to the two-turn inductor exhibits significantly higher magnitude than the one-turn counterpart. This result points out the advantage of reducing the series resistance using this technique and highlights another application of the proposed modeling methodology.

V. CONCLUSION

Accurate modeling of one-turn inductors is achieved using a transmission line based equivalent circuit and a systematic parameter extraction approach. Model–experiment correlations show excellent agreement up to 20 GHz for inductors of different sizes, and for several load impedances connected at the device output port. The frequency-dependence of the circuit elements is considered based on a physical interpretation of the associated effects, which allows model scalability and reliable evaluation of performance through the calculation of two-port Q-factor curves. Furthermore, the approach also shows applicability for comparing the performance of one-turn inductors consisting of one and two metal traces in parallel.

ACKNOWLEDGMENT

The authors acknowledge Imec, Leuven, Belgium, for supplying the test structures.

REFERENCES

- [1] B. El-Kareh and L. N. Hutter, *Silicon Analog Components Device Design, Process Integration, Characterization, and Reliability*, 2nd ed. Cham, Switzerland: Springer, 2019.
- [2] R. Bajwa and M. K. Yapici, "Integrated on-chip transformers: Recent progress in the design, layout, modeling and fabrication," *Sensors*, vol. 19, no. 16, p. 3535, Aug. 2019, doi: [10.3390/s19163535](https://doi.org/10.3390/s19163535).
- [3] H.-M. Hsu, J.-H. Huang, T.-H. Peng, and N.-C. Liu, "Design of coil length of on-chip transformer with high turn ratio and high coupling performance," *IEEE Trans. Electron Devices*, vol. 59, no. 11, pp. 3061–3068, Nov. 2012, doi: [10.1109/TED.2012.2210896](https://doi.org/10.1109/TED.2012.2210896).
- [4] C. Detcheverry, W. van Noort, R. Hoofman, L. Tiemeijer, V. H. Nguyen, G. Verheyden, P. Bancken, R. Daamen, and R. Havens, "The effect of copper design rules on inductor performance," in *Proc. 33rd Conf. Eur. Solid-State Device Res.*, Sep. 2003, pp. 107–110, doi: [10.1109/ESSDERC.2003.1256822](https://doi.org/10.1109/ESSDERC.2003.1256822).
- [5] L. F. Tiemeijer, R. J. Havens, N. Pavlovic, and D. M. W. Leenaerts, "Record q symmetrical inductors for 10-GHz LC-VCOs in 0.18- μm gate-length CMOS," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 713–715, Dec. 2002, doi: [10.1109/LED.2002.805740](https://doi.org/10.1109/LED.2002.805740).
- [6] E. S. Mawuli, Y. Wu, D. K. B. Kulevome, Z. Qingfeng, C. Zhao, H. Liu, Y. Yu, and K. Kai, "Distributed characterization of on-chip spiral inductors for millimeter-wave frequencies," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dec. 2020, pp. 1–4, doi: [10.1109/NEMO49486.2020.9343469](https://doi.org/10.1109/NEMO49486.2020.9343469).

- [7] S. Spataro, N. Salerno, G. Papotto, and E. Ragonese, "The effect of a metal PGS on the Q-factor of spiral inductors for RF and mm-wave applications in a 28-nm CMOS technology," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 30, no. 10, Oct. 2020, Art. no. e22368, doi: [10.1002/mmmce.22368](https://doi.org/10.1002/mmmce.22368).
- [8] M. S. M. Montesdeoca, S. M. Angulo, D. M. Duarte, J. Del Pino, J. A. G. Y. García, and S. L. Khemchandani, "An analytical scalable lumped-element model for GaN on Si inductors," *IEEE Access*, vol. 8, pp. 52863–52871, 2020, doi: [10.1109/ACCESS.2020.2980926](https://doi.org/10.1109/ACCESS.2020.2980926).
- [9] H. Zheng, Y. Wu, K. Zhang, L. Wang, M. Wang, and E. Li, "Wide-band modeling on-chip spiral inductors using frequency-dependent conformal ADI-FDTD method," *IEEE Access*, vol. 7, pp. 184940–184949, 2019, doi: [10.1109/ACCESS.2019.2960284](https://doi.org/10.1109/ACCESS.2019.2960284).
- [10] T.-S. Horng, K.-C. Peng, J.-K. Jau, and Y.-S. Tsai, "S-parameter formulation of quality factor for a spiral inductor in generalized two-port configuration," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 11, pp. 2197–2202, Nov. 2003, doi: [10.1109/TMTT.2003.818584](https://doi.org/10.1109/TMTT.2003.818584).
- [11] H. Gao, X. Sun, Y. Hua, X. Zhang, R. Wang, and G. P. Li, "A composite transistor to suppress kink phenomenon in HBTs for broadband conformal," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1113–1115, Oct. 2010, doi: [10.1109/LED.2010.2057240](https://doi.org/10.1109/LED.2010.2057240).
- [12] Y.-M. Wu, T. Qiang, C. Wang, K. K. Adhikari, X. Lv, and Y. Wu, "GaAs-based IPD-fabricated center-frequency-controllable bandpass filter with asymmetrical differential inductor and air-bridge enhanced capacitor," *IEEE Access*, vol. 7, pp. 137784–137793, 2019, doi: [10.1109/ACCESS.2019.2918950](https://doi.org/10.1109/ACCESS.2019.2918950).
- [13] R. Torres-Torres, R. Murphy-Arteaga, and J. A. Reynoso-Hernandez, "Analytical model and parameter extraction to account for the pad parasitics in RF-CMOS," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1335–1342, Jul. 2005, doi: [10.1109/TED.2005.850644](https://doi.org/10.1109/TED.2005.850644).
- [14] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 15, no. 4, pp. 483–490, Aug. 1992, doi: [10.1109/33.159877](https://doi.org/10.1109/33.159877).
- [15] H. Johnson and M. Graham, *High Speed Signal Propagation: Advanced Black Magic*, 1st ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2003.
- [16] J. Zhang, J. L. Drewniak, D. J. Pommerenke, M. Y. Koledintseva, R. E. DuBroff, W. Cheng, Z. Yang, Q. B. Chen, and A. Orlandi, "Causal RLGC(f) models for transmission lines from measured S-parameters," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 1, pp. 189–198, Feb. 2010, doi: [10.1109/TEMC.2009.2035055](https://doi.org/10.1109/TEMC.2009.2035055).
- [17] D. F. Williams, "Metal-insulator-semiconductor transmission lines," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 2, pp. 176–181, Feb. 1999, doi: [10.1109/22.744292](https://doi.org/10.1109/22.744292).
- [18] G. Antonini, "SPICE equivalent circuits of frequency-domain responses," *IEEE Trans. Electromagn. Compat.*, vol. 45, no. 3, pp. 502–512, Aug. 2003, doi: [10.1109/TEMC.2003.815528](https://doi.org/10.1109/TEMC.2003.815528).
- [19] Clayton R. Paul, *Inductance: Loop and Partial*, 1st ed. Hoboken, NJ, USA: Wiley, 2010.
- [20] E. Bogatin, "Design rules for microstrip capacitance," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 11, no. 3, pp. 253–259, Sep. 1988, doi: [10.1109/33.16649](https://doi.org/10.1109/33.16649).
- [21] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*. New York, NY, USA: Dover, 1946.



EDUARDO MOCTEZUMA-PASCUAL was born in Veracruz, Mexico. He received the B.S. degree in electronics from Tecnológico de La Piedad, Michoacán, Mexico, in 2016, and the M.Sc. and Ph.D. degrees from the National Institute of Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico, in 2018 and 2022, respectively. He is currently with Intel, Guadalajara, Mexico, working on the development of interconnects for high-speed computing platforms.



MIGUEL A. G. LASO (Fellow, IEEE) received the M.Sc. and Ph.D. degrees in telecommunications engineering from the Public University of Navarra (UPNA), Pamplona, Spain, in 1997 and 2002, respectively. From 1998 to 2001, he was a Doctoral Fellow Student with the Electrical and Electronic Engineering Department, UPNA, where he was an Assistant Professor, from 2001 to 2006. From 2002 to 2003, he was also a Research Fellow with the Payload Systems Division, Euro-

pean Space Research and Technology Centre, European Space Agency (ESTEC-ESA), Noordwijk, The Netherlands. Since 2006, he has been an Associate Professor (Professor Titular), where he is involved in teaching and research duties related to optical communications and microwave engineering. He is currently the Head of the Microwave Components Group (MCG), UPNA. He is also the Co-Founder of TAFCO Metawireless S.L., a spin-off company of UPNA. He has authored or co-authored dozens of journal articles and contributed to major international conferences. He has also led projects with public and private funding within the MCG and UPNA. He holds several international patents, some of them used by the space industry. His current research interests include periodic structures, inverse scattering problems, synthesis techniques for filters and multiplexers in the microwave and millimeter-wave frequency ranges, and their applications in wireless and space communications. He is also a member of several professional and scientific international associations, including the Optical Society of America (OSA), the International Society for Optics and Photonics (SPIE), the American Society for Engineering Education (ASEE), and MTT-5 Filters and the MTT-S Education Committee. He is also a TPRC Member of the MTT-S International Microwave Symposium (IMS), a TPC member of the European Microwave Conference (EuMC), and a reviewer for several other international conferences and journals. He was the Co-Chair of the EuMC'18 (Madrid) and the Education Resources Development Subcommittee. He is the Chair of the Working Group of Standards for Microwave Filter Definitions, IEEE Standards Committee. He received several prizes, including the Spanish National Prize to the Best Doctoral Dissertation in telecommunications from the Spanish Telecommunications Engineers Association (COIT/AEIT), in 2002; the Junior Research Award of UPNA, in 2003; and the 2005 Spanish National Prize for the Best Project in Innovation in Higher Education from the Spanish Ministry of Education and Science. He was an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, from 2019 and 2022. He is the President of the URSI Spanish National Committee.



GERMÁN ALVAREZ-BOTERO (Senior Member, IEEE) received the Ph.D. degree from the National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico. He was a Postdoctoral Researcher with the RF Research Group, Federal University of Santa Catarina (UFSC), Florianópolis, Brazil; the High-Frequency Electronics and Telecommunications Research Group (CMUN), National University of Colombia, Bogotá, Colombia; and the Microwave Components Group (MCG), Public University of Navarra (UPNA), Pamplona, Spain. He has also been a Visiting Researcher with the Institut Supérieur de l'Aéronautique et de l'Espace (ISAE-SUPAERO), Toulouse, France; and a Titular Researcher with the Electronics and Telecommunications Department, Center for Scientific Research and Higher Education of Ensenada (CICESE), Mexico. He is currently a Senior Researcher with the Department of Electrical, Electronics and Communications, UPNA. His research interests include the design, characterization, and modeling of materials and components for RF/microwave applications.



REYDEZEL TORRES-TORRES (Senior Member, IEEE) received the Ph.D. degree in electronics, in 2003. He is currently a full-time Researcher with the Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Puebla, Mexico. Since 1998, he has been a part of teams working on microwave signal propagation in both industry and academic environments. He belongs to the National System of Researchers (SNII) of Mexico.