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RESEARCH ARTICLE

A New High Voltage Gain Transformer-Less Step-Up DC–DC Converter With Double Duty-Cycles: Design and Analysis

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ABSTRACT This paper proposes a new high gain step-up non-isolated transformer-less DC-DC converter, achieved through the effective integration of an active switched-inductor network with switched-capacitors. A substantially high voltage gain is achieved considering the quantity of components employed in its structure. Benefiting from double duty cycles, a notable attribute of the propounded circuit is its capability to obtain a consistent voltage gain through diverse duty cycle configurations. The second duty cycle introduces an additional degree of freedom to both the design procedure and the converter control system design. The pole placement control method is employed to regulate the converter, controlling both duty cycles simultaneously. The attainment of a high voltage gain, such as a gain of 20, is feasible through the use of low duty cycle values ($D_1 = 50\%$ and $D_2 = 35\%$). Also, the power switches are subject to less voltage stresses ($V_{S1} = V_{S2} = 0.26V_{out}$ and $V_{S3} = 0.48V_{out}$), enabling the implementation of low voltage rating MOSFETs with low on-resistance, resulting in improved efficiency. Moreover, the output switch under zero-voltage switching (ZVS) conditions and low turn-off switching losses of the input switches lead to an increased efficiency. Omitting the use of a transformer or coupled-inductors in this design reduces the converter size and weight, eliminates the challenges of leakage inductors, and also simplifies analysis, design, and fabrication procedure. The operation principles, steady-state analysis, design considerations, and efficiency calculations are provided in detail, followed by dynamic modeling and control analysis. To assess the merits of the propounded converter, a comparison study is conducted against those of other relevant converters. Ultimately, for the purpose of validating the suggested design, the converter simulation model in PSIM software is tested, and a 300W laboratory prototype is fabricated and evaluated.

INDEX TERMS Active switched-inductor, DC-DC converter, high voltage gain, non-isolated, step-up, transformer-less.

I. INTRODUCTION

In recent years, there has been a notable surge in the application of step-up DC-DC converters characterized by high voltage conversion ratios. Consequently, developing and introducing new topologies for these converters, employing diverse techniques to enhance voltage gain (VG) while simultaneously improving performance, have become prominent subjects of extensive research in the field of power electronics [1]. In the industrial domain, these converters are extensively utilized across a diverse range of applications. This includes their integration into power supplies, DC microgrids, and systems for electric traction. Their utility extends to the automotive sector, data centers, robotic technologies,

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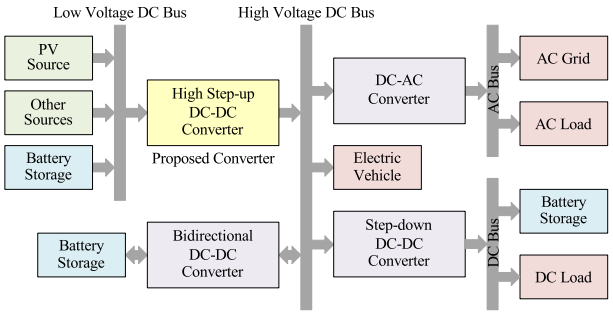


FIGURE 1. Application of the proposed converter in a DC microgrid.

satellite systems, and the illumination of streets. Furthermore, they play a crucial role in various renewable energy sources (RES), encompassing fuel cells, solar panels, and wind turbines, demonstrating their wide-ranging applicability [1], [2]. Step-up converters are used in these applications to boost low input voltages, often below 50 V, to higher outputs, such as 400 V [1], [2], [3]. Figure 1 illustrates the role of the converter in a DC microgrid application.

In theory, conventional DC-DC converters like boost, quadratic boost, and flyback converters can achieve high voltage conversion ratios at increased duty cycles. However, in practice, several factors constrain the VG or boost factor, including the elevated stress on the power switch, issues with the diode reverse recovery, and the conduction losses in the inductor [1], [2], [3]. Therefore, it is essential to modify the configurations of traditional step-up converters, aiming to improve crucial performance indicators [4], for example, in [5], the authors propounded a boost converter with soft-switching operation through an auxiliary circuit. Another example, in [6], zero-voltage-switching (ZVS) of main switches is achieved by applying an active snubber. Transformers or coupled inductors (CI) enhanced converters through their turn ratio, allowing VG to be adjusted via this ratio. Nevertheless, this integration introduces several disadvantages, including increased volume and cost, high switch voltage spikes because of the leakage inductance of the transformer, and core saturation. In contrast, transformerless structures are advantageous due to their straightforward design and ease of analysis. These configurations are not only cost-effective but also yield higher efficiency [1], [2], [3].

In the pursuit of achieving elevated VG, numerous step-up DC-DC converters have incorporated a range of unique boosting techniques. These encompass switched capacitors (SC), switched-inductors (SL), active switched-inductors (A-SL), and coupled-inductors. Moreover, methods such as voltage lift, voltage multipliers (VM), along with interleaved and cascaded connections, have been utilized. Additionally, combinations of these mentioned techniques have also been utilized to enhance converter performance [3], [7], [8], and [9]. The topologies presented in [10], [11], and [12] have used interleaved and CI techniques. Moreover, bidirectional converters are introduced in [13], [14], and [15], based on CI, interleaved, and interleaved combined with SC techniques, respectively. While the interleaving and CI techniques are well suited to high-power applications, these approaches increase the number of components and magnetic devices. The SC method is highly preferred for step-up converters due to its proficiency in enhancing VG and reducing voltage stress [16], [17], [18]. Yet, achieving higher VG necessitates additional SC cells, resulting in increased losses and decreased efficiency [17], [18]. Also, these converters faced significant current spikes or inrush currents during switching, impacting switch current stress and overall efficiency [17], [18]. Another method employed for augmenting VG is the SL technique, which yields notably effective outcomes, particularly when combined with the SC technique [19], [20], [21]. However, this necessitates the use of numerous components for obtaining high VG [22], [23].

The A-SL technique, another effective strategy for enhancing the boost factor, charges inductors in parallel through dual power switches, subsequently releasing their stored energy in series upon switch deactivation [24], [25], [26], [27]. Implementing SCs or VM cells at the A-SL based converter output can effectively boost VG and minimize voltage stress on switches [28], [29], [30], [31], [32], [33]. However, this implementation of the SC technique might add the drawback of inrush current to the converter [28], [31], [32]. In [33], the A-SL structure was enhanced by adding a ladder-type VM cell with a regenerative design, effectively elevating the VG but necessitating an additional switch and magnetic core. Furthermore, enhancing the conversion ratio can be achieved by replacing each inductor in the A-SL unit with a passive switched inductor (P-SL) cell, albeit at the cost of a higher component count [34], [35]. The concept of extending the A-SL units was introduced in [36], followed by [37] replacing the converter inductors with P-SL cells for enhanced performance. Furthermore, in [38], an inverting SC unit was added to the output of the converter in [37], reducing switch voltage stress compared to the structures in [36] and [37]. However, as a drawback, it should be mentioned that the number of inductors and semiconductors is too high in these topologies [36], [37], [38].

Employment of CIs in A-SL based converters is feasible [39], [40], [41], [42], [43]. The CIs' turn ratio (n) markedly contributes to enhancing VG while also alleviating voltage stress on the switches. Furthermore, this approach introduced an additional design parameter (n), providing greater flexibility in converter design. A drawback of these converters [42], [43] is the addition of a third magnetic core due to the CIs, resulting in increased volume and weight. Furthermore, it is noteworthy that once the converter is designed and implemented, the turn ratio value becomes fixed. Thus, this aspect of design flexibility is a one-time adjustable parameter [39], [40], [41], [42], [43].

The concept of integrating a third switch into the A-SL configuration was introduced in [44] to develop a converter for DC microgrid applications. Within this arrangement, inductors initially receive a charge in parallel via switches S_1 and S_2. Following the deactivation of these switches and the

activation of third switch (S_3), a subsequent charging phase occurs, this time in a series arrangement of the inductors. Ultimately, the deactivation of the third switch triggers the release of energy stored in the inductors [44], [45]. The primary benefit of this approach is that the third switch adds another duty cycle (D_2) to the converter parameters; thus, with different combinations of duty cycles (D_1 and D_2), high VG can be obtained. Also, an extra degree of freedom is added to the control system of the converter. The drawback lies in the positioning of the third switch on the converter output side, resulting in its voltage stress being equivalent to the output voltage [44], [45], [46]. For diminishing switch voltage tension while concurrently amplifying VG, the employment of the P-SL and SC cell is an effective strategy [47]. Moreover, the configuration of three-switch A-SL converters can be enhanced through the application of clamp capacitors [48], [49], [50], switched capacitors [51] or switched inductor-capacitor network [52]. Furthermore, an auxiliary switch and the resultant second duty cycle can be added to the extendable A-SL structures, as illustrated in [53] and [54]; however, the main drawback of high component count remains. In [55], a VM cell, comprising inductors and capacitors, is implemented at the converter output. This necessitates a bulky, heavy magnetic core in the VM cell. Hence, an alternative approach, eliminating the need for this core, is preferable. Finally, it should be noted that the presented converters in [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], and [55] function using dual duty cycles, thereby offering an additional control variable. Nonetheless, a control analysis and an elucidation of how this extra control variable (the second duty cycle) has been utilized, remains absent and not provided in the literatures [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], and [55].

A meticulous literature analysis and a detailed investigation into A-SL-based high step-up DC-DC converters unveil the necessity for their performance enhancement and optimization. In this paper, an innovative transformer-less topology is proposed, realized through the efficient integration of the A-SL network with SCs. The main contributions are listed below:

- Achieving a high VG is feasible, considering the number of components incorporated within its structural design.
- The switches are subject to less voltage stresses, facilitating the employment of switches with lower voltage ratings and on-resistance.
- Versatility to attain a uniform VG is obtained through varied duty cycle configurations.
- The converter control system is enhanced with an augmented degree of freedom (using second duty cycle), and a control analysis for simultaneously controlling both duty cycles is provided.
- Omitting the use of a transformer or coupled inductor in this design reduces the converter size and weight and simplifies its design and implementation.

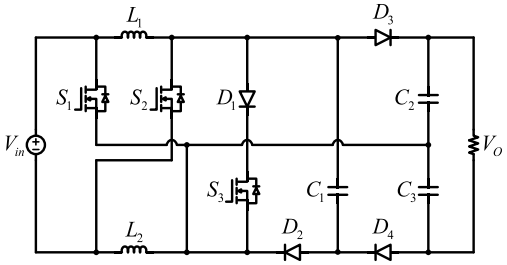


FIGURE 2. Circuit layout of the proposed converter (PC).

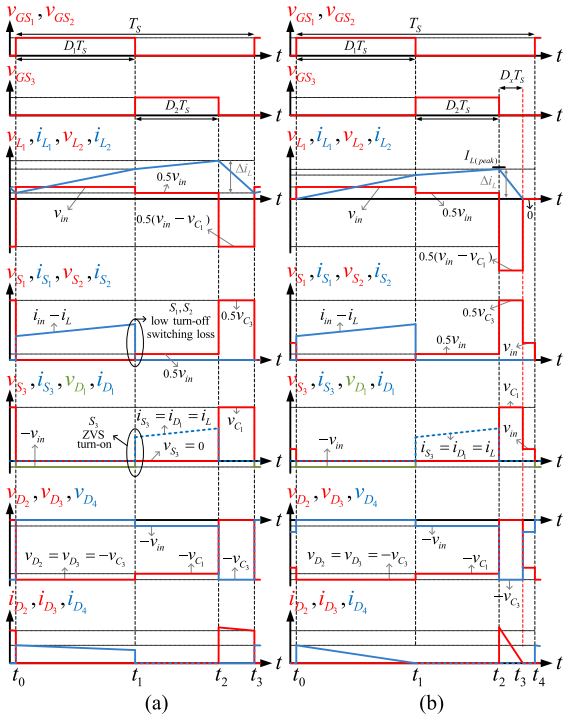


FIGURE 3. Steady-state waveforms of the PC (a) CCM and (b) DCM.

- The output switch under ZVS conditions and low turn-off switching losses of the input switches lead to increased efficiency.

The paper structure is organized, as follows: Section II elucidates the proposed converter topology and functioning in CCM and DCM, and then, Section III undertakes steady-state analysis. Design considerations are delineated in Section IV, while Section V addresses power losses and efficiency calculations. Control analysis is covered in Section VI, and Section VII presents a comparative analysis to highlight the proposed converter capabilities. Experimental and simulation results validating the converter analysis and performance are presented in Section VIII, with concluding remarks in Section IX.

II. PROPOSED TOPOLOGY AND OPERATION PRINCIPLE

Figure 2 illustrates the circuit layout of the proposed converter (PC), which is an integration of the modified A-SL network, formed by two inductors (L_1, L_2) and three power MOSFETs (S_1, S_2, S_3) with SCs. The functioning of the

PC is categorized into two primary modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). For simplifying the analysis, some assumptions are made: (a) all components are considered ideal and without losses, (b) the capacitors are sufficiently large, warranting the assumption of constant voltage during different operational modes, and (c) the inductors L_1 and L_2 are identical ($L_1 = L_2 = L$) and sufficiently large to validate a linear variation premise for their currents.

A. CCM OPERATION

Essential waveforms of the PC, encompassing the voltage and current across all components with the exception of capacitors, are depicted in Figure 3(a). This illustration reveals that the PC operates in three distinct modes within each switching cycle (Modes I, II and III). Moreover, Figure 4 illustrates the respective current trajectories corresponding to each of these operational modes.

Mode I $[t_0 - t_1]$*:*

At $t = t_0$, upon receiving the same control signal, switches S_1 and S_2 are simultaneously activated; this results in a parallel connection between inductors L_1 and L_2 and input source V_{in}, with the input source charging the inductors and increasing their current (i_{L1} and i_{L2}) linearly. The path of current flow pertinent to this state is shown in Figure 4(a); switch S_3, diodes D_1, D_2, and D_3 are off-state, and only diode D_4 is conducting. As a result, capacitor C_3 is charged, and capacitors C_1 and C_2 are discharged. Moreover, capacitor C_2 provides the energy of the output load. Utilizing KVL and KCL in the equivalent circuit of this state results in the derivation of the following equations.

$$v_L = v_{in} \tag{1}$$
$$v_{C_3} - v_{C_1} = v_{in} \tag{2}$$
$$v_{C_2} + v_{C_3} = v_O \tag{3}$$
$$i_{C_2} = -i_O \tag{4}$$
$$i_{C_3} = -i_{C_1} - i_O \tag{5}$$
$$i_{in} = 2i_L + i_{C_3} + i_O \tag{6}$$

Mode II $[t_1 - t_2]$*:* At $t = t_1$, the gate signal of switches S_1 and S_2 is cut off, and control signal V_{GS3} is applied to switch S_3; therefore, S_1 and S_2 are turned off, and S_3 is activated. Given that the off-state voltage across switches S_1 and S_2 is considerably low in this mode, equating to half of the input voltage, the losses associated with their turn-off switching are diminished. Moreover, as shown in Figure 3(a), The activation of switch S_3 under ZVS conditions effectuates a notable decrease in switching losses. Figure 4(b) illustrates the equivalent circuit of this mode; diode D_1 is conducting, but diodes D_2, D_3, and D_4 are reversed-biased. As a result, the inductors and the input source are connected in series, and half of the input voltage is applied to each inductor. Thus, the inductors continue to charge, but the slope of their current increase is half that of the previous mode. Capacitor C_1 remains at the same charge level; however, capacitors C_2 and C_3 are discharged and supply the output load. By applying the KVL and KCL in this mode, the following equations can be obtained.

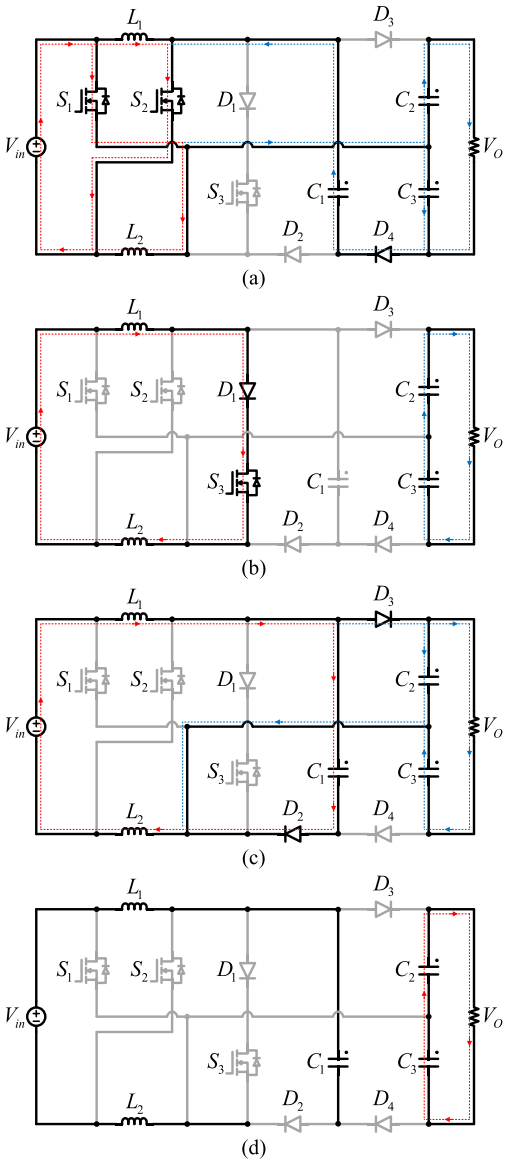


FIGURE 4. Propounded converter in various operational modes. (a) Mode I, (b) Mode II, (c) Mode III and (d) Mode IV (DCM).

$$v_L = v_{in}/2 \tag{7}$$
$$i_{C_1} = 0 \tag{8}$$
$$i_{C_2} = i_{C_3} = -i_O \tag{9}$$
$$i_{in} = i_L \tag{10}$$

Mode III $[t_2 - t_3]$*:* At $t = t_2$, the gate signal V_{GS3} is cut off, and switch S_3 and diode D_1 are turned off. Diode D_4 is still off-state, but diodes D_2 and D_3 start to conduct; therefore, the input source energy and the stored energy of inductors L_1 and L_2 are transferred and charge capacitors C_1 and C_2. So i_{in}, i_{L1}, and i_{L2} decrease linearly. Moreover, capacitor C_3 provides energy and is discharged. Using the equivalent circuit of this

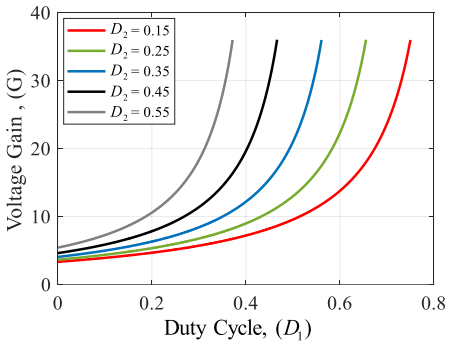


FIGURE 5. Voltage gain curves of the proposed structure.

mode, depicted in Figure 4(c), the subsequent equations are derived, as follows:

$$2v_L = v_{in} - v_{C_1} \tag{11}$$
$$v_{C_1} = v_{C_2} \tag{12}$$
$$i_{in} = i_L = i_{C_1} + i_{C_2} + i_O \tag{13}$$
$$i_{C_3} = -i_O \tag{14}$$

B. DCM OPERATION

In DCM operation, the voltage across inductors L_1 and L_2 drops to zero prior to the completion of the switching cycle. Consequently, the operation is segmented into four distinct modes of operation. Analogous to the CCM operation, the modes I, II, and III are illustrated in Figures 4(a), 4(b), and 4(c), respectively. The first three DCM operating modes follow a similar behavior; therefore, this section exclusively elucidates mode IV of DCM, which is represented in Figure 4(d). The waveform of the essential components is illustrated in Figure 3(b).

Mode IV $[t_3 - t_4]$*:* This mode starts when the current of the inductors L_1 and L_2 reaches zero; hence, the voltage across them is zero. All the semiconductor devices are in a deactivated state. Meanwhile, capacitors C_2 and C_3 are discharged because of providing energy for the load. Thus, their current equals to -i_O in this mode.

III. STEADY-STATE ANALYSIS

A. CCM OPERATION

In this section, the voltage gain of the proposed converter along with voltage and current stresses of its components are calculated. By applying volt-second balance law to inductor L, using (1), (7), and (11), the following equation is written.

$$\int_{t_0}^{t_1} v_{in}dt + \int_{t_1}^{t_2} \frac{1}{2}v_{in}dt + \int_{t_2}^{t_3} \frac{1}{2}\left(v_{in} - v_{C_1}\right)dt = 0 \tag{15}$$

Utilizing (2), (3), (12) and (15), the voltage across capacitors C_1, C_2 and C_3 along with the output voltage can be obtained as written below:

$$V_{C_1} = V_{C_2} = \frac{1 + D_1}{1 - D_1 - D_2}V_{in} \tag{16}$$

TABLE 1. Semiconductors voltage stress.

Device	Mode I	Mode II	Mode III
S_1, S_2	0	$\frac{1-D_1-D_2}{2(3+D_1-D_2)}V_O$	$\frac{2-D_2}{2(3+D_1-D_2)}V_O$
S_3	0	0	$\frac{1+D_1}{3+D_1-D_2}V_O$
D_1	$-\frac{1-D_1-D_2}{3+D_1-D_2}V_O$	0	0
D_2, D_3	$-\frac{2-D_2}{3+D_1-D_2}V_O$	$-\frac{1+D_1}{3+D_1-D_2}V_O$	0
D_4	0	$-\frac{1-D_1-D_2}{3+D_1-D_2}V_O$	$-\frac{2-D_2}{3+D_1-D_2}V_O$

TABLE 2. Capacitors current in different operation states.

Capacitor	Mode I	Mode II	Mode III
C_1	$-\frac{1}{D_1}I_O$	0	$\frac{1}{1-D_1-D_2}I_O$
C_2	$-I_O$	$-I_O$	$\frac{D_1+D_2}{1-D_1-D_2}I_O$
C_3	$\frac{1-D_1}{D_1}I_O$	$-I_O$	$-I_O$

$$V_{C_3} = \frac{2 - D_2}{1 - D_1 - D_2}V_{in} \tag{17}$$
$$V_O = G_{CCM}V_{in} = \frac{3 + D_1 - D_2}{1 - D_1 - D_2}V_{in} \tag{18}$$

where, G_{CCM} is the voltage gain of the proposed converter. Figure 5 depicts the curves related to the voltage gain for different values of D_2, as is evident, G_{CCM} can be adjusted using two duty cycles (i.e., D_1 and D_2); thus, the exact value of the voltage gain can be obtained with different combinations of these duty cycles.

For the selection of appropriate components essential for the fabrication of the proposed converter, it is imperative to calculate the voltage and current value that each component must be capable of enduring. The calculation of the voltage stress in semiconductors is achievable through the analysis of equivalent circuits at intervals when they are in a state of inactivity. By writing KVL in each operation mode, and using (16)-(18), the voltage across of the semiconductors is obtained and provided in Table 1.

By applying ampere-second principle to capacitors C_2 and C_3, using (4), (9), and (14), the following equations are written.

$$\int_0^{(D_1+D_2)T_S} -I_O dt + \int_{(D_1+D_2)T_S}^{T_S} I_{C_2}^{III}dt = 0 \tag{19}$$
$$\int_0^{D_1T_S} I_{C_3}^{I}dt + \int_{D_1T_S}^{T_S} -I_O dt = 0 \tag{20}$$

From these equations, the currents of the capacitors C_2 and C_3 in modes III and I are calculated, respectively.

$$I_{C_2}^{III} = \frac{D_1 + D_2}{1 - D_1 - D_2}I_O, \quad I_{C_3}^{I} = \frac{1 - D_1}{D_1}I_O \tag{21}$$

Furthermore, by considering the converter ideal performance, the following equation can be written for the input current:

$$\int_0^{D_1T_S}(2I_L + I_{C_3}^I + I_O)dt + \int_{D_1T_S}^{T_S} I_L dt = G_{CCM} I_O \quad (22)$$

Using (21) and (22), the average current of the inductors is obtained, as follows:

$$I_L = \frac{2}{1 - D_1 - D_2} I_O \quad (23)$$

Using (21), (23), as well as the capacitors current relationships derived via KCL for each operational mode discussed in Section II, the equations for the capacitors currents, expressed in relation to the output load current (I_O), are formulated and presented in Table 2. The current stress of the semiconductors can be determined using the following formulas.

$$I_{S_1} = I_{S_2} = \frac{1 + D_1 - D_2}{D_1(1 - D_1 - D_2)} I_O \quad (24)$$

$$I_{S_3} = I_{D_1} = \frac{2}{1 - D_1 - D_2} I_O \quad (25)$$

$$I_{D_2} = I_{D_3} = \frac{1}{1 - D_1 - D_2} I_O \quad (26)$$

$$I_{D_4} = \frac{1}{D_1} I_O \quad (27)$$

B. DCM OPERATION

Utilizing the volt-second balance principle on the input inductors, accompanied by several derivations, enables the determination of the voltages across capacitors C_1, C_2, C_3, as well as the output voltage.

$$V_{C_1} = V_{C_2} = (2D_1 + D_2 + D_x)V_{in}/D_x \quad (28)$$

$$V_{C_3} = (2D_1 + D_2 + 2D_x)V_{in}/D_x \quad (29)$$

$$V_O = G_{DCM} V_{in} = \left(\frac{2(2D_1 + D_2 + D_x)}{D_x} + 1\right) V_{in} \quad (30)$$

Additionally, through the application of the charge balance principle to the capacitors, followed by a sequence of derivations, it becomes possible to calculate the current flowing through the inductors.

$$I_L = \frac{2}{D_x} I_O \quad (31)$$

Assuming $I_L = I_{L(\text{peak})}/2$, then $I_{L(\text{peak})}$ can be obtained, as follows:

$$I_{L(peak)} = \frac{4V_O}{D_x R_{Load}} \quad (32)$$

Furthermore, the following equation can be formulated for the inductors, as below:

$$\Delta i_L = \frac{V_L \Delta t}{L} \Rightarrow I_{L(peak)} = \frac{2D_1 + D_2}{2Lf_S} V_{in} \quad (33)$$

Using (32) and (33), the time duration of the mode III is obtained.

$$D_x = \frac{8\tau G_{DCM}}{2D_1 + D_2} \quad (34)$$

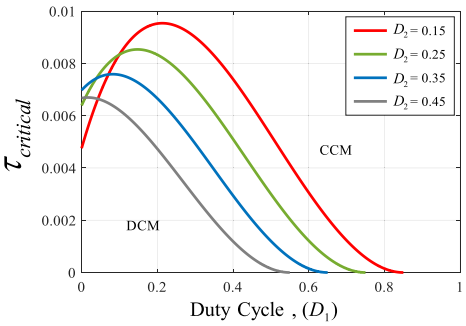


FIGURE 6. Boundary of CCM and DCM.

where, τ is a dimensionless variable, and it is defined, as follows:

$$\tau = \frac{f_S L_{eq}}{R_{Load}} \quad (35)$$

Using (30) and (34), the DCM voltage gain of the PC is achieved.

$$G_{DCM} = \left(3 + \sqrt{9 + \frac{(2D_1 + D_2)^2}{\tau}}\right)/2 \quad (36)$$

To ascertain the boundary condition distinguishing between the CCM and DCM operations, G_{CCM} equals G_{DCM}. Hence, the critical value of τ is obtained by (37) and plotted in Figure 6 for different values of D_2.

$$\tau_{critical} = (2D_1 + D_2)^2 / \left(\left(\frac{3 + 5D_1 + D_2}{1 - D_1 - D_2}\right)^2 - 9\right) \quad (37)$$

IV. DESIGN CONSIDERATIONS

The prototype is designed to demonstrate the PC high voltage gain capability, with specified input and output voltages set at 20V and 400V, respectively. Moreover, the efficiency assessment will be undertaken with output energies between 100W and 300W. Thus, the output power range must be taken into consideration for these assessments. Using (18), it is possible to determine the values of duty cycles D_1 and D_2; as depicted in Figure 7, the regulation of the output voltage at 400V can be achieved through various combinations of these duty cycles.

A. INDUCTORS DESIGN

The inductances must be selected according to (37) and (38) to ensure the CCM operation. Moreover, utilizing (39), it is possible to calculate the current ripple rate of the inductors.

$$L \geq \frac{\tau_{critical} R_{Load}}{f_S} \quad (38)$$

$$\alpha_L = \frac{\Delta i_L}{I_L} = \left(\frac{(2D_1 + D_2)(1 - D_1 - D_2)^2}{4(3 + D_1 - D_2)}\right) \frac{R_{Load}}{f_S L} \quad (39)$$

Within the operational range, the harshest condition for the inductors occurs at an output power of 100W. The minimum values of the inductors securing the CCM operation of the

TABLE 3. Minimum value of the capacitances.

(D_1, D_2)	C	$f_S = 20$kHz	$f_S = 25$kHz	$f_S = 40$kHz	$f_S = 50$kHz
0.4, 0.45	C_1	25.81 µF	20.65 µF	12.90 µF	10.32 µF
	C_2	16.83 µF	13.47 µF	8.41 µF	6.73 µF
	C_3	10.72 µF	8.57 µF	5.36 µF	4.28 µF
0.5, 0.34	C_1	19.70 µF	15.76 µF	9.84 µF	7.88 µF
	C_2	16.74 µF	13.40 µF	8.37 µF	6.70 µF
	C_3	8.95 µF	7.16 µF	4.48 µF	3.58 µF
0.6, 0.23	C_1	19.75 µF	15.80 µF	9.87 µF	7.89 µF
	C_2	14.86 µF	11.88 µF	7.43 µF	5.94 µF
	C_3	7.14 µF	5.71 µF	3.57 µF	2.86 µF

prototype are plotted versus duty cycles for different switching frequencies in Figure 8.

B. CAPACITORS DESIGN

It is essential to precisely determine the capacities of the associated capacitances to constrain the oscillation of voltage across the capacitors. The capacitors encounter their most critical condition when the output power attains a level of 300W ($R_{Load} = 533\Omega$). Considering a permissible voltage ripple specified at $\alpha = 1\%$ ($\Delta V_C = 0.01 \times V_C$), the determination of the circuit capacitances can be achieved through the application of the ensuing equations.

$$C_1 \geq \frac{(3 + D_1 - D_2)}{(1 + D_1)(\alpha) f_S R_{Load}} \tag{40}$$

$$C_2 \geq \frac{(D_1 + D_2)(3 + D_1 - D_2)}{(1 + D_1)(\alpha) f_S R_{Load}} \tag{41}$$

$$C_3 \geq \frac{(1 - D_1)(3 + D_1 - D_2)}{(2 - D_2)(\alpha) f_S R_{Load}} \tag{42}$$

The minimum value of the capacitances for different duty cycle combinations and switching frequencies are calculated and listed in Table 3. Based on the preceding calculations, the capacitance values can be chosen. Opting for capacitors with a higher capacitance value can lead to a reduction in voltage ripple; furthermore, these capacitors typically exhibit lower power losses due to their reduced equivalent series resistance (ESR).

V. EFFICIENCY AND NON-IDEAL VOLTAGE GAIN

To determine the efficiency of the proposed converter, a meticulous calculation of the power losses incurred by each component, encompassing input inductors, semiconductors, and capacitors, proves essential. By applying the formulas delineated in Table 4 alongside (43), the computation of power losses is undertaken, subsequently enabling the determination of the efficiency as per (44).

$$P_{Loss} = P_L + P_S + P_D + P_C \tag{43}$$

$$\eta = 100 P_O / (P_O + P_{Loss}) \tag{44}$$

Furthermore, the derivation of the non-ideal voltage gain can be accomplished with the application of (45).

$$G' = G / (1 + (P_{Loss}/P_O)) \tag{45}$$

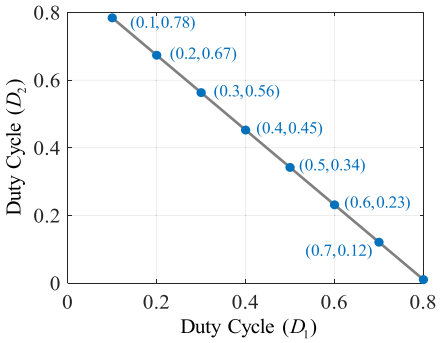


FIGURE 7. Different possible combinations of duty cycles (D_1 and D_2) to obtain a 400V output voltage from a 20V input.

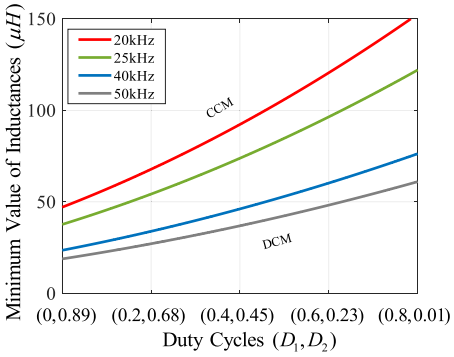


FIGURE 8. Minimum value of the inductances (L_1 and L_2) required for CCM operation (V_{in} = 20V, V_{out} = 400V and P_{out} = 100W).

It merits attention that the assessment of the efficiency is conducted by drawing upon the specifications of the components deployed in the prototype, as specified in the ensuing details.

$$\begin{aligned}
V_{in} &= 20V,\ R_{Load} = 533\Omega,\ r_{L_1} = r_{L_2} = 10m\Omega,\\
r_{C_{1,2,3}} &= 100m\Omega,\\
r_{S_{1,2}} &= 12m\Omega,\ t_{\mathrm{on}_{S_{1,2}}} = 77ns,\ t_{\mathrm{off}_{S_{1,2}}} = 57ns,\\
C_{OSS_{S_{1,2}}} &= 550pF,\\
r_{S_3} &= 38m\Omega,\ t_{\mathrm{on}_{S_3}} = 49ns,\ t_{\mathrm{off}_{S_3}} = 51ns,\\
C_{OSS_{S_3}} &= 390pF,\\
V_{F(D_{1,2,3,4})} &= 0.75V,\ t_{rr(D_1)} = 20ns,\ t_{rr(D_{2,3,4})} = 28ns,\\
r_D &= 10m\Omega.
\end{aligned}$$

Figure 9(a) provides a visual representation of how the non-ideal characteristics of the components influence the converter efficiency and its voltage gain. As illustrated by Figure 7, the attainment of a 400V output voltage regulation is feasible via diverse amalgamations of duty cycles. Figure 9(b) elucidates and delineates the impact of choosing specific duty cycles on the converter efficiency. The dependency of power switch energy losses on switching frequency necessitates an examination of its influence on the converter efficiency; Figure 9(c) demonstrates that lowering the switching frequency boosts the converter efficiency.

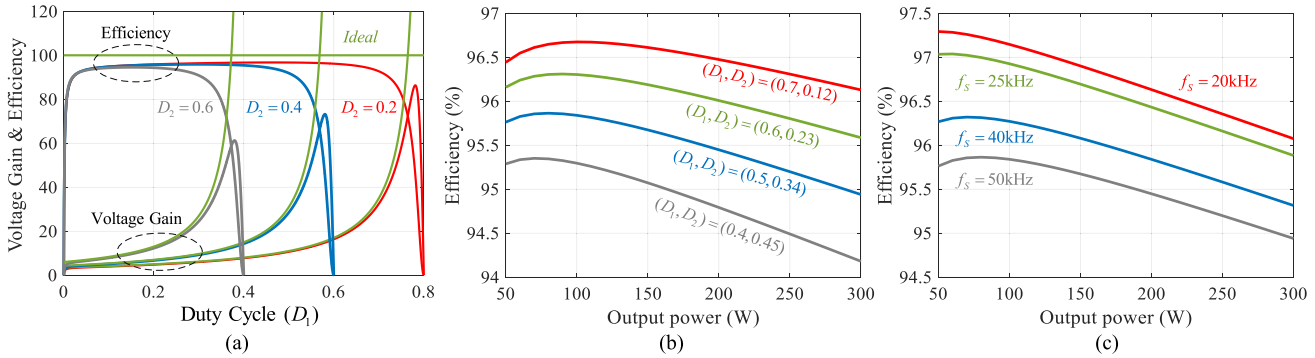


FIGURE 9. Efficiency analysis (a) Impact of non-ideality on efficiency and voltage gain ($R_{Load} = 533\Omega$, $f_S = 50$kHz), (b) Efficiency vs output power ($V_{in} = 20$V, $V_{out} = 400$V, $f_S = 50$kHz), and (c) Efficiency vs output power ($V_{in} = 20$V, $V_{out} = 400$V, $D_1 = 0.5$, $D_2 = 0.34$).

TABLE 4. Required equations for power loss calculation.

P_L	$\sum_{i=1}^{2}\left(r_{L_i} I_{L_i(rms)}{}^2 + P_{Core_{L_i}}\right)$
P_S	$\sum_{i=1}^{3}\left(r_{S_i} I_{S_i(rms)}{}^2 + (V_{S_i(on)} I_{S_i(on)} t_{on_{S_i}} + V_{S_i(off)} I_{S_i(off)} t_{off_{S_i}} + C_{OSS_{S_i}} V_{S_i}{}^2) f_S / 2\right)$
P_D	$\sum_{i=1}^{4}\left(V_{f_{D_i}} I_{D_i(ave)} + r_{D_i} I_{D_i(rms)}{}^2 + (V_{D_i} I_{D_i(off)} t_{rr_{D_i}}) f_S / 2\right)$
P_C	$\sum_{i=1}^{3}\left(r_{C_i} I_{C_i(rms)}{}^2\right)$

VI. DYNAMIC MODELING AND CONTROL ANALYSIS

In this section, all the power semiconductors, inductors, and capacitors are assumed to be in their ideal states. But for accurate state variable separation in each operational state, the inductor incorporates parasitic series resistors labeled as r_L, and the capacitors feature parasitic series resistors denoted as r_C are considered. Employing the state-space averaging technique facilitates the derivation of both the average model and the small-signal model. This method involves obtaining system equations for all operating modes and then averaging them over a single commutation period, taking into consideration the time duration of each mode. In all three switching subintervals, the system equations can be expressed by (46), where $m = 1, 2$ and 3. Moreover, matrices A_1, A_2, A_3, B_1, B_2, and B_3 are provided in Table 5.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{C_1}}{dt} \\ \frac{dv_{C_2}}{dt} \\ \frac{dv_{C_3}}{dt} \end{bmatrix} = [A_m] \begin{bmatrix} i_L \\ v_{C_1} \\ v_{C_2} \\ v_{C_3} \end{bmatrix} + [B_m] v_{in} \tag{46}$$

The control method involves the pole placement technique, and the small signal model of the converter is computed and derived from the state-space averaged model. Utilizing the small signal modeling approach, the state variables and control inputs are represented as a combination of two components: a fixed part ($\overline{X}, \overline{D}$) and a variable part ($\tilde{x}, \tilde{d}$), i.e.:

$$\begin{cases} x = \overline{X} + \tilde{x} \\ D = \overline{D} + \tilde{d} \end{cases} \tag{47}$$

The small signal model for the proffered converter is derived by applying this approach to the averaged state-space model and by disregarding their squared values.

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \\ y = E\tilde{x} + F\tilde{u} \end{cases} \tag{48}$$

The definitions for state variables ($\tilde{x}$), control inputs ($\tilde{u}$), and output signals (y) are, as follows:

$$\tilde{x} = \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \end{bmatrix}, \quad \tilde{u} = \begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \end{bmatrix}, \; y = \begin{bmatrix} I_L \\ V_{C1} \end{bmatrix} \tag{49}$$

Using the specifications of the proposed converter, the matrices A, B, E, and F are represented as follows:

$$A = \begin{bmatrix} -0.0002 & -0.0002 & 0 & -0.0002 \\ -0.0990 & -3.25 & 0 & 3.25 \\ 0.1140 & 0.75 & -0.0001 & -0.7501 \\ 0 & 2.5 & -0.0001 & -2.5001 \end{bmatrix} \times 10^6 \tag{50}$$

$$B = \begin{bmatrix} 0.7319 & 0.6653 \\ 4.1905 & 4.2143 \\ -4.8492 & -4.8492 \\ 0.0239 & 0.0001 \end{bmatrix} \times 10^6 \tag{51}$$

$$E = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}, \quad F = [0] \tag{52}$$

Utilizing the pole placement method allows the positioning of the poles of the closed-loop system at any desired location, given the system complete state controllability. The controllability matrix for the proposed converter is expressed as below:

$$\Phi_C = \left[B \vdots AB \vdots A^2B \vdots \cdots \vdots A^{n-1}B\right] \tag{53}$$

TABLE 5. State equations matrices and transfer functions.

Matrices	$A_1=\begin{bmatrix} -\frac{r_L}{L} & 0 & 0 & 0 \\ 0 & -\frac{R+2r_c}{C_1r_c(2R+3r_c)} & -\frac{2(R+2r_c)}{2R+3r_c}-1 & -\frac{R+2r_c}{2R+3r_c}-1 \\ 0 & -\frac{1}{C_2(2R+3r_c)} & -\frac{2}{C_2(2R+3r_c)} & -\frac{1}{C_2(2R+3r_c)} \\ 0 & -\frac{R+r_c}{C_3r_c(2R+3r_c)} & -\frac{1}{C_3(2R+3r_c)} & -\frac{R+2r_c}{C_3r_c(2R+3r_c)} \end{bmatrix}$ $B_1=\begin{bmatrix} \frac{1}{L} \\ -\frac{R+2r_c}{C_1r_c(2R+3r_c)} \\ -\frac{1}{C_2(2R+3r_c)} \\ -\frac{R+r_c}{C_3r_c(2R+3r_c)} \end{bmatrix}$ $A_2=\begin{bmatrix} -\frac{r_L}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2(R+2r_c)} & -\frac{1}{C_2(R+2r_c)} \\ 0 & 0 & -\frac{1}{C_3(R+2r_c)} & -\frac{1}{C_3(R+2r_c)} \end{bmatrix}$ $B_2=\begin{bmatrix} \frac{1}{2L} \\ 0 \\ 0 \\ 0 \end{bmatrix}$ $A_3=\begin{bmatrix} 0 & -\frac{R+r_c}{L(4R+6r_c)} & \frac{r_c}{L(4R+6r_c)} & -\frac{R+r_c}{L(4R+6r_c)} \\ -\frac{4Rr_L+6r_Lr_c}{C_1r_c(2R+3r_c)} & -\frac{R+2r_c}{C_1r_c(2R+3r_c)} & -\frac{1}{C_1(2R+3r_c)} & \frac{R+r_C}{C_1r_c(2R+3r_c)} \\ \frac{(R+r_c)\left(\frac{(4Rr_L+6r_Lr_c)}{r_c(2R+3r_c)}+1\right)}{C_2(R+2r_c)} & \frac{R+r_c}{C_2r_c(2R+3r_c)} & \frac{(R+r_c)\left(\frac{1}{2R+3r_c}-\frac{1}{R+r_c}\right)}{C_2(R+2r_c)} & -\frac{(R+r_c)\left(\frac{1}{R+r_c}+2R+3r_c\right)}{C_2(R+2r_c)} \\ \left(-\frac{4Rr_L+2Rr_c+6r_Lr_c+3r_c^2}{C_3(2R^2+7Rr_c+6r_c^2)}\right) & -\frac{R+2r_c}{C_3(2R^2+7Rr_c+6r_c^2)} & -\frac{2R+4r_c}{C_3(2R^2+7Rr_c+6r_c^2)} & -\frac{R+2r_c}{C_3(2R^2+7Rr_c+6r_c^2)} \end{bmatrix}$ $B_3=\begin{bmatrix} \frac{3R+5r_c}{L(4R+6r_c)} \\ -\frac{R+2r_c}{C_1r_c(2R+3r_c)} \\ \frac{R+r_c}{C_2r_c(2R+3r_c)} \\ -\frac{R+2r_c}{C_3(2R^2+7Rr_c+6r_c^2)} \end{bmatrix}$
Transfer Functions	$G_1(s)=\frac{I_L(s)}{d(s)}=\frac{(3.329\times10^9\ s^4)+(1.68\times10^{16}\ s^3)+(3.384\times10^{20}\ s^2)+(1.314\times10^{24}\ s)+(4.705\times10^{26})}{s^6+(5.898\times10^6\ s^5)+(4.579\times10^{11}\ s^4)+(1.087\times10^{16}\ s^3)+(1.036\times10^{20}\ s^2)+(3.88\times10^{23}\ s)+(4.705\times10^{26})}$
	$G_2(s)=\frac{V_{C_1}(s)}{d(s)}=\frac{(8.041\times10^9\ s^4)+(1.313\times10^{16}\ s^3)+(2.577\times10^{20}\ s^2)+(9.61\times10^{23}\ s)+(4.705\times10^{26})}{s^6+(5.898\times10^6\ s^5)+(4.579\times10^{11}\ s^4)+(1.087\times10^{16}\ s^3)+(1.036\times10^{20}\ s^2)+(3.88\times10^{23}\ s)+(4.705\times10^{26})}$

If the rank of the matrix Φ_C is 4 (equivalent to the number of state variables, $\tilde{x}$), the system is fully controllable. Subsequently, two additional integral states are determined, as follows:

$$\dot{q}(t)=r(t)-y(t) \Rightarrow \begin{cases} \dot{q}_1(t)=r_1(t)-y_1(t)=r_1(t)-I_L(t) \\ \dot{q}_2(t)=r_2(t)-y_2(t)=r_2(t)-V_{C_1}(t) \end{cases} \tag{54}$$

Using the newly introduced integral states, the equations for both the state and output are reformulated, as follows:

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \cdots \\ \dot{q}(t) \end{bmatrix}=\begin{bmatrix} A & \vdots & 0 \\ \cdots & \vdots & \cdots \\ -E & \vdots & 0 \end{bmatrix}\begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix}+\begin{bmatrix} B \\ \cdots \\ 0 \end{bmatrix}\tilde{u}(t)+\begin{bmatrix} 0 \\ \cdots \\ I \end{bmatrix}r(t)$$
$$y(t)=\begin{bmatrix} E & \vdots & 0 \end{bmatrix}\begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{55}$$

In the equation above, $r(t)$ represents the input reference vector and is expressed by the following equation.

$$r(t)=\begin{bmatrix} I_{L,ref} & V_{C_1,ref} \end{bmatrix}^T \tag{56}$$

Derived from (55), the new matrices $\overline{A}$ and $\overline{B}$ are determined, as follows:

$$\overline{A}=\begin{bmatrix} A & \vdots & 0 \\ \cdots & \vdots & \cdots \\ -E & \vdots & 0 \end{bmatrix},\quad \overline{B}=\begin{bmatrix} B \\ \cdots \\ 0 \end{bmatrix} \tag{57}$$

The controllability matrix for the system in (55) can be expressed by the following equation.

$$\begin{aligned} \overline{\Phi}_C &= \begin{bmatrix} B & \vdots & A\Phi_C \\ \cdots & \vdots & \cdots \\ 0 & \vdots & -E\Phi_C \end{bmatrix} \\ &= \underbrace{\begin{bmatrix} B & \vdots & A \\ \cdots & \vdots & \cdots \\ 0 & \vdots & -E \end{bmatrix}}_{M}\begin{bmatrix} I & \vdots & 0 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & \Phi_C \end{bmatrix} \end{aligned} \tag{58}$$

If Φ_C is determined to have complete rank, the system described in (55) is fully controllable, if the rank of the matrix M is $n+m$ (where n and m represent the number of variable states ($\tilde{x}$) and output signals (y), respectively). Thus, the following equation with matrix K can be written.

$$\tilde{u}(t)=-K\begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix}=-\begin{bmatrix} K_x & \vdots & K_q \end{bmatrix}\begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{59}$$

The matrices K_x and K_q are expressed, as follows:

$$K_x = \begin{bmatrix} K_{11} & K_{12} & K_{13} & K_{14} \\ K_{21} & K_{22} & K_{23} & K_{24} \end{bmatrix}, \quad K_q = \begin{bmatrix} K'_{11} & K'_{12} \\ K'_{21} & K'_{22} \end{bmatrix} \tag{60}$$

Inserting (59) into (55) results in the following equation.

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \cdots \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A - BK_x & \vdots & -BK_q \\ \cdots & \vdots & \cdots \\ -E & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} + \begin{bmatrix} 0 \\ \cdots \\ I \end{bmatrix} r(t)$$

$$y(t) = \begin{bmatrix} E & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{61}$$

The current challenge is to identify the control signal $\tilde{u}(t)$ using the state feedback gain matrix K, ensuring the placement of closed-loop system eigenvalues at specific locations. Various methods exist for establishing the system controller matrix $K = [K_x, K_q]$. The MATLAB software's control systems toolbox features a beneficial pole-placement function. This function takes the system (55) and the desired eigenvalue locations as inputs to calculate the state feedback gain matrices. To ensure system stability, matrices K_x and K_q are established, as written below:

$$K_x = \begin{bmatrix} -3.6816 & 318.6502 & 282.7084 & 345.2654 \\ 3.7047 & -322.3272 & -285.8514 & -348.9611 \end{bmatrix} \tag{62}$$

$$K_q = \begin{bmatrix} -0.5606 & 1.1205 \\ 0.5667 & -1.1332 \end{bmatrix} \times 10^5 \tag{63}$$

The block diagram illustrating the control method is presented in Figure 10(a). This diagram visually outlines the steps involved in implementing the aforementioned equations to regulate the I_L and V_{C1} of the proposed converter. For instance, when aiming to control I_L and V_{C1} to the desired value $r(t)$, as illustrated in Figure 10(a), the initial step involves comparing $r(t)$ with the respective current and voltage. Subsequently, the integral states vector $\dot{q}(t)$ is derived from (54). $q(t)$ is obtained, through the integration of $\dot{q}(t)$, and in accordance with (59), it is multiplied by the vector K_q. Additionally, based on (59), the vector K_x is multiplied by $x(t)$. The collective outcome of these computations yields the vector $\tilde{u}(t)$ as defined in (59). After being multiplied by vector B and added to vector $Ax(t)$, this vector yields $\dot{x}(t)$ and subsequently $x(t)$. Upon multiplication by vector E, the vector $x(t)$ leads to $y(t)$. All these procedures are illustrated in Figure 10(a). Figures 10(b) and 10(c) depicts the integral state feedback loops for the proposed converter. This system has poles assigned by the matrices K_x and K_q at the desired locations and follows the input references $I_{L,ref}$ and $V_{C_1,ref}$.

The transfer functions of the system, i.e., (61), are obtained and provided in Table 5. Moreover, the related bode diagrams are depicted in Figure 11. According to the data in Figure 11, the gain margin (GM) values for inductor L current and

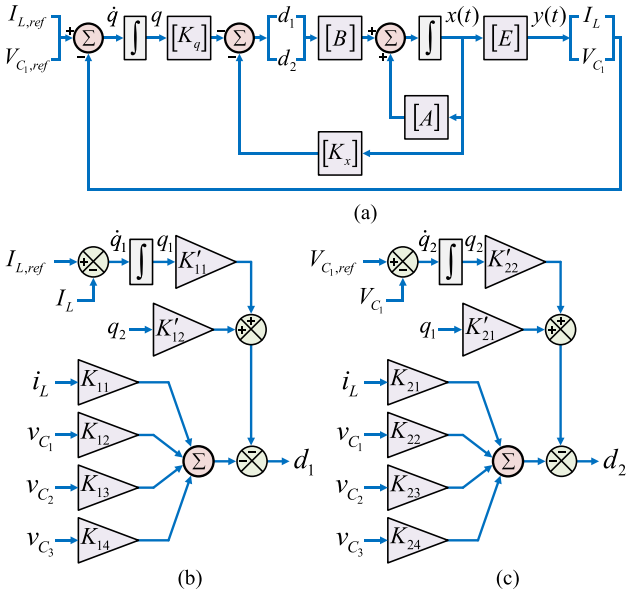


FIGURE 10. Control system of the proposed converter, (a) Block diagram of the pole-placement control method, (b) Regulator loop of the first output (I_L) and (c) Regulator loop of the second output (V_{C1}).

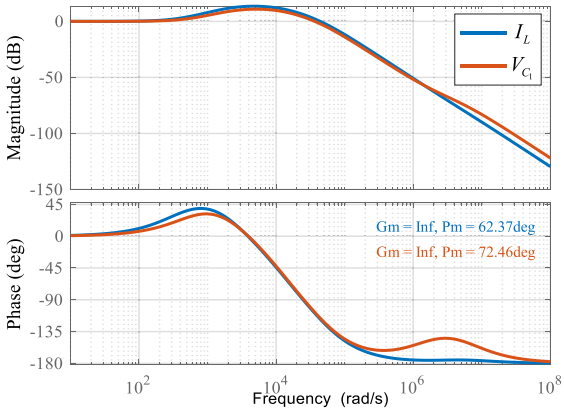


FIGURE 11. Bode diagram of transfer functions $G_1(s)$ and $G_2(s)$.

capacitor C_1 voltage exceed 10 (GM (I_L and V_{C1}) > 10), and the phase margin (PM) of them is 62.3783 and 72.4654, respectively, which are in the desired range (GM ≥ 10 and $60 \leq$ PM ≤ 80). Thus, the closed-loop system is stable and the system poles are located at suitable places.

VII. COMPARISON STUDY

The core purpose behind the proposed topology is the enhancement and modification of A-SL-based converters, targeting the achievement of superior performance while employing the least possible number of components. Therefore, conducting a comparative study is essential to assess the extent of the enhancements achieved. Table 6 lists the characteristics of the PC and other similar structures [29], [36], [37], [44], [45], [47], [48], [49], [50], [51], [53], [54], [55], encompassing parameters such as VG, voltage stress on power switches, total voltage stress exerted on power diodes, and component count.

TABLE 6. Comparison with similar topologies.

Ref.	Voltage Gain	Switches Voltage Stress	Diodes Voltage Stress	Number of S / D	Number of C / L	TDC
[33]	$\frac{3-D^2}{(1-D)^2}$	$S_1,S_2:\frac{1-D}{3-D^2}$ $S_3:\frac{2}{3-D^2}$	$\frac{8-6D}{3-D^2}$	3 3	3 3	12
[36]	$\frac{1+3D}{1-D}$	$S_1:\frac{4}{3(1+3D)}$ $S_2:\frac{1}{1+3D}$ $S_3:\frac{1+D}{1+3D}$ $S_4:\frac{3+5D}{3(1+3D)}$	$\frac{4+D}{1+3D}$	4 5	1 4	14
[37]	$\frac{1+5D}{1-D}$	$S_1,S_2:\frac{1+D}{1+5D}$ $S_3:\frac{1+3D}{1+5D}$	$\frac{6+8D}{1+5D}$	3 12	1 6	22
[44]	$\frac{1+D_1}{1-D_1-D_2}$	$S_1,S_2:\frac{2-D_2}{2(1+D_1)}$ $S_3:1$	$\frac{3-D_1-2D_2}{1+D_1}$	3 2	1 2	8
[45]	$\frac{2}{1-D_1-D_2}$	$S_1,S_2:\frac{1}{2}$ $S_3:1$	$\frac{4-D_1-D_2}{2}$	3 3	2 2	10
[47]	$\frac{1+3D_1-D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{1+D_1-D_2}{1+3D_1-D_2}$ $S_3:1$	$\frac{5-D_1}{1+3D_1-D_2}$	3 8	1 4	16
[48]	$\frac{2-D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{1}{2}$ $S_3:\frac{1+D_1}{2-D_2}$	$\frac{4-D_1-2.5D_2}{2-D_2}$	3 3	2 2	10
[49]	$\frac{3-D_1-2D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{3-D_2}{2(3-D_1-2D_2)}$ $S_3:\frac{1+D_1}{3-D_1-2D_2}$	$\frac{5-D_1-3D_2}{3-D_1-2D_2}$	3 4	3 2	12
[50]	$\frac{3-D_1-D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{1}{3-D_1-D_2}$ $S_3:\frac{2}{3-D_1-D_2}$	$\frac{5-D_1-D_2}{3-D_1-D_2}$	3 4	3 2	12
[51]	$\frac{2(1+D_1)}{1-D_1-D_2}$	$S_1,S_2:\frac{3+D_1-D_2}{8(1+D_1)}$ $S_3:\frac{1}{2}$	$\frac{11+D_1-5D_2}{4(1+D_1)}$	3 4	3 2	12
[53]	$\frac{2}{1-D_1-D_2}$	$S_1,S_2:\frac{1}{2}$ $S_3:1$	$\frac{4-D_1-D_2}{2}$	3 3	2 2	10
[54]	$\frac{3-D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{1}{3}$ $S_3:\frac{2}{3}$ $S_4:\frac{2+D_1}{3-D_2}$	$\frac{18-3D_1-8D_2}{3(3-D_2)}$	4 4	3 3	14
[55]	$\frac{4D_1+2D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{2-D_2}{2(4D_1+2D_2)}$ $S_3:\frac{1+D_1}{4D_1+2D_2}$	$\frac{6-3D_2}{4D_1+2D_2}$	3 3	4 4	14
PC	$\frac{3+D_1-D_2}{1-D_1-D_2}$	$S_1,S_2:\frac{2-D_2}{2(3+D_1-D_2)}$ $S_3:\frac{1+D_1}{3+D_1-D_2}$	$\frac{7-D_1-4D_2}{3+D_1-D_2}$	3 4	3 2	12

Ref: References; PC: Proposed Converter; S: Switch; C: Capacitor; D: Diode; L: Inductor; TDC: Total device count.

In the realm of high step-up converters, the VG stands as the foremost parameter for assessment. The curves illustrating the VG for each topology are depicted in Figure 12(a). It is evident that the PC boasts the highest VG.An optimal converter configuration seeks to minimize components while achieving a high VG. To assess this aspect, the curves depicting VG to the total device count (VG/TDC) for each converter are plotted in Figure 12(b). This visual presentation highlights that the PC outperforms others in VG when accounting for the component count.

Figure 12(c) presents the total voltage stress exerted on the power switches, where it is distinctly observable that the lowest stress is attributed to the PC. The voltage stress experienced by the A-SL cell switches, S_1 and S_2, differs from the stress encountered by the auxiliary switch, S_3. This discrepancy arises due to the positioning of S_3 on the output side of the circuit, which results in it bearing a comparatively higher level of stress. Therefore, the comparative plot of the stress exerted on switches S_1 and S_2 is presented in Figure 12(d), while the corresponding stress plot for S_3 is depicted in Figure 12(e). Figure 12(d) illustrates that the least amount of stress is associated with both [33] and the PC. Nonetheless, it is important to note that the converter mentioned in [33] possesses a reduced VG and lacks the advantages conferred by double-duty cycles. Figure 12(e) reveals that the voltage stress imposed on the auxiliary switch of the other converters is significantly high. For example, in [44], [45], [47], and [53], it equals the output voltage. In contrast, the voltage stress on the PC auxiliary switch is notably low.

Finally, the total voltage stress across the power diodes is compared in Figure 12(f). Four of the twelve converters assessed exhibit lower stress levels, while the remaining nine demonstrate higher stress levels compared to the PC; thus, the PC stress level falls within a favorable and acceptable range.

VIII. EXPERIMENTAL AND SIMULATION RESULTS

To validate the theoretical analysis and viability of the proffered design, an experimental model is assembled and tested in the laboratory. It should boost a 20V input voltage

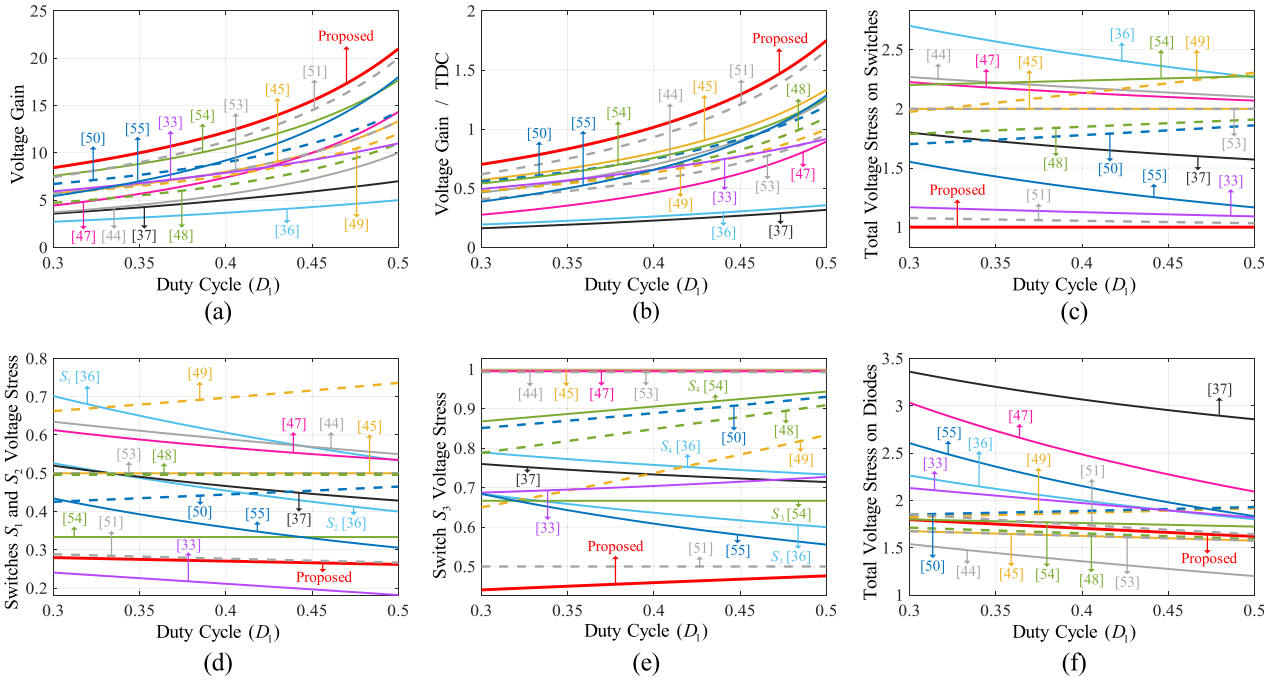


FIGURE 12. Comparison results ($D_2 = 0.35$). (a) Voltage gain as a function of the duty ratio, (b) Voltage gain to total device count, (c) Summation of voltage stress across the switches, (d) Voltage stress of switches S_1 and S_2, (e) Voltage stress of the auxiliary switch and (f) The total voltage stress exerted on diodes.

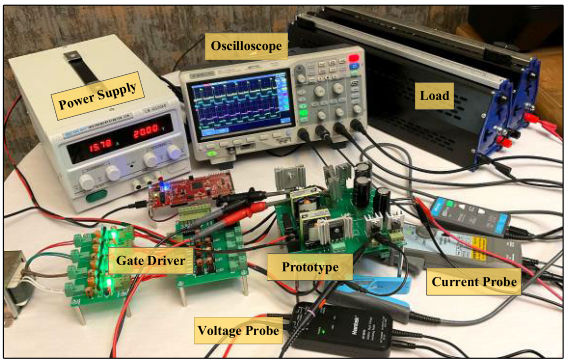


FIGURE 13. Experimental setup.

TABLE 7. Details of the implemented prototype.

Parameter	Value/Description
Rated Power	100-300W
Input Voltage	20V
Output Voltage	400V
Switching Frequency	f_S=25kHz
Inductors L_1 and L_2	L=150μH, r_L=10mΩ
Power Switches S_1 and S_2	IRFP4228PbF, $R_{DS(ON)}$=12mΩ
Power Switch S_3	IRFP4229PbF, $R_{DS(ON)}$=38mΩ
Diode D_1	BYV32E-200
Diodes D_2, D_3, and D_4	SBR10U300CT
Capacitors	100μF

to a 400V output load voltage within the power range of 100-300W. As demonstrated in Figure 7, the output voltage can be adjusted to 400V through different settings of the duty cycles; here, as an example, the duty cycles are selected to be $D_1 = 50\%$ and $D_2 = 35\%$. Employing a microcontroller of the TMS320F28379D model, control pulses with a frequency of 25kHz are generated, and using a gate driver are applied to the MOSFETs in an open-loop control mechanism for obtaining steady-state experimental waveforms. The specifics of the prototype and its individual components are detailed in Table 7, accompanied by a visual depiction of the model within its experimental setting, as portrayed in Figure 13. Figure 14 depicts the waveforms collected from the prototype under a 300W load.

The voltage across the capacitors and output load is provided in Figure 14(a). As is evident, the output voltage stands at 400V, with a VG around 20, underscoring the converter ability to attain a significant VG. Furthermore, it is observable that the voltage across each capacitor approximates half of the output voltage. The voltage and current waveforms of the input switches S_1 and S_2 are shown in Figure 14(b). As is evident, in mode I, they are active and conducting, in mode II, low voltage is exerted on them, culminating in minimal turn-off switching losses. Figure 14(c) depicts the waveforms related to output switch S_3 and diode D_1. Observation reveals that this switch is activated under ZVS conditions, and the diode is subjected to a notably low voltage stress.

The current waveform related to inductors L_1 and L_2 is provided in Figure 14(c). It is obvious that the inductors are charged in operation modes I and II and discharged in mode III. The measured average current through inductors is equal to 10.2A, which is in accordance with the theoretical value calculated from (23). Furthermore, it can be seen that when

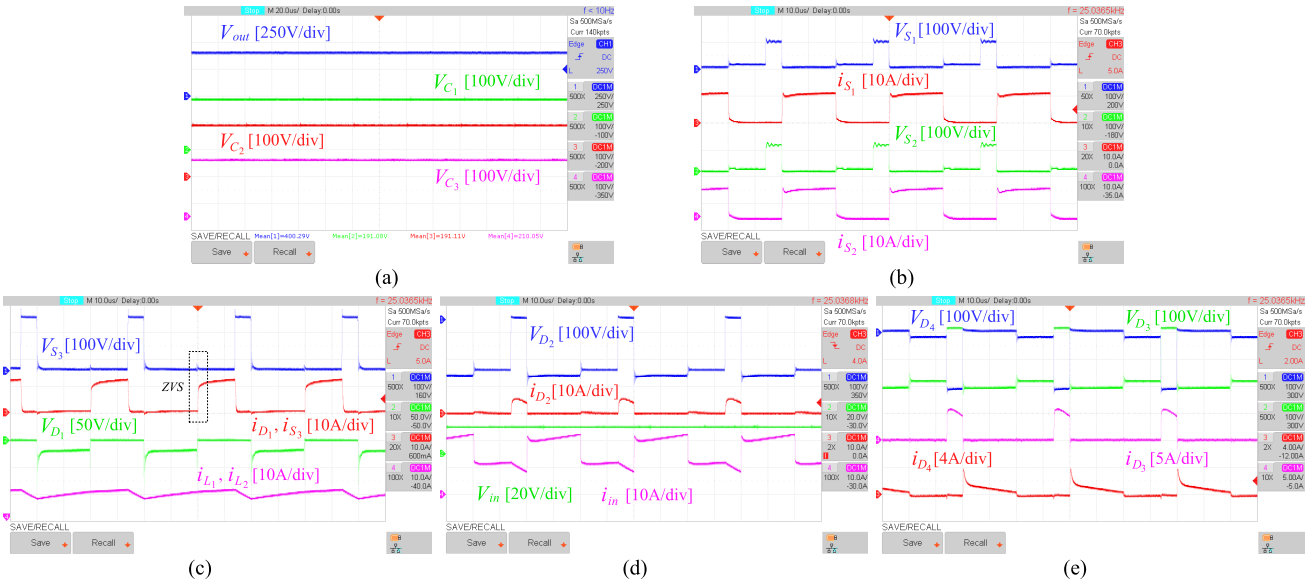


FIGURE 14. Steady-state experimental waveforms of the prototype (P_{out} = 300W), (a) Output load and capacitors C_1, C_2, and C_3 voltage, (b) Voltage and current waveforms of switches S_1 and S_2, (c) Voltage and current waveforms of switch S_3 and diode D_1, along with inductors L_1 and L_2 current,. (d) Input voltage and current along with diode D_2 waveforms and (e) Diodes D_3 and D_4 waveforms.

TABLE 8. Theoretical and experimental values comparison.

Parameters	Theoretical	Experimental
V_{out}	400.6V	400V
V_{C1}=V_{C2}	190.8V	191V
V_{C3}	209.7V	210V
V_{D1}	18.8V	19V
V_{D2}=V_{D3}	209.7V, 190.8V	210V, 190V
V_{D4}	18.8V, 209.7V	19V, 210V
V_{S1}=V_{S2}	9.4V, 104.8V	10V, 106V
V_{S3}	190.8V	192V

the output power is 300W, the inductors current ripple rate is approximately 34%, and the converter operates in CCM. In addition, the input voltage and the current drawn from the source are shown in Figure 14(d).

The voltage and current waveforms of all diodes are provided in Figures 14(c)-14(d), which correspond precisely with the theoretical waveform illustrations presented in Figure 3(a). The maximum voltage subjected to the diodes is about 210V which is considerably lower than the output. Utilizing (45), the theoretical output voltage is determined to be 400.6V; subsequently, the voltage stress on components is ascertained through Table 1. Table 8 juxtaposes these figures against the empirically measured values, thereby corroborating the theoretical analysis.

Figure 15 presents the distribution of losses among the components when operating at 300W, clearly indicating that the principal losses within the showcased circuit originate from the switches, followed by losses associated with the diodes. The predominant portion of the losses experienced by the diodes is related to their forward voltage drop. In Figure 16, the efficiency curve is theoretically plotted using (44), juxtaposed with the experimentally measured efficiency across various output power levels ranging from

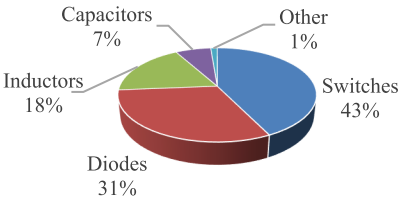


FIGURE 15. Power losses distribution in the PC (300W).

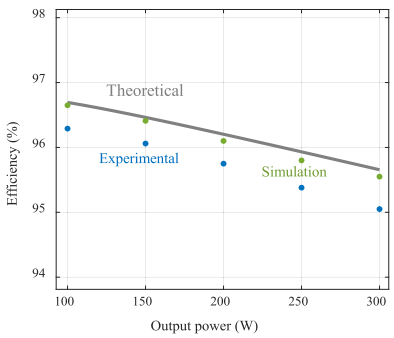
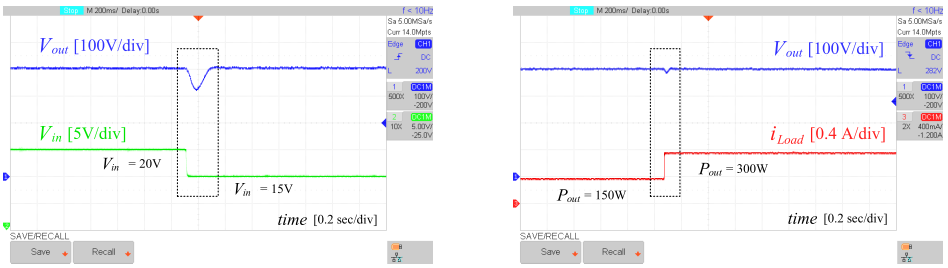


FIGURE 16. Experimental, simulation and theoretical efficiency versus output power.

100W to 300W. As is evident, the efficiency of the converter is higher than 95%.

To assess the system stability and dynamic performance, a step change in the input voltage, specifically from 20V to 15V, is applied to the prototype operating under a closed-loop control scheme. Subsequently, the associated dynamic response is depicted in Figure 17(a). It is manifest that following transient fluctuations lasting approximately 200ms, the output voltage is adeptly regulated to 400V. Furthermore, examining the effect of the load abrupt shift from 150W to 300W, Figure 17(b) displays the corresponding



(a) (b)

FIGURE 17. Dynamic performance of the PC, (a) Response to the input step change and (b) Response to the load step change.

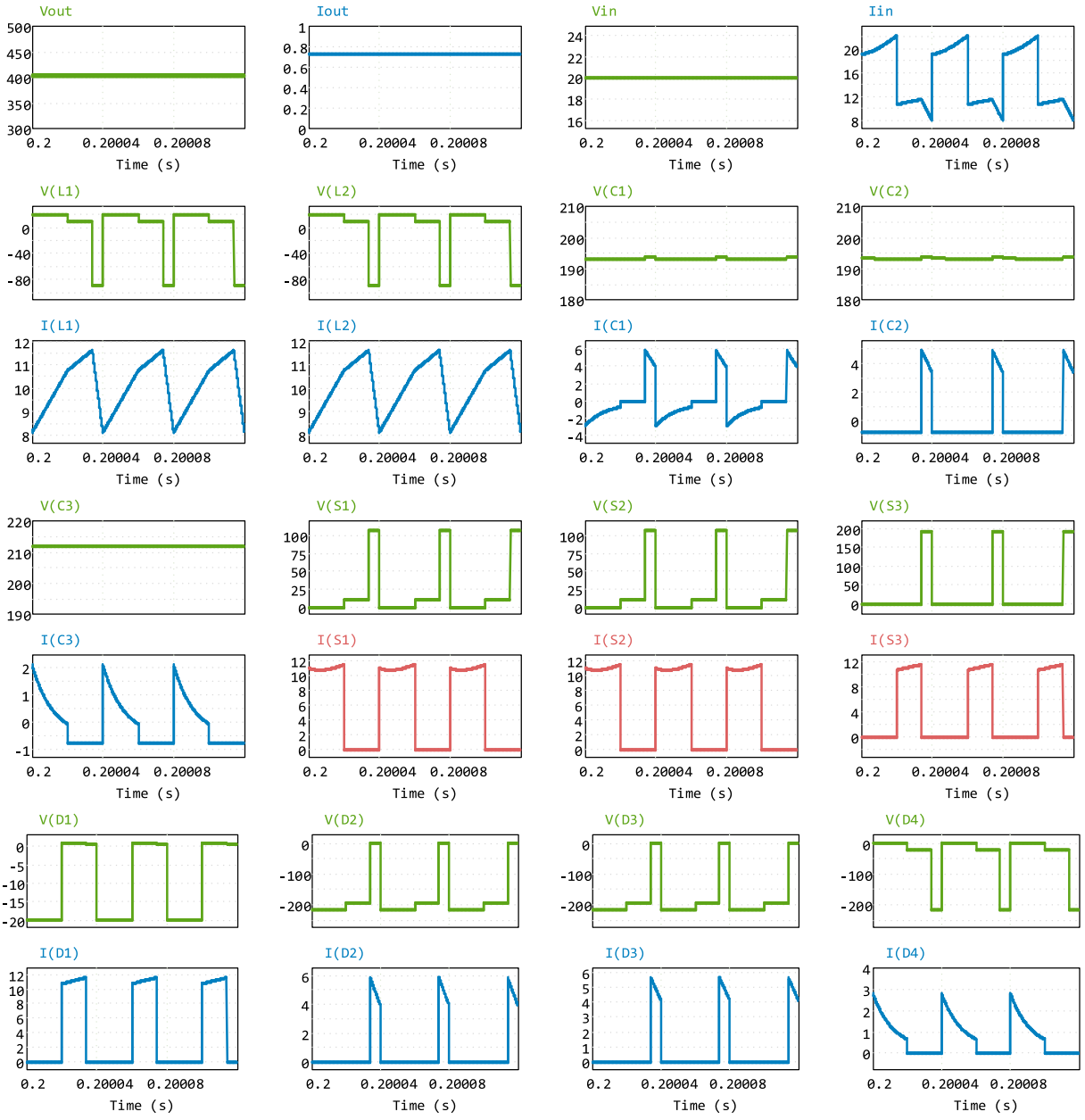


FIGURE 18. Steady-state simulation waveforms of the proposed converter (P_{out} = 300W).

dynamic response. Notably, it demonstrates a swifter adjustment to the target output voltage of 400V, accompanied by diminished transient fluctuations.

Finally, the proposed converter is simulated using PSIM software to complement this study and to clearly illustrate all the waveforms associated with the proposed

converter. The simulation parameters are selected based on Table 7.

A 20V supply is applied, and the load resistance is 547Ω ($P_{out} = 300$W). The duty cycles are chosen to be $D_1 = 50\%$ and $D_2 = 35\%$. The output voltage is 400V. The obtained simulation waveforms are illustrated in Figure 18. Moreover, the efficiency of the simulated model is measured and the results are added to Figure 16. Upon detailed observation and scrutiny of these waveforms, it can be deduced that the results from theoretical analyses, laboratory experiments, and simulations are all congruent and mutually validate each other accuracy.

IX. CONCLUSION

In this paper, a new topology for DC-DC conversion was proposed, characterized by a high voltage gain (VG) capability without reliance on transformers or coupled inductors. This was achieved by effectively integrating an active switched-inductor network with switched capacitors, providing double-duty cycles. The operational principle and the steady-state analysis were provided in detail, followed by design guidelines, efficiency analysis, and small-signal modeling with pole placement control analysis. A 20V to 400V lab-based prototype was implemented and experimented with, to validate the theoretical analysis. It was illustrated that by utilizing the second duty cycle, high VG ($G = 20$) is attainable through the use of low duty cycle values ($D_1 = 50\%$ and $D_2 = 35\%$). Also, the output switch under ZVS conditions and low turn-off switching losses of the input switches were achieved. Furthermore, an additional control variable was added; hence, the converter control mechanism was improved. In a comparative study with other similar topologies, the characteristics of the PC were thoroughly assessed, revealing that the PC exhibits the highest VG and lowest voltage stress of its switches in this category. Low voltage stress exerted on the switches ($V_{S1} = V_{S2} = 105$V and $V_{S3} = 192$V) enables the implementation of low voltage rating MOSFETs with low on-resistance, resulting in improved efficiency. Furthermore, the diodes experience low voltage stress ($V_{D1} = 20$V, $V_{D2} = V_{D3} = V_{D4} = 210$V). Omitting the use of a transformer or coupled inductors in this structure reduced the converter size and weight, eliminated the challenges of leakage inductors, and also streamlined analysis, design, and fabrication. At the power of 300W and the gain of 20, the efficiency was measured to be 95%. Consequently, the proposed converter is suitable for applications requiring high step-up conversion.

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