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RESEARCH ARTICLE

A Wide-Dynamic-Range, DC-Coupled, Time-Based Neural-Recording IC With Optimized CCO Frequency

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ABSTRACT This paper presents a wide-dynamic-range, DC-coupled, time-based neural-recording integrated circuit (IC), which is resilient against stimulation artifacts, for bidirectional neural interfaces. The proposed neural-recording IC based on delta-sigma modulation consists of an input G_m cell, current-controlled oscillator (CCO)-based integrator, phase quantizer, and tri-level current-steering DACs. The feedback current-steering DACs embedded in the current sources of the input G_m cell enable the recording IC to achieve a wide enough dynamic range to directly digitize the neural signals on top of stimulation artifacts while maintaining a moderately high input impedance. Moreover, the free-running frequency of the CCO-based integrator is set to be the optimum frequency of 0.49 times the sampling rate, thereby achieving high loop gain while utilizing inherent clocked averaging (CLA). Designed and post-layout simulated in a 65-nm process, the neural-recording IC achieves an SNDR of 76.3 dB over a signal bandwidth of 10 kHz while consuming low power of 5.04 μW with a sufficiently wide linear input range of 200 mV_{PP}.

INDEX TERMS Bidirectional neural interface, current-controlled oscillator (CCO), closed-loop neuromodulation, linear input range, neural recording, optimization, time-based delta-sigma modulator (DSM), wide dynamic range.

I. INTRODUCTION

Analog front-ends with a wide dynamic range (DR) are one of the essential components of neural-recording integrated circuits (ICs) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10],

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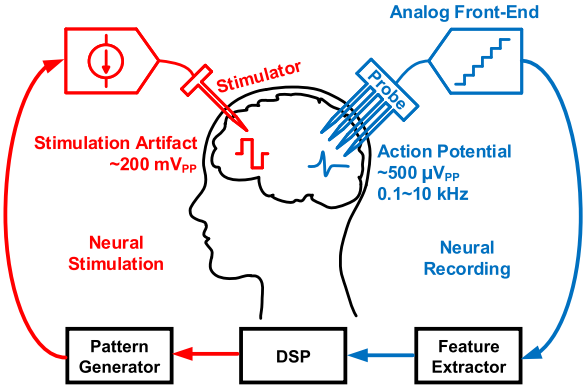

FIGURE 1. Overall block diagram of bidirectional neural interfaces.

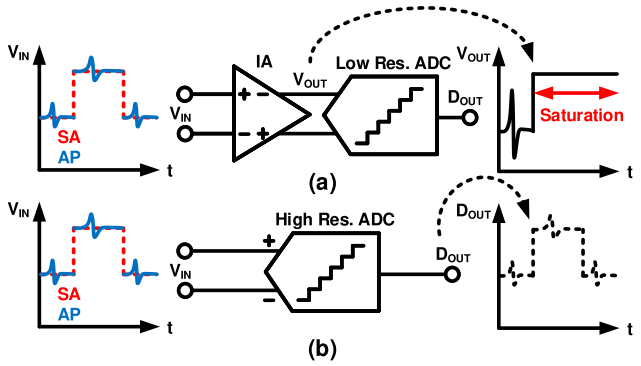

FIGURE 2. Architectures of the neural-recording front-end: (a) conventional architecture using an IA and low-resolution ADC; (b) direct-digitization architecture using a high-resolution ADC.

[11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. As shown in Fig. 1, ICs for bidirectional neural interfaces need to acquire weak neural signals while avoiding the recording channel saturation caused by large stimulation artifacts from stimulation circuits [29], [30], [31]. The magnitude of the stimulation artifacts could reach up to a few hundreds of mV at the input of the recording channel, while action potentials (APs) are recorded as less than 1 mV_{PP}. Such small neural signals on top of the large stimulation artifacts have made the design of neural-recording ICs challenging.

Fig. 2 shows two architectures of neural-recording ICs. The traditional recording IC architecture shown in Fig. 2(a) consists of an instrumentation amplifier (IA) and analog-to-digital converter (ADC) [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], and it can relax the resolution requirement of the following ADC by using a high-gain IA [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51]. In this structure, however, the signal-to-noise and distortion ratio (SNDR) performance can be degraded by the saturation of the IAs when a large stimulation artifact comes to the input of IA. To address this saturation issue by enhancing the DR, the neural-recording ICs with a low-gain IA or an amplifier

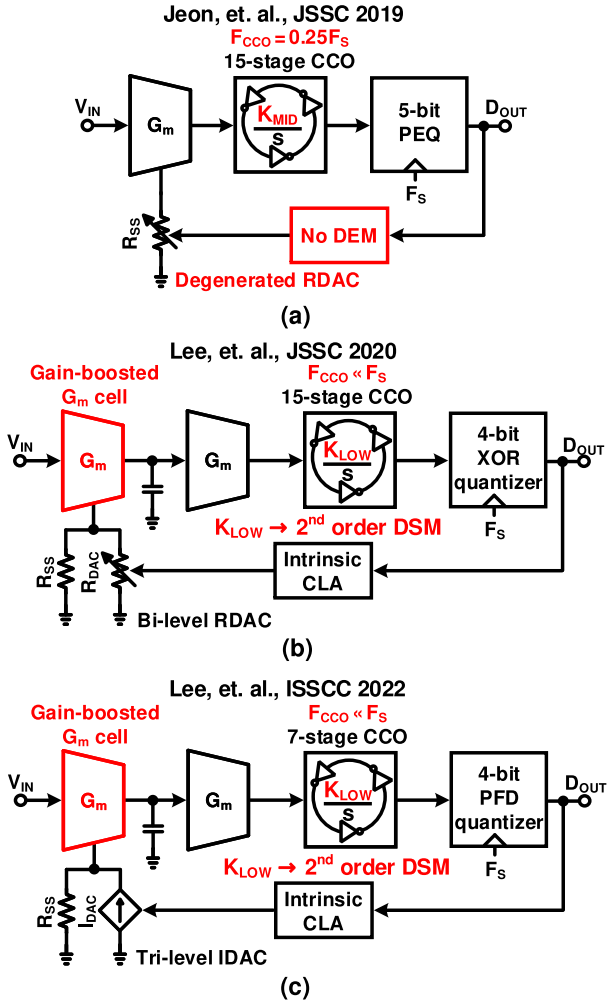

FIGURE 3. Prior DC-coupled, time-based DSMs for neural recording applications: (a) 1st-order DSM with degeneration RDAC, (b) 2nd-order DSM to compensate low K_{CCO}, (c) 2nd-order DSM using PFD quantizer.

stage using an adaptive gain were proposed [52], [53], [54], [55], [56]. However, all of these IA-based recording ICs suffer from low input impedance (Z_{in}) and insufficient DR performance. Capacitively-coupled IA (CCIAs) [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [57], [58], [59], [60], [61], [65], [66], [67], [68] and current-balanced IA (CBIAs) [46], [47], [48], [49], [50], [51] with an input chopper are generally used as the amplification stage, and they cannot offer sufficiently high Z_{in}, resulting in the attenuation of the neural signals, the reduction of common-mode rejection ratio, and more susceptibility to artifacts. Z_{in} can be increased by Z_{in} boosting techniques [52] but at the cost of additional power and area overheads.

Alternatively, many direct digitization architectures have been demonstrated for wider DR and high input impedance (Fig. 2(b)) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. They are composed of only an ADC, which directly digitizes the neural signal. Because the front-end gain stage is removed, the ADC in this topology

should have lower input-referred noise than the ADC of the architecture shown in Fig. 2(a). In addition, the ADC should support a wide input DR of a few hundreds of mV while maintaining a high linearity to acquire small neural signals even under conditions with large artifacts. To satisfy all these requirements, closed-loop architectures with noise-shaping techniques based on delta-sigma-modulators (DSMs) are preferred. While the DSMs for direct digitization enhance DR performance, they are not friendly to process and supply voltage scaling. This is because most of the DSMs used in this structure utilize conventional analog loop filters, such as active RC filters and G_m-C integrators [2], [3], [4], [10], [11], [12], [13], [14], [15], [16].

Recently, time-based quantizers, which use a pair of current-controlled oscillators (CCOs) and D flip-flops (DFFs) as a loop-filter and quantizer, have gained significant attention [6], [7], [8], [9], [17], [18], [25], [69], [70], [71]. Unlike the traditional analog loop filters, the time-based quantizers are favorable under a low supply voltage since the output of the integrator in the closed-loop system is represented not by a voltage amplitude but by its time-domain information [5], [7], [71], [72]. Moreover, the time-based quantizers have inherent dynamic-element-matching (DEM) characteristics, thereby achieving high energy efficiency by eliminating the additional DEM circuit [6], [18], [69], [70], [71], [72].

Thanks to their superior characteristics, time-based quantizers have been used in DC-coupled DSMs for neural-recording ICs, providing a wide DR with moderate Z_{in} [5], [6], [18]. Since these recording ICs with time-based quantizers do not need AC-coupling input capacitors and choppers [5], [6], moderate Z_{in} can be achieved without any additional impedance-boosting technique.

Fig. 3 shows prior DC-coupled time-based DSMs designed to record neural signals. Fig. 3(a) shows a DC-coupled time-based 1st-order DSM using a feedback-controlled resistor digital-to-analog converter (R-DAC). Here, the R-DAC is embedded on the source side of the input G_m cell as its source-degeneration resistor [5]. This structure can improve the DR thanks to the linearized source-degenerated G_m cell and noise shaping by the DSM. Moreover, since the R-DAC is not directly connected to the inputs of the G_m cell, the DC-coupled structure can be used, resulting in a moderately large Z_{in}. However, it cannot utilize the intrinsic clocked-averaging (CLA) property of the CCO-based integrator as the DEM operation because the R-DAC is implemented in the form of series-connected unit resistors. As a result, the bandwidth of the DSM is limited to 200 Hz because of DAC mismatches, and the achieved bandwidth is insufficient to record APs.

To mitigate the performance degradation by DAC mismatches, DC-coupled time-based 2nd-order DSMs shown in Figs. 3(b) and 3(c) have been demonstrated [6], [18]. The 2nd-order DSM in Fig 3(b) uses a G_m cell, and a feedback-controlled R-DAC is connected to the tail current source of the G_m cell in parallel [6]. Here, since the R-DAC consists of

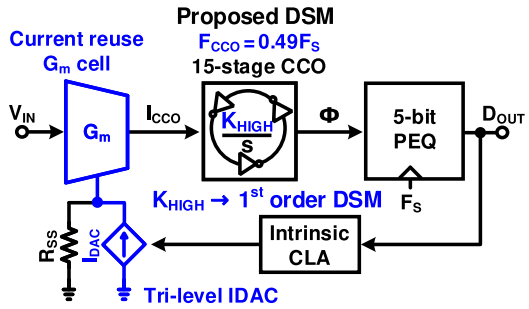

FIGURE 4. Overall block diagram of the proposed 1st-order DSM with high K_{CCO} and low ISI error.

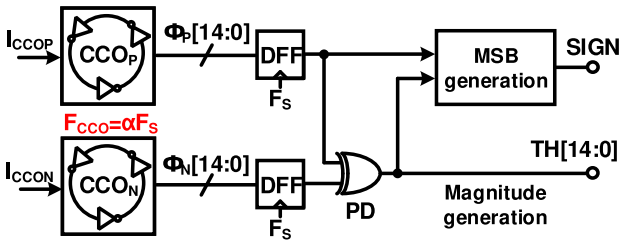

FIGURE 5. Block diagram of the time-based quantizer.

parallelly connected unit resistors, this topology can utilize the intrinsic CLA of CCO, achieving a wider bandwidth compared to the topology in Fig. 3(a). The DSM shown in Fig. 3(c), which is the extended version of Fig. 3(b), newly adopts a phase-frequency detector (PFD) quantizer to reduce the number of the CCO stages compared to that of Fig. 3(b) [18]. In addition, a tri-level current-steering DAC (I-DAC) is adopted instead of the R-DAC to achieve better power and area efficiency [18].

However, the DSMs in Figs. 3(b) and 3(c) use an additional G_m cell to compensate for their small loop gain. The CCOs in Figs. 3(b) and 3(c) have low free-running frequency F_{CCO} to utilize the intrinsic CLA feature [6], [18]. For example, the F_{CCO} of the work presented in [6] is 60 kHz, which is much lower than the sampling frequency F_S of 1.28 MHz. This results in a low gain of the CCO, K_{CCO}, reducing the loop gain of the whole CCO-based DSM. Thus, to compensate for performance degradation by such a small loop gain, the 2nd-order DSM structure and gain-boosting amplifier are required, thus consuming additional power with additional noise by the gain-boosting amplifier. Furthermore, the first integrators shown in Figs. 3(b) and 3(c) operate on the voltage domain rather than the time domain, so the integrators require additional capacitors and enough voltage headroom.

To address these issues, this paper proposes a neural-recording IC based on a DC-coupled time-based 1st-order DSM with an optimum F_{CCO}, which is much higher than those of the prior works. With the optimum F_{CCO}, the CCO achieves a high loop gain without an additional G_m-C integrator and offers a well-known DEM pattern with low ISI errors through its inherent CLA. As a result, the DSM achieves a DR wide enough to record small neural signals on

top of stimulation artifacts while avoiding the use of 2nd-order structure and a power-hungry gain-boosting amplifier.

This article is organized as follows. Sections II and III present the operation and design of the proposed time-based DSM operating with optimum CCO frequency, respectively. Section IV shows the post-layout simulation results of the designed neural-recording IC. Finally, the conclusion is given in Section V.

II. CIRCUIT OPERATION

Fig. 4 shows a simplified single-ended representation of the proposed time-based DSM, which consists of a current-reuse G_m cell, 15-stage CCO, phase-extended quantizer (PEQ), and tri-level I-DAC. The G_m cell converts the input voltage signal, V_{IN}, to a current signal, I_{CCO}, which serves as the input of the CCO. The 15-stage CCO with PEQ works as an integrator and quantizer in the DSM. The output of PEQ controls the feedback tri-level I-DAC. The I-DAC is embedded into the G_m cell to maintain moderately high Z_{in}, constructing a DC-coupled structure. In the proposed work, F_{CCO} is set to be $0.49F_S$ to provide intrinsic CLA with low ISI errors and a high loop gain, thereby achieving high SNDR only with 1st-order modulation.

A. TIME-BASED QUANTIZER

The structure of the time-based quantizer is similar to that of the phase quantizers in [5] and [71]. The time-based quantizer is composed of dual CCOs (CCO_P and CCO_N), DFFs, phase detector (PD), and MSB generation circuit, as shown in Fig. 5. The DFFs sample the output voltages of every stage of the dual CCOs, providing $\Phi_P[14:0]$ and $\Phi_N[14:0]$ to the PD and MSB-generation circuit. The sampling frequency F_S is set to 2.56 MHz. Such a not fast clock speed can be used thanks to the neural-recording application. So, even if the phase difference between the input and clock of DFF is small, output transition times of DFFs can be kept much shorter than $1/F_S$. Then, the XOR PD produces a thermometer code, TH[14:0], from $\Phi_P[14:0]$ and $\Phi_N[14:0]$. Due to the relationship between phase and frequency, the number of ones in TH[14:0] represents the integrated magnitude difference between I_{CCOP} and I_{CCON} ($\Delta I_{CCO} = I_{CCOP} - I_{CCON}$). As an example, consider a time-based quantizer using a three-stage dual CCOs. When ΔI_{CCO} is 0, the outputs of the two CCOs become identical. For example, $\Phi_P[2:0] = \Phi_N[2:0] = 101$. Then, as a result, the PD generates TH[2:0] = 000. On the other hand, when $\Delta I_{CCO} = \Delta I_{LSB}$, $\Phi_P[2:0] = 101$ and $\Phi_N[2:0] = 100$. Then, TH[2:0] is 001. Here ΔI_{LSB} is the minimum detectable current by this quantizer. The number of ones in TH[2:0] proportionally increases with the integrated value of ΔI_{CCO}.

To increase the resolution of the quantizer and DSM, we employ the MSB generation circuit in [5] and [71]. The MSB generation circuit detects the lead/lag status of the phases of the dual CCOs, creating a sign bit for the tri-level I-DAC. It is implemented with simple digital logic gates and detects the transition point (TP) of one CCO and the front edge (FE) of the TH[14:0]. The MSB is generated by conducting an AND operation between the TP and FE and summing the result with a 15-bit OR gate [71]. The detailed operation of the magnitude and MSB generation circuits is described in [5] and [71].

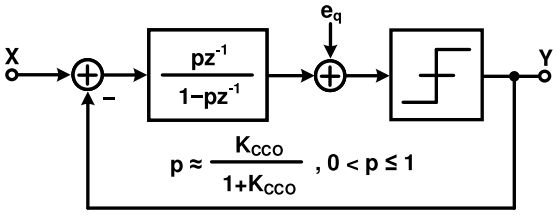

FIGURE 6. Model of the 1st-order DSM for analyses on the effect of the finite DC gain of the CCO-based integrator.

B. THE EFFECTS OF FINITE GAIN OF THE CCO

Fig. 6 shows a z-domain model of the 1st-order DSM [73], and the model is presented to analyze the effect of the finite DC gain of the CCO-based integrator. The noise transfer function (NTF) of 1st-order DSM is expressed as follows:

$$NTF = 1 - pz^{-1}, \tag{1}$$

where $p \approx K_{CCO}/(1+K_{CCO})$. When K_{CCO} is infinite, the magnitude of NTF at DC is zero, thus attenuating the noise at DC. As K_{CCO} decreases, the gain of the NTF at DC increases. Hence, the noise at low frequencies is less attenuated compared to the ideal case. As a result, in the DSM based on the time-based quantizer, it is necessary to obtain as high K_{CCO} as possible.

To design a CCO with high K_{CCO}, we analyze the relationship between F_{CCO} and K_{CCO}. In terms of F_{CCO}, K_{CCO} can be expressed as follows:

$$K_{CCO} = \Delta F_{CCO}/\Delta I_{CCO} \approx F_{CCO}/I_{CCO}, \tag{2}$$

where the first-order approximation is applied for simplicity. For a given I_{CCO}, F_{CCO} should be increased as high as possible to maximize K_{CCO}.

In prior works, the effect of K_{CCO} on SNDR is not significant because of their high F_{CCO} [69], [71]. In high-speed ADCs, where F_S is several hundreds of MHz, F_{CCO} can be designed to be high enough while satisfying $F_{CCO} \ll F_S$ [69], [71]. Here, the inequality of $F_{CCO} \ll F_S$ is one of the requirements for effectively utilizing intrinsic CLA as DEM, which will be explained in the following subsection. In contrast, the F_S of the DSMs designed for neural-recording applications is not higher than several MHz. Hence, it is difficult to obtain high F_{CCO} while satisfying $F_{CCO} \ll F_S$. For example, in a recently proposed 1st-order DSM structure [5], the neural-recording IC adopts the F_{CCO} of $0.25F_S$ to prevent a significant reduction of K_{CCO}. Thus, the recording IC cannot utilize the intrinsic CLA as DEM, degrading the overall SNDR performance. On the other hand, the F_{CCO} of the neural-recording IC in [6] is 60 kHz, which is much lower than the F_S of 1.28 MHz. Hence, this structure can utilize the intrinsic CLA as DEM. However, to mitigate

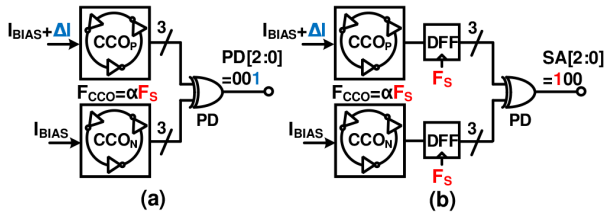

FIGURE 7. Simplified block diagram of the three-stage CCO-based quantizer (a) without and (b) with DFFs.

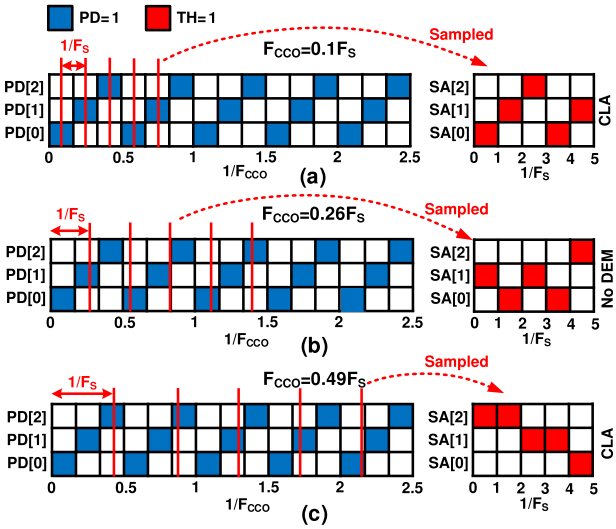

FIGURE 8. Output patterns of the three-stage CCO-based quantizer without DFFs (PD[2:0]) and with DFFs (TH[2:0]) over various F_{CCO}/F_S ratios of (a) 0.1, (b) 0.26, and (c) 0.49.

the performance degradation by low K_{CCO}, a 2nd-order DSM structure should be employed, resulting in additional power and area consumption.

C. INTRINSIC CLOCKED-AVERAGING (CLA)

The outputs of the time-based quantizer in Fig. 5 have intrinsic CLA characteristics. As a result, DEM can be applied to the DSM, up-modulating unwanted tones caused by DAC mismatches without additional circuits [71]. However, since inappropriate output patterns of the DAC cannot perfectly resolve the mismatch issues and may even cause ISI errors, F_{CCO}/F_S, which dominantly decides the output patterns of DAC, should be carefully determined to maximize the SNDR.

For simplicity, Figs. 7(a) and 7(b) show CCO-based quantizers with and without DFFs, respectively, with only three stages instead of the 15 stages used in the proposed work. The structure in Fig. 7(a) is additionally shown to explain the operation of the structure in Fig. 7(b). In Fig. 7(b), the DFFs sample the outputs of the CCOs. Then, the PD receives the sampled output of each CCO and detects the phase difference between them, generating SA[2:0].

Fig. 8 shows PD[2:0] and SA[2:0] according to three different F_{CCO}/F_S ratios. Assume that the CCOs are running at the frequency of F_{CCO} with a constant I_{CCO}. When a minimum detectable current, $\Delta I = \Delta I_{LSB}$, is applied

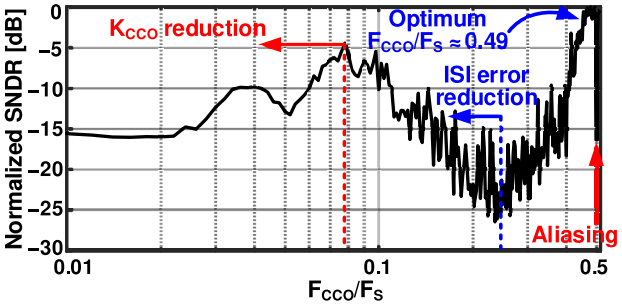

FIGURE 9. Simulated SNDR performance over F_{CCO}/F_S.

to CCO_P, the PD in Fig. 7(a) generates the thermometer code that represents the information of the integrated ΔI_{LSB} by the number of ones, *i.e.*, PD[2:0] = 001. Due to the inherent CLA of the dual-CCO structure, PD[2:0] changes sequentially in the order of 001, 010, and 100, at every $1/(6F_{CCO})$, as shown in the left column of Fig. 8 [69], [71]. Since the same pattern of PD[2:0] is repeated at every $1/(2F_{CCO})$, unwanted tones generated by the DAC mismatches are up-modulated to $2F_{CCO}$, which is generally out of the signal band.

SA[2:0] is equivalent to the sampled value of PD[2:0] at $1/F_S$. Fig. 8(a) shows PD[2:0] and SA[2:0] when $F_{CCO}/F_S = 0.1$. Since F_S is fast enough compared to F_{CCO}, SA[2:0] is similar to the pattern of PD[2:0], providing the intrinsic CLA. On the other hand, when $F_{CCO}/F_S = 0.26$, the pattern of PD[2:0] is not properly sampled to SA[2:0] (Fig. 8(b)) in contrast to Fig. 8(a). In this case, SA[2:0] does not have well-known DEM patterns, so the SNDR performance of the DSM is degraded. When $F_{CCO}/F_S = 0.49$, the time-based quantizer provides intrinsic CLA by sampling the rotation of PD[2:0], as shown in Fig 8(c). Unwanted tones by the DAC mismatches are up-modulated to $F_S - 2F_{CCO}$ since the change with $2F_{CCO}$ is sampled at F_S.

D. OPTIMAL FREE-RUNNING FREQUENCY OF THE CCO

To characterize the effects of F_{CCO}/F_S on the SNDR performance, the SNDR of the 1st-order time-based DSM over F_{CCO}/F_S is provided in Fig. 9. In these simulations, F_S and the signal bandwidth were set to 2 MHz and 10 kHz, respectively. K_{CCO} was assumed to be proportional to F_{CCO}. The mismatches among unit cells of the DAC were set to have a 1% standard variation. We assumed that the ISI errors occur at 0→1 and 1→0 transitions only. For the F_{CCO}/F_S range between 0.01 and 0.078 in Fig. 9, as F_{CCO}/F_S decreases, the SNDR decreases. It is because of the reduced K_{CCO}. On the contrary, for the range of F_{CCO}/F_S between 0.078 (the red dotted line) and 0.24 (the blue dotted line), as F_{CCO}/F_S increases, the SNDR decreases in spite of increased K_{CCO}. This is because the imperfect DEM patterns, which are similar to the SA pattern in Fig. 8(b), cause more ISI errors in the DAC due to large transitions in the DAC output values. As F_{CCO}/F_S increases beyond the value at the blue dotted line, the SNDR increases again thanks to reduced ISI errors and enhanced K_{CCO}. Finally, F_{CCO}/F_S of about 0.49 is the

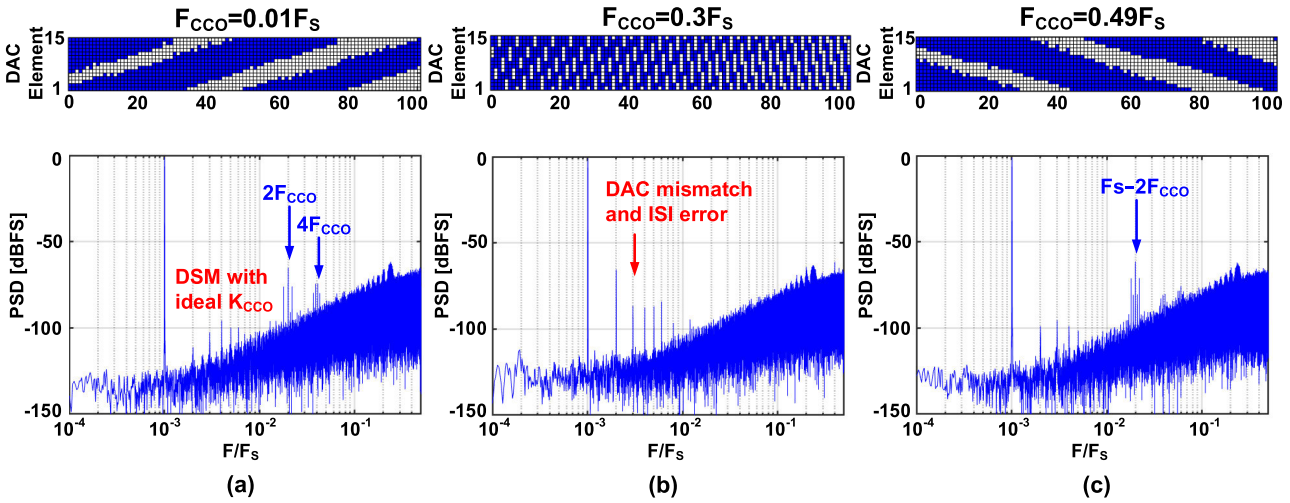

FIGURE 10. Simulated DAC element-selection pattern and power spectral density of the 1st-order time-based DSM when F_{CCO}/F_S is (a) 0.01, (b) 0.3, and (c) 0.49. The integrator built with ideal CCOs was used for the simulations.

optimum point where the transition is minimized and K_{CCO} is high at the same time. As a result, the DSM achieves a high loop gain while avoiding ISI errors. At $F_{CCO}/F_S = 0.5$, the distortions due to the DAC mismatch are folded into the signal band. As a result, the SNDR performance is degraded.

To observe the effects of DAC mismatches and ISI errors on the output power spectral density (PSD), element-selection patterns of the DAC and output PSD for F_{CCO}/F_S of 0.01, 0.3, and 0.49 are presented in Fig. 10. To clearly observe the effects of DAC mismatches and ISI errors, p in Eq. (1) is set to 1, thereby showing ideal noise shaping for all three cases. When $F_{CCO}/F_S = 0.01$, F_S is fast enough to sample the intrinsic CLA of the dual-CCOs, providing the up-conversion of the DAC mismatch errors to the multiplied frequencies of $2F_{CCO}$, as shown in Fig. 10(a). On the other hand, when $F_{CCO}/F_S = 0.3$, as shown in Fig. 10(b), the element-selection pattern of the DAC does not have effective DEM patterns. This is attributed to the misalignment between the rotating speed of the code ones ($2F_{CCO}$) and the sampling rate F_S. Consequently, the third-order harmonics are not attenuated sufficiently. Furthermore, the similar patterns are repeated more often, and errors caused by DAC mismatches are less alleviated. Similar to Fig. 8(b), the unit elements of DAC frequently show large amount of transition in Fig. 10(b), *i.e.,* a 15-bit pattern change from 111111100000000 to 000000011111111. This type of abrupt change in unit elements increases the second-order distortions due to ISI errors [69], [74], [75]. As shown in Fig. 10(c), when $F_{CCO}/F_S = 0.49$, the rotating thermometer codes in the dual-CCOs have a well-known DEM pattern like the pattern in Fig. 10(a). As a result, the element-selection pattern provides proper intrinsic CLA to the DAC with small code transitions per $1/F_S$. In the PSD, the distortions due to the DAC mismatch are clearly up-converted to $F_S - 2F_{CCO}$, thereby improving the SNDR of the DSM. When $F_S >$ 500 kHz, the unwanted tones are up-modulated to beyond 10 kHz, which is higher than the bandwidth of neural signals.

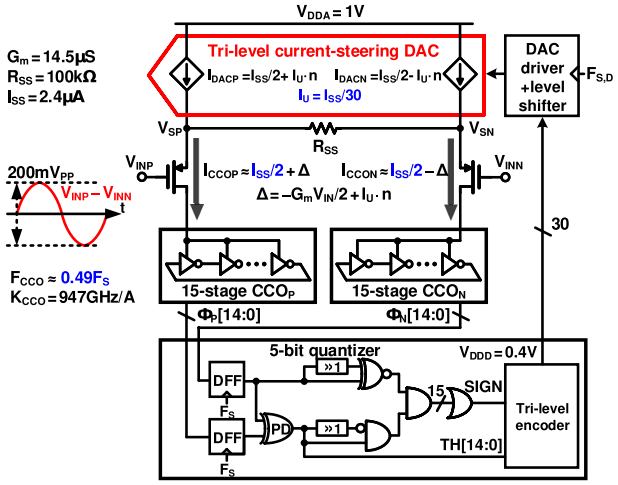

FIGURE 11. Detailed block diagram of the proposed neural-recording IC.

III. CIRCUIT IMPLEMENTATION

A. OVERALL NEURAL RECORDING IC

A detailed block diagram of the proposed neural-recording IC, which is based on the 1st-order DSM, is shown in Fig. 11. To extend the linear input range while keeping the DC-coupled input stage, a tri-level I-DAC is used as a tail current source and gives feedback to the input G_m cell. As shown in Fig. 11, the I-DAC is embedded in the G_m cell, while the I-DAC is not directly connected to the input to maintain its DC-coupled input. The unit current of I-DAC, I_U, is set to be $I_{SS}/30$, where I_{SS} is the total current flowing through the input transistors. The I-DAC divides I_{SS} into two currents, I_{DACP} and I_{DACN}. The ratio between I_{DACP} and I_{DACN} is controlled by the tri-level output codes of the quantizer. When a differential input, $V_{IN} = V_{INP} - V_{INN}$, is applied to the input of the recording IC, the resulting residue current, $\Delta = -G_m V_{IN}/2 + I_U \times n$, flows in the G_m cell, where n represents the magnitude of the 5-bit tri-level I-DAC, n= −15, −14, …, 15. The F_{CCO} is set to be $0.49F_S$

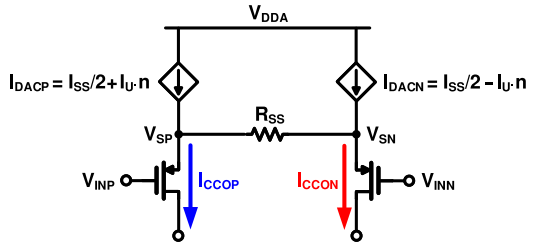

FIGURE 12. Circuit diagram of the proposed G_m cell with embedded tri-level I-DAC.

for maximizing high K_{CCO} and minimizing ISI errors, and the F_S is set to be 2.56 MHz. The analog and digital supply voltages, V_{DDA} and V_{DDD}, are set to be 1 V and 0.4 V, respectively.

B. SMALL-SIGNAL ANALYSIS OF THE PROPOSED G_M CELL

The proposed recording IC employs a current-reuse technique with the tri-level I-DAC to improve noise efficiency and linearity. Fig. 12 shows a circuit diagram of the proposed G_m cell to present the design method and advantages. I_{SS} is one of the main parameters to determine the input voltage range and power consumption, which should be minimized as much as possible while maintaining the target input voltage range. The output currents of input transistors, I_{CCOP} and I_{CCON}, can be derived by the superposition of the currents determined by I_{DACP}, I_{DACN}, and $V_{INP} - V_{INN}$. Hence, I_{CCOP} and I_{CCON} can be expressed as follows:

$$I_{CCOP} = -\frac{1}{\frac{1}{g_m}+\frac{R_{SS}}{2}}\frac{V_{INP}-V_{INN}}{2} + \alpha I_{DACP} + \beta I_{DACN}, \tag{3}$$

$$I_{CCON} = +\frac{1}{\frac{1}{g_m}+\frac{R_{SS}}{2}}\frac{V_{INP}-V_{INN}}{2} + \beta I_{DACP} + \alpha I_{DACN}, \tag{4}$$

where g_m is the transconductance of the two input transistors. Here α and β are expressed as follows:

$$\alpha = \frac{\frac{1}{2g_m}+\frac{R_{SS}}{2}}{\frac{1}{g_m}+\frac{R_{SS}}{2}}, \quad \beta = \frac{\frac{1}{2g_m}}{\frac{1}{g_m}+\frac{R_{SS}}{2}}. \tag{5}$$

Substituting $I_{DACP} = I_{SS}/2 + I_U \times n$ and $I_{DACN} = I_{SS}/2 - I_U \times n$ into Eqs. (3) and (4), I_{CCOP} and I_{CCON} are described as following equations:

$$I_{CCOP} = \frac{I_{SS}}{2} - G_m\frac{V_{IN}}{2} + (\alpha-\beta)I_U n, \tag{6}$$

$$I_{CCON} = \frac{I_{SS}}{2} + G_m\frac{V_{IN}}{2} - (\alpha-\beta)I_U n, \tag{7}$$

where $G_m = 1/(1/g_m + R_{SS}/2)$. The differential output current of the G_m cell, $I_{CCOP} - I_{CCON}$, is expressed as follows:

$$I_{CCOP} - I_{CCON} = -G_m V_{IN} + 2(\alpha-\beta)I_U n. \tag{8}$$

Note that the feedback loop of the DSM forces $I_{CCOP} - I_{CCON}$ to become 0, and $I_U n$ is I_{SS} at the maximum

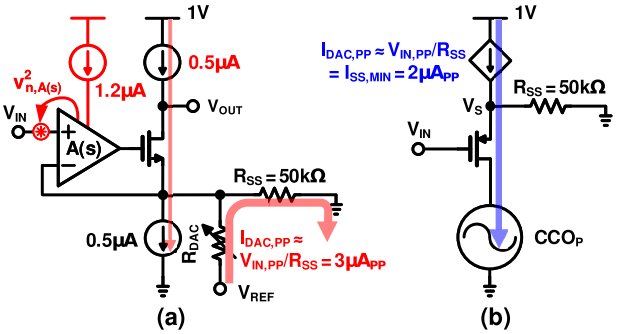

FIGURE 13. Comparison between (a) a prior gain-boosted G_m cell [6] and (b) the proposed current-reuse G_m cell.

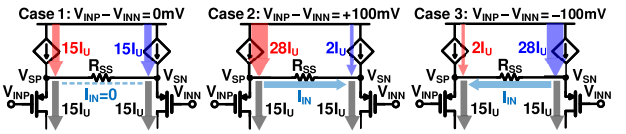

FIGURE 14. Operation of the G_m cell with the tri-level I-DAC.

target V_{IN}, $V_{IN,PP}$. Since $\alpha - \beta = (R_{SS}/2)G_m$ according to Eq. (5), the minimum required I_{SS}, $I_{SS,MIN}$, can be derived as follows:

$$I_{SS,MIN} = \frac{V_{IN,PP}}{R_{SS}}. \tag{9}$$

According to Eq. (9), the minimum I_{SS} can be set to 2 μA when R_{SS} = 100 kΩ and $V_{IN,PP}$ = 200 mV_{PP}. Considering the process variation of R_{SS} and design margin, I_{SS} is set to be 2.4 μA in our design. Meanwhile, Eq. (9) is derived from Eq. (8) regardless of g_m value. Since $I_{SS,MIN}$ remains constant even with small g_m, the proposed G_m cell does not require additional g_m-boosting techniques.

Fig. 13 compares the prior gain-boosted G_m cell [6] and the proposed current-reuse G_m cell. In Fig. 13(a), the R-DAC connected in parallel with the degeneration resistor consumes considerable static current because it has to subtract the large current generated by the input signal, $V_{IN,PP}/R_{SS}$. Under the limited power constraint, the input transistor has to be biased with a small current, such as 0.5 μA, exacerbating the linearity and noise efficiency. To solve this issue, the prior G_m cell in [6] adopts a gain-boosting amplifier at the input. However, this structure degrades the noise efficiency factor (NEF) because of the additional power consumption and the noise of the gain-boosting amplifier. On the other hand, the proposed structure, shown in Fig. 13(b), employs a current reuse technique to address the limitations of the prior G_m cell. While the R-DAC in the prior work dissipates a large current, the proposed G_m cell reuses the current from the I-DAC to bias both input transistors and the CCOs, enabling low noise and high linearity without the gain-boosting technique.

C. OPERATION OF THE G_M CELL WITH I-DAC

Fig. 14 shows the operation of the proposed G_m cell with the I-DAC under three different input conditions. The negative feedback loop forces I_{CCOP} and I_{CCON} to become identical.

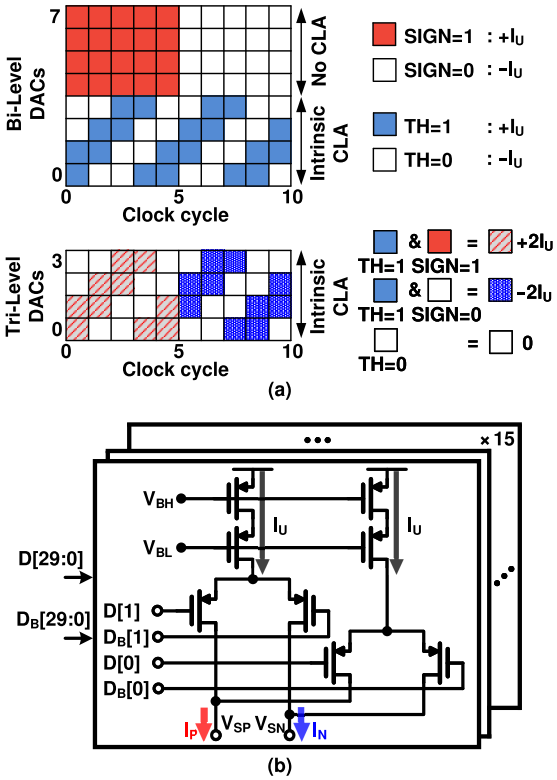

FIGURE 15. (a) Conceptual diagram of DAC element control without tri-level encoding (top) and with tri-level encoding (bottom) (b) schematic of the tri-level I-DAC.

When $V_{INP} - V_{INN} = 0$ mV, I_{DACP} and I_{DACN} draw the same current of $15I_U$. When $V_{INP} - V_{INN} = +100$ mV, V_{SP} increases, and V_{SN} decreases to maintain the same g_m of input transistors. As a result, I_{CCOP} and I_{CCON} are still the same as $15I_U$. The feedback DAC prevents the reduction of I_{CCOP} by increasing I_{DACP} to $28I_U$ and decreasing I_{DACN} to $2I_U$. On the other hand, when $V_{INP} - V_{INN} = -100$ mV, the feedback loop generates $I_{DACP} = 2I_U$ and $I_{DACN} = 28I_U$, ensuring a stable operation at the edge of the linear input range.

Fig. 15(a) shows a conceptual diagram of the DAC element control. It demonstrates the operation of the tri-level encoder and I-DAC, in which '$+4I_U$' is provided to the output during the first five cycles and '$-4I_U$' is provided during the last five cycles. For simplicity, TH[3:0] is assumed. Note that the SIGN bit controls the same number of unit cells with the number of TH bits for the bi-level DAC case. Here, TH bits have intrinsic CLA characteristics. However, SIGN bit does not have the CLA characteristics because the SIGN bit is just a single bit representing the lead and lag status. Therefore, the degradation caused by DAC mismatches cannot be minimized perfectly. On the other hand, the proposed neural-recording IC adopts a tri-level I-DAC with an encoder that applies the intrinsic CLA characteristic to SIGN bit. As shown in the bottom of Fig. 15(a), the SIGN and TH bits are encoded in tri-level manner ($+2I_U$, 0, and $-2I_U$), providing intrinsic CLA characteristics. For the tri-level encoding, the tri-level I-DAC shown in Fig. 15(b) is implemented. The unit cell of tri-level I-DAC consists of two constant current sources, I_U, controlled by two bits. D[29:0] represents the tri-level-encoded thermometer code generated from SIGN and TH[14:0]. Then, the tri-level I-DAC steers the output current depending on D[29:0], resulting in having intrinsic CLA characteristics. Although the tri-level encoder occupies additional area, the overhead is negligible. The encoder is implemented with simple digital logic gates. Each output node of the DACs, V_{SP} and V_{SN}, is connected to the source of the input transistors, providing a feedback-controlled current to the G_m cell.

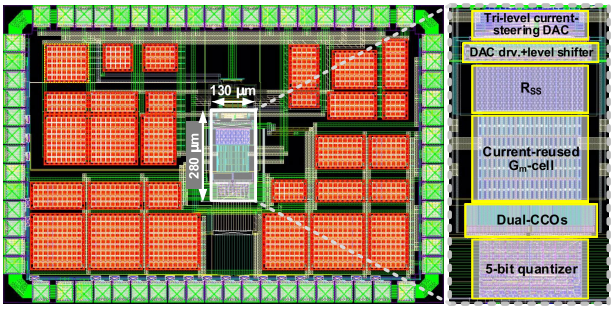

FIGURE 16. Layout of the proposed DC-coupled time-based neural-recording IC with optimized CCO frequency.

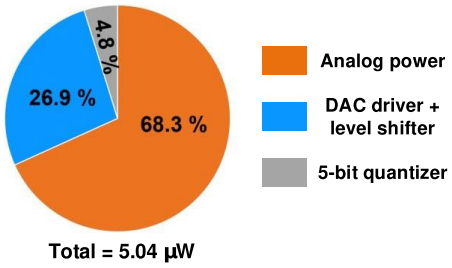

FIGURE 17. Power breakdown of the neural recording IC.

IV. SIMULATION RESULTS AND DISCUSSION

A. POST-LAYOUT SIMULATION RESULTS

In this section, post-layout simulation results of the proposed neural-recording IC are presented. The proposed neural-recording IC is designed in a 65-nm CMOS technology, occupying an active area of 0.0364 mm^2 (Fig. 16). Fig. 17 shows a power breakdown of the designed recording IC. The proposed DSM consumes a low power of 5.04 μW thanks to the proposed current-reuse G_m cell and the 1st-order DSM structure. The output PSD of the recording IC with 2^{14} points and the element-selection pattern of DAC are shown in Fig. 18. The mismatches occurred during the layout process is up-modulated to about F_S–$2F_{CCO}$. In Fig. 19, the SNDR is plotted as a function of the input amplitude. The proposed recording IC achieves a peak SNDR of 76.3 dB when the amplitude of the input sinusoidal signal is 200 mV_{PP}. When the input signal is 500 μV_{PP}, our neural-recording IC achieves SNDR of 25.9 dB. This wide DR allows the IC to record the

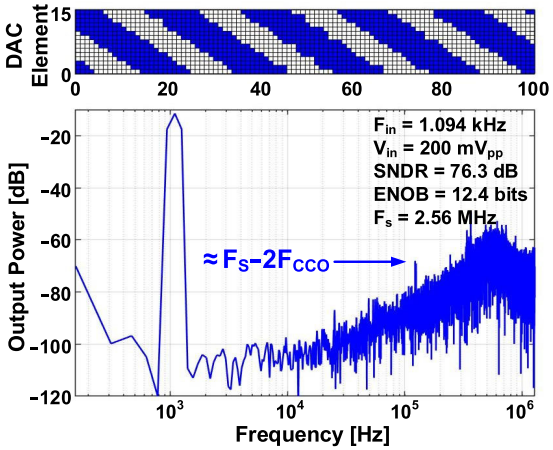

FIGURE 18. Element-selection pattern of the DAC and output spectrum of the proposed neural-recording IC. A high SNDR is achieved even with the 1_{st}-order NTF by setting $F_{CCO} \approx 0.49F_S$.

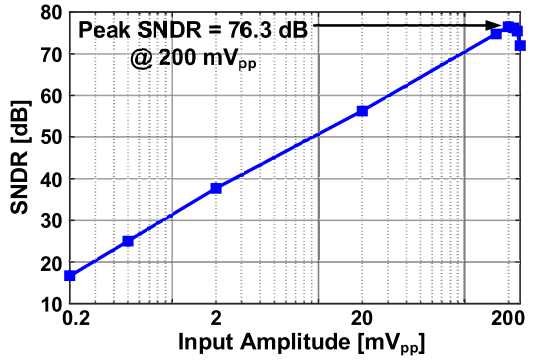

FIGURE 19. SNDR versus the input amplitude.

weak neural signals in the presence of large stimulation artifacts. Although its quantization noise is shaped by the 1st-order characteristics, high SNDR performances are achieved thanks to the large CCO gain (K_{CCO} = 947 GHz/A) at $F_{CCO} \approx 0.49F_S$. Furthermore, the element-selection pattern of DAC shows effective DEM patterns, so the proposed IC would maintain low 2nd-order and 3rd-order harmonics. As shown in Section II-D and Fig. 10, the DAC mismatch tones caused by layout and fabrication mismatches would not degrade SNDR since it is up-modulated far from the signal bandwidth.

In such DC-coupled structures, the offsets of the G_m-cell should be minimized due to lack of the chopper stabilization technique. According to the post-layout Monte-Carlo simulation, 3σ deviation of the input referred DC offset is about 0.66 mV, which is much less than the input linear range of 200 mV_{pp}. Therefore, the input DC offset of G_m-cell does not have a significant effect on recording weak neural signals.

B. PERFORMANCE SUMMARY AND DISCUSSIONS

Table 1 shows a performance summary of the proposed neural-recording IC and state-of-the-art neural-recording ICs employing a time-based quantizer. Thanks to the optimized

TABLE 1. Performance summary of the proposed IC and comparison with state-of-the-art time-based DSMs for neural recording applications.

Parameter	This work[a]	JSSC'19 [5]	JSSC'20 [6]	ISSCC'22 [17]	CICC'24 [28]
Process (nm)	65	180	110	180	180
Area (mm^2)	**0.036**	0.225	0.078	0.108	0.090
NS Order	**1**	1	2	2	2
Power (μW)	**5.0**	3.9	6.5	5.0	11.7[b]
Peak Input (mV_{pp})	200	200	300	560	125
Signal Type	LFP, AP	LFP	LFP, AP	LFP, AP	LFP, AP
BW (Hz)	**10 k**	200	10 k	10 k	10 k
F_s (Hz)	2.56 M	819.2 k	1.28 M	2.56 M	1.28 M
F_{CCO}/F_s (Hz)	**0.48**	0.25	0.047	-	~10
SNDR (dB)	76.3	81.3	80.4	85.1	78.6
SFDR (dB)	86.7	91.2	92.2	97.0	97.7
Z_{in} Boost	**No**	No	No	Yes	Yes
Z_{in}@DC (Ω)	∞	∞	∞	> 421 M	304 M
Z_{in}@BW (Ω)	2.38 M @ 10 kHz (6.7 pF)	160 M @ 200 Hz (5.0 pF)	13.3 M @ 10 kHz (1.2 pF)	147 M @ 10 kHz (0.1 pF)	-
FOM[c] (dB)	169	158	172	178	166[d]

[a]This work is based on post-layout simulation results. [b]Decimator power is excluded.
[c]FOM = SNDR + 10log(BW/Power) [d]Averaged over 12 chips

CCO frequency ($F_{CCO} \approx 0.49F_S$), the presented 1st-order DSM shows comparable SNDR and figure-of-merit performance with recently reported neural-recording ICs based on higher-order DSMs [6], [17], [28]. Moreover, the proposed DSM has the smallest area and the lowest power consumption among neural-recording ICs based on a time-based quantizer thanks to the 1st-order DSM structure, providing high scalability for multi-channel implantable neural recording devices [76].

A prior high-speed DSM in [70] also has the time-based DSM's optimum F_{CCO} of nearly half of F_S to obtain effective DEM characteristics with low ISI errors. However, the high-speed DSM uses the 2nd-order structure and inherently obtains high K_{CCO} under the F_s over 330 MHz, which is too high for neural-signal acquisition applications. In neural-recording applications, the F_S of the DSMs cannot be higher than even several MHz due to power consumption. This low F_S inevitably limits K_{CCO}. Hence, it is very important to find the optimum F_{CCO} that achieves high K_{CCO} while minimizing ISI errors. As shown in Fig. 9, $F_{CCO} = 0.49F_S$ is the singular point that achieves high K_{CCO} and low ISI errors at the same time. As a result, the proposed recording IC can achieve much higher bandwidth compared to the recording IC in [5] based on a 1st-order and time-based DSM structure, thanks to the optimum F_{CCO}. Furthermore, the proposed IC achieves compatible performances with the recording ICs based on 2nd-order DSM structures even with a 1st-order DSM structure, thereby achieving much more reduced area.

Finally, the Z_{in} of the proposed IC is moderately high, but somewhat lower than those of other recording ICs in [5] and [6] that employ a DC-coupled structure. This is attributed to the large size of the input transistors, which are conservatively designed to minimize the flicker noise. Z_{in} of the proposed DSM at 200 Hz and 10 kHz is 119 MΩ and 2.38 MΩ, respectively, estimated by the input gate capacitance (6.7 pF). However, the proposed IC can sufficiently support the

recording of both local field potentials (LFPs) and APs through microelectrode-type probes [77], [78], which have a range of the impedance of 100 – 300 kΩ at 1 kHz. Note that Z_{in} of the proposed work is about 80 times larger [77]. In addition, the high scalability of the proposed IC with its small area allows for decent compatibility with the microelectrode-type probes, in which the number of channels can be increased up to 1024 [78]. Z_{in} of the proposed work can be improved by optimizing the transistor size. As the size of the input transistors decreases, Z_{in} increases inversely, and the flicker noise grows by square root. Using this, the size of the transistor can be further adjusted to the optimum [5].

V. CONCLUSION

A wide-DR neural-recording IC based on DC-coupled time-based 1st-order DSM, which can record small neural signals superposed onto stimulation artifacts, is presented. This work also demonstrates the relation among F_{CCO}/F_S, K_{CCO}, ISI error, and SNDR performance of the 1st-order DSM to find optimum F_{CCO}/F_S. With the optimum $F_{CCO} \approx 0.49F_S$, the CCO achieves a high loop gain without an additional G_m-C integrator and offers a well-known DEM pattern with low ISI errors through inherent CLA. As a result, the proposed IC achieves a 200-mV_{PP} linear input range and 76.3-dB SNDR at 10-kHz signal BW while consuming low power of 5.04 μW with 1st-order DSM structure, resulting in comparable performance and smaller area than prior neural-recording ICs based on the 2nd-order DSM.

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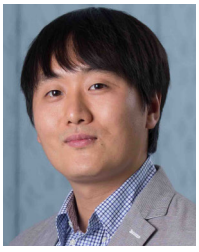

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