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RESEARCH ARTICLE

High-Precision Mapping and Analysis of Wafer-Scale Distortions in InP Membranes to Si 3D Integration

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ABSTRACT Heterogeneous integration helps to maximize the performance of photonics or electronics devices by leveraging the strengths of diverse material platforms within a unified process flow. A promising approach is the 3D integration of InP photonic or electronic membranes to other substrate materials containing photonics or electronics ICs via adhesive bonding. However, wafer-scale spatial distortions arising from the bonding process can compromise fabrication. Herein, we used electron-beam metrology to investigate the distortion of InP membranes resulting from wafer-scale bonding with benzocyclobutene (BCB). We measured both the linear and residual components of distortions across the tested wafers. First, bonding of InP substrate with BCB on various carrier substrates (Si, InP, SiC, and glass) was realized, which unveiled post-bonding membrane expansion factors in the range of ~0-325 ppm and beyond that for the glass carrier. The diversion of these values from theoretical estimations was linked to the adhesive bonding process. Next, we examined the effect of BCB thickness in the ranges of 1-12μm, residual mechanical stress, and the impact of defects on distortions. Using these findings, we experimentally verified that the largest part of distortions can be efficiently pre-compensated to overcome the challenges of multilayer overlay errors in the fabrication of heterogeneously integrated photonic and electronic devices.

INDEX TERMS Adhesive bonding, metrology, 3D integration, overlay lithography, electronics-photonics integration.

I. INTRODUCTION

Photonic integration is a rapidly evolving field, which has the potential to revolutionize a multitude of applications, ranging from telecommunications to quantum computing. In the past years, multiple material platforms were introduced for the fabrication of photonic integrated circuits, such as Si photonics, InP photonics, SiN_x photonics, etc. Each of them has their key advantages in a narrow range of applications. A growing trend is heterogeneous integration, which harnesses the best features of different platforms and unites devices from different materials in a single assembly on a chip scale or full wafer scale. The scope of heterogeneous integration covers a wide range of applications, including ultra-low linewidth lasers [1], optical comb generation, optical phase arrays [2], and integrated circuits for low-loss optical transceivers [3]. Another promising application is the 3D co-integration of III-V membrane-based optical

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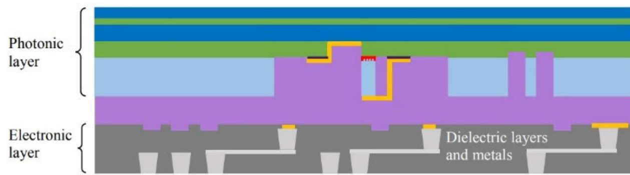


FIGURE 1. Schematic image of InP photonics and CMOS electronics co-integration [4].

transceivers onto complementary metal-oxide semiconductor (CMOS) or InP-based high-speed electronics. This approach can enable parasitic-free interconnects between photonics and electronic circuits, using lithography-enabled precision and density, at wafer scale [4], [5]. In Fig.1, a schematic image of Si electronics co-integrated with InP membrane photonics layer is shown. Most importantly, for all of these integration approaches, a key part of the process is the bonding of devices fabricated on two or more different platforms together. This can be achieved by direct bonding [6] or adhesive bonding [7]. Adhesive bonding has advantages for heterogeneous integration as it offers high flexibility in the choice of the bonding layer thickness (10s of nm – 10s of um), low requirements on wafer topology, and easy wafer-scale processing [8].

The introduction of the bonding process in the fabrication of heterogeneously integrated devices has opened new possibilities for integration but has also introduced new challenges. One such challenge is the precise alignment of bonded substrates for overlay lithography [9], [10], [11]. While alignment algorithms have advanced in sophistication, the precision of alignment is now confronted by physical mechanisms inherent to the fabrication process, such as wafer warping [12], complex surface topology, or layer dislocations resulting from bonding [13]. These phenomena might be caused by several factors, including non-uniformity of temperature distribution during layer formation, non-uniformity of bonding layer thickness, or mismatched coefficients of thermal expansion between different materials [14], [15]. This last factor is inherent to adhesive bonding using BCB, since to cure the BCB, both wafers have to be heated to high temperatures (above 200 °C). For direct bonding using plasma-activated oxides, the situation (i.e., bond temperature) is very similar.

Apart from resulting in mechanical damage to devices when the amount of stress is too high, these distortions also manifest as shifts in the positions of markers during overlay lithography (run-out of overlay error, ROE), e.g., in a DUV scanner lithography tool or mask aligner tool. The distortions that cause ROE contain both linear and non-linear components, as well as residual components that do not fall into the aforementioned categories [16]. While most wafer-scale alignment algorithms can mitigate the linear and non-linear distortions if these are accurately assessed, the residual distortion part remains, leading to poor alignment and subsequently compromised device performance or even wafer rejection by a particular lithography system [17]. In particular, it becomes a challenge to perform the global alignment for overlay lithography before and after bonding due to these membrane distortions [18], [19]. Hence, it is important to investigate the source of these distortions and quantify them to successfully select the right overlay strategies and guarantee high overlay accuracy when needed.

This paper aims to provide a quantitative analysis of distortions in indium phosphide (InP) membranes bonded with Benzocyclobutene (BCB) under different conditions. We define distortion as a physical shift of a point on the membrane surface relative to its position prior to some processing operation, such as before and after bonding, in a predefined frame of reference. The distortion in a particular wafer region is quantified as a vector value. To fully evaluate these distortions, we used a least-square estimation method to decouple the linear components of distortion in the form of stretching and non-orthogonality from residual distortions which we plot as vector maps across the 3-inch wafer area, while non-linear distortions are not examined. Experimentally, Electron Beam Lithography (EBL) tool is used for marker fabrication and metrology, the displacement of markers after bonding is extracted from the EBL log files, and fitted using a 6-parameter model where both linear and residual components are extracted [18], [20].

The paper has the following structure. In section II we describe the fitting model that we use to quantify the linear distortions and extract residual distortion maps from the raw data. In section III, we give an overview of the EBL metrology method. In section IV, we provide a detailed analysis of data obtained from several experiments. In our first set of experiments, we used Si, InP, 3C-SiC, and Glass as carrier substrates to bond with the InP membrane. This allowed us to explore how the membrane distortions are affected by a wide range of coefficients of thermal expansion (CTE) mismatch between InP and these carriers, as the bonding is carried out at temperatures above 200°C. The same experiment was carried out to compare different BCB thicknesses in a wide range of 1-12 um for the case of bonding InP to Si substrate. We also bond an InP wafer with pre-bonding defects and analyze how the presence of those affects both linear and residual distortions. In addition, we demonstrate the presence of residual stress in the membrane, which is the stress left after high-temperature processing is finished and one of the substrates is removed. This is realized by etching trenches that separate the 3-inch membrane into smaller areas, and then analyzing the membrane distortions introduced after the etching step. Finally, we propose an alignment strategy that can handle these distortions to achieve high overlay accuracy. In section V, we summarize and conclude the obtained results.

II. DESCRIPTION OF THE FITTING MODEL

Overlay lithography distortion patterns represent the displacement of markers from their anticipated positions. These patterns contain both linear and non-linear distortions,

as well as residual distortions. In short, linear and non-linear components describe this displacement with linear and non-linear parameters, respectively, while the errors that remain after removing these components from the original distortion pattern are referred to as residual distortions [16]. Hence, it is important to decouple these components and study the main underlying physics that affect them. The goal is to understand the magnitude of these distortions for better overlay compensation on one hand and to improve the fabrication process to limit them on the other. We note that we do not study non-linear distortions in this paper. We will show throughout the paper that linear distortions are dominant while residual maps might contain non-linearities that are not significant. Hence, the accurate fitting of the linear distortion parameters and assessment of residual distortion maps is sufficient to encompass membrane distortion and link it to the bonding process.

To decouple wafer-scale linear distortions and extract the residual distortions of the studied samples in this paper, we used a six-parameter least-square estimation method to fit our data according to the following equations [16]:

$$x_{opt} = x.cos\,(P_1) - y.sin\,(P_1) + P_2 + x.(1 + P_4) + y.tan(P_6) \quad (1)$$

$$y_{opt} = x.sin\,(P_1) + y.cos\,(P_1) + P_3 + y.\,(1 + P_5) + x.tan(P_6) \quad (2)$$

Here, P_1 is the rotation in radian. P_2 and P_3 are the shifts (translation) in x- and y-directions in μm, respectively. P_4 and P_5 are the scaling factors in parts-per-million (ppm) in x- and y-directions, respectively. Negative values of P_4 and P_5 point to membrane compression, while positive values point to expansion. P_6 is the non-orthogonality factor in radian. Here, the input marker coordinates (x,y) are fitted to design coordinates (x_0, y_0) and the result of the fitting is the marker coordinates (x_{opt}, y_{opt}) that contain all the linear components of the overall distortion. Markers displacement represented by distortion patterns that result from several linear components are shown in Fig.2. It should be noted that distortion patterns are typically in the order of a few micrometers/nanometers compared to the 3-inch wafer scale, which necessitates expanding them by orders of magnitude to make them visible. Their magnitude can be assessed by comparison with the scale arrows.

Next, by subtracting the fitted output coordinates (x_{opt}, y_{opt}) from the original input coordinates (x,y), the residual distortion pattern is extracted. Throughout this study, we use the standard deviation (STDev) in nm of errors arising from residual components to assess the quality of the fitting, since we fit linear components while the residual components remain as a source of error. Thus, minimization of the STDev is necessary to ensure that the linear and residual distortion components are fully decoupled. To achieve the best fitting results, several minimization algorithms were tested. We found that the lowest errors can be reached with two algorithms that are suitable for multi-parameter fitting. These

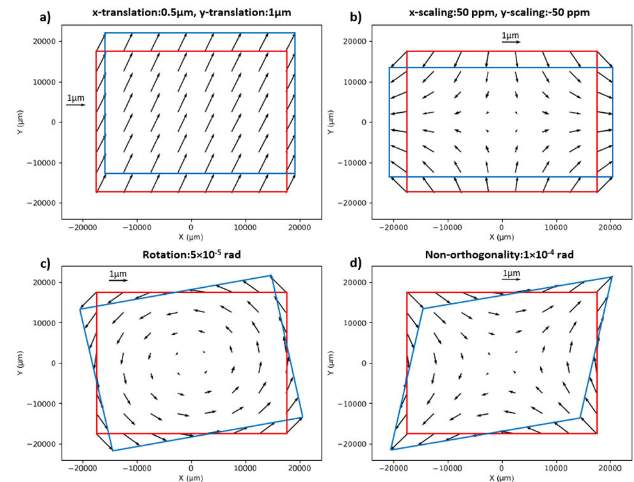


FIGURE 2. Effect of decomposed linear distortions on the displacement of markers.

are the quasi-Newton method of Broyden, Fletcher, Goldfarb, and Shanno (BFGS) [21] and the trust-region (trust-constr) method [21], [22]. Despite that these methods are based on a different rationale for optimization, the obtained values for P_1- P_5 are all similar and within 5% deviation, while the values of P_6 are close to 0. However, we continue with BGFS in this study as it is faster. Moreover, given that overlay systems working on the wafer scale can only compensate for the fitted distortions, the STDev values from residual distortions are representative of the achievable minimum overlay error if all linear distortions are eliminated [16].

Among the linear components P_1-P_6, the translation weakly interacts with scaling and the rotation weakly interacts with non-orthogonality if the center coordinate of the distortion pattern is not determined precisely. This signifies that careful optimization of the fitting is required to ensure accurate extraction of P_1-P_6 values [16]. In practice, to achieve optimal fitting results of P_1-P_6, we first use a null initial guess for all parameters, and the parameters optimization is bounded with a range that is two orders of magnitude larger than what is physically possible. Next, we feed the model with the optimal translation and rotation values within a lower range to exactly pinpoint the center coordinate and ensure that P_1-P_6 are fully decoupled. After registering the fitted optimal values of P_1-P_6 and the STDev of residual errors in nm, the residual distortions are extracted by subtracting the fitted output coordinates from the original input coordinates. To simplify our terminology, the resulting maps are referred to in this paper as *distortion maps*, which represent the distortion part that cannot be fitted. Throughout this paper, only residual distortion maps are shown since the full understanding of linear distortions is captured with the optimal values of P_1-P_6. Moreover, since the parameters (P_1- P_3), *i.e.*, x- and y-translation and substrate rotation, depend on the initial positioning of the substrate relative to the stage [18], these do not contribute to the physical distortion of

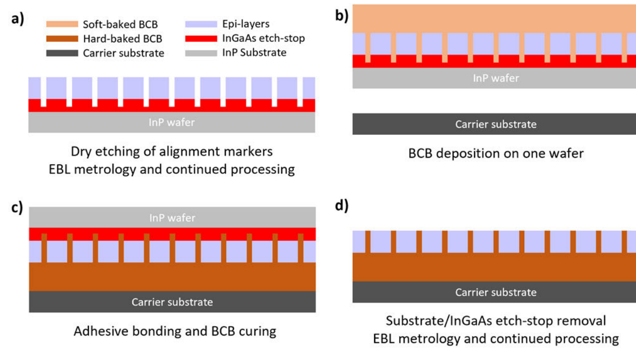


FIGURE 3. Simplified process flow steps relevant to this study, a): marker fabrication, b) substrates preparation for bonding, c): Adhesive bonding, d): InP substrate and etch-stop layer removal.

the membrane and their results are omitted from this paper. However, we note that their fitted values are very close to the values registered in EBL metrology logs. Accounting for the EBL errors presented in supplementary materials (section VI), the error range of P_4-P_5 is 2ppm and 6ppm and the range for P_6 is 4×10^{-6}rad and 1×10^{-5}rad for results obtained from dedicated fabrication runs and photonic device fabrication runs, respectively. The reason for the higher metrology errors from the latter is the lower frequency of EBL recalibration, which slightly increases the effect of drift. Finally, we note that as long as marker fabrication and reading are possible, this method is applicable to study processing-induced distortions of other membrane materials and systems, and other substrate sizes/dies as well.

III. E-BEAM METROLOGY METHOD

Here we discuss the process flow for our e-beam metrology on adhesively bonded membranes. This study encompasses fabrication runs made specifically for this study employing a standard epi-stack and process flow, which are labeled as *dedicated* runs. We also used results from functional photonic device fabrication runs. Bonding is a single step within multiple steps required to fabricate functional devices. So the main goal of using the other runs is to assess the fitting model on complex fabrication schemes, and to verify that the bonding parameters that affect membrane distortion also extend to photonic fabrication schemes. To simplify the fabrication flow, we only detail the common steps between dedicated and functional photonics runs while other steps are described in general. A simplified process flow is shown in Fig.3. For dedicated runs the standard epi-stack consists of 300 nm InP and 300 nm InGaAs etch-stop layer, yielding a membrane thickness of 300 nm after bonding and subsequent removal of InP substrate and InGaAs etch-stop. For functional photonics fabrication runs, the stack thickness can vary between 300 to 1500 nm of III-V semiconductor multi-layers depending on their functionality. Their final fab-out membrane thickness is usually close to these thicknesses since most of the semiconductor materials remain after fabrication. We note that the markers used in both dedicated and functional photonics runs as *negative* markers since they yield lower beam intensity than their surroundings during e-beam reading. However, we also describe the flow for fabricating *positive* gold markers, which are used in one experiment to study the relationship between InP membrane stress and distortion. For the carrier substrates' choice, we required a sufficiently wide range of CTE mismatch between the InP membrane and carrier substrate. Hence, the chosen substrates are: InP with identical CTE to the InP membrane of 4.75×10^{-6}/°C [23], Si and 3C-SiC with CTEs of 2.55×10^{-6}/°C [24] and 2.77×10^{-6}/°C [25], respectively, and finally glass substrate with a low CTE of 4.8×10^{-7}/°C [26].

The fabrication starts with creating markers where we deposit 50 nm of plasma-enhanced chemical vapor deposition (PECVD) SiNx as hard mask for dry etching. The mask is coated with ZEP520A resist and patterned with EBL. The nitride is then dry etched in pure CHF_3 RIE plasma. Next, we deeply etch into the epi-layers using CH_4/H_2 ICP RIE plasma until the InGaAs etch-stop is shallowly etched to guarantee visible markers after bonding. Similarly, the experiment with positive markers only differs in the marker fabrication stage where we use a lift-off process of 50/100/50 nm Ti/Au/Ti stack. Ti is used for optimal adhesion to the BCB and the substrate. Next, we read these markers in EBL to obtain the pre-bond analysis data (Fig.3.a). For functional photonics wafer runs, other pre-bonding device fabrication processes follow at this stage, which include metal deposition and rapid thermal annealing, semiconductor dry and wet etching, and permanent oxide deposition. These processes mainly affect the topography and residual stress of the InP wafer to be bonded, which can yield different results compared to the dedicated runs. Next, we prepare for bonding by depositing PECVD SiO_2 on both the InP wafer and the carrier substrate and follow it by spin-coating AP3000 and baking it at 135°C to promote adhesion. We subsequently spin-coat BCB on the InP wafer and soft-bake it at 100°C, which achieves a flat top surface (Fig.3.b). The latter can require BCB thicknesses up to a few tens of μm if the initial device topography is high [27]. Therefore, the investigated thicknesses are 1μm, 2μm, and 12μm. The corresponding BCB to these thicknesses are Cyclotene 3022–35, −46, and −63, respectively. We note that unless otherwise specified the default thickness is 2μm since it is the most often used for functional photonics membranes, and in other platforms as well [19].

Next, we align the wafers by their major flats in a commercial EVG620 aligner and lock them into a cassette holder, which is transferred to EVG520 bonding tool. For bonding, we use a force of 700N under vacuum and a low ramp rate of 5°C/min until 280°C is reached and stabilized for 1hr to fully cross-link the BCB material (Fig.3.c). During bonding, the temperature uniformity is high since the top and bottom parts of the bonder are controlled separately within 0.1°C difference. After bonding, the InP substrate and InGaAs etch-stop layer are wet etched in HCl:H_2O and H_2SO_4:H_3PO_4:H_2O, respectively (Fig.3.d). For InP carrier substrates, we use protective multi-layer coatings to preserve

the carrier substrate during wet etching and then remove these coatings afterward [28]. The precise coordinates of the markers are then read out using EBL to assess the effect of bonding on membrane distortion. Moreover, although the thickness non-uniformity of BCB before bonding is below 5%, the latter can increase drastically after bonding because BCB becomes liquid and can reflow during bonding [10]. Hence, reflectometry was used to extract the post-bonding BCB thickness non-uniformity maps for further analysis.

The EBL we used is Raith EBPG5150. Before lithography or metrology, the sample is placed onto a 3" holder that secures it against three pins from the top surface by clamping it from the backside with a spring mechanism. The locations of the 3 pins are shown in supplementary materials. This EBL fixing mechanism differs from other lithography tools that secure the sample to the holder with vacuum and fully flatten it. After loading the holder into the loadlock and reaching $\sim 10^{-7}$ mbar of vacuum, the holder is transferred to the EBL chamber where lithography (marker fabrication) or metrology (marker reading) is carried out. The system is configured to recognize square 20×20 μm^2 markers. The markers are distributed across the full 3" wafer area in all experiments. To investigate the influence of mapping resolution on the accuracy of analysis, the dedicated runs contain maps of markers with three uniform pitch selections in the (x,y) directions. Note that the x- and y-directions are perpendicular and parallel to the major wafer flat, respectively. The pitches in (x,y) coordinates are 5×5 mm^2 labeled as *coarse* maps that contain $\sim$100 markers, 2.5×2.5 mm^2 labeled as *fine* maps containing $\sim$600 markers, and 1.25×1.25 mm^2 labeled as *ultra-fine* maps containing $\sim$1800 markers. Wafers from photonic device runs use a pitch of $\sim 6 \times 8 mm^2$ with a similar resolution to the coarse maps. To choose optimal beam parameters for our study, we investigated the influence of those on the markers reading/writing accuracy and repeatability using a bare 3" wafer. The goal is to measure systematic errors to ensure the accuracy of results in the following sections. The main EBL systematic errors arise from beam drift and current used during marker lithography/metrology [29]. Therefore, we investigated beam currents in a large range of 5-190 nA. Evaluation of the EBL metrology accuracy shows that using smaller beams (low beam current) and averaging the data from several readings of the same marker slightly increases the accuracy of results. More details can be found in supplementary materials. Based on this, we chose the optimal beam currents of 100 nA for lithography and 5nA for metrology for dedicated runs, while functional photonics runs use similar currents. For metrology, after an EBL job is carried out we use its log to extract the found marker positions and all relevant details that are used for analysis, the data is then fitted to extract linear and residual components of the distortion as described earlier. We note that distortions induced by the pins are spotted close to pin locations in all of our maps, even rotating the wafer 90° with respect to the holder resulted in the same distortions, and an example of these patterns is shown in supplementary materials. Most importantly, these are minimal compared to the linear and residual distortions after bonding, and hence their influence is minimal on the derived values. These distortions might result from wafer bow variations between processes, since the latter is not fully neutralized on the wafer scale by the pins.

IV. RESULTS AND ANALYSIS

A. ASSESSMENT OF POST-BONDING MEMBRANE DISTORTIONS

To better explain the different distortions, we first present a baseline experiment where a 300nm-thick InP membrane is bonded to Si using 12μm BCB. The reason for choosing 12μm BCB as baseline is that it is suitable for the co-integration of electronics with photonics. The bonding temperature is 280 °C for 1h. Fig.4.a shows the pre-bond residual distortion map. The found values of the x- and y-scaling are 2.7$\pm$1ppm and 0.9$\pm$1ppm, respectively. The non-orthogonality is found to be 3.4×10^{-6} rad, while STDev of residual errors is 22.1 nm. This indicates that the found marker positions are slightly distorted in the order of a few tens of nm from the design map. The map in Fig.4.a shows that the displacement of markers in the edge contributes more to the residual distortions. The reason might be the presence of non-uniform residual stress during lithography, which is released after SiN_x removal and e-beam metrology, for instance, because of the 2-dimensional bow profile. Further details and explanations on this can be found in supplementary materials. The inset in Fig.4.a shows bell plots representing the distribution of found marker positions relative to the design coordinates for the pre-bond and post-bond maps. STDev increases significantly after bonding in comparison to the pre-bond case, so residual distortions are more present in the post-bond case. For the post-bond experiment, fitting with methods BFGS and trust-constr yield x-scaling values of 323.461$\pm$1ppm and 323.462$\pm$1ppm, y-scaling value of 322.910$\pm$1ppm and 323.075$\pm$1ppm, non-orthogonality value of $1.14 \pm 2 \times 10^{-6}$rad and $1.13 \pm 2 \times 10^{-6}$rad, and STDev values of 104.26 nm and 104.28 nm, respectively. This is consistent with other wafers studied in this paper, and similar scaling values were reported as well [19]. The residuals map (vectors) aligned to the BCB thickness uniformity map (colored map) is shown in Fig.4.b. It can be seen that the length of the vectors increases by a factor of three and the position of the longest vectors is present in the center as well as in the edge compared to the pre-bond map, suggesting that these residual distortions are linked to the bonding process. We have summarized the values of linear distortions and residual errors for all experiments in this paper in the Table.S1 of the supplementary materials.

We note that expansion values above 500 ppm can start to interfere with the light emission properties of III-V-based semiconductors [30]. Despite that the presented values are below this threshold, they might still need to be taken into account when designing devices where small values of strain play an important role in the device performance. For

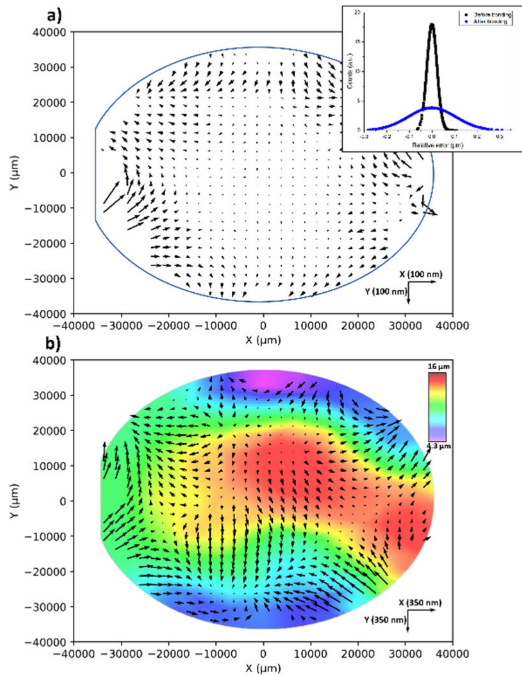


FIGURE 4. a): Pre-bond distortion map of the InP wafer, inset: bell plots of residual errors before and after bonding, b): post-bond distortion map of the InP membrane overlapped with the thickness variation map from reflectometry.

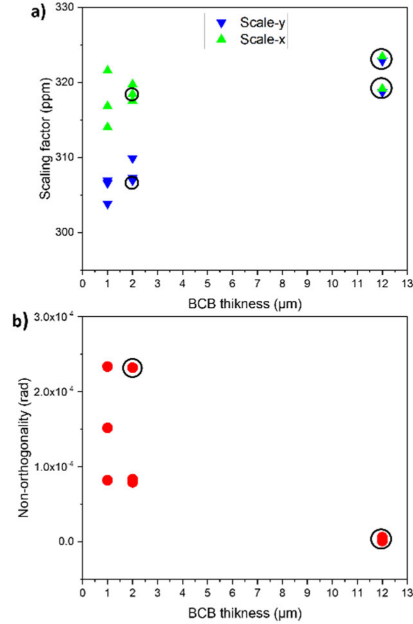


FIGURE 5. Linear distortions of the InP membrane vs BCB thickness, a): x- and y-scaling factors, b): non-orthogonality. Circled data points represent dedicated wafer runs, while the rest are from other functional photonics runs.

instance, for a polarization-insensitive semiconductor optical amplifiers working in the O-band, a value of 300 pm in strain represents a 15% increase from the desired strain for optimal polarization insensitivity [31].

B. EFFECT OF BCB THICKNESS AND THICKNESS NON-UNIFORMITY ON MEMBRANE DISTORTIONS

Fig.5 shows results obtained on membrane scaling in both directions and non-orthogonality for InP membranes bonded on Si with different BCB thicknesses. Each point in the x-scaling, y-scaling, and non-orthogonality represents one bonding experiment with negative markers. The values enclosed by a black circle are extracted from dedicated runs while the rest are from functional photonics runs. The values of x-scaling are within 316-322ppm for BCB thicknesses of 1 and 2 μm and slightly increase up to 323 ppm for 12 μm BCB. Similarly, the values for y-scaling increase from the range of 303-307 ppm for 1 μm BCB to 306-310 ppm for 2 μm BCB, and up to $\sim$322 ppm for BCB thickness of 12 μm. Across all of our measurements, the x-scaling is higher than the y-scaling. This difference is below 1ppm for bonding with 12μm BCB and amounts to values up to 15ppm for experiments with BCB thickness below 2 μm. The mechanism behind this anisotropic expansion is unclear. It might be the result of an anisotropic distribution of forces during the bonding or the presence of an anisotropic behavior in the CTE or the mechanical properties of the substrate carriers. In either case, higher BCB thicknesses help in the reflow of BCB during bonding to better accommodate for these residual stresses, which might be the reason why this anisotropy is lower in the experiment with 12 μm BCB compared to lower thicknesses [32]. As for non-orthogonality, we found no correlation between its variation *vs* BCB thickness based on the results presented in Fig.5.b, especially given the high variation of non-orthogonality from sample to sample for BCB thickness below 2 μm. This variation and the variation of x- and y-scaling factors across samples might be linked to the different pre-bonding and post-bonding processing steps that the samples went through and/or the thickness variations of the membrane.

We also bonded InP with 90° angle mismatch between the membrane and the Si wafer to see its effects on the values presented earlier. The BCB thickness is 2μm and the wafer was read with the Si flat facing the direction used in all other experiments. A post-bond picture and distortion map of the wafer are shown in supplementary data. Results of the fitting are 325.112±1 ppm, 317.741±1 ppm, and $1.659\pm2 \times 10^{-6}$ rad for x-scaling, y-scaling, and non-orthogonality, respectively. The x and y directions are defined with respect to the carrier Si substrate for direct comparison with earlier experiments. Here, x-scaling remains higher than y-scaling similar to earlier experiments but with a slightly lower value difference of 7-8 ppm compared to earlier values in the range of 10-15 ppm for the same BCB thickness. This suggests that the distortion is not dependent on the relative orientations between the two wafers. The slight difference is linked more to an anisotropic behavior in the bonding forces or the Si carrier relative to the InP membrane. The latter might be the reason why this difference in the 12 μm BCB sample is low since the separation between the membrane and Si is higher.

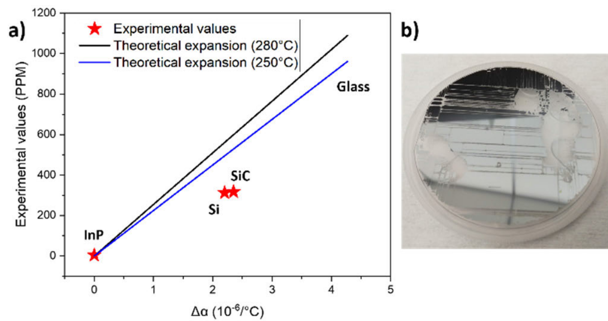


FIGURE 6. Calculated and experimental values of the InP membrane expansion vs CTE mismatch, b) image of the bonded membrane-on-glass before removal of the InGaAs etch stop.

To further study this, we analyzed the thickness non-uniformity results from the dedicated 12 μm BCB wafer (Fig.4.b). Here, the vector direction and length slightly correspond to the direction where the BCB thickness changes more abruptly in the thickness map. However, the full distortion map and thickness variation map do not entirely overlap, hinting that other effects take place simultaneously. This might be related to the inherent residual stress present in all measurements, or more likely the presence of residual stresses during/after bonding. However, these effects do not induce significant distortions as compared to the linear scaling factors that we found in our experiments.

C. EFFECT OF SUBSTRATE MATERIALS ON MEMBRANE DISTORTIONS

Carrier substrates for membrane photonics are usually chosen for their functionality. However, the substrate choice is crucial for the success of integration with adhesive bonding [32]. This is because the substrates and the membrane are bonded at temperatures above 200 °C. Thus, their CTE mismatch results in residual stresses and membrane distortion after bonding when the temperature falls back to room temperature. An equation to describe membrane scaling *vs* CTE is given as follows:

$$P = \Delta T . \Delta \alpha \quad (3)$$

Here, P can be the average of P_4 and P_5, ΔT is the bonding temperature minus room temperature, and $\Delta\alpha$ is the CTE mismatch. To investigate the effect of substrate choice on the scaling in x- and y- directions, we first calculated the theoretical values of scaling for InP membrane for different carrier substrates and for bonding temperatures of 250°C and 280°C, which are most often used in literature [32]. We also plotted the average of P_4 and P_5 from our experiments where the BCB thickness is 2 μm and the bonding temperature is 280 °C. Results are shown in Fig.6.a.

The thermal expansion of InP is higher than all other substrates used in this study, which is why the membrane scaling here is limited to expansion (positive values of P_4 and P_5). In the case of bonding InP to InP carrier, a CTE mismatch of 0 is calculated from theory. However, our experimental findings reveal an average scaling factor of 4.53±1 ppm. This points to the presence of expansion within the InP membrane, even for InP to InP bonding. This expansion is likely attributed to the partial relaxation of residual stresses that may exist in the BCB layer, which are around 40 Mpa [28]. This situation likely arises due to the significantly higher thermal expansion of BCB as a polymer compared to InP and other semiconductors. Consequently, the residual stresses that accumulate within the BCB layer could potentially impact the InP membrane more significantly than the underlying InP substrate. The latter is due to the substantial difference in thickness between the substrate and the membrane, with the substrate being three orders of magnitude thicker.

The average scaling factors measured on Si and SiC wafers are 312.4±1 and 317±1 ppm, respectively. These values are consistent with a multitude of photonic device runs on Si that are not presented [33], [34], and also InP electronics on Si [19]. These values deviate by 248.6±1 and 282.2±1 ppm from the anticipated theoretical expansion values. Therefore, it is reasonable to suspect that this difference in the expansion was liberated after bonding as residual stress. To better explain this, we deconstruct the expansion of the membrane into two distinct segments. The values acquired through experimentation, denoted as P_4 and P_5, are designated as *residual expansion*, while the variance between the experimental and theoretical values is termed *released expansion*. It can be that the released expansion results from the relatively higher elastic deformation of BCB in comparison to the InP semiconductor membrane on top [32]. Another explanation for the significant difference between experimental and theoretical values could be related to the crosslinking of BCB during the temperature ramp-up phase of the bonding. It is evident that a point of permanent adhesion between the two wafers on the wafer scale occurs before the 100% crosslinking in BCB that is achieved at 280 °C. Using Equation 3 and plugging in the measured value of P, we calculated the temperature at which the expansion stopped, and it was found to be around 170 °C which, according to the reference [32], corresponds to a degree of crosslinking slightly below 50%. Hence, this could potentially co-exist with the previously mentioned mechanism, and is further supported by experiments in section IV.d. In Fig.6.b, an image depicting the bonding outcome to the SiO_2 substrate is presented. Alongside the noticeable locations indicating membrane detachment, there are discernible vertical and horizontal lines. These are only visible after the removal of the InP substrate. Theoretically, the membrane should experience an expansion of 1088.9 ppm due to the substantial CTE mismatch of an order of magnitude between InP and glass. The presence of such lines, where the InP membrane has split, suggests that the extent of released expansion surpasses the values previously observed for Si, which would require plastic deformation of the membrane and therefore formation of these lines. Although extraction of the values of P_4 and P_5 was not possible as a result of

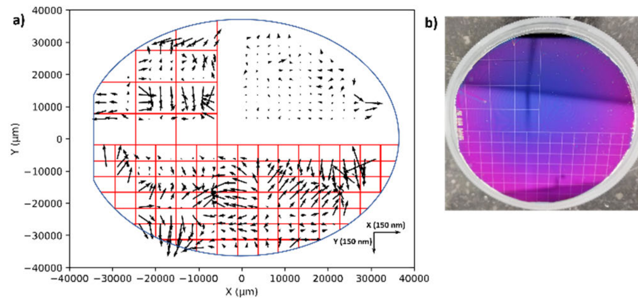


FIGURE 7. Post-etch distortion map of the InP membrane-on-Si, b) image of the InP cutting pattern on ZEP520A resist before etching.

the membrane damage, these should be much higher than the largest values of 325±1 ppm recorded in this study to cause the membrane to rupture, which underscores the necessity for a more customized bonding approach for materials with high CTE mismatch. Finally, we note that in these experiments P_4 is also higher than P_5 by 11.22±2 ppm, 7.19±2 ppm, and 5.14±2 ppm for Si, SiC, and InP substrates, respectively. These values seem to increase with the CTE mismatch, which further confirms that it is more related to the bonding or the properties of the carrier substrate.

D. EFFECT OF THE RESIDUAL STRESSES ON MEMBRANE DISTORTIONS

Here, we investigated the presence of residual stresses on the InP membrane to evaluate its effect on distortion and to distinguish from the effects discussed in section IV.c. For this, we used the bonded sample with results shown in Fig.4 where we further etched the InP membrane into isolated areas of different sizes, as shown in Fig.7. The lines are fully etched through the InP membrane, and are 50 μm in width to ensure accommodation of any deformations resulting from stress release. For the layout, the top-right part was left pristine as a full quarter, the top-left quarter of the wafer contains 10×10 mm^2 squares, and the bottom part was etched into 5×5 mm^2 squares. The goal is to investigate the effect of residual stress alone. Here, as the residual stress distributes across the full scale of the membrane, etching smaller isolated areas leads to a redistribution of residual stress across each area. This residual stress redistribution depends on the sizes of the isolated areas as well [35]. Thus, we fitted each part individually where (x_0, y_0) are the post-bond positions before etching (membrane intact) and (x, y) are the post-bond positions after etching, *i.e.*, the membrane is cut according to the lines. We found that the x-scaling and y-scaling factors of the three regions are all within 2 ppm of the original map positions before cutting, and their non-orthogonality is below 5×10^{-6} rad from the original map positions. This signifies that the residual stress from the InP membrane has a low impact on the linear distortions, which is in the order of a few micrometers. However, the residual distortion shows a completely different behavior. Fig.7.a represents the distortion map for the different regions. The arrows representing distortions lying in 5×5 mm^2 and 10×10 mm^2 cut areas have a higher magnitude compared to the top-right quarter where the membrane is left intact. This suggests that a part of the residual stress in these regions is released as strain, leading to a displacement of the separated small square membranes individually. This is also reflected on the STDev values of errors, which are 43.7 nm, 40.8 nm, and 16.2 nm, for regions with 5×5 mm^2 square separations, 10×10 mm^2 square separations, and no square separation, respectively.

As mentioned in section IV.c, the measured distortion scaling factors of InP-on-Si and InP-on-SiC are noticeably below what is expected from theoretical calculations. This was linked to two possible coexisting mechanisms with residual stress from the membrane being one of those. Thus, releasing the residual stress induced by the InP membrane can reveal its contribution to both linear and residual distortions. To further investigate this, we performed a bonding experiment of an InP membrane with gold markers (i.e., positive markers) on top of Si, so that the InP membrane can be totally removed and only the BCB layer with gold markers remains. The bonding parameters remain the same compared to the experiment shown in section IV.a, i.e., we bond with 12 μm BCB on a Si substrate and at 280 °C. After bonding, substrate removal, and the complete removal of the InP membrane with wet etching, metrology is carried out and marker locations are extracted and fitted with the model. For linear distortions, we found values of 326.63±1 ppm for x-scaling, 315.93±1 ppm for y-scaling, and $3.1 \pm 3 \times 10^{-6}$ for non-orthogonality, which are comparable to the values obtained with negative markers in section IV.a.

This signifies that the contribution of residual stress from the InP membrane to the difference between theoretical and expected scaling values shown in the previous section is much weaker compared to the other mechanism. Thus, the deviation of values from theory seen in section IV.c of >240 ppm is likely linked to the permanent adhesion of the two substrates at a lower crosslinking percentage of BCB than the expected value of 100% crosslinking. We also note that the difference between x-scaling and y-scaling is ∼10.7±2 ppm here, which is significantly higher than the value <1ppm from the previous experiment, suggesting that the anisotropic behavior that is witnessed in these samples mainly arises from the substrate carrier. We also note that the STDev here is ∼30% higher than in previous the experiment, suggesting that more residual errors arise after the removal of the membrane. However, this might be related to the difference in BCB non-uniformity values in the two experiments as seen in the BCB thickness non-uniformity maps (Fig.8 vs Fig.4.b). In Fig.8, saddle points visible in the distortion map correlate with small gradients in the BCB thickness while higher distortions correlate with strong gradients in BCB thickness. These gradients arise during the BCB reflow between two plain wafers under pressure, and are caused by non-uniformity of the bonding forces, such as non-planarity of the bonding glass and unequal forces applied from two pins on each side of the bonding cassette.

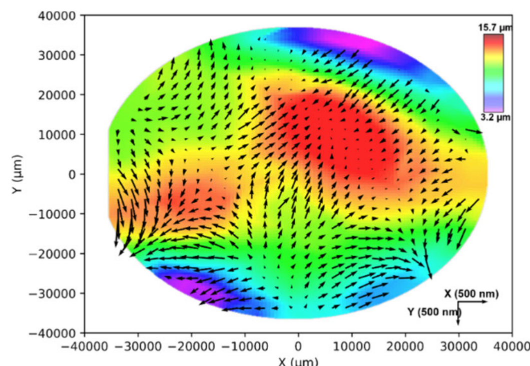


FIGURE 8. Post-bond distortion map of the InP membrane overlapped with BCB thickness variation map for the wafer with 12μm BCB thickness and gold markers (the InP membrane is completely removed).

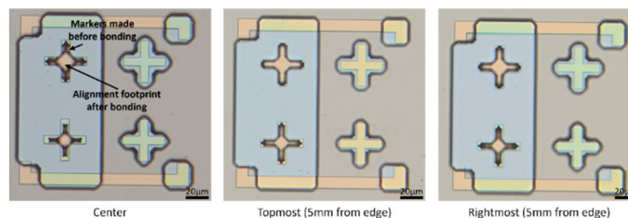


FIGURE 9. Overlay alignment patterns from three different locations in the fabricated wafer, with the designs compensated for the scaling.

Finally, we note that the dominant distortion in this study is the scaling, with values consistently found in the 300-330ppm range throughout all of the differently processed wafers, except for bonding on InP substrate revealing almost no scaling. For device fabrication on InP membranes containing distortions, the large parts of linear distortions can be corrected in the design phase to lower the overall distortions from a few micrometers to the sub-micrometer level, while the non-linear residual distortions can be corrected by the alignment schemes of the advanced optical lithography tools, such as the ArF scanner. The latter uses a similar mechanism to EBL where local distortions are compensated for in local cell exposures. Functional InP membrane photonics on Si substrate fabricated with EBL were consistently demonstrated [36]. Their fabrication involves double-side processing before and after bonding where EBL corrects for the local distortions before exposing the cell, hence achieving overlay accuracy below 20 nm. For the vertical integration of membrane photonics on top of electronics substrates, we note that the post-bond alignment, *i.e.*, translation and rotation between the two substrates, can be preserved without influencing the bonding parameters by introducing hard pillars from the photonics side to avoid slippage [10]. Moreover, distortion of the electronics substrate is negligible compared to the membrane photonics by view of its three orders of magnitude larger thickness. Thus, taking all of these points into consideration could enable the intended application of photonics and electronics co-integration.

This overlay strategy has also been reported in the fabrication process of InP electronics on Si electronics, where the large part of scaling is corrected by scaling the design, and the distortions that are left are corrected by the lithography tool [19]. Moreover, we recently fabricated photonics where a proximity lithography tool was required for a post-bond lithography. The tool does not have internal mechanisms for image scaling, therefore the optical mask used must be pre-compensated with anticipated expansion. To generate the mask, we read and fitted our post-bond distortion data, and corrected for the linear part. The overlay pattern across different positions from the wafer is shown in Fig.9. These indicate that the large part of distortions, which is in the order of 10μm for edge markers, is corrected to lesser than 1μm.

In the case when a scanner or stepper lithography is used, the maximum errors that can be compensated must fall below 1μm. So by pre-compensating the reticle for the 300 ppm linear expansion, the errors that are left arise from the residual distortions and are well within this range. Residual errors are then compensated internally where the tool can read local markers and correct for the local distortion. This has been already shown for stepper lithography, and could be further expanded to other tools [11], [19].

E. EFFECT OF DEFECTS ON MEMBRANE DISTORTIONS

The presence of defects, such as large hard inorganic dust particles and epitaxial defects, has been shown to affect post-bonding distortions on the scale of the full intact membrane area for direct bonding techniques [18]. Bonding with BCB is usually more tolerant to these defects. This is why it is important to assess the effect of the local presence of defects on the linear and residual components of distortion in this study. Knowledge of the extent of this distortion is crucial to deciding on post-bonding lithography strategies that can account for these errors. To test this, we used a wafer with an epitaxial defect located in the center of the wafer with topography above 2 μm, and the wafer was bonded to Si with 2 μm BCB. After bonding and substrate removal, the membrane was found to be cracked in the center along the y-direction (Fig.10.a). The crack originated from the defect. Its vertical propagation is highly likely due to the stress from pins used to hold the bonding stack inside the bonding cassette, which are located on the top and bottom sides of the wafer. We first fitted the full map to assess the distortion. Fig.10.a shows the post-bonding distortion map where all markers were fitted at the same time. The line where the membrane broke is visible both in the microscope and in the map and the extra separation between markers at the two sides of the line is around 10 μm. This high separation is most likely linked to the formation of a crack during the bonding phase. We also fitted the right and left sides of the maps separately to extract the residual distortion maps, results are shown in Fig.10.b. The STDev of errors in nm for both maps are similar to results obtained in section IV.c. The x- and y-scaling factors are found to be 312.9±1, 318.5±1 ppm for the right map, and 313.8±1,329.7±1 ppm for the left map, respectively. Values of x-scaling are

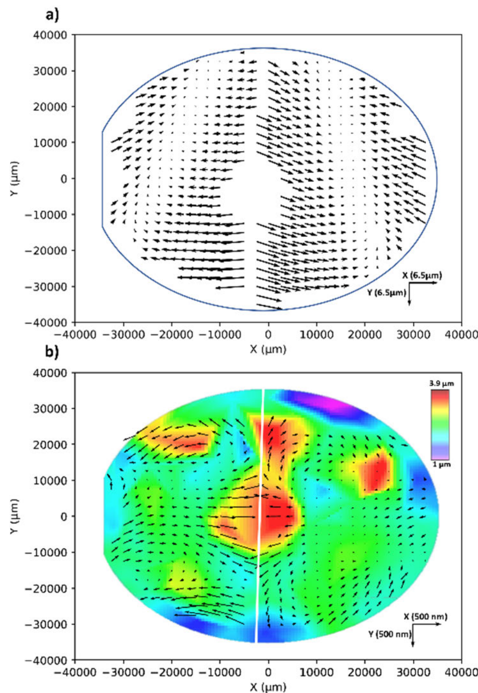


FIGURE 10. a): Post-bond distortion map of the defective InP membrane with full wafer fitting, b): post-bond distortion map of the defective InP membrane overlapped with BCB thickness variation with fitting left and right membranes separately, the white line indicates the position of the crack.

slightly smaller than previous values of similar experiments by 5±2 ppm. Moreover, the map in Fig.10.b shows that the vectors near the cleaved line and particularly near the defect are larger than in the center of the two separate membranes. These observations point to a redistribution of the membrane residual stress on the water level. Hence, the presence of such defects can be detrimental to overlay lithography both when compensating for linear distortions alone and afterward when dealing with residual distortions that increase the minimum achievable overlay error.

V. CONCLUSION

In this study, we developed a general method with high accuracy to analyze linear and residual distortions in membrane layers for 3D integration. We used the method to investigate the deformation of InP membranes resulting from wafer-scale bonding with BCB. Various angles of the bonding process have been investigated, revealing key factors affecting membrane distortion. We found that linear distortions are mostly affected by the CTE mismatch of bonding substrates (such as Si, InP, SiC, and glass), in a large expansion range of 0-325 ppm, while residual distortions depend on a multiplicity of factors. These are found to correlate with the post-bond BCB thickness non-uniformity and InP membrane residual stress. We also observed that the presence of defects influences all distortions on the wafer scale, which can be detrimental to overlay lithography for membrane devices. By accurately quantifying these distortions using the method proposed in this work and compensating them, vertical integration of membrane devices on top of electronics substrates can be enabled. These findings provide valuable guidance toward the development of advanced technologies that rely on improving 3D integration processes and overlay lithography.

REFERENCES

[1] C. Xiang, W. Jin, O. Terra, B. Dong, H. Wang, L. Wu, J. Guo, T. J. Morin, E. Hughes, J. Peters, Q.-X. Ji, A. Feshali, M. Paniccia, K. J. Vahala, and J. E. Bowers, ''3D integration enables ultralow-noise isolator-free lasers in silicon photonics,'' *Nature*, vol. 620, no. 7972, pp. 78–85, Aug. 2023, doi: 10.1038/s41586-023-06251-w.

[2] C. Xiang, W. Jin, D. Huang, M. A. Tran, J. Guo, Y. Wan, W. Xie, G. Kurczveil, A. M. Netherton, D. Liang, H. Rong, and J. E. Bowers, ''High-performance silicon photonics using heterogeneous integration,'' *IEEE J. Sel. Topics Quantum Electron.*, vol. 28, no. 3, pp. 1–15, May 2022, doi: 10.1109/JSTQE.2021.3126124.

[3] S. Matsuo, T. Fujii, and T. Hiraki, ''Membrane InP-based photonics devices on Si,'' *Photon. Rev.*, vol. 2023, Aug. 2023, Art. no. 230205, doi: 10.11470/photo.230205.

[4] W. Yao, X. Liu, M. K. Matters-Kammerer, A. Meighan, M. Spiegelberg, M. Trajkovic, J. J. G. M. van der Tol, M. J. Wale, X. Zhang, and K. Williams, ''Towards the integration of InP photonics with silicon electronics: Design and technology challenges,'' *J. Lightw. Technol.*, vol. 39, no. 4, pp. 999–1009, Feb. 15, 2021, doi: 10.1109/jlt.2020.3043799.

[5] S. Abdi, V. Nodjiadjim, R. Hersent, M. Riet, C. Mismer, T. de Vries, K. A. Williams, and Y. Jiao, ''Research toward wafer-scale 3D integration of InP membrane photonics with InP electronics,'' *IEEE Trans. Semicond. Manuf.*, early access, 2024, doi: 10.1109/TSM.2024.3382511.

[6] T. Fujii, T. Sato, K. Takeda, K. Hasebe, T. Kakitsuka, and S. Matsuo, ''Epitaxial growth of InP to bury directly bonded thin active layer on SiO_2/Si substrate for fabricating distributed feedback lasers on silicon,'' *IET Optoelectronics*, vol. 9, no. 4, pp. 151–157, Aug. 2015, doi: 10.1049/iet-opt.2014.0138.

[7] V. Dragoi, G. Mittendorfer, C. Thanner, P. Lindner, M. Alexe, L. Pintilie, M. Hamacher, and H. Heidrich, ''III/V wafer bonding technology for wafer-level fabrication of GaInAsP/InP microring resonators,'' in *Proc. Int. Semiconductor Conf.*, Sep. 2006, pp. 129–132, doi: 10.1109/smicnd.2006.283949.

[8] M. Spiegelberg, J. van Engelen, T. de Vries, K. Williams, and J. van der Tol, ''BCB bonding of high topology 3 inch InP and BiCMOS wafers for integrated optical transceivers,'' in *Proc. 23rd Annu. Symp. IEEE Photon. Soc. Benelux*, Brussels, Belgium, Nov. 2018, pp. 160–163.

[9] S. E. Steen, D. LaTulipe, A. W. Topol, D. J. Frank, K. Belote, and D. Posillico, ''Overlay as the key to drive wafer scale 3D integration,'' *Microelectron. Eng.*, vol. 84, nos. 5–8, pp. 1412–1415, May 2007, doi: 10.1016/j.mee.2007.01.231.

[10] S. Abdi, T. de Vries, M. Spiegelberg, K. Williams, and Y. Jiao, ''Novel wafer-scale adhesive bonding with improved alignment accuracy and bond uniformity,'' *Microelectron. Eng.*, vol. 270, Feb. 2023, Art. no. 111936, doi: 10.1016/j.mee.2023.111936.

[11] I. Ostermay, A. Thies, T. Kraemer, W. John, N. Weimann, F.-J. Schmückle, S. Sinha, V. Krozer, W. Heinrich, M. Lisker, B. Tillack, and O. Krüger, ''Three-dimensional InP-DHBT on SiGe-BiCMOS integration by means of benzocyclobutene based wafer bonding for mm-wave circuits,'' *Microelectron. Eng.*, vol. 125, pp. 38–44, Aug. 2014, doi: 10.1016/j.mee.2013.11.012.

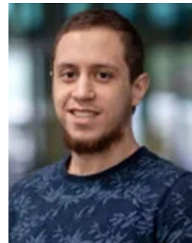
[12] A. J. D. Boef, ''Optical wafer metrology sensors for process-robust CD and overlay control in semiconductor device manufacturing,'' *Surf. Topography, Metrology Properties*, vol. 4, no. 2, Feb. 2016, Art. no. 023001, doi: 10.1088/2051-672x/4/2/023001.

[13] D. Pasquariello, M. Camacho, F. Ericsson, and K. Hjort, ''Crystalline defects in InP-to-silicon direct wafer bonding,'' *Jpn. J. Appl. Phys.*, vol. 40, no. 8R, p. 4837, Aug. 2001, doi: 10.1143/jjap.40.4837.

[14] E. Suhir, ''Adhesively bonded assemblies with identical nondeformable adherends and 'piecewise continuous' adhesive layer: Predicted thermal stresses in the adhesive,'' *Int. J. Solids Struct.*, vol. 37, no. 16, pp. 2229–2252, Apr. 2000, doi: 10.1016/s0020-7683(98)00317-5.

[15] E. Suhir, ''Predictive analytical thermal stress modeling in electronics and photonics,'' *Appl. Mech. Rev.*, vol. 62, no. 4, Jun. 2009, Art. no. 040801, doi: 10.1115/1.3077136.

[16] J. D. Armitage Jr. and J. P. Kirk, "Analysis of overlay distortion patterns," *Proc. SPIE*, vol. 921, pp. 207–223, Jan. 1988, doi: 10.1117/12.968368.
[17] M. Hamacher, H. Heidrich, U. Troppenz, D. Syvridis, D. Alexandropoulos, S. Mikroulis, A. Kapsalis, C. W. Tee, K. Williams, V. Dragoi, M. Alexe, D. Cristea, and M. Kusko, "Waferbonded active/passive vertically coupled microring lasers," *Proc. SPIE*, vol. 6896, pp. 171–178, Feb. 2008, doi: 10.1117/12.762507.
[18] A. Sakanas, E. Semenova, L. Ottaviano, J. Mørk, and K. Yvind, "Comparison of processing-induced deformations of InP bonded to Si determined by e-beam metrology: Direct vs. adhesive bonding," *Microelectron. Eng.*, vol. 214, pp. 93–99, Jun. 2019, doi: 10.1016/j.mee.2019.05.001.
[19] N. G. Weimann, D. Stoppel, M. I. Schukfeh, M. Hossain, T. Al-Sawaf, B. Janke, R. Doerner, S. Sinha, F.-J. Schmückle, O. Krüger, V. Krozer, W. Heinrich, M. Lisker, A. Krüger, A. Datsuk, C. Meliani, and B. Tillack, "SciFab—A wafer-level heterointegrated InP DHBT/SiGe BiCMOS foundry process for mm-wave applications," *Phys. Status Solidi A*, vol. 213, no. 4, pp. 909–916, Apr. 2016, doi: 10.1002/pssa.201532549.
[20] S. Abdi, A. Zozulia, J. Bolk, E. J. Geluk, K. Williams, and Y. Jiao, "Study of spatial distortion in InP nanophotonic membranes on different carrier substrates," in *Proc. 24th Eur. Microelectron. Packag. Conf. Exhib. (EMPC)*, Sep. 2023, pp. 1–5, doi: 10.23919/empc55870.2023.10418368.
[21] J. Nocedal and S. J. Wright, *Numerical Optimization* (Springer Series in Operations Research and Financial Engineering). New York, NY, USA: Springer, 2006, doi: 10.1007/978-0-387-40065-5.
[22] M. Lalee, J. Nocedal, and T. Plantenga, "On the implementation of an algorithm for large-scale equality constrained optimization," *SIAM J. Optim.*, vol. 8, no. 3, pp. 682–706, Aug. 1998, doi: 10.1137/s1052623493262993.
[23] I. Kudman and R. J. Paff, "Thermal expansion of $In_xGa_{1-x}P$ alloys," *J. Appl. Phys.*, vol. 43, no. 9, pp. 3760–3762, Sep. 1972, doi: 10.1063/1.1661805.
[24] Y. Okada and Y. Tokumaru, "Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 k," *J. Appl. Phys.*, vol. 56, no. 2, pp. 314–320, Jul. 1984, doi: 10.1063/1.333965.
[25] N. M. Sultan, T. M. B. Albarody, H. K. M. Al-Jothery, M. A. Abdullah, H. G. Mohammed, and K. O. Obodo, "Thermal expansion of 3C-SiC obtained from in-situ X-ray diffraction at high temperature and first-principal calculations," *Materials*, vol. 15, no. 18, p. 6229, Sep. 2022, doi: 10.3390/ma15186229.
[26] R. Roy, D. K. Agrawal, and H. A. McKinstry, "Very low thermal expansion coefficient materials," *Annu. Rev. Mater. Sci.*, vol. 19, no. 1, pp. 59–81, Aug. 1989, doi: 10.1146/annurev.ms.19.080189.000423.
[27] S. Abdi, T. de Vries, M. Spiegelberg, K. Williams, and Y. Jiao, "Wafer-scale adhesive bonding with hard benzocyclobutene anchors for wafer assembly and heterogeneous integration," in *Proc. 34th Annu. SEMI Adv. Semiconductor Manuf. Conf. (ASMC)*, May 2023, pp. 1–4, doi: 10.1109/ASMC57536.2023.10121131.
[28] S. Abdi, V. Nodjiadjim, R. Hersent, M. Riet, C. Mismer, T. de Vries, K. A. Williams, and Y. Jiao, "Towards wafer-scale integration of InP membrane photonics on InP substrates for high-speed datacenter applications," in *Proc. 26th Annu. Symp. IEEE Photon. Soc. Benelux Chapter*, 2022. [Online]. Available: https://photonics-benelux.org/wp-content/uploads/pb-files/proceedings/2022/Novel_integration_platform_concepts/Novel_integration_platform_concepts_1.pdf
[29] C. K. Chen, "Electron-beam lithography error sources," *Proc. SPIE*, vol. 471, pp. 2–7, Jun. 1984, doi: 10.1117/12.942306.
[30] G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit, "Adhesive bonding of InP/InGaAsP dies to processed silicon-on-insulator wafers using DVS-bis-benzocyclobutene," *J. Electrochem. Soc.*, vol. 153, no. 12, Oct. 2006, Art. no. G1015, doi: 10.1149/1.2352045.
[31] D. W. Feyisa, S. Abdi, R. van Veldhoven, N. Calabretta, Y. Jiao, and R. Stabile, "Low polarization sensitive O-band SOA on InP membrane for advanced photonic integration," *J. Lightw. Technol.*, early access, 2024, doi: 10.1109/jlt.2024.3369232.
[32] X. Wang and F. Niklaus, "Polymer bonding," in *3D and Circuit Integration of MEMS*. Hoboken, NJ, USA: Wiley, 2021, pp. 331–359, doi: 10.1002/9783527823239.ch15.
[33] M. Spiegelberg and K. A. Williams, "3D-integration on wafer level of photonic and electronic circuits," Dept. Elect. Eng., Technische Univ. Eindhoven, Eindhoven, The Netherlands, Tech. Rep., 2021. [Online]. Available: https://research.tue.nl/en/publications/3d-integration-on-wafer-level-of-photonic-and-electronic-circuits
[34] L. Shen, "Ultrafast photodetector on the InP-membrane-on-silicon platform," Dept. Elect. Eng., Technische Univ. Eindhoven, Eindhoven, The Netherlands, Tech. Rep., 2016. [Online]. Available: https://research.tue.nl/en/publications/ultrafast-photodetector-on-the-inp-membrane-on-silicon-platform
[35] G. Abadias, E. Chason, J. Keckes, M. Sebastiani, G. B. Thompson, E. Barthel, G. L. Doll, C. E. Murray, C. H. Stoessel, and L. Martinu, "Review article: Stress in thin films and coatings: Current status, challenges, and prospects," *J. Vac. Sci. Technol. A, Vac., Surf., Films*, vol. 36, no. 2, Mar. 2018, Art. no. 020801, doi: 10.1116/1.5011790.
[36] Y. Jiao et al., "Indium phosphide membrane nanophotonic integrated circuits on silicon," *Phys. Status Solidi A*, vol. 217, no. 3, Feb. 2020, Art. no. 1900606, doi: 10.1002/pssa.201900606.



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