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RESEARCH ARTICLE

Power Module With Low Common-Mode Noise and High Reliability

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ABSTRACT Silicon carbide devices provide higher switching speed and switching frequency than their silicon counterpart. However, these characteristics generate significant electromagnetic interference such as conducted common-mode (CM) noise. This paper proposes a novel power module to reduce CM noise without compromising size, thermal performance, and reliability of the power module. A specific part of the bottom copper layer of a directed-bonded copper is etched to reduce CM capacitance. Epoxy is used to increase mechanical reliability by supporting ceramic and top copper layers. This supporting epoxy also prevents an encapsulant from leaking into the etched area. Design methodologies for the proposed power module are provided in detail. Conventional and proposed power modules were prototyped and CM noise was experimentally measured with 400-V input, 200-V output, and 50-kHz switching frequency. The CM noise of the proposed power module was reduced by 5 dBμV. Thermal cycling tests were conducted to confirm the degradation of the proposed power module. Cross-sections of the power modules and measured electrical characteristics verify the reliability of the proposed power module.

INDEX TERMS Power module design, common-mode noise, parasitic capacitance, thermal resistance, thermal cycling test.

I. INTRODUCTION

Wide bandgap devices such as silicon carbide (SiC) devices have been widely employed due to their higher switching speed and switching frequency compared to silicon devices [1], [2]. Nevertheless, these characteristics make it more sensitive to parasitic components and causes electromagnetic interference (EMI) such as conducted common-mode (CM) noise.

Various approaches were introduced to reduce the CM noise. Passive filters such as Y-capacitors and/or CM chokes are the common solutions, and active filters are also utilized to reduce low-frequency noise [3], [4]. Symmetric circuit topologies are a representative circuit-level design to reduce CM noise [5], [6]. In-phase and anti-phase CM currents are canceled out due to the topological symmetry. Impedance balance techniques balance the circuit without symmetry though it requires additional capacitors and/or inductors [7], [8].

Several power module designs have been reported to attenuate the CM noise. A resistor-capacitor (RC) snubber built on a silicon substrate was added in the power module, resulting in low parasitic oscillation [9]. Integration of CM filters within the power module was presented [10], [11], [12], [13]. Y-capacitors which are placed between the positive DC (referred to as DC+) or the negative DC (referred to as DC-) node and ground was inserted in the module [10], [11]. A CM

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filter was integrated into the power module improving the CM noise from 10 to 100 MHz [12], [13]. A decoupling capacitor was added between every bare die to reduce CM noise based on a mathematical modeling [14]. However, integration of the CM filter may complicate manufacturing process and decrease mechanical reliability.

Alternative methods involve stacking additional substrates such as direct bonded coppers (DBCs), direct bonded aluminums (DBAs), and printed circuit boards (PCBs) [15], [16], [17], [18], [19], [20], [21], [22], [23]. The incorporation of vias within the ceramic layer of secondary DBCs diverts CM current and alters the effective CM capacitance [15]. The propagation path of CM noise was enhanced by including a middle copper layer in the stacked DBC substrate [16]. DiMarino et al. proposed a multi-stack DBA design to screen CM current in 10-kV power module packaging [17], [18], [19]. The screening method was further analyzed and compared in [20]. Ma et al. introduced a novel structure positioning the voltage-pulsating node, or AC node, between the DC+ and DC– nodes [21]. This may compromise thermal performance, complicate manufacturing processes, and reduce cost efficiency due to additional substrates, though it effectively reduces CM capacitance. An alternative approach mounts a PCB onto the DBC to minimize the area of the AC node on the top copper layer [22], [23], [24]. Nevertheless, the integration of PCB and DBC may not ensure manufacturing and high reliability.

Heatsinks have been designed to manipulate the impedance within the CM noise propagation path. One approach uses separate heatsinks integrated with CM snubbers to mitigate CM noise [25]. Another strategy introduces the utilization of nonmetallic heatsinks to achieve reduced CM capacitance [26]. Nevertheless, these methods encounter difficulties when the design flexibility of the heatsinks is restricted.

Substrate designs in [27], [28], [29], [30], and [31] were effective to attenuate CM noise. The layout of the top copper layer was designed to reduce the area of which voltage pulsates [27]. Another approach connected the bottom copper of a substrate to the DC– node through vias [28]. The bottom copper layer consumes the current flowing through the ceramic layer, working as a shield allowing the CM current to bypass the ground. However, the thermal interface material between the substrate and baseplate needs to be an insulator. Work in [29] designed the inner layout of the power module to compensate for large capacitive coupling of an organic DBC substrate. Etching a part of the bottom copper layer and replacing the area with low-permittivity material reduces CM capacitance [30], [31], [32] though its mechanical reliability remains uncertain.

This study proposes a novel power module to reduce the CM noise as an extension of the research conducted in [30]: the proposed module replaces a specific area of bottom copper with air to reduce the CM capacitance between the pulsating nodes and a grounded baseplate. In addition, epoxy is used to increase mechanical reliability by supporting ceramic and top copper layers. This supporting epoxy also prevents an encapsulant from leaking into the etched area. The bottom copper was designed considering the vertical heat flow from the dies to the baseplate not to increase thermal resistance. Equivalent thermal resistances are confirmed by experimentally measuring structure functions. The proposed configuration does not compromise the size and isolation voltage of the power module.

A steady-state thermal analysis by Ansys Icepak and thermal resistance were performed to verify that the proposed configuration does not compromise the thermal performance. Additionally, thermal cycling tests (TCTs) were conducted based on AQG324 standards [34] to verify reliability against mechanical stress resulting from passive temperature changes. Although there are a few failure modes, such as those involving aluminum wires [35], [36] and solder layers [36], [37], [38], this study focuses on the area near the air region and the supporting epoxy. The proposed power module was examined for both mechanical and electrical reliability. Several cross-sections were observed using a scanning electron microscope (SEM) to confirm the mechanical stress near the air region and the supporting epoxy. The output characteristics (drain current versus drain-source voltage) of the switching devices were compared to evaluate the degradation level of electrical performance.

A detailed process for the manufacturing of the proposed module is presented to validate its feasibility. Selection of the epoxy material to secure the air region and its packaging methods are explained.

The rest of this paper is organized as follows. Section II provides a comprehensive overview of the proposed power module design. Methodology to reduce CM capacitance and thermal design are introduced. Section III provides detailed explanations regarding the estimation of capacitance, assessment of mechanical reliability, evaluation of thermal performance, and the manufacturing process of the proposed module. In Section IV, CM noise attenuation is experimentally verified. In addition, results of TCTs and thermal resistance measurements are presented. Section V concludes the paper.

II. PROPOSED POWER MODULE DESIGN TO REDUCE CM CAPACITANCE

A. NOISE PROPAGATION FROM POWER MODULE THROUGH PARASITIC CAPACITORS

Power modules using wide bandgap devices such as SiC introduce increased CM noise due to their capability of high switching speed and switching frequency. Fig. 1(a) shows a half-bridge power module where high-side bare die is Q_1 and low-side bare die is Q_2. Voltage source V_{in} is the DC input voltage. Parasitic CM capacitances C_N, C_O, and C_P are connected to nodes N_N, N_O, and N_P, respectively. Among these capacitances, C_O has the most significant impact on the CM current i_{CM} because of the pulsating voltage at N_O. Fig. 1(b) shows the high-frequency equivalent circuit for CM noise where $v(\omega)$ represents the pulsating voltage at N_O and V_{in} is shorted. Resistance R_{CM} denotes the impedance of line

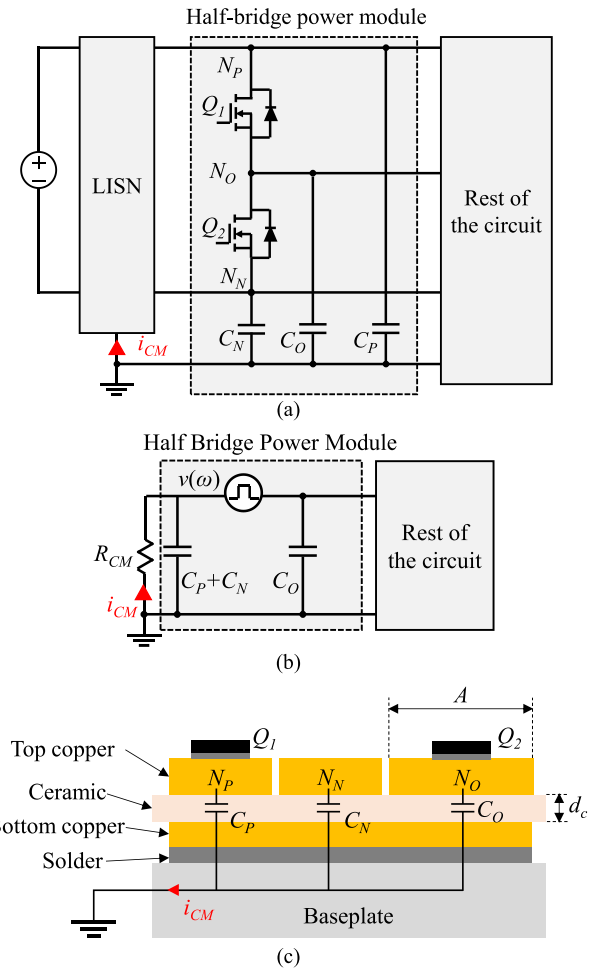

FIGURE 1. (a) Half-bridge power module and its parasitic capacitances. (b) High-frequency equivalent circuit of (a). (c) Cross-section view of the conventional power module.

impedance networks LISN shown in Fig. 1(a). The pulsating noise source $v(\omega)$ generates considerable i_{CM} through C_O, while C_P and C_N work as Y capacitors. Therefore, reducing C_O effectively decreases CM noise or i_{CM}.

Fig. 1(c) presents a cross-section view of the power module. The DBC includes top copper, ceramic, and bottom copper layers. The drain pads of Q_1 and Q_2 are soldered on the top copper layer. The capacitance C_O shown in Fig. 1(c) is given by (1),

$$C_O = \varepsilon_0 \varepsilon_c \frac{A}{d_c} \tag{1}$$

where ε_o, A, ε_c, and d_c are the permittivity of free space (8.85×10^{-12} F· m^{-1}), area of N_O, relative permittivity of the ceramic material, and thickness of the ceramic layer, respectively. The proposed power module reformulates (1) by slightly adjusting the configuration near N_O.

B. PROPOSED DESIGN TO REDUCE C_O

Fig. 2 shows the proposed configuration of the power module. A portion of the bottom copper beneath N_O is etched out

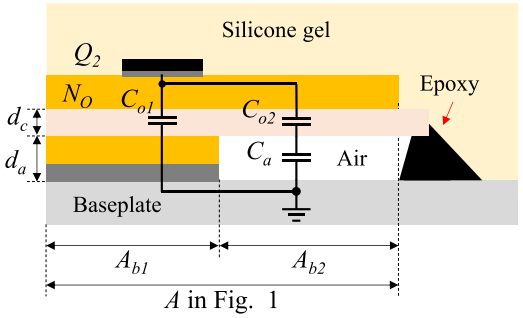

FIGURE 2. Proposed configuration near N_O. A part of bottom copper layer is replaced by air and epoxy prevents silicone gel from entering the etched area.

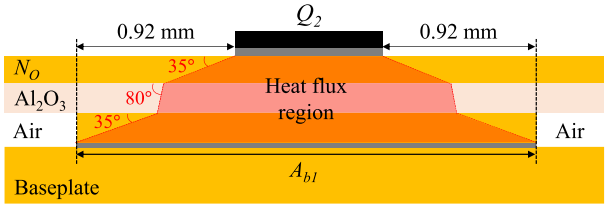

FIGURE 3. Remaining bottom copper area beneath N_O based on the heat flux region.

and replaced by air. Epoxy supports the ceramic and top copper layers and prevents the encapsulation material, e.g., silicone gel, from entering the air region. It is noted that the bottom copper layer, which does not contribute to the thermal performance, should be selectively removed. More details about the thermal design are provided in Section II-C. The new CM capacitance $C_{O.new}$ is the combination of capacitances of C_{O1}, C_{O2}, and C_a as in (2)-(5).

$$C_{O.new} = C_{O1} + \frac{C_{O2}C_a}{C_{O2}+C_a} \tag{2}$$

$$C_{O1} = \varepsilon_0 \varepsilon_c \frac{A_{b1}}{d_c} \tag{3}$$

$$C_{O2} = \varepsilon_0 \varepsilon_c \frac{A_{b2}}{d_c} \tag{4}$$

$$C_a = \varepsilon_0 \frac{A_{b2}}{d_a} \tag{5}$$

In (3)-(5), A_{b1} represents the remaining area of the bottom copper layer under N_O; A_{b2} denotes the area of the etched space; d_a is the thickness of the air region. It is noted that $C_{O.new}$ is smaller than the original C_O and thus generates smaller i_{CM}.

C. THERMAL DESIGN

The bottom copper layer is designed to be etched considering heat flux to not compromise the thermal performance. Fig. 3 shows the remaining bottom copper area A_{b1}. The region is determined based on the head spreading angles which are 35° for the copper layers and 80° for the Al_2O_3 ceramic layer, respectively [33]. The area except A_{b1} beneath N_O is etched out. Prototype power modules used the DBC that

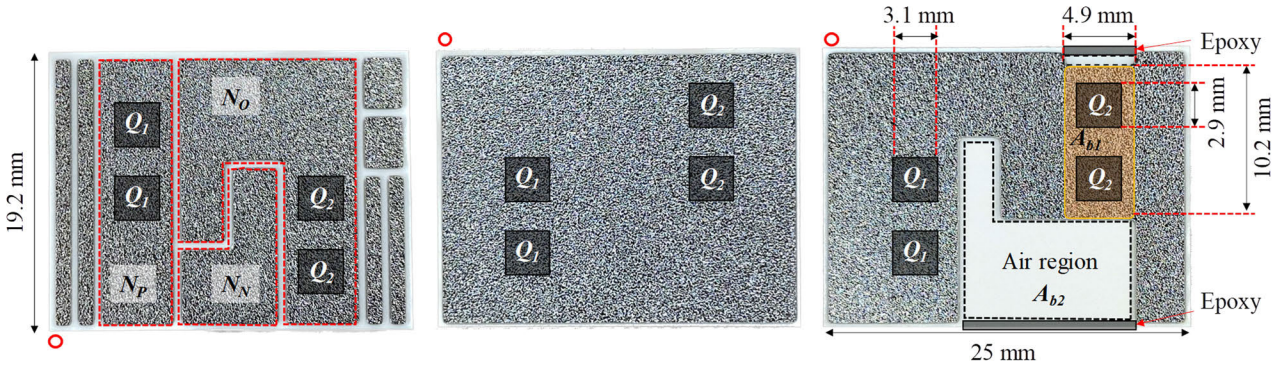

FIGURE 4. DBC substrates used in this study. (a) Top view. (b) Bottom view of the conventional DBC. (c) Bottom view of the proposed DBC.

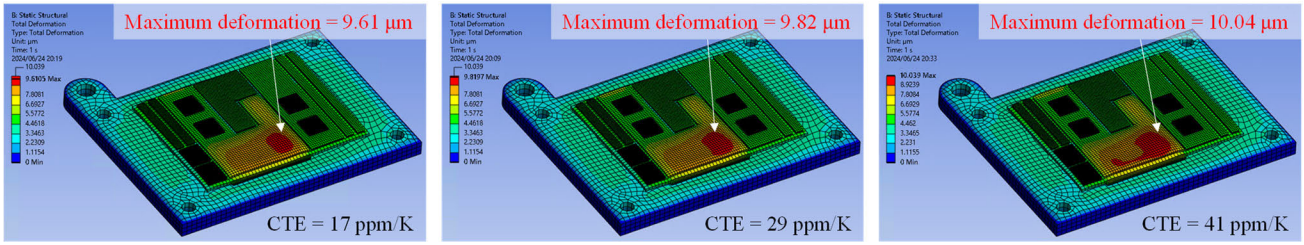

FIGURE 5. Simulated mechanical deformation with various supporting epoxies. (a) CTE = 17 ppm/K. (b) CTE = 29 ppm/K. (c) CTE = 41 ppm/K.

consists of copper-Al_2O_3-copper layers with thicknesses of 0.3, 0.38, and 0.3 mm, respectively. At least 0.92-mm distance from each edge of Q_2 needs to remain considering the heat spreading angle and thickness of each DBC layer. Thermal simulation results and measurement results of the thermal resistance verify the design which are provided in Section III-C and Section IV-D, respectively.

III. PROTOTYPE POWER MODULE

Power modules were prototyped to verify the effectiveness of the proposed CM noise attenuation scheme. Fig. 4 presents photographs of 25 × 19.2 mm^2 DBC. Fig. 4(a) shows the layout of the top copper layer with the location of Q_1 and Q_2 where two dies are connected in parallel. The areas outlined by red dashed lines present the nodes N_P, N_O, and N_N. Fig. 4(b) describes the bottom copper layer of the conventional module. The whole layer is fully filled with copper. Fig. 4(c) presents the bottom copper of the proposed design. The region indicated by black dashed lines represents the air region beneath the node N_O, of which is A_{b2}. The orange region provides the remaining area not to degrade thermal performance as explained in Section II-B or Fig. 3. The prototype power module in Fig. 4(c) secured 1-mm distance from all edges of the bare dies configuring Q_2. The black shaded areas adjacent to the air region are the supporting epoxy as explained in Section II-A or Fig. 2. Table 1 summarizes the components used in the power modules.

TABLE 1. Specifications of proposed power module.

Components		Description
SiC die		S4503/750 V/56 A/26 mΩ by Rohm
DBC		19.2 mm x 25 mm
	Top Cu	0.3-mm thickness
	Ceramic	Al_2O_3/0.38-mm thickness
	Bottom Cu	0.3-mm thickness
Baseplate		C1020/2-mm thickness
Solder		(between dies and top copper layer) Pb95Sn5, 48.1 W/m·K, 0.1-mm thickness (between bottom copper layer and baseplate) SAC305, 58 W/m·K, 0.3-mm thickness
Supporting Epoxy		CTE = 17 ppm/K, viscosity = 56 Pa·s, relative permittivity = 3.8, curing condition: 130°C/5 min + 160°C/10 min
Aluminum wire		(source connection) 400-µm diameter (gate connections) 125-µm diameter
Thermistor		HM104J1A by Littelfuse
Silicone gel		For power module encapsulation (80°C, 1-hour curing)

A. ESTIMATION OF C_O

The prototype power module etched 106.4-mm^2 A_{b2} from 156.4-mm^2 A where $d_c = 0.38$ mm and $\varepsilon_c = 9.8$. The remaining copper area A_{b1} is 50.0 mm^2. Eq (3) provides 11.39 pF for C_{O1}. Assuming 0.15-mm thickness of the bottom solder layer, i.e., $d_a = 0.45$ mm, C_{O2} and C_a are obtained as 24.26 pF and 2.09 pF by (4)-(5), respectively. The CM capacitance of the proposed module $C_{O.new}$ becomes 13.31 pF by (2). The proposed module reduced the CM capacitance by 62.7% compared to that of conventional module, 35.71 pF. The CM

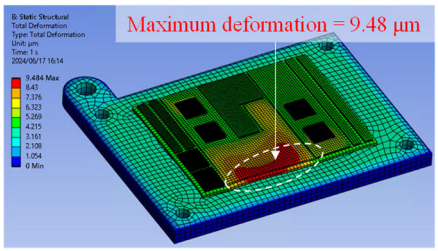

FIGURE 6. Simulated mechanical deformation without supporting epoxy.

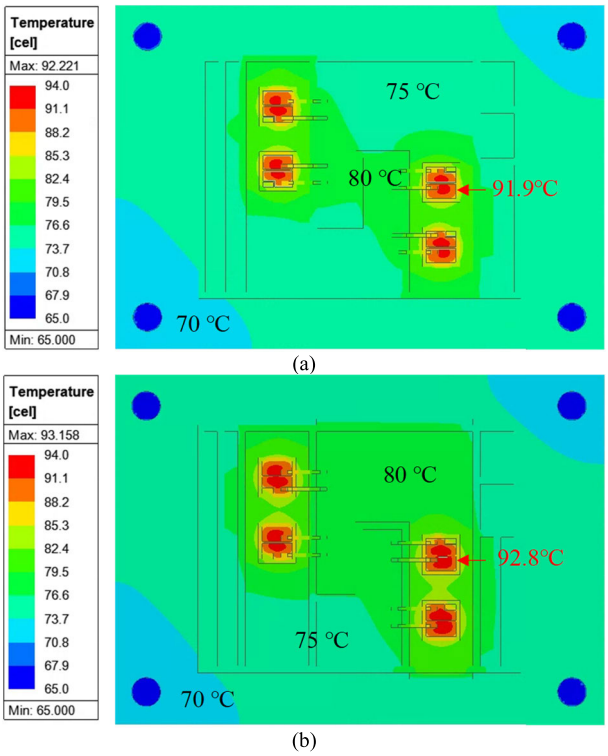

FIGURE 7. Steady state thermal simulation results. (a) Conventional module. (b) Proposed module.

capacitances of the conventional and the proposed modules were also simulated by Ansys 2023 R2 Q3D Extractor as 40.75 pF and 20.38 pF, respectively, resulting in 49.99% reduction. It is noted that the supporting epoxy hardly contributes to the CM capacitance. This is because the epoxy was mostly injected beneath the edge of the ceramic layer rather than beneath N_O as shown in Fig. 2. Simulated CM capacitance without the epoxy was derived to be 20.18 pF.

B. SIMULATED MECHANICAL DEFORMATION

Mechanical characteristics of the power modules were simulated by Ansys 2023 R2 Workbench Mechanical. Thermal load of 10 W was applied to the top surface of each die, with a film coefficient of 4 kW/m^2· K assigned to the baseplate of the power module. The ambient temperature was set to 65 °C. A static structural analysis was carried out assuming that the gravity is 9.8 m/s^2 and the five surfaces except the top surface of the baseplate fixed in position, considering the baseplate constrained from the coolant jacket or frame. In addition,

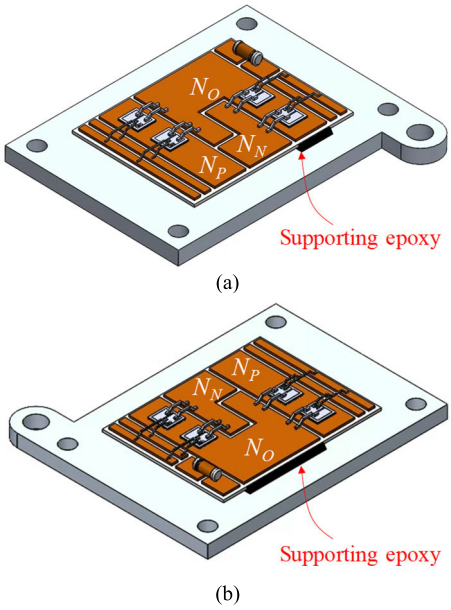

FIGURE 8. Locations where the supporting epoxy is applied. (a) Isometric view. (b) Reversed isometric view.

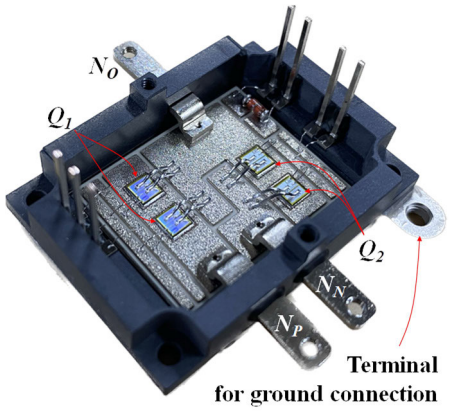

FIGURE 9. Prototype of the proposed module.

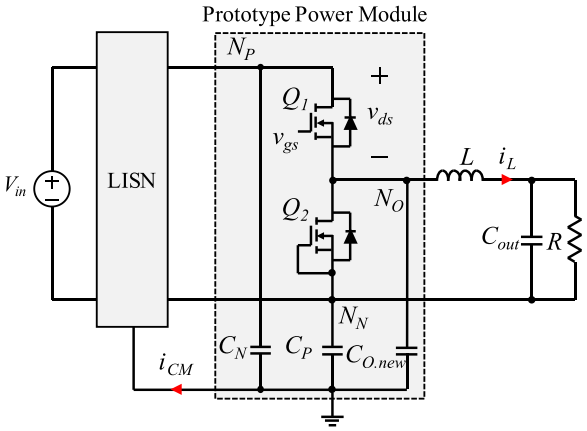

FIGURE 10. Experimental setup to measure the CM noise. Two NNBM8124 LISNs were used to separate CM noise.

the screw hole of each busbar is designated as another fixed surface. It is noted that the fixed positions can be different from the actual packaging conditions.

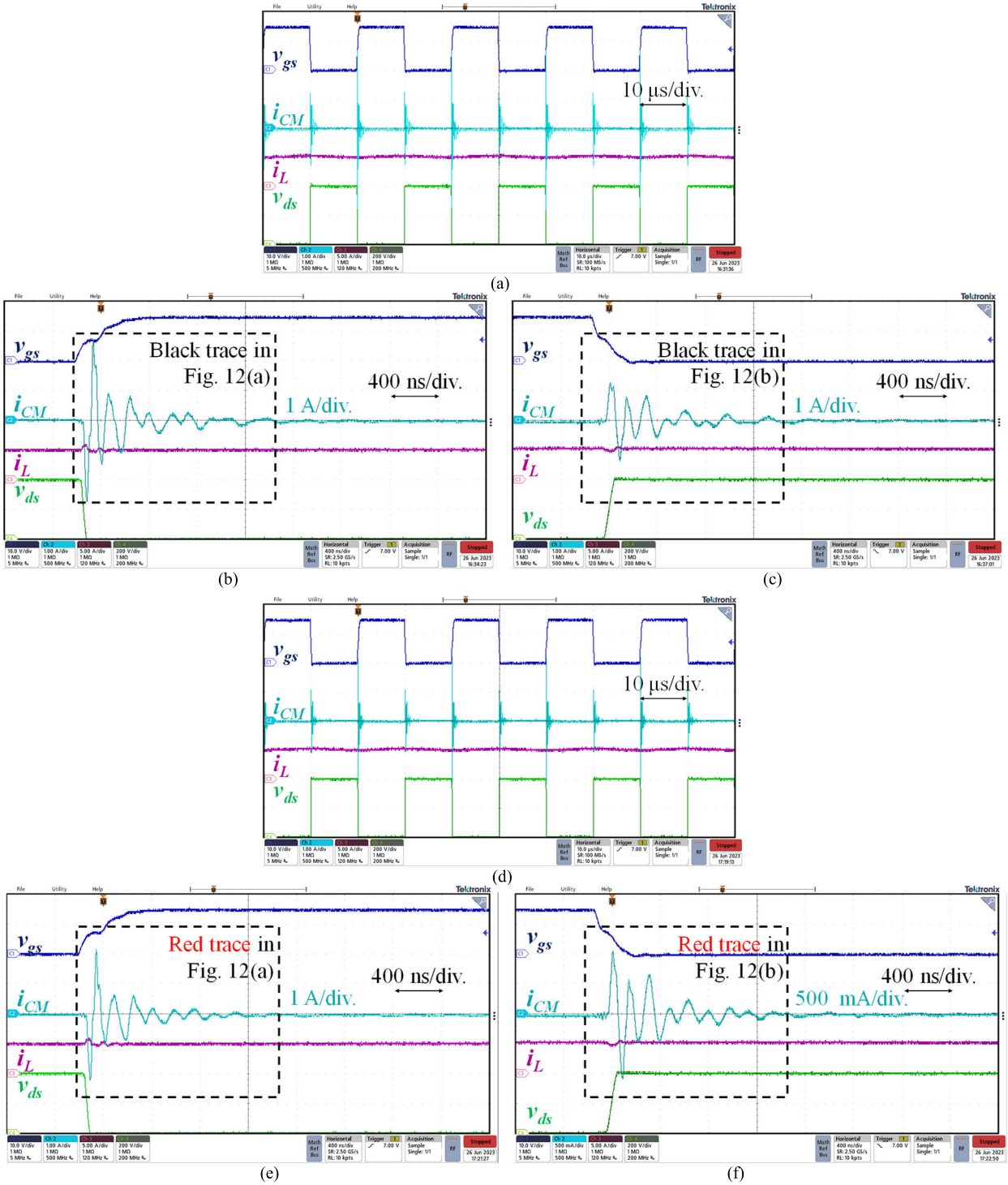

FIGURE 11. Experimental waveforms of the conventional module in (a) steady-state operation, (b) turn-on transition, and (c) turn-off transition. Experimental waveforms of the proposed module in (d) steady-state operation, (e) turn-on transition, and (f) turn-off transition.

Figs. 5(a), 5(b), and 5(c) show the simulation results of the proposed power module with 17-ppm/K, 29-ppm/K, and 41-ppm/K coefficient of thermal expansion (CTE) for the supporting epoxy, respectively. It is noted that the busbars are not presented for a clear view. Maximum deformations are observed to be 9.61 μm, 9.82 μm, and 10.04 μm, respectively. The results represent low CTE introduces low deformation. In this study, epoxy with 17-ppm/K CTE is used. It is noteworthy that CTE values lower than 15-ppm/K are not general for epoxy or resin.

Fig. 6 describes the simulation result of the proposed power module without supporting epoxy. It experienced large mechanical deformation at N_O near the busbar as indicated by the dashed circle. It is observed that most of the

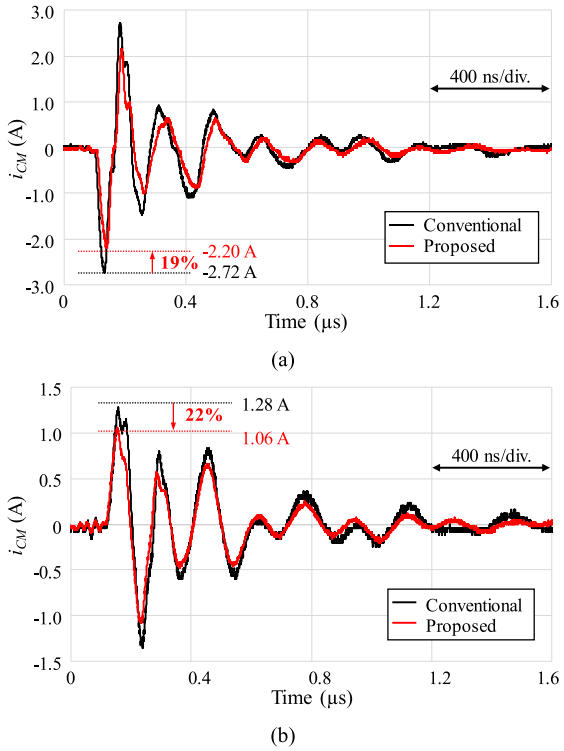

FIGURE 12. Comparison of i_{CM}. Black and red traces are for the conventional and proposed modules, respectively. (a) At turn-on instants (time scale: 400 ns/div.). (b) At turn-off instants (time scale: 400 ns/div).

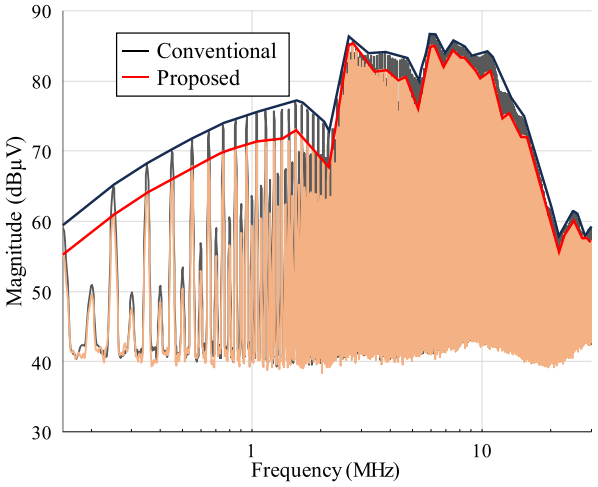

FIGURE 13. Measured CM noise of the conventional (black) and proposed (red) modules.

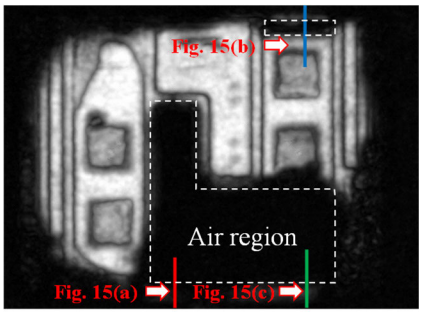

FIGURE 14. C-SAM image of the proposed power module after TCT.

deformation is concentrated on the edge of N_O, which can cause severe failures near the busbar, though the 9.48-μm maximum deformation is comparable with the proposed module. Section IV-B further provides evidence of the improved mechanical robustness.

C. THERMAL PERFORMANCE

A steady-state thermal simulation of the conventional and proposed modules was performed by Ansys 2023 R2 Icepak assuming that the coolant temperature is 65° with 8-liter/minute flow rate. A Thermal load of 10 W was assigned to the top surface of each die. The thermal conductivity of the supporting epoxy was set as 0.2 W/m· K. Figs. 7(a) and 7(b) show the simulation results of the conventional and the proposed modules, respectively. The maximum temperature of Q_2 near the etched area is 91.9 °C and 92.8 °C for the conventional and the proposed power module, respectively. It is noted that almost no thermal degradation is confirmed though the thermal distribution in N_O becomes slightly different. The thermal performance was also verified by measurement in Section IV-C.

D. MANUFACTURING PROCESS OF THE PROPOSED POWER MODULE

This section introduces the manufacturing process to validate manufacturability of the proposed power module [29]. The reflow soldering was conducted after placing all components in a jig. After the reflow, the supporting epoxy is applied to the corner of the etched areas as shown in Figs. 8(a) and 8(b). The epoxy was selected with low CTE based on the simulated results in Section III-B, which is 17 ppm/K in this study. In addition, the viscosity of the epoxy should be high enough to maintain its shape until curing. This study employs an epoxy with 56-Pa· s viscosity. The epoxy is cured in a temperature chamber after injection. The chamber was set 130°C for 5 minutes and 160°C for the next 10 minutes, which should be properly set based on the epoxy material being used.

A case was integrated, and wire bonding was carried out afterwards. Encapsulant which is silicone gel in this study is finally packaged. The gel underwent curing at a temperature of 80°C for 1 hour within a temperature chamber.

Fig. 9 shows the prototype power module without silicone gel for a clear view. A terminal at the baseplate was designed to facilitate the ground connection. It is noted that the size and outward view of the proposed power module are almost the same as the conventional power module.

IV. EXPERIMENTAL VERIFICATION

A. EXPERIMENTAL SETUP

Fig. 10 shows the experimental setup to measure the CM noise and the specifications are listed in Table 2. Two line impedance stabilization networks (LISN) NNBM8124 are

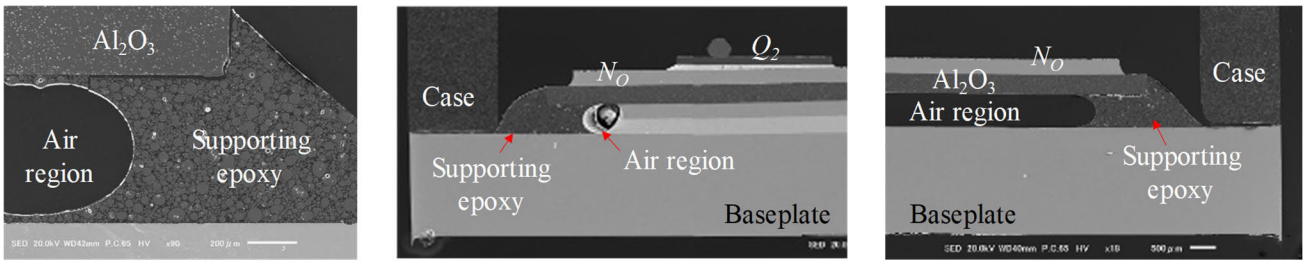

FIGURE 15. Cross-section images captured by SEM along (a) red line, (b) blue line, and (c) green line in Fig. 14.

TABLE 2. Specifications of the circuit to measure CM noise.

Input voltage	400 V
Output voltage	200 V
Switching frequency	50 kHz
L	7 mH
P_o	1 kW
C_{out}	401.8 µF
R	40 Ω
LISN	NNBM8124
DC Power Supply	HX01000-12G2
Spectrum Analyzer	RSA306B

used to separate the CM noise and connected to the DC power supply HX01000-12G2. Currents i_{CM} and i_L flow through the LISN and the inductor L, respectively. The gate-source and drain-source voltage of Q_1 are defined as v_{gs} and v_{ds}, respectively. Gate and source nodes of Q_2 were shorted to prevent false turn-on. The oscilloscope Tektronix MDO34 with 1-GHz frequency bandwidth and 5-GS/s sampling rate was used to capture the waveforms. Current i_{CM} was measured by a current probe, IWATSU SS-281-A-H with a sensitivity of 200 mV/A and a frequency bandwidth up to 30 MHz. A Tektronix TCP0030A was used to sense i_L. A Tektronix THDP0200 differential voltage probe measured v_{ds} with a frequency bandwidth of 200 MHz. The same gate driver boards were used for both modules to equalize the switching speeds and guarantee fair comparison.

B. CM NOISE MEASUREMENT

Fig. 11(a) shows the experimental waveforms of the conventional modules with 10 μs/division. Figs. 11(b) and 11(c) enlarge Fig. 11(a) presenting turn-on and -off instants with 400-ns/division time scale. Each channel shows v_{gs} (bule trace, 10 V/div.), i_{CM} (sky-blue, 1 A/div.), i_L (Magenta, 5 A/div.), and v_{ds} (200 V/div.), respectively. Experimental waveforms of the proposed module are shown in Figs. 11(d), 11(e), and 11(f). Fig. 11(d) describes with 10-μs/division time scale and Figs. 11(e) and 11(f) present turn-on and -off instants with 400-ns/division time scale, respectively.

The i_{CM} of the conventional and proposed modules during 1.6 μs after turn-on and -off of Q_1 are compared in Fig. 12. At the turn-on instant in Fig. 12(a), peak magnitudes of i_{CM} were 2.72 A and 2.20 A for the conventional (black trace) and proposed modules (red), respectively. The proposed module achieved a 22% reduction in i_{CM} compared to the conventional module. Similarly, i_{CM} was decreased in the proposed module by 20% at the turn-off instant as shown in Fig. 12(b). All traces are found in Fig. 11 as shown by black dashed boxes.

Fig. 13 compares the measured CM noise spectra of the conventional (black) and proposed (orange) modules in the frequency domain. The noise separator CMDM8700B was connected to the LISNs to analyze CM noise. The spectrum analyzer RSA306B was used in conjunction with the software SignalVu by Tektronix. A peak detector with 9-kHz resolution bandwidth was used to capture the CM noise. The proposed module exhibited lower amplitude than the conventional module by 5 dBμV in the frequency range below 2 MHz. At higher frequency, improvement by 1–5 dBμV was observed.

C. THERMAL CYCLING TEST

Thermal cycling tests (TCT) were conducted to validate the reliability against mechanical stress resulting from passive temperature changes. The lowest and highest storage temperatures were set at –40°C and 125°C, and each temperature was maintained for 30 minutes based on AQG324 standards [34]. The TCT underwent a total of 1000 cycles to assess thermal fatigue in the supporting epoxy. Constant-depth mode scanning acoustic microscope (C-SAM) captured horizontally inverted images of the proposed power module as shown in Fig. 14. White dashed area is the air region which is not observed by C-SAM. This study confirms the reliability of the power module in both mechanical and electrical aspects.

The proposed power module was cut along the red, blue, and green lines to examine the mechanical stress near the supporting epoxy. Their cross sections are observed as shown in Figs. 15(a), 15(b), and 15(c), respectively. Those were captured by scanning electron microscope (SEM). No deformation of epoxy and ceramic layer was observed. The SEM images confirmed that the supporting epoxy sustained the DBC well even after the TCT.

To evaluate the degradation level of electrical performance, the output characteristics (drain current versus drain-source voltage) of both conventional and proposed power modules

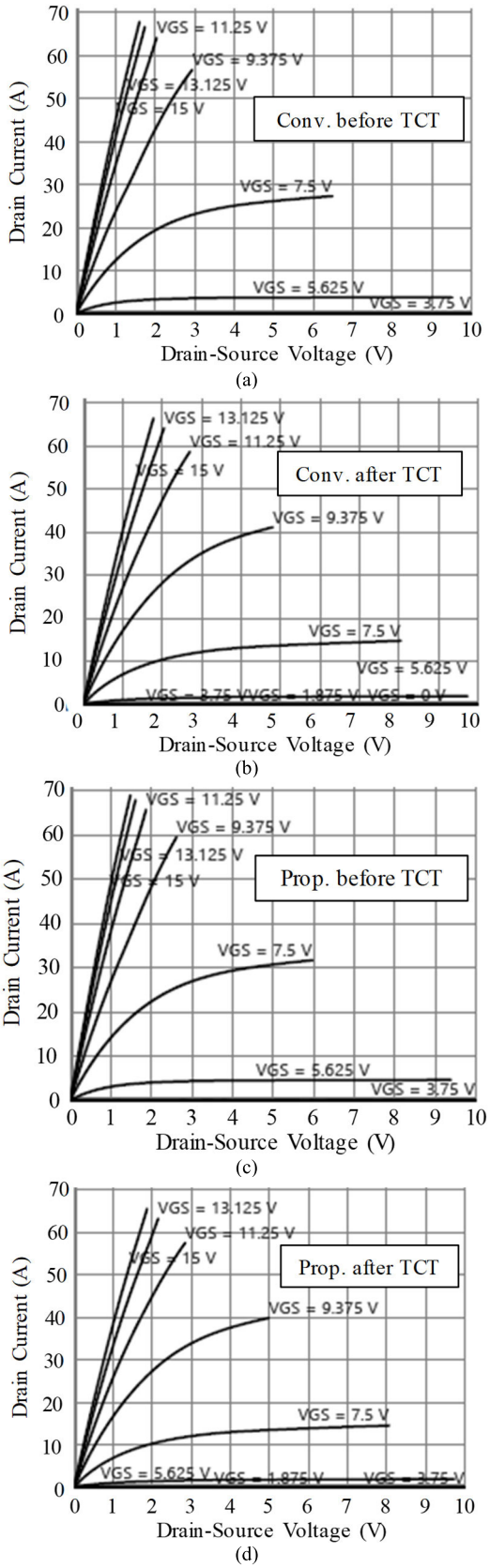

FIGURE 16. Measured output characteristics of Q_2. (a) Conv. before TCT. (b) Conv. after TCT. (c) Prop. before TCT. (d) Prop. after TCT.

were measured using the Keysight B1506A device analyzer. Fig. 16 shows the output characteristics of Q_2. Figs. 16(a) and 16(b) present those of conventional module before and after TCT, respectively, while Figs. 16(c) and 16(d) describe the characteristics of proposed module before and after TCT, respectively. The results are similar to those of the conventional module. In addition, other characteristics such as transfer characteristics, body diode forward characteristics, and capacitances were also equivalent to those of the conventional power module after TCT. This demonstrates that the proposed module maintains its electrical performance on par with the conventional module.

D. THERMAL RESISTANCE

Structure functions were measured with Power Tester 1500A by Mentor Graphics (Now Siemens EDA) to verify that the proposed module does not compromise the thermal performance. Fig. 17(a) shows the setup for measuring the thermal resistance from the Q_2 to the baseplate $R_{th.Q2}$. The power modules were set on the cold plate by the two fixtures from the top frame with 0.5-N· m torque. The thermal resistance $R_{th.Q2}$ of each module was measured after the body diode of

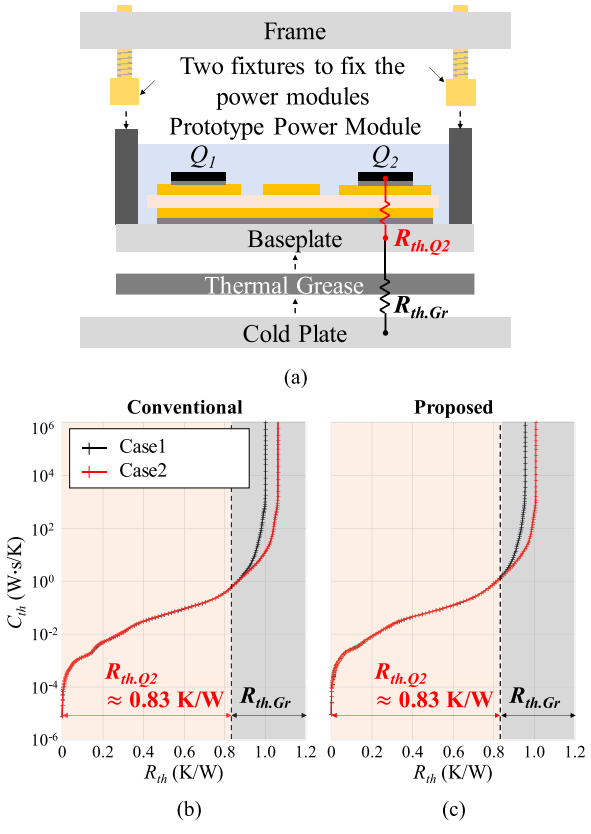

FIGURE 17. (a) Setup for measuring structure function. Measured structure functions of (b) the conventional and (c) proposed modules. Case 1 and Case 2 are with enough and small amount of thermal grease, respectively, to separate $R_{th.Q2}$ and the thermal resistance of thermal grease $R_{th.Gr}$.

Q_2 carried 13 A for 30 seconds. The gate-source voltage v_{gs} of Q_2 was adjusted to –3 V, allowing the current pass through the body diode exclusively. This measurement was conducted twice, i.e., with enough (Case 1) and small (Case 2) amount of thermal grease, to separate $R_{th.Q2}$and the thermal resistance of thermal grease $R_{th.Gr}$.

Figs. 17(b) and 17(c) show the structure functions of the three modules where C_{th} denotes their thermal capacitance. Red and black traces represent Case1 and Case2, respectively. The point where the two traces meet represents $R_{th.Q2}$. Both modules provide almost the same $R_{th.Q2}$, 0.83 K/W, which proves compatible thermal performance of the proposed module.

V. CONCLUSION

This paper proposes a novel SiC power module to reduce CM noise and improve reliability. A specific portion of the bottom copper layer in a DBC was replaced with air. The measured CM capacitance was reduced by 62.7%, and CM noise captured by LISN and peak detector was attenuated by 5-dBμV. This design did not compromise the thermal resistance of the power module. The simulated temperature of the proposed module was higher than the conventional counterpart by 0.9° only. Epoxy with 17-ppm/K CTE was added between the top copper layer of the DBC and the baseplate to reinforce mechanical reliability. Images by C-SAM and SEM proved the mechanical ruggedness of the proposed power module. The output characteristics and the thermal resistance of the proposed module showed less degradation during the thermal cycling test than the conventional counterpart.

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