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RESEARCH ARTICLE

Neuromorphic Spiking Sensory System With Self-X Capabilities

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ABSTRACT Effectively interfacing synthetic systems with a tangible world using a growing number and variety of sensors under the constraints of precision, resilience, and adaptability is indispensable. In particular, system integration employing leading-edge technologies is both rewarding and challenging because of signal swings, manufacturing deviations, and noise. Utilizing the general self-X concept and the transition from a common amplitude-domain to biology-inspired adaptive spike-domain processing offers a viable solution. In this work, a neuromorphic concept and the first prototype of an adaptive spiking sensory front-end with self-X properties were designed and fabricated using XFAB CMOS 0.35 μm technology. The chip includes synapse, neuron, self-adaptive spike-to-rank coding (SA-SRC), and adaptive coincidence detection (ACD) cells with areas 0.086 mm x 0.046 mm, 0.06 mm x 0.041 mm, 0.75mm x 1.3 mm, and 0.123 mm x 0.336 mm, respectively. The cells were applied to achieve an adaptive sensor signal-to-spike converter (ASSC) feeding SA-SRC, followed by a decoder to a 4-bit digital code. Characterization achieved differential non-linearity (DNL), integral non-linearity (INL), missing codes, effective number of bits (ENOB), and signal-to-noise and distortion ratio (SINAD), with values of 0.41 LSB, 0.3 LSB, no missing codes, 3.82 bits, and 24.79 dB respectively. The system consumed 321 μW of power, required 158 pJ per conversion, and had a conversion speed of 492 ns. A final angular decoder system application with Tunnel Magnetoresistance (TMR) sensors revealed our spiking sensory front-end's ability to reduce the angle measurement error from 24.95 to 12.72 degrees due to adaptation after system perturbation.

INDEX TERMS Neuromorphic spiking sensory system, presentation of information in the spike domain, spiking neural networks, self-X, adaptive spiking sensory systems.

I. INTRODUCTION

The fields of sensor technology and sensory systems are experiencing rapid growth and diversification, with a wide range of practical applications [15]. With the continuous development of novel sensory concepts and physical transduction elements coupled with substantial advancements in integration technology, both new and existing components are becoming progressively smaller [16]. On one hand, integration technologies have simplified the utilization of sensors and related systems; on the other hand, they have introduced greater challenges for the design of corresponding electronics. The incorporation of state-of-the-art technologies for the realization of mixed-signal systems yields advantages in terms of the power efficiency and processing speed, as noted in [18] and [19]. This phenomenon can primarily be attributed to the lower supply voltages and decreased capacitance values. As integration technologies for scaling continue to progress, traditional analog designs that rely on the representation of information in the amplitude domain

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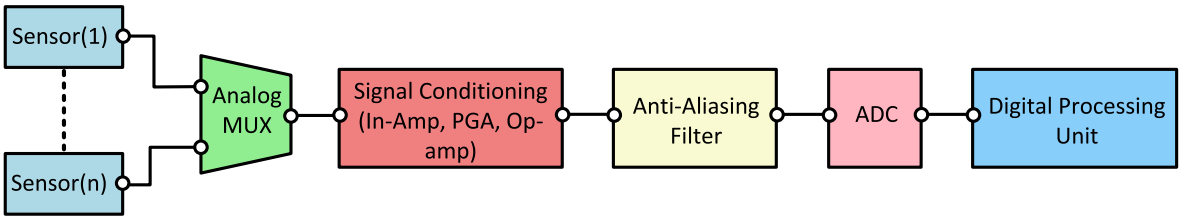

FIGURE 1. The block diagram of the traditional sensor signal interface chain is shown. Sensor signal conditioning includes several functions, such as using programmable gain amplifiers (PGAs) with operational amplifier (op-amp) circuits to adjust the signal to the ADC's full-scale voltage. An anti-aliasing filter reduces signal noise to comply with the ADC's resolution needs.

face increasingly formidable challenges [17], [20], [23], [24]. As elucidated in [21] and [22], circuit design faces complexities, including challenges, such as reduced signal amplitude, diminished intrinsic device gain, heightened noise levels, exacerbated device mismatch, dwindling supply voltage, and variations in the manufacturing process. These obstacles collectively underscore the evolving landscape and the heightened demand for modern analog design practitioners. Effectively establishing connections with numerous sensors in either single or multi sensor systems presents notable challenges [25].

The development of reliable analog front ends (AFEs) is of utmost importance for the comprehensive effectiveness of application systems [45]. To ensure optimal performance, sensor systems require analog front-ends that offer high accuracy, robustness, and adaptability, along with self-X attributes including self-calibration, self-healing, self-adaptation, self-optimization, and self-trimming, as emphasized in [46]. Fig. 1 shows the conventional signal interface chain of a sensor [46]. This interface serves critical functions, including sensor signal conditioning, anti-aliasing filtering, and analog-to-digital conversion (ADC). The small sensor signal may be further amplified through an additional gain stage after the in-amp. This stage uses programmable gain amplifiers (PGAs) based on operational amplifier (op-amp) circuits to match the signal to the ADC's full-scale voltage. The anti-aliasing filter then minimizes signal noise to meet the ADC's resolution requirements. If an active filter is used, it can also provide additional amplification. Additionally, the fully-differential active filter can function as the ADC driver, managing its high input load and aligning the filtered signal to the ADC's common-mode voltage. The ADC unit then converts the conditioned analog signal to digital form for interfacing with the digital processing unit. In particular, complex mixed-signal systems such as analog-to-digital converters (ADCs) encounter these challenges when transitioning to smaller technology nodes [22], [26], [27], [28].

State-of-the-art approaches are dedicated to addressing the difficulties related to analog-to-digital converters (ADCs), and numerous configurations have been suggested in scholarly works. Semtech Inc. introduced the Zooming ADC concept, embodied in chips such as SX8724, which boasts digital reconfigurability. The aim was to overcome the limitations associated with traditional ADCs. The core principle underlying Zooming ADC is a well thought two-step process. It commences with an initial low-resolution ADC stage responsible for the coarse conversion of the input signal. The output of this stage subsequently undergoes processing using a digital-to-analog converter (DAC). The divergence between the original input signal and the DAC's output constitutes what we refer to as the 'residue,' which is then subjected to further refinement in the second stage. In the second stage, a fine ADC with a restricted conversion range was employed. In recent years, there has been a surge in the introduction of hybrid ADCs [48], [49], [50], [51], [52], which effectively combine the strengths of diverse architectural approaches to attain superior performance that transcends the capabilities of a single architecture. The Zooming ADC, a prime example within this category [51], ingeniously merges successive-approximation-register (SAR) ADC and delta-sigma modulator ADC designs, capitalizing on their unique attributes to achieve remarkable resolutions and energy efficiency.

The proposed study [29] introduced an architecture for an analog-to-digital converter (ADC) called a pipelined Hopfield neural network memristive ADC. This approach aims to leverage the advantages of memristors in terms of their area and power efficiency, thereby overcoming constraints typically associated with traditional ADCs. The integration of memristors enables the development of an analog-to-digital converter (ADC) based on neural networks. Their proposed architecture comprised three modules: a random perturbation unit (RPU), neuron unit, and 2T2R synaptic unit. The 2T2R synaptic units consisted of two memristors, an inverter, a PMOS tube, and an NMOS tube, all of which were controlled by the RPU. The RPU primarily consists of operational amplifiers, data selectors, NAND gates, a random number generator (RNG), and a T trigger.

The researchers in [30] introduced an artificial neural network (ANN) analog-to-digital converter (ADC) that incorporates subranging and non-uniform memristors. This design addresses the device-mismatch issue by employing a trainable memristor weight that can be adapted. The proposed architecture consists of a composite structure featuring a 2T1R weight unit circuit, a converter stage with amplifiers to enhance the gain, neurons composed of a trans-impedance amplifier (TIA) and inverter, and a feedback circuit for control purposes. Furthermore, the researchers in [31] and [32] presented a synthesizable ADC that aims

to overcome the obstacles encountered in conventional ADC design. The ADC architecture comprises three distinct hardware layers parallel to a conventional neural network structure: the foundational input layer, intricate hidden layer, and ultimate output layer. To construct these layers, resistive random-access memory (RRAM) crossbar arrays and static CMOS inverters were employed. Moreover, they employed scalable and synthesized operational amplifiers and analog inverters within the RRAM crossbar. To obtain the output, they applied Thevenin's theorem to RRAM crossbar arrays.

However, the ADCs featured in [29], [30], [31], [32], [48], [49], [50], [51], and [52] employed amplitude-coded signals, a technique that utilizes varying signal amplitudes to represent different data values. Although widely recognized, this method faces challenges in contemporary CMOS technology nodes. In contrast, adjusting the dimensions of transistors and the supply voltage in CMOS technology results in a decreased gate delay within digital circuits. Consequently, this advancement in CMOS scaling results in improved time resolution and sparking increased interest in the time domain, as documented in [33]. This incentive prompted researchers to design systems that utilize spike or time-coded signals, characterized by their technology-agnostic attributes, which maintain resilience even as technology advances, as evidenced in the studies cited [34], [35], [36]. Converting continuous input signals into pulse frequencies by utilizing a significant array of spikes may lead to escalated energy usage, particularly when the spiking neural network (SNN) architecture becomes more extensive and complex. As a result, these characteristics may not align with the requirements of power-efficient and resilient devices in the context of edge computing, as discussed in [37], [38], and [39]. In response to these challenges, a prior version of the sensor-to-spike-to-digital converter (SSDCα) chip was engineered to employ spike timing, along with the adapted concept of acoustic localization for a novel ADC concept [40]. In this endeavor, the concept was opportunistically leveraged and applied to different domains. Nonetheless, this design lacks adaptivity, which is crucial for sustaining system functionality during aging, drift, damage, or lesions. The capacity to devise a precise, robust, adaptable design and resilience is of paramount importance to ensure the success of the application system.

Subsequently, the pivotal components of our envisioned neuromorphic spiking sensory system, distinguished by its inherent self-X capabilities and utilization of spike-based or time-coded signals, were successfully integrated into our chip [47]. The implemented system incorporates a technology-agnostic attribute and retains its robustness despite technological advancements. This adaptive methodology has the potential to address a spectrum of challenges, including various types of degradation, such as static and dynamic, as well as reversible and irreversible. In previous research [41], [42], [43], [44], we introduced the concept of utilizing spike timing to adapt acoustic localization to a novel neuromorphic spiking sensory system.

The structure of the paper is outlined as follows: Section II discusses insights drawn from biological sensory systems, focusing on the adaptation of acoustic localization principles to a novel neuromorphic spiking sensory system. Section III delves into the neuromorphic system electronics, aiming to develop a self-X capable neuromorphic spiking sensory system that transmits information via spike timing, integrating the adaptive sensor signal-to-spike converter (ASSC) and self-adaptive spike-to-digital converter (SA-SDC) components. Section IV covers the integration of neuromorphic system components, highlighting the spike domain segment's completion using the chip. Section V presents the characterization and application of the neuromorphic chip, showcasing the measurement characteristics of the implemented system on the fabricated chip. Finally, Section VI provides the conclusion of the study.

II. INSIGHTS DRAWN FROM BIOLOGICAL SENSORY SYSTEMS

Organisms possess an impressive capacity to perceive both physical and chemical attributes [1], [2]. In addition, they exhibit adaptability to environmental variations and the emergence of faults and lesions. Neural networks play pivotal roles in orchestrating this regulatory process. Within living entities, sensory systems focus on harboring a myriad of sensors interconnected with peripheral neural ensembles [3].

Acoustic localization is an exception to this pattern. It involves the localization of various objects, such as predators, water, prey, or food, through the utilization of spatially separated pairs of sensors [4], [5], [6], [7], [8], [9]. Organisms utilize the time lag between signal arrivals in their two ears, termed the interaural time difference (ITDs), to determine the source of a sound. Temporal information can then be mapped onto a network of nerve cells as a spatial representation. A theory supporting this mapping was proposed by Jeffress (1948). Jeffress (1948) formulated a theory based on the three fundamental assumptions, outlined by Ashida and Carr [4]. These assumptions are:

1. An organized configuration of ascending nerve fibers within the conduction pathways functions as a delay line. 2. Subsequently, an ensemble of coincidence detectors transforms the synchronized inputs into the output spike rates. 3. Ultimately, a neuronal place map was created within the cell array by implementing deliberate alterations in the spiking rates.

Fig. 2a presents a unique SNN model tailored to acoustic localization. Fig. 2b shows a neuromorphic spiking sensory system that incorporates adaptive mechanisms within a dual-stage framework, effectively mimicking Jeffress's model [10]. Our primary goal is not to enhance acoustic localization but to adapt this concept to a novel neuromorphic spiking sensory system. In the initial phase, the incoming sensor signal is transformed into a pair of spikes by an adaptive sensor signal-to-spike converter (ASSC). These spikes exhibit a variation in time difference (TD) contingent upon the incoming sensor signal. In Fig. 2b, the second

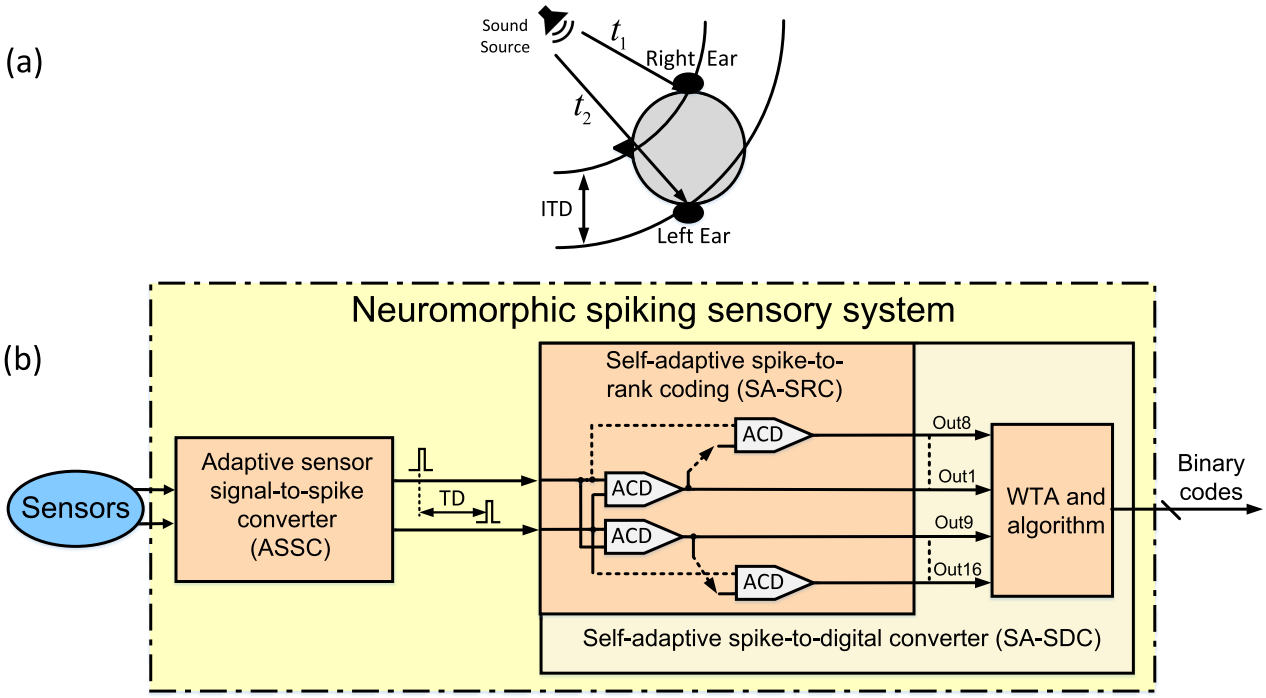

FIGURE 2. (a) Acoustic localization mechanism. The brain determines the position of a sound source by analyzing the interaural time differences (ITDs) between the signals received at each ear, denoted as t_1 and t_2, with t_2 representing the time the sound reaches the left ear and t_1 the right ear. (b) Architectural representation of the proposed neuromorphic spiking sensory systems. The adaptive sensor signal-to-spike converter (ASSC) unit converts the sensor's signal into two distinct spikes occurring at different times, dependent on the sensor input. The self-adaptive spike-to-rank coding (SA-SRC) block then produces a digital code based on the temporal difference between these spikes. The SA-SRC comprises two primary components: adaptive coincidence detection (ACD) and winner-take-all (WTA), which include memory.

component, known as the self-adaptive spike-to-digital converter (SA-SDC), incorporates Jeffress's (1948) theoretical framework based on three fundamental assumptions. The first assumption is actualized through synaptic weights, whereas the second is executed by an array of adaptive coincidence detectors (ACD). These detectors transform the time differences (TDs) of the dual input pulses into ranked spike code. Finally, the third assumption is realized by winner-take-all (WTA) mechanisms and algorithms, to transmute the ranked spike code into a digital representation.

III. NEUROMORPHIC SYSTEM ELECTRONICS

The increasing need for sensor systems in IoT and Industry 4.0, capable of efficient performance in dynamic settings and addressing the constraints of traditional amplitude-based sensors, has become evident. The objective of this study was to develop a novel neuromorphic spiking sensory system with self-X capability. This system exhibits promising attributes, such as operating at a low voltage, robustness against noise, and minimal power consumption, thereby addressing the challenges posed by technology scaling. The neuromorphic spiking sensory system is designed to convey information via spike timing, rendering it well suited for integration into sophisticated electronic sensor systems. The envisioned neuromorphic spiking sensory system comprises the ASSC and SA-SDC components, as depicted in Fig. 2.

A. ADAPTIVE SENSOR SIGNAL-TO-SPIKE CONVERTER (ASSC)

The sensor response span rarely matches the SA-SDC input range, as shown in Fig. 3. In cases where the sensor's operating range is narrower than the input span of the SA-SDC, as shown in Fig. 3a, the SA-SDC's dynamic range remains underutilized, leading to non-utilization of all available ACDs. Conversely, when the sensor span surpassed the SA-SDC input range, as indicated in Fig. 3c, the sensor data became inaccessible. Additionally, instances exist where the spans are both equal, but offset (Fig. 3b). In another scenario, there is a difference in duration (400 ns and 600 ns) and a 200 ns offset between the spans, as shown in Fig. 3d. Frequently, the spans exhibit inequality and offset, necessitating level-shifting and amplification in the time domain to align them. The lack of alignment between the spans necessitates either a costly expansion of the dynamic range of the SA-SDC, or results in the loss of sensor data. Consequently, achieving optimal performance requires aligning both the sensor and the SA-SDC spans. To accomplish this, the ASSC serves as an essential conditioning circuit, ensuring that the spans are equal without the need for level-shifting. Remarkably, the ASSC is sufficiently versatile to simultaneously amplify and level shift the sensor signal in the time domain. Using our approach, we adapted the zooming ADC concept from the amplitude domain to spike domain.

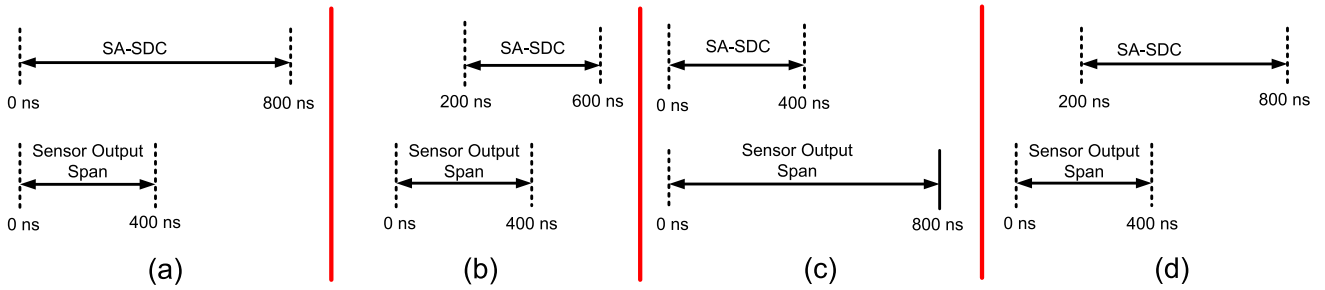

FIGURE 3. Here are instances where corrections are required: (a) The sensor's range is smaller than the SA-SDC's input range. (b) Another scenario emerges when the sensor and SA-SDC appear to have matching operational ranges, yet there is an observable offset or misalignment between them that warrants correction. (c) The sensor's range surpasses the input range of the SA-SDC. (d) Both the sensor and SA-ADC feature distinct ranges and experience a positional offset.

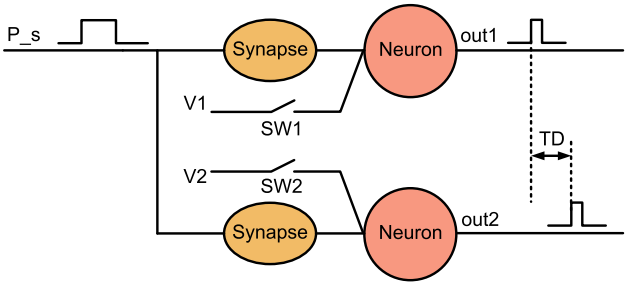

FIGURE 4. Block diagram of proposed adaptive sensor signal-to-spike converter (ASSC). ASSC consists of two elements: a pair of synapses and a pair of neurons. The synaptic inputs are interconnected, with each synapse's output connected to a neuron. Furthermore, each neuron is linked to an individual switch, which in turn is connected to the V1 and V2 inputs.

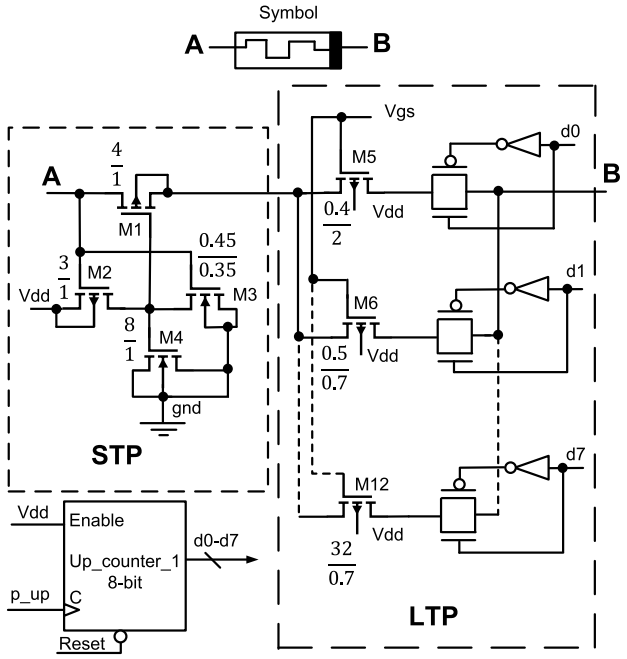

FIGURE 5. The synapse schematic of the ASSC and ACD blocks. The CMOS-emulated memristor mimics the synaptic plasticity found in biological synapses, including both long-term plasticity (LTP) and short-term plasticity (STP). This circuit embodies the adaptive synapse (AS) in our proposed design, with transistor dimensions in μm. In the ACD block, the up-counter is controlled by the autonomous control circuit shown in Fig. 8.

The proposed ASSC comprises two components, two synapses and two neurons as shown in Fig. 4. Synaptic inputs are interlinked with the output of each synapse linked to a neuron. Additionally, every neuron is connected to a single switch, which is then connected to V1 and V2 inputs. In a previous study [11], [42], we introduced an adaptive synapse concept that employs a CMOS-emulated memristor as a synapse equivalent to mimic both the short-term plasticity (STP) and long-term plasticity (LTP) observed in biological synapses. A schematic of the proposed adaptive synapse is shown in Fig. 5.

Several biological neuronal models, possess a range of distinct properties. The attributes necessary for successful implementation of the proposed design were examined. This implementation functions akin to a neural network time delay, where the time required for the initial spike corresponds inversely to the magnitude of the incoming charge. These attributes are intrinsic to all spiking neuron models. To align with the specifications of this study while minimizing the count of adaptation variables and transistors, we modified and eliminated unnecessary components from the leaky integrate-and-fire (LIF) neuron model proposed by Indiveri in 2003 [12]. Indiveri's LIF analog neuron model, designed to replicate the intricacies of biological neurons, encompasses a comprehensive set of elements, including provisions for establishing an arbitrary refractory period, modulating the neuron's threshold voltage, regulating the spike frequency adaptation, introducing positive feedback, integrating a transistor for current leakage, integrating a membrane capacitor, and incorporating a digital inverter for pulse generation. This neuron circuit, although notably flexible in its construction, is primarily oriented toward emulating biological neurons. Consequently, this design approach yielded an increased number of adaptation variables and higher transistor count. We modified the neuron model proposed by Abd and König [42] to align it with the specific requirements of ACD while concurrently improving power efficiency, enhancing processing speed, and optimizing area

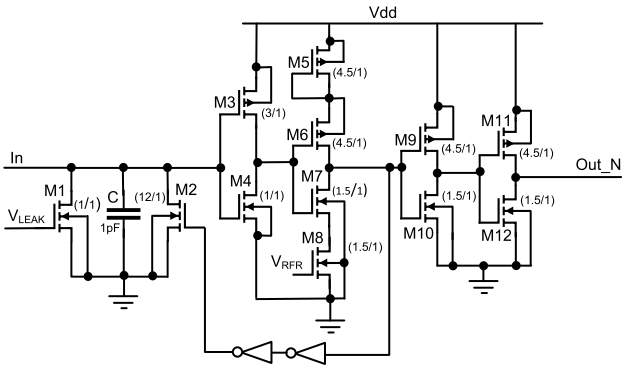

FIGURE 6. The analog leaky integrate-and-fire (LIF) neuron circuit, is customized to suit the requirements of implementing the ASSC and SA-SDC components. This circuit, characterized by transistor sizes measured in μm, represents a streamlined adaptation of Indiveri's neuron model and is tailored to align with the specific demands of this application.

utilization. Fig. 6 shows a schematic of the modified neuron model.

The ASSC operates in two distinct phases. In the initial phase, switches sw1 and sw2 are engaged, thereby allowing the membrane capacitors of neurons to undergo a charging process up to voltage levels V1 and V2, respectively. The second phase involves the opening of these switches, followed by the application of a precisely timed pulse to the synapses. This pulse finalizes the integration process of the membrane capacitors within the neurons, driving them toward the activation threshold, thereby inducing the generation of neuronal spikes. It is crucial to note that the time difference between the occurrences of these spikes is contingent on the voltage discrepancy between V1 and V2. Conventional signal conditioning systems commonly employ instrumentation amplifiers that function as signal-processing amplifiers. However, these systems rely on amplitude coding and are consequently more susceptible to the caveats of rapid technological advancement. In our envisioned neuromorphic spiking sensory system, amplification occurs within the time domain. The ASSC gain is calculated using the following equation:

$$ASSC\ gain = \frac{ASSC\ output\ span\ at\ weight\ A}{ASSC\ output\ span\ at\ weight\ B}. \quad (1)$$

The synaptic weights were regulated by both their Vgs values and the corresponding settings of their upper counters. Weight A can denote any adjustable weight configured to achieve the desired gain, while weight B signifies the weight of the synapses when the Vgs values are set to zero and the upper counters are set to 255. Because there are two synapses, this requires the use of two up-counters, Vgs1 and Vgs2. At the current stage of the work, the synaptic weights of the ASSC are controlled in an open-loop manner by adjusting the synapse weights via the counter, as well as Vgs1 and Vgs2. Fully automated control is part of the second hierarchical layer, which will be implemented in the subsequent phase of the project.

The offset refers to the difference between the sensor span and SA-SDC input span values that shift the transition from the "first code" digital output of the SA-SDC to the subsequent code increment. This offset is measured in the least significant bit (LSB) and can be calculated using the following equation:

$$offset = \frac{TDS}{LSB}. \quad (2)$$

where the time difference span (TDS) is the time difference between the sensor span and the SA-SDC input span. The gain and offset can be modulated by adjusting synaptic weights. The quantifiable bit capacity, denoted as the number of bits (NoB) achievable through the SA-SDC, is contingent on the time span of the ASSC, which can be extended through the application of gain. The determination of the maximum achievable number of bits, referred to as the maximum number of bits (MNoB) that the ASSC can provide, can be computed using the following equation:

$$MNoB_{ASSC} = ld(MNoL_{ASSC}). \quad (3)$$

where the maximum number of ASSC levels ($MNoL_{ASSC}$) is computed using the following equation:

$$MNoL_{ASSC} = \frac{time\ span\ of\ the\ ASSC}{LSB}. \quad (4)$$

B. SELF-ADAPTIVE SPIKE-TO-DIGITAL CONVERTER (SA-SDC)

The proposed SA-SDC comprises two integral elements. The first is self-adaptive spike-to-rank coding (SA-SRC), followed by the winner-take-all (WTA) mechanism and the algorithm, as illustrated in Fig. 2. SA-SRC produces spike orders that precisely mirror the temporal disparities among incoming spikes received by its inputs. These spike-order codes embody a coding approach contingent on the precise sequential organization of spikes within a cluster of neurons, which is directly influenced by the firing sequence of these neurons [13], [14].

In the current stage of development, the proposed SA-SRC utilizes a total of sixteen adaptive coincidence detection (ACD) units, as depicted in Fig. 7. The SA-SRC architecture is divided into upper and lower segments, generating outputs (Out1 - Out8 and Out9 - Out16) and accommodating single-ended or differential sensory inputs. Each segment employs two inputs (in1 and in2), with in1 directly entering the ACDs in the upper segment, and in2 forming the delay chains. In the lower segment, in2 is directly linked to ACDs, whereas in1 undergoes sequential processing. The temporal extent of the delay chain is influenced by the neuron firing time, which is modulated by synapse weights that adapt to timing variations. For a comprehensive understanding of the adaptation synapse, including detailed timing charts and explanations, more details on the adaptation synapse can be found in [42]. The central component of the SA-SRC architecture comprises an ACD, which is realized through the integration of a solitary neuron (N) and two adaptive

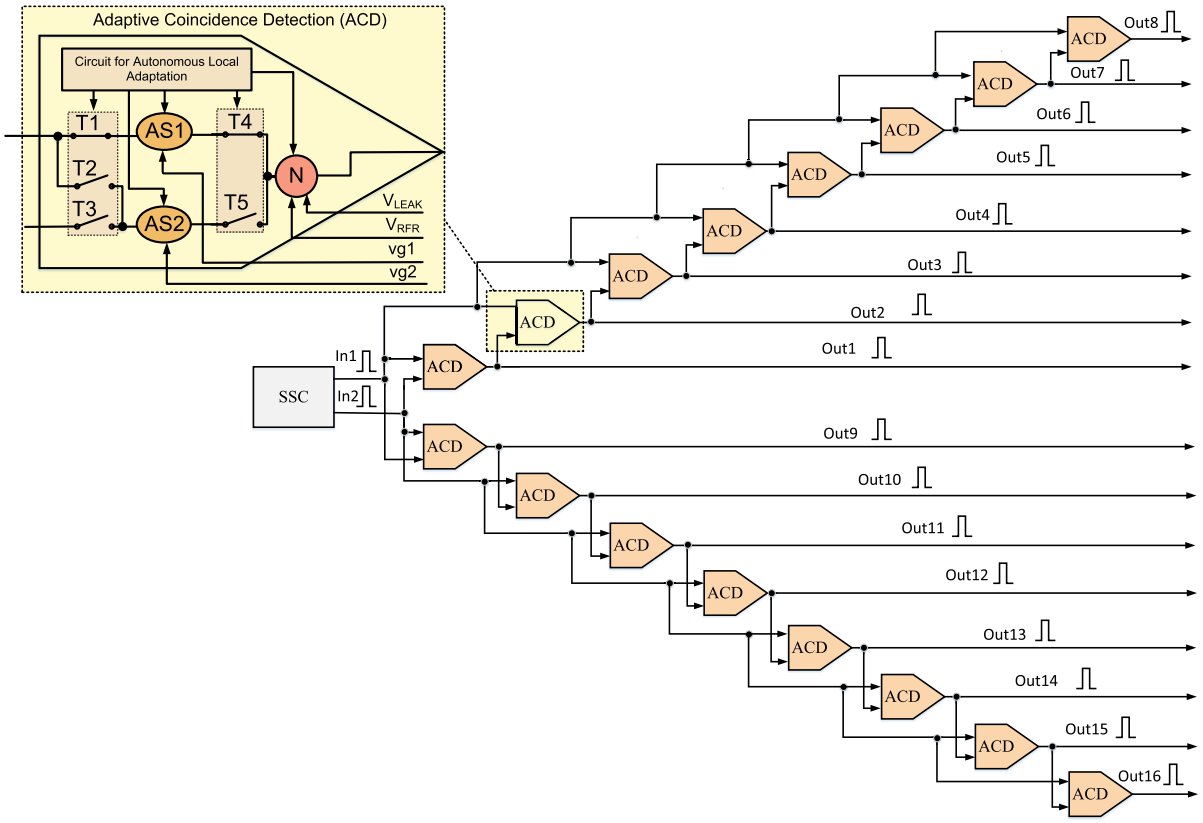

FIGURE 7. Proposed self-adaptive spike-to-rank coding (SA-SRC) scheme. The key component of the SA-SRC is the adaptive coincidence detection (ACD) block. The SA-SRC contains 16 adaptive coincidence detectors (ACDs), each comprising two adaptive synapses (ASs) and a neuron (N). The SA-SRC produces spikes that generate rank codes based on the time interval between the two input spikes. The SA-SRC harnesses self-X capabilities, underpinned by a dual-layer adaptivity framework. The initial layer is driven by the autonomous ACD circuit, while the subsequent layer leverages V_{LEAK} and V_{RFR} for neural regulation, and vg1 and vg2 to oversee synaptic operations.

synapses (AS), as depicted in Fig. 7. Schematics of the neuron and synapse are shown in Figs. 6 and 5, respectively.

The SA-SRC operates in two modes: normal and adaptive. In the normal mode, both synapses of the ACD are linked to the neuron. In this mode, the transmission gates T1, T3, T4, and T5 are active (on), while T2 is inactive (off), as illustrated in Fig. 7. In the adaptation mode, a two-layer adaptation hierarchy is used. The first layer operates at the ACD level and has two states: In the first state, the weight of the first synapse is adjusted, with only the first synapse connected to the neuron. All first synapses across the ACDs are linked in parallel (one column) and their weights are adjusted simultaneously. In this state, transmission gates T1 and T4 are on, while T2, T3, and T5 are off. In the second state, the weight of the second synapse is adjusted, with only the second synapse connected to the neuron. All second synapses across the ACDs are connected in parallel and their weights are adjusted at the same time. In this state, transmission gates T2 and T5 are on, whereas T1, T3, and T4 are off.

The synaptic weight determines when the neuron fires, making the firing time directly proportional to the synaptic weight. Two pulses, adapt_pulse and in1, monitor the neuron's firing time before and after the rising edge of the neuron's pulse, respectively. This monitoring is performed by an autonomous control circuit, as shown in Fig. 8. According to Fig. 8, the output of the first AND gate (left) should be 0 if the output of the neuron has not shifted left, as depicted in Fig. 9. Similarly, the output of the second AND gate (right) should be 1 if the output of the neuron has not shifted right, as shown in Fig. 9. The outputs of the first and second AND gates (left and right shift) are stored in D flip-flops DFF1 and DFF2. The first and second counters then adjust and store the weights of the first and second synapses, respectively. The Clear input serves multiple functions: it clears the outputs of DFF1 and DFF2 to prepare for the next weight check, discharges the neuron capacitor, and acts as the counter clock signal after inversion. The multiplexer passes the AND3 gate output at a specific time by setting the Read signal to zero. The selection signal of the multiplexer activates after completing the comparison of the adapt_pulse, in1, and Out_N signals and storing the results (left and right) in DFF1 and DFF2. The reset in the autonomous control circuit, as shown in Fig. 8, resets DFF3, DFF4, and DFF5. The Reset signal triggers the adaptation mode. DFF3 and DFF4 store the adaptive signals of the first and second synapses. The output Adapt signal from the NOR gate indicates that

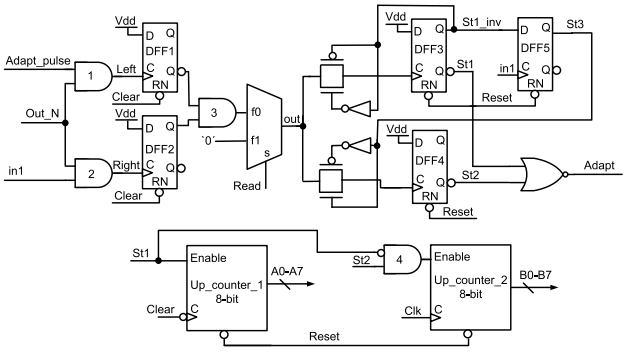

FIGURE 8. In the first layer, the autonomous control circuit within ACD achieves the self-adaptation of synaptic weights.

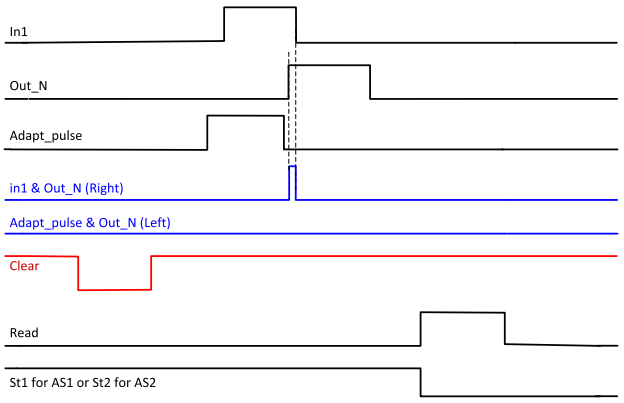

FIGURE 9. The timing diagram for the adaptive synapse. Two pulses, adapt_pulse, and in1, verify the neuron's firing time before and after the neuron's rising edge, respectively. When the neuron fires at a particular moment, the right signal is 1, and the left signal is 0. The Read signal is utilized to read data after a designated period.

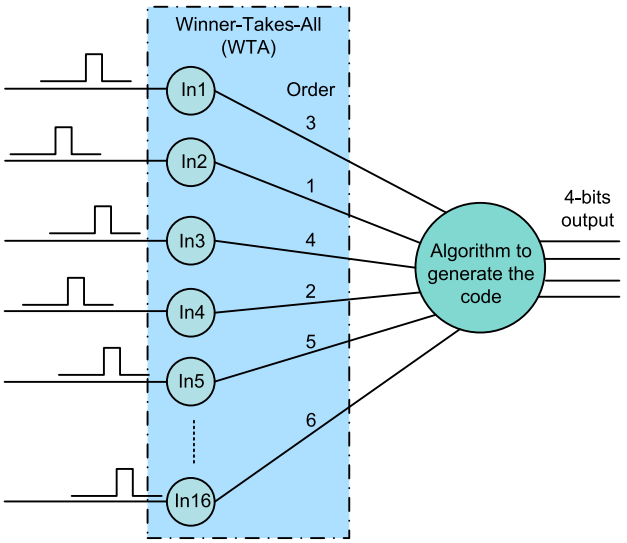

FIGURE 10. The implementation of the architecture of a state machine diagram of the WTA and the algorithm. To transform the rank order code outputs of the SA-SRC into digital values, the WTA identifies incoming signals and assigns an order based on their arrival time.

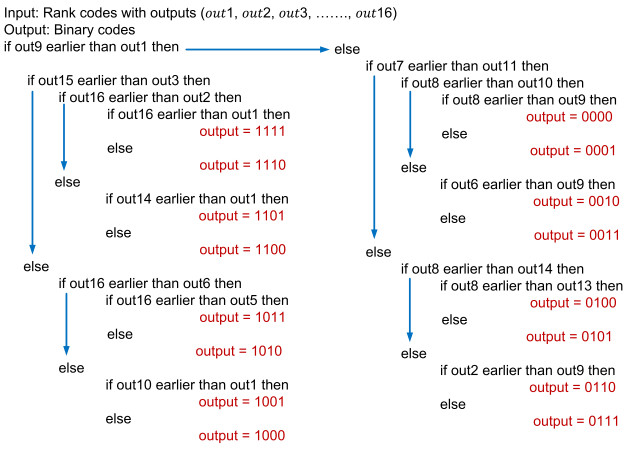

FIGURE 11. The rank code decoding algorithm is employed for the conversion of rank codes into binary codes.

the ACD is in self-adaptation mode when it is 0. The autonomous control circuit leads to unsupervised adaptation. At the first adaptation level, simultaneous adjustments for all ACDs occurred concurrently, ensuring uniform delays across connections. The primary factors affecting ACD performance are process, voltage, and temperature (PVT) variations, packaging effects, and aging effects. These factors are mitigated by the self-X feature of the ACD unit, achieved through two adaptation layers. The adaptation process is described in detail in [42].

The second level oversees hierarchical adjustments, focusing on variables such as V_{LEAK}, V_{RFR}, vg1, and vg2, and awaiting the completion of the first-level solution. The adaptation process involves resetting the membrane capacitor, manual adjustments to variables, and iterative updates, as explained in [42]. For a comprehensive understanding and detailed development, refer to [42] and [47].

The SA-SRC cell on-chip currently comprises 16 outputs, which are sparse rank-coded spikes. To convert the rank order code outputs of the SA-SRC into digital numbers, we designed the WTA circuit and algorithm using Verilog, a hardware descriptive language. WTA cells are responsible for determining the winner among SA-SRC outputs. The WTA detects incoming signals and assigns a corresponding order with respect to the time of arrival, as shown in Fig. 10. For example, in2 is the first; therefore, it assigns a value of 1 to in2. Similarly, in4 comes after in2, and it obtains a value of 2. Fig. 11 depicts the algorithm implemented on Red Pitaya 2, which is aimed at decoding rank codes into binary codes. The current conversion of the rank-order code into digital numbers is a possibility for demonstrators and can be subject to improvement.

The ideal SA-SDC produces a finely tuned digital output code determined by the precise time difference between the signals in1 and in2. In an optimal operational setting, the SA-SDC should consistently generate digital output representations evenly distributed across the complete spectrum of time differences between in1 and in2. Every digital output representation represents a fractional expression of

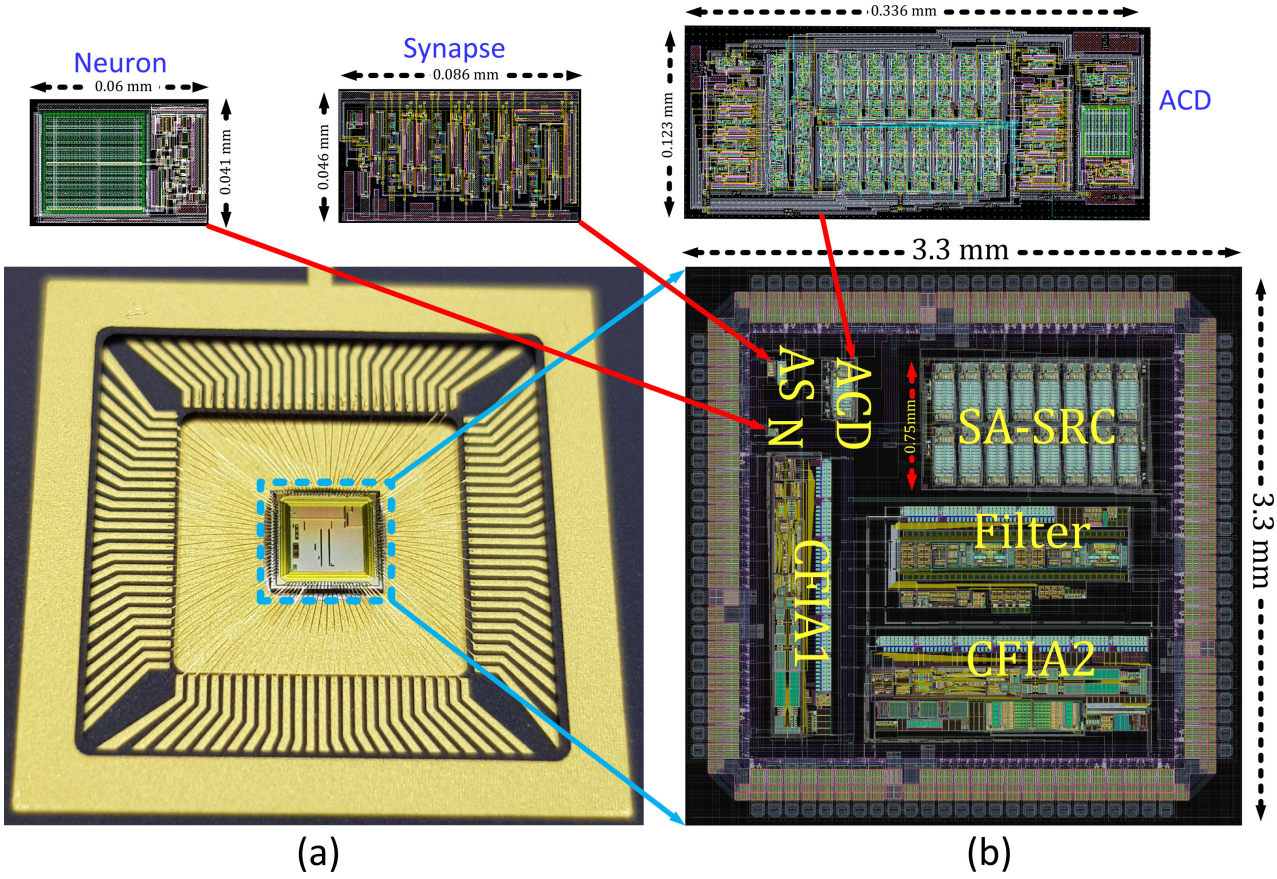

FIGURE 12. MPC USIX chip. (a) Upon completion of the manufacturing process, the chip exhibits both the bonding wires and the sealing ring, indicating the integration of key components for functionality and connectivity. (b) The chip layout incorporates the pad frame, emphasizing its comprehensive design.

time difference. The even distribution is contingent on the weight of the least significant bit (LSB), which is determined by the converter resolution and full-scale time difference (FSTD). The term "Full-Scale" (FS) denotes the extent of the time difference range between in1 and in2, within which SA-SDC processes the input signal, encompassing the maximum possible time difference between the two inputs. The LSB weight was calculated using the following formula:

$$LSB = \frac{FSTD}{2^n} \tag{5}$$

In this equation, n represents the number of bits used for resolution. Expanding the cascade by incorporating additional ACDs enhances the capability to measure the temporal gaps between in1 and in2, thereby augmenting the resolution of the SA-SDC. The number of ACDs required to attain a specific number of bits (NOB) can be determined using equation (6) [42].

$$NOB_{SA-SDC} = ld(x). \tag{6}$$

The parameter 'x' in the equation corresponds to the number of ACDs utilized. In the current developmental phase, our design incorporated 16 ACDs units, as illustrated in Fig. 7. The calculation of the NOB_{SA-SDC} can be determined using equation (6), resulting in a precision of four bits. The conversion speed of the neuromorphic spiking sensory system was determined using the following equation.

$$Conversion\ time = time_{ASSC} + time_{SA-SDC}. \tag{7}$$

Here, the $time_{ASSC}$ corresponds to the duration required for ASSC operation, which can be adjusted based on the synaptic weights to achieve the desired gain. The $time_{SA-SDC}$ encompasses the duration required for SA-SDC to convert the time difference value between two spikes received at its input into a digital code. It is a composite of two integral components, SA-SRC and the WTA mechanism, with its associated algorithm. The following equation was used to calculate the $time_{SA-SDC}$,:

$$time_{SA-SDC} = time_{SA-SRC} + WA\ time. \tag{8}$$

The WA time represents the duration required by the WTA mechanism and algorithm to transform the rank-order code outputs of SA-SRC into digital values. The duration depends on both the time and quantity of ACDs employed in its construction. The time span was computed using the following equation:

$$time_{SA-SRC} = number\ of\ ACDs * time_{ACD}. \tag{9}$$

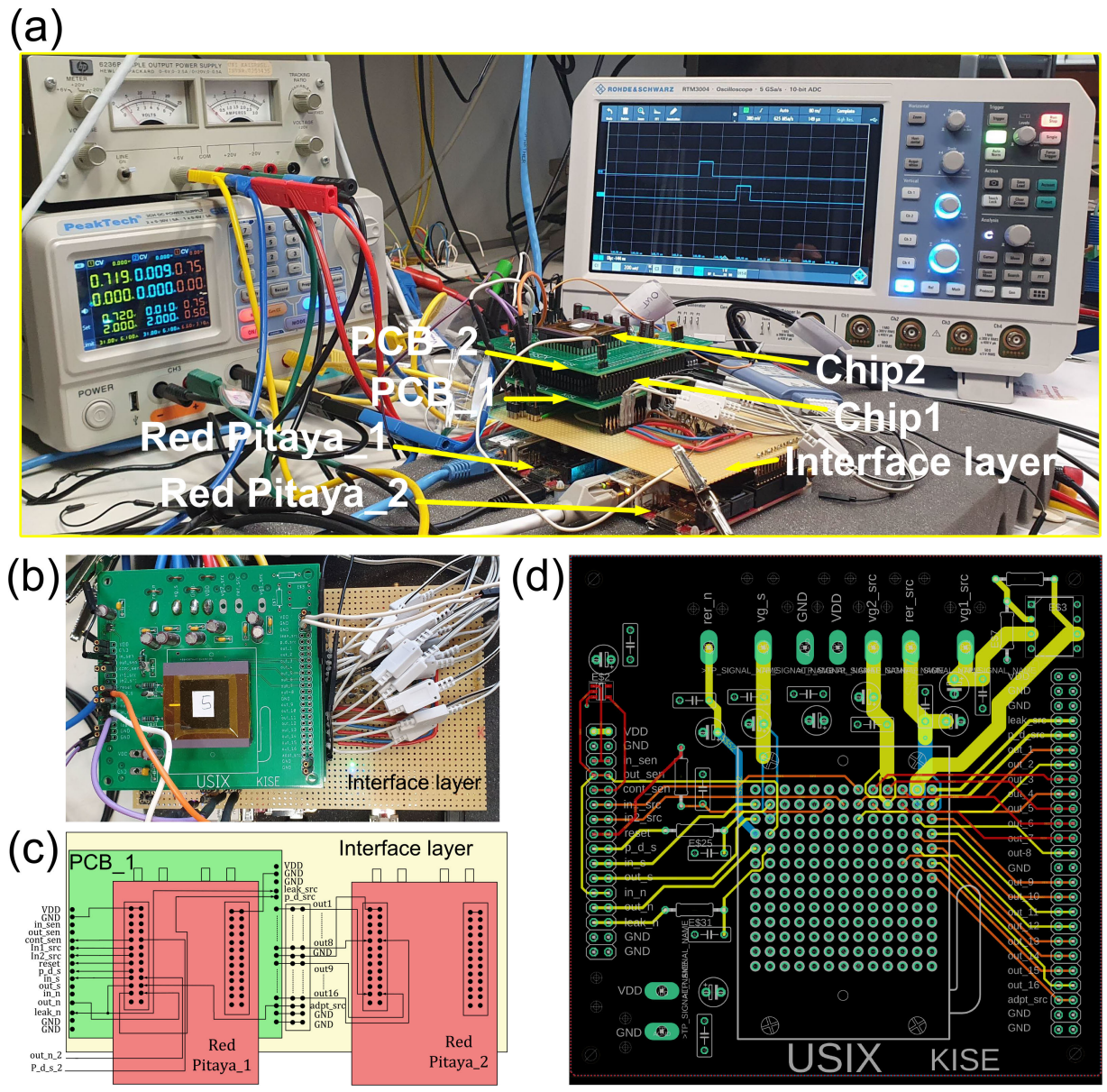

FIGURE 13. (a) The laboratory setup demonstrates the measurement characteristics of a neuromorphic spiking sensory system. Two MPC USIX chips are employed for this experiment. The first chip includes SA-SRC, synapse, and neuron cells, while the second chip consists of synapse and neuron cells. (b) The top view of the configuration shows the second chip on PCB_2 and a portion of the interface layer. The interface layer facilitates connections between the Red Pitaya boards and the PCBs. (c) The block diagram illustrates the connections between Red Pitaya_1, Red Pitaya_2, PCB_1, and the interface layer. (d) Illustrate the PCB used for the first and second chips.The four-layer PCB prototype was designed using Eagle Autodesk software. Separate power and ground planes, along with decoupling capacitors near the chip power pins, were included to reduce system noise.

The duration of each ACD varied with the weight of the synapses, which was determined during adaptation. The synaptic weights can also vary according to the specific process, voltage, and temperature (PVT) conditions at any given time.

IV. INTEGRATION OF NEUROMORPHIC SYSTEM COMPONENTS

In our chip, we addressed the aforementioned problems through two distinctive contributions to enhance the capabilities of the universal sensor interface with self-X properties (USIX), as detailed in a previous study [46]. The USIX on the multi-project-chip (MPC) has this name because we have integrated the essential components for both amplitude- and spike-domain representation, all in conjunction with the incorporation of self-X functionalities for analog front ends (AFE). The objective of this study was to complement the spike domain segment by utilizing the chip and the outcomes of the measurements.

A. CHIP DESIGN AND DEMONSTRATION BOARD

Within our chip, we incorporated critical components that are essential to the neuromorphic spiking sensory system.

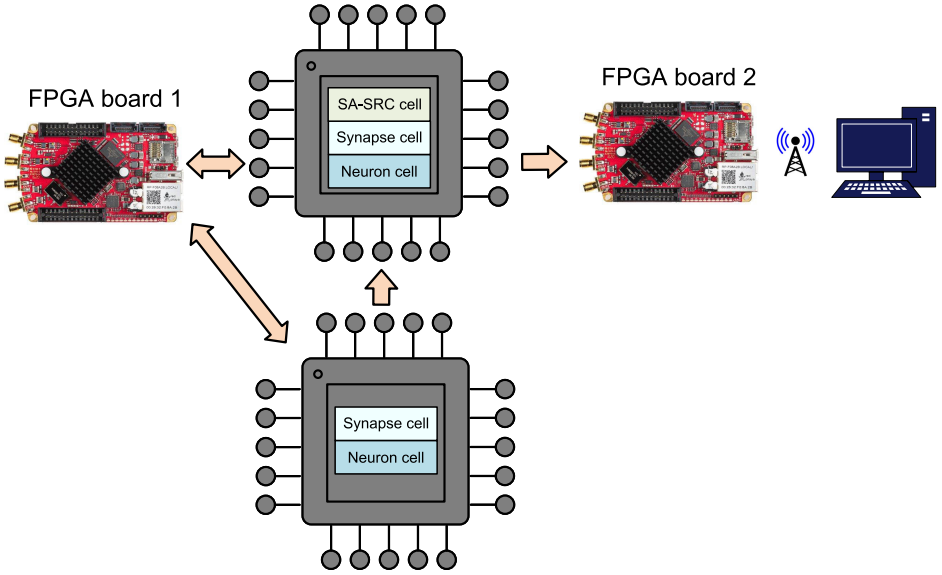

FIGURE 14. The figure illustrates the block diagram of the physical hardware implementation used for the demonstration prototyping, which aims to evaluate the essential components of the adaptive neuromorphic spiking sensory system. Two FPGA evaluation boards from Red Pitaya were used. The first board was configured to create a control module within the programmable logic (PL) to manage the SA-SRC cells, synapses, and neurons of the ASSC. The second board was utilized to implement the Winner-Takes-All (WTA) mechanism and the algorithm for decoding rank codes.

These components included neuron, synapse, adaptive self-adaptive spike-to-rank coding (SA-SRC), and coincidence detection (ACD). Fig. 12a shows detailed insights into the post-manufacturing chip, whereas Fig. 12b shows the chip layout implementation. The protective coating, along with the upper metal layer on the chip, obscures the features of the die. The initial findings and detailed characterization pertaining to the SA-SRC block have been previously documented [47], [53].

The initial component of the proposed sensor system, the ASSC, incorporates a configuration comprising two synapses and two neurons. To realize a practical implementation of this design, our approach necessitated the utilization of two chips, because each chip houses a single neuron and synapse. Comprehensive physical hardware-level assessment and testing of our adaptive neuromorphic spiking sensory system during the demonstration prototyping phase, we opted for the FPGA assessment platform provided by Red Pitaya as our chosen embedded computing system. To complete the integration, we employed a specialized PCB with an integrated socket to extend the capabilities of the Red Pitaya and create a comprehensive demonstration board, as shown in Fig. 13.

B. IMPLEMENTATION AND ARCHITECTURE

Fig. 14 shows a block diagram of the physical hardware implementation for demonstration prototyping aimed at accelerating the neuromorphic spiking sensory system. In this experimental setup, two FPGA evaluation boards from Red Pitaya were employed. The first board was employed to generate a control module within the programmable logic (PL) responsible for managing the SA-SRC cells, synapses, and neurons of the ASSC. On the second board, we implemented both the Winner-Takes-All (WTA) mechanism and algorithm used for decoding rank codes.

In Fig. 16 and Fig. 15, we present a comprehensive depiction of the implemented architecture for the adaptive neuromorphic spiking sensory system on Red Pitaya boards 1 and 2. We utilized Verilog hardware descriptive language to implement a control module within Red Pitaya's programmable logic (PL), as illustrated in Fig. 16. This module governs the essential components of the proposed system: the ASSC and SA-SRC. It manages the cells within these blocks, comprising two synapse cells, two neurons, and one SA-SRC cell. The module performs several critical tasks. First, it manages the reset p_up1, p_up2, P_s, and V_{LEAK} I/O pins associated with synapse and neuron cells. Second, it generates signals to regulate the SW1 and SW2 functionalities of TMUX1102DBVR chips. Third, it manages the V_{LEAK}, adapt, and adapt_pulse I/O pins functionality of the SA-SRC cell. To accomplish these functions, the control module leverages the general-purpose I/O pins provided by the Red Pitaya, establishing a direct connection to the I/O pins of the chips. The TMUX1102 switches from Texas Instruments are precision complementary metal-oxide semiconductor (CMOS) switches. Both the WTA and algorithm were executed on dedicated Red Pitaya board 2, as shown in Fig. 15. We successfully integrated the MUX, enabling seamless switching of the RAM block addresses. This allowed us to alternate between the address from the algorithm module during the writing process and that provided by the processor during the reading operations.

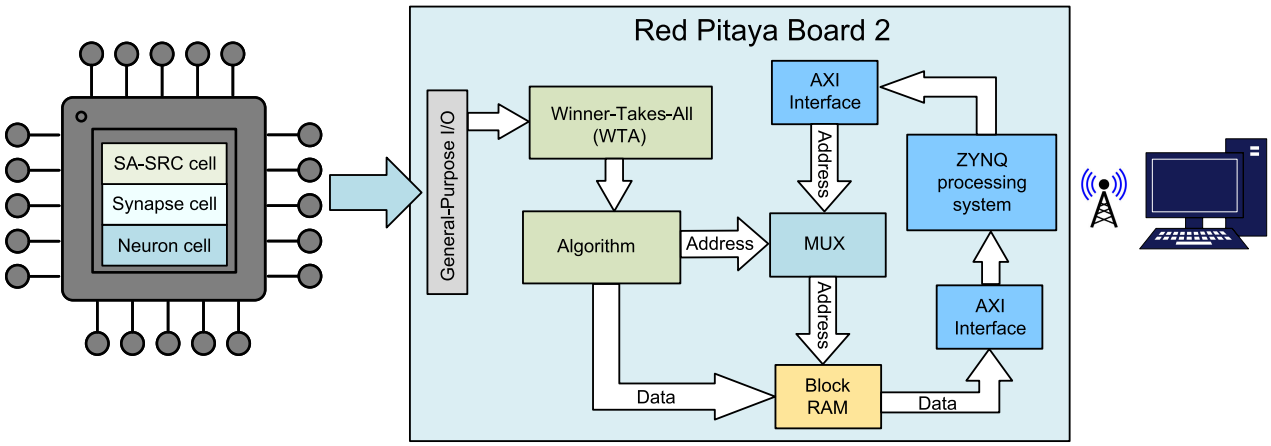

FIGURE 15. The execution of module architecture on Red Pitaya board 2 encompasses the simultaneous implementation of both the Winner-Takes-All (WTA) mechanism and the algorithm. This ensures a comprehensive integration of functionalities.

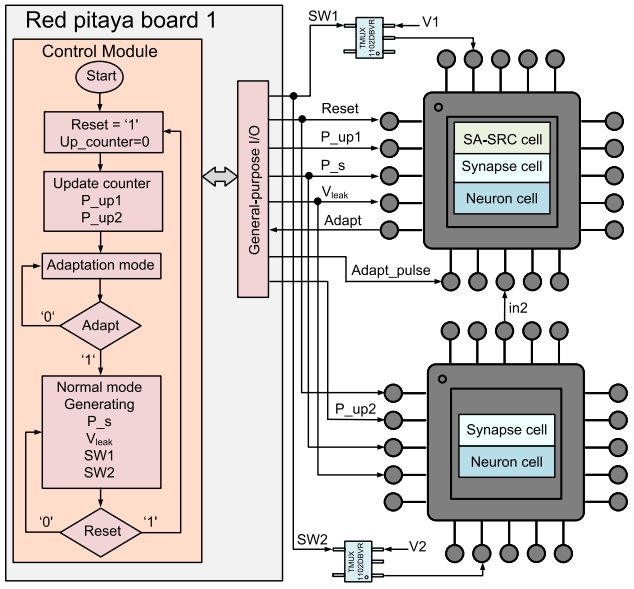

FIGURE 16. The control module's flow diagram in the programmable logic leverages the flexible general-purpose I/O pins on the Red Pitaya, forming a direct interface with the synapse, neuron cells, and SA-SRC integrated into the chip. These I/O pins are also connected to the TMUX1102DBVR chips.

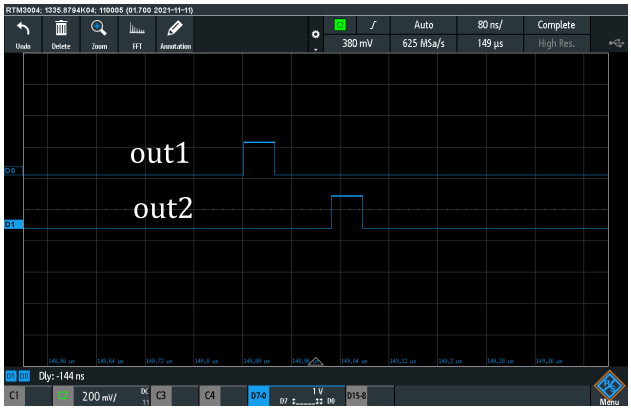

FIGURE 17. The output of the ASSC at V1 and V2 is equal to 0.9 V and zero volts, respectively.

V. NEUROMORPHIC CHIP CHARACTERIZATION AND APPLICATION

The purpose of this experiment is to demonstrate the measurement characteristics of a neuromorphic spiking sensory system implemented on a fabricated chip. In this experimental procedure, our initial step involves characterization of the initial block within our proposed system, referred to as the ASSC. Following this initial characterization, we interconnected the ASSC with the SA-SDC to comprehensively characterize the entire system under investigation.

The ASSC produces a pair of spikes with a temporal gap between them contingent on the disparity in voltage levels between V1 and V2. Illustrated in Fig. 17 is the output of the ASSC when V1 is set to 0.9 V and V2 is maintained at 0 V. The synapse weights of the ASSC are regulated by the up-counters and voltages vs1 and vs2. Initially, the up counters are initialized to a value of 255, and the voltage levels vs1 and vs2 are configured to 2.4 V and 2.35 V, respectively. Under these specific synapse weights, the transfer function of the ASSC exhibits an offset, as shown in Fig. 18. The magnitude of this offset can be computed using equation (2) and is determined to be 77.6 LSB. To rectify this offset, adjustments were made to the synaptic weights, as shown in Fig. 18. In this modified configuration, the up-counters were retained at a value of 255, and both vs1 and vs2 were set to 2.4 V. The LSB of the neuromorphic spiking sensory system will be calculated during characterization of the SA-SDC block, as will be shown later. This LSB was used for both ASSC and SA-SDC blocks.

To characterize the transfer function of the ASSC, the voltage differential between V1 and V2 was incrementally adjusted, spanning the range from -1.45 V to 1.45 V, with increments of 0.05 V. The gain was modulated by adjusting the synaptic weights within the ASSC. Fig. 19 and Fig. 20

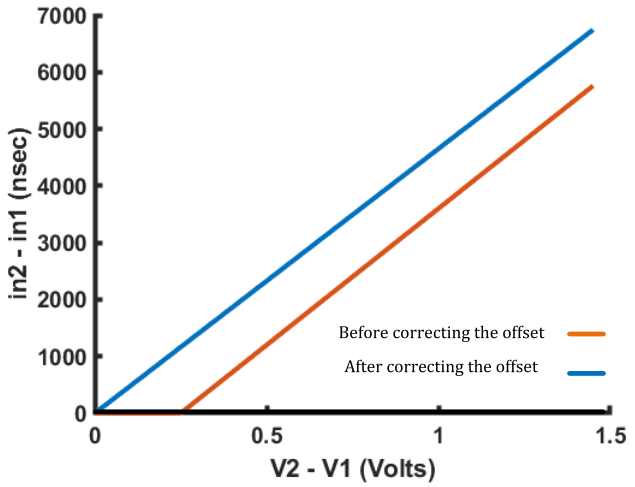

FIGURE 18. demonstrates the proficiency of the ASSC in rectifying offset errors. The synaptic weights were adjusted to correct this offset.

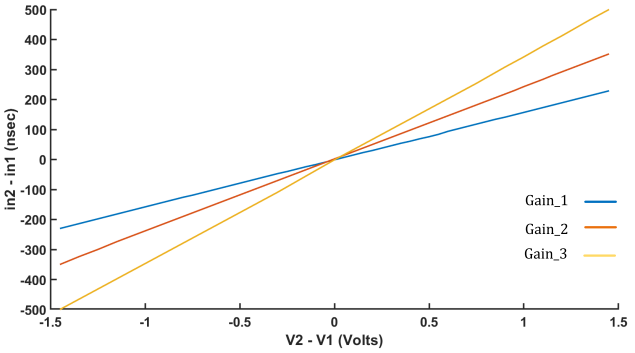

FIGURE 19. The transfer function of the ASSC system is determined through a measurement procedure specifically designed for low-gain scenarios.

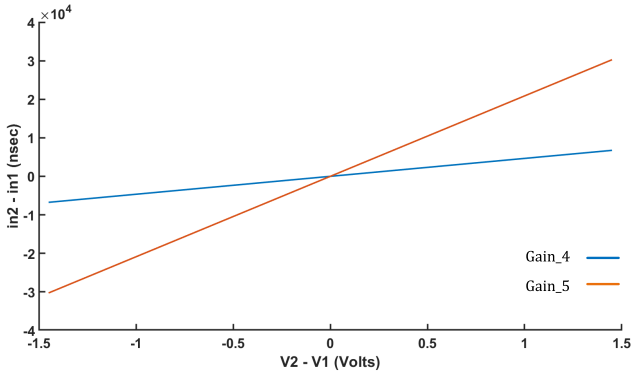

FIGURE 20. The transfer function of the ASSC system is determined through a measurement procedure specifically designed for high-gain scenarios.

depict the transfer function of the ASSC obtained using measurement processes for various gains. The duration of the ASSC was extended through adjustments in the gain settings, resulting in a corresponding increase in the number of bits that could be effectively resolved by SA-SDC. The

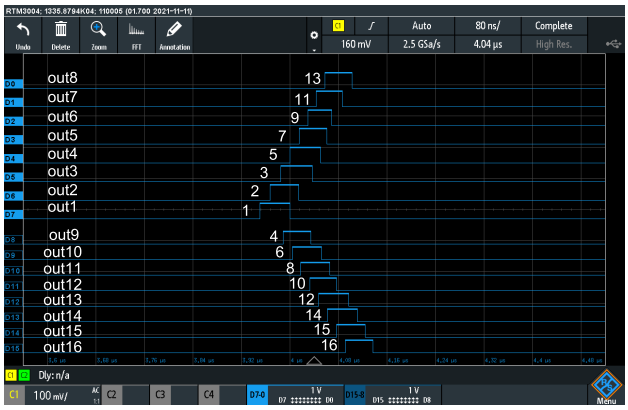

FIGURE 21. The SA-SRC's output was measured with the inputs V1 and V2 of the ASSC set to 0 V and 0.2 V, respectively.

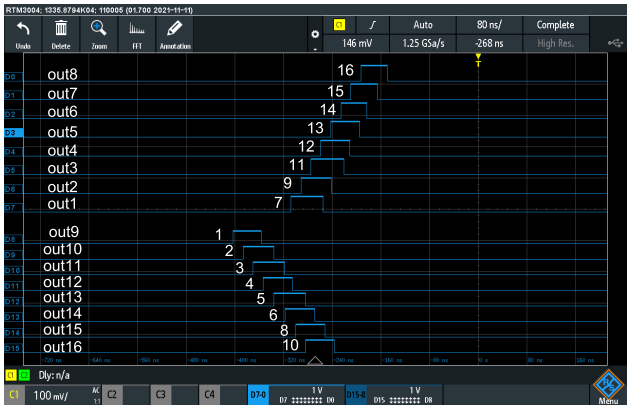

FIGURE 22. The SA-SRC's output was measured with the inputs V1 and V2 of the ASSC set to 0.55 V and 0 V, respectively.

attainable MNoB_{ASSC}, resulting from adjustments in gain, can be computed using equation (3), yielding a value of 11.98 bits, which can be effectively resolved by the SA-SDC.

The initial component of the SA-SDC, referred to as the SA-SRC, has 16 outputs, each of which generates a corresponding spike. The sequence of these spikes accurately reflects the time difference between the spikes received at the input from the initial ASSC block. Fig. 21 provides a visual representation of the SA-SRC output when the inputs V1 and V2 of the ASSC are set to 0 V and 0.2 V, respectively. Fig. 22 shows an additional instance portraying the SA-SRC output under different input voltage conditions, with the values of V1 and V2 set to 0.55 V and 0 V, respectively, within the ASSC. The SA-SRC outputs, labelled from out1 to out16, function as representations of the individual spike order codes. The numerical annotations of the output waveforms indicated the sequential order of the spike codes relative to each other.

Based on the experimental findings, we established the ability of an SA-SRC cell to produce 16 distinctive spike-order codes, each corresponding to a specific temporal disparity between its input signals. This is equivalent to encoding information into a 4-bit binary representation in

the current study. The SA-SRC input range was identified and characterized by changing and measuring the time delay between the signals in1 and in2. The experimentally measured range spanned from −120 ns to +120 ns. Hence, the FSTD equates to 240 ns, and the least significant bit (LSB) can be determined through the calculation provided by equation (5), resulting in a value of 15 ns. Regarding the speed, the current SA-SRC demonstrator achieved a conversion time of 370 ns. On Red Pitaya board 2, both the WTA circuit and algorithm are executed. This process involves translating the rank-order code outputs of the SA-SRC cell into digital values and saving these values in thePL block RAM. The process of converting the rank to dense digital code is 1.035 ns. The SA-SDC time denotes the period required for the SA-SDC to transform the time difference value between two spikes received at its input into digital code, as computed by equation (8), resulting in 371.035 ns. The conversion speed of the neuromorphic spiking sensory system was assessed using equation (7), which yielded a result of 491.035 ns.

Evaluating the performance of the neuromorphic spiking sensory system involves the testing of various parameters. These parameters, outlined in the converter specifications, fall into two categories: those related to the transfer function and those representing the distortion introduced to the converted signal. In the first group, the static parameters, including the integral non-linearity (INL), differential non-linearity (DNL), and missing codes were included. These metrics provide crucial insights into system accuracy and functionality. The SA-SDC was ideally designed with a step width of one LSB, representing the minimum unit in its time-to-digital conversion. The discrepancy between this ideal and the actual measurement is defined as the differential non-linearity (DNL) error. Additionally, integral non-linearity (INL) measures the maximum deviation from the actual response curve to the ideal curve. Furthermore, a well-designed SA-SDC should eliminate missing code issues that occur when gaps exist in the digital output code, indicating that certain output values are never produced. This is frequently owing to the unavailability of analog input values that are capable of producing particular codes.

The standard procedure for evaluating the DC characteristics of the SA-SDC, including the INL, DNL, missing code, and transfer function, involves a specific test setup. In this setup, a function generator was configured to produce a gradual voltage ramp ranging from the minimum input voltage to the maximum. This voltage ramp was applied to the ASSC inputs represented as V1 and V2. These inputs lead to the generation of time delays in the ASSC outputs, identified as out1 and out2. This time delays the transition within the range of -120 ns to +120 ns, effectively covering the complete input spectrum of the SA-SDC. This test comprehensively assessed the performance characteristics of the device. The SA-SDC samples were collected as the input ramp gradually traversed the entire SA-SDC conversion range. The ramp rate of ascent was controlled to ensure that each SA-SDC

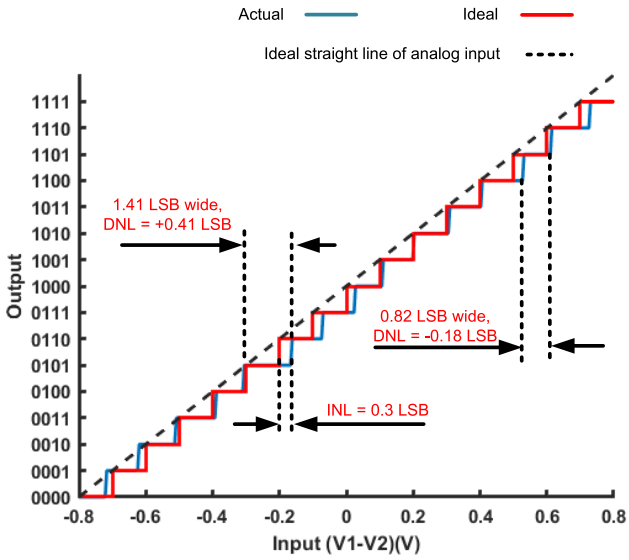

FIGURE 23. The transfer function of the neuromorphic spiking sensory system with self-X capabilities for both ideal and actual case.

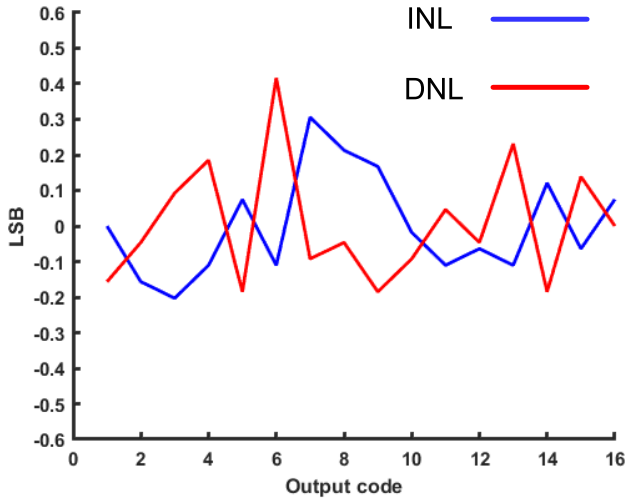

FIGURE 24. The measured DNL and INL curves correspond to the depicted curve in Fig. 23.

code was sampled multiple times, typically for approximately 20 instances in this experiment. During this procedure, the ASSC gain was adjusted to 'gain_1' by fine-tuning the synaptic weights within the ASSC, as illustrated in Fig. 19. Subsequently, the digital outputs generated by the SA-SDC were stored in the PL block RAM for the entire duration of the linear ramp input.

The measurements were conducted under standard conditions, with a supply voltage of 3.3 V and a temperature of 23 °C. In Fig. 23, the neuromorphic spiking sensory system transfer function of the experiment illustrates the correlation between the SA-SDC output and the voltage difference between the input signals V1 and V2 of the ASSC on the horizontal axis. The limitations observed in

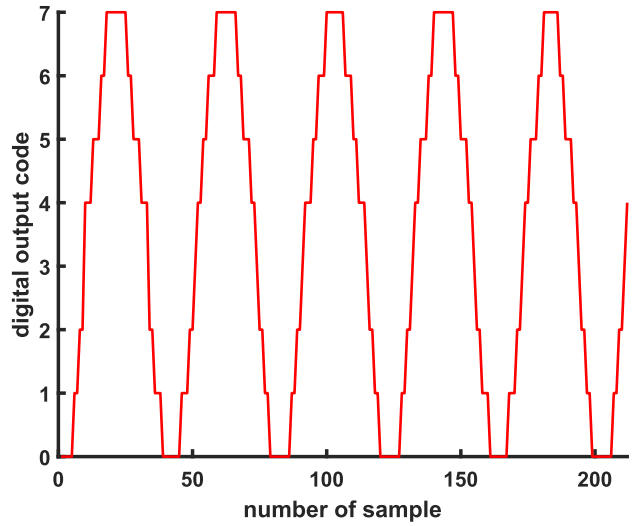

FIGURE 25. Illustrating the performance of the neuromorphic spiking sensory system, the reaction to a sinusoidal signal is observed. This signal has specific characteristics: 0.8 Vp-p amplitude, 3 kHz frequency, and a 0.4 V DC offset. In this scenario, V2 receives the signal, while V1 is intentionally set to zero.

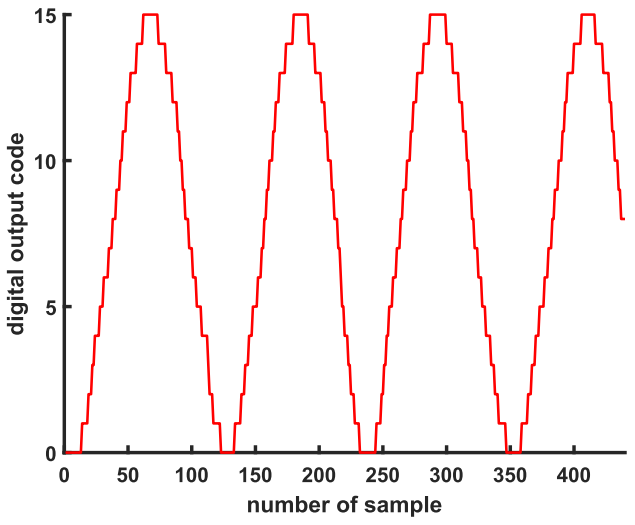

FIGURE 27. Displaying the neuromorphic spiking sensory system's capabilities, the response to fully differential sinusoidal input signals applied to V1 and V2 was observed. These signals exhibited distinct attributes, with an amplitude of 0.8 Vp-p, frequency of 1 kHz, and a 0.4 V DC offset.

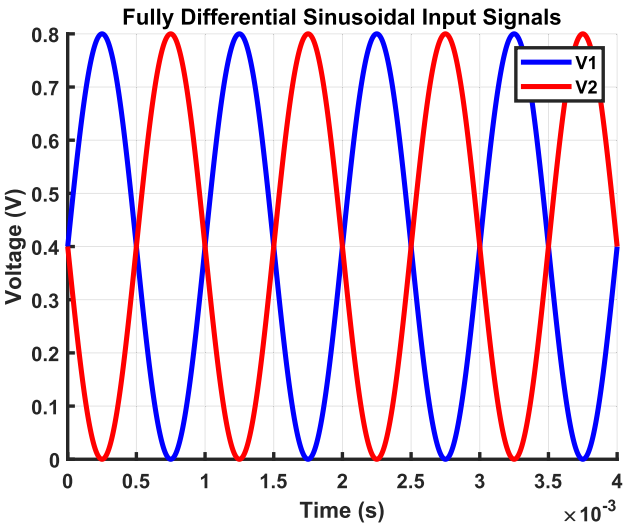

FIGURE 26. The picture depicts the fully differential sinusoidal input signals that were administered to V1 and V2. These signals featured specific characteristics: 0.8 Vp-p amplitude, 1 kHz frequency, and a 0.4 V DC offset.

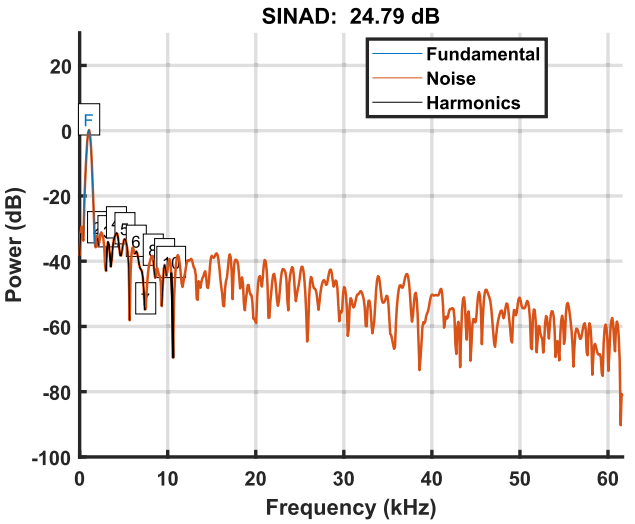

FIGURE 28. The FFT output of the neuromorphic spiking sensory system unveils its reaction to fully differential sinusoidal input signals. This observation is based on the signals applied to V1 and V2, as depicted in Fig. 26.

the experimental results for 16 distinct spike order codes or four bits of our current prototype are due to chip size restrictions and not the underlying information processing concept. The key parameters of the SA-SDC, comprising the INL, DNL, and count of missing codes (NOMCs), showcase values, with INL at 0.3, DNL at 0.41 LSB, and zero missing codes, as illustrated in Fig. 23. Furthermore, Fig. 24 provides detailed DNL and INL curves, offering a more comprehensive view of the results presented in Fig. 23.

The second category of parameters for assessing the neuromorphic spiking sensory system comprises of dynamic attributes. These include metrics, such as the effective number of bits (ENOB) and signal-to-noise and distortion ratio (SINAD), which play a pivotal role in the system's performance evaluation. Typically, these parameters are derived from the fast Fourier transform (FFT) of digital samples obtained from the converter output when subjected to a pure sine wave input. SINAD represents a comprehensive metric encompassing not only the signal-to-noise ratio, but also harmonic distortion and other unwanted components in the output of the neuromorphic spiking sensory system. It quantifies the ratio between the desired signal power and

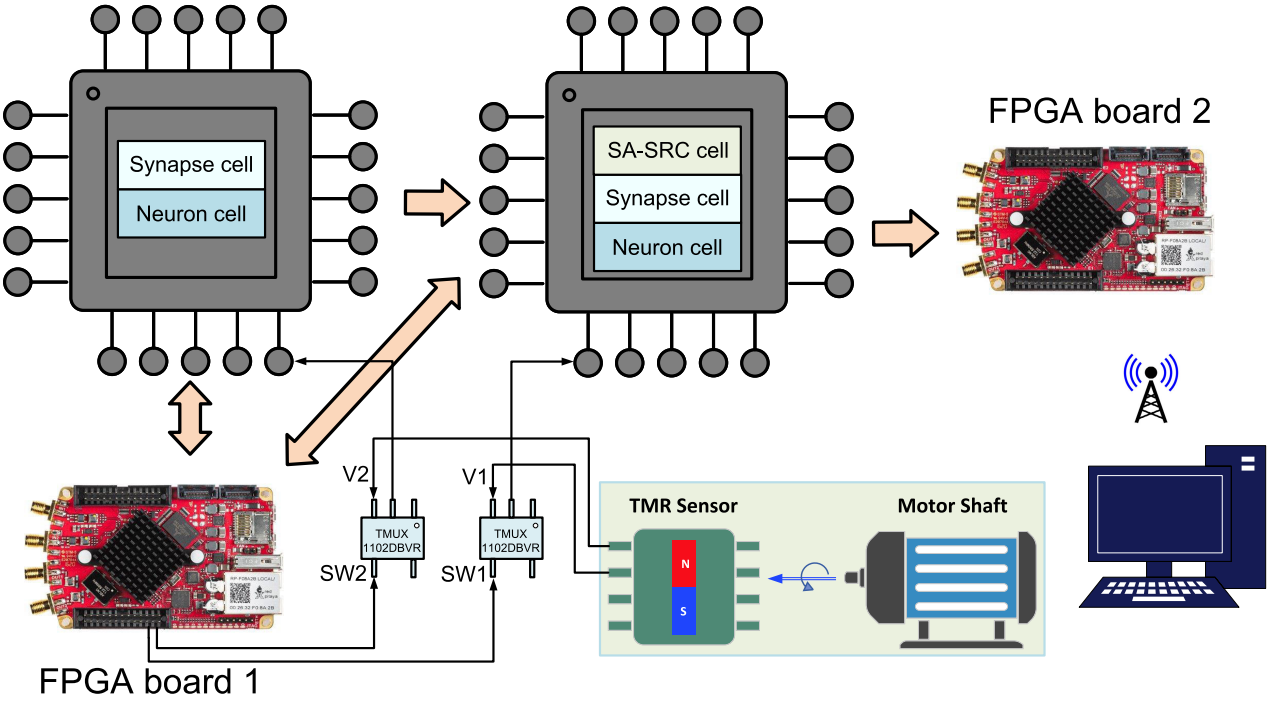

FIGURE 29. Functional setup depicting the implementation of the TMR interface with the proposed neuromorphic spiking sensory system.

the combined power of all undesired elements such as noise and distortion. ENOB signifies the measured performance of the neuromorphic spiking sensory system based on its response to the input signal. A key consideration is that, as noise, especially distortion components, increases, it subsequently diminishes the ENOB of the system. These dynamic parameters are crucial for gaining a deeper understanding of the system performance and shedding light on their efficiency.

Initially, we evaluated the system by subjecting it to a sinusoidal signal with an amplitude of 0.8 Vp-p, frequency of 3 kHz, and DC offset of 0.4 V. The sampling frequency of the neuromorphic spiking sensory system was 130 kHz, with V2 receiving the signal and V1 set to zero. The corresponding system outputs are shown in Fig. 25. In the assessment of dynamic performance, as well as parameters such as SINAD and ENOB, fully differential sinusoidal input signals characterized by a 0.8 Vp-p amplitude, 1 kHz frequency, and 0.4 V DC offset were applied to V1 and V2, as shown in Fig. 26. The sampling frequency of the neuromorphic spiking sensory system was established at 130 kHz. The ASSC gain, denoted as 'gain_1,' was regulated by modifying the synaptic weights within the ASSC. A visual representation of this process is shown in Fig. 19. Subsequently, the digital outputs generated by the neuromorphic spiking sensory system were systematically stored in the block RAM of the PL.

The overall system output, shown in Fig. 27, is graphically represented, where the x-axis corresponds to the sample number, and the y-axis signifies the digital output data. Fig. 28 shows the output signal when examined in the frequency domain through the execution of a fast Fourier transform (FFT). The dynamic parameters were derived from the FFT analysis of the digital sample dataset. Evaluation of the dynamic performance of the neuromorphic spiking sensory system includes parameters such as SINAD and ENOB, which yield specific values. The SINAD parameter registers at 24.79 dB, and ENOB at 3.82 bits for the current work.

A prototype demonstration highlights the integration of our proposed neuromorphic spiking sensory system with a Tunnel Magnetoresistance (TMR) sensor, specifically, the AFF755B TMR sensor from Sensitec. This experiment assessed and tested our adaptive neuromorphic spiking sensory system and the TMR sensor, as shown in Fig. 29. The TMR sensor was equipped with a pair of balanced, fully differential configurations, generating two distinct differential signals separated by 90 °, namely, sine and cosine outputs. A block diagram of the proposed interface with the TMR sensor is shown in Fig. 30. In the present configuration of the laboratory setup, the hardware can interface with a single differential signal, as illustrated in Fig. 30. In the upcoming stages, there are plans to increase the number of bits, enhance the capacity of the system to handle two differential signals, and implement this capability on a single chip using advanced technologies. This advancement aims to calculate and enhance the angle measurements by positioning the system to compete effectively with the state-of-the-art technologies.

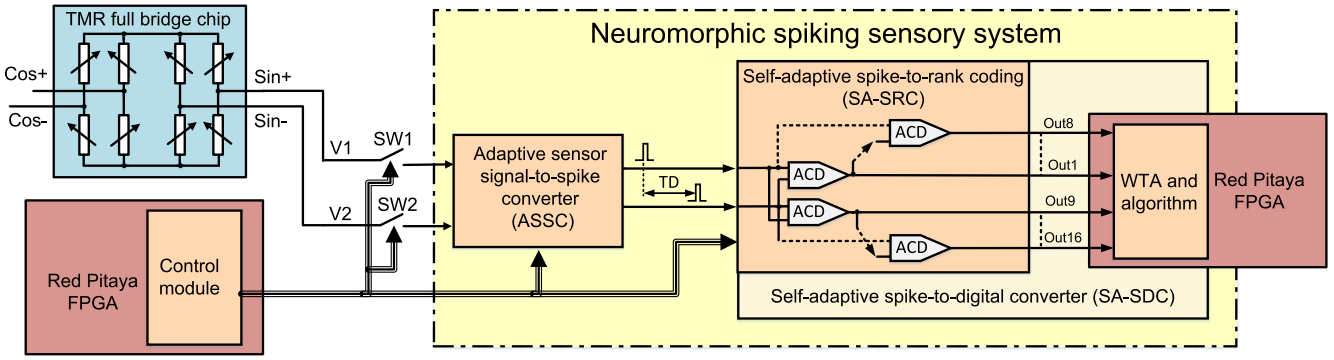

FIGURE 30. Block diagram for TMR interface implementation with the proposed neuromorphic spiking sensory system.

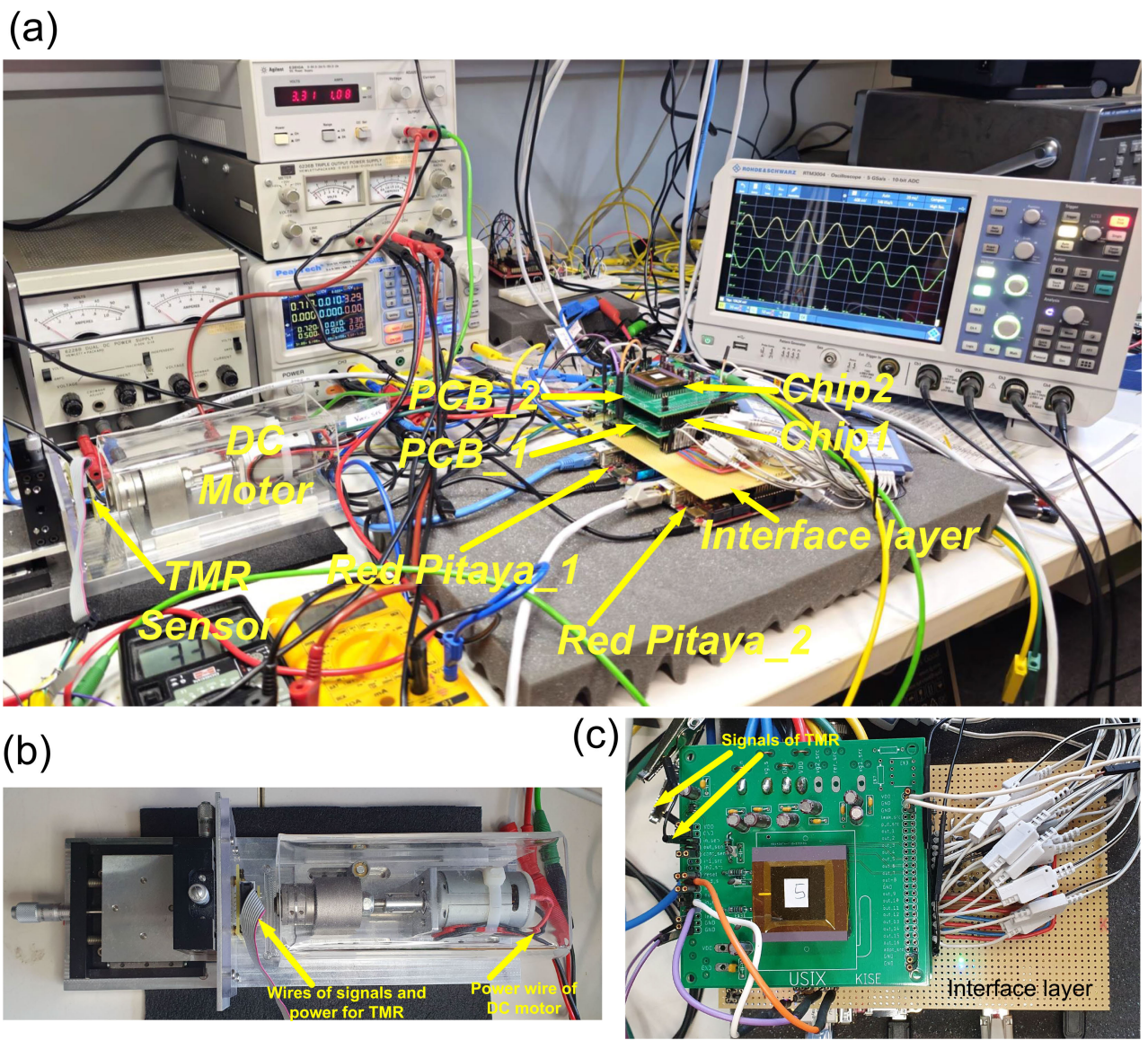

FIGURE 31. (a) Laboratory configuration for TMR interface implementation with the proposed neuromorphic spiking sensory system. Fig. 13 (c) and (d) show the block diagram of the connections between Red Pitaya_1, Red Pitaya_2, PCB_1, and the interface layer, as well as the PCB itself. (b) The top view configuration of the TMR and DC motor. (c) The top view of the configuration highlights the TMR signal connections to the neuromorphic spiking sensory system.

Simultaneously, another researcher within our group is concentrating on studying the self-x concept for sensor systems at higher and multiple levels, and the angular decoder serves only as a case study [54]. The primary aim of this prototype demonstration was to validate the functionality of the electrical interface in real sensor applications by focusing on sensor readout digitization. Moreover, emphasis was placed on the capability of the ASSC block to synchronize both the sensor and SA-SDC spans with variations in the amplitude of the sensor signal. A block diagram of the proposed interface with the TMR sensor is shown in Fig. 30. The outputs of the TMR sensor sin+ and sin- are directed to the inputs of the ASSC, denoted as V1 and V2, respectively. The ASSC functions as a crucial conditioning circuit that aligns the spans of the sensor and the SA-SDC. It exhibits versatility by simultaneously amplifying and level-shifting the sensor signal in the time-domain.

The magnet is mounted onthe front of the motor shaft and thus revolves, while the PCB with the TMR is stationary, facing the magnet with a tunable gap. The configuration of the laboratory arrangement is illustrated in Fig. 31, which shows its integration with a TMR sensor. The TMR sensor was initially positioned 4 mm from the magnetic detector in front of the motor shaft. As illustrated in Fig. 32, the TMR sensor yielded differential outputs of approximately 0.225 Vp-p. To align both the sensor and the SA-SDC span, adjustments to the synapse weights, specifically the gain and offset, were executed. In this revised setup, the up-counters were maintained at a value of 255, and both vs1 and vs2 were set to 1.8 V. The sampling frequency of the neuromorphic spiking sensory system was set to 7.7 kHz, which was sufficient to encompass the maximum expected frequency from the DC motor when operating at its highest speed. Subsequently, the digital outputs generated by the neuromorphic spiking sensory system were methodically stored in PL block RAM. The comprehensive system output depicted in Fig. 33 graphically represents the sample number on the x-axis and the digital output data on the y-axis.

To address the channel limit in the current phase of the study, we initially read and converted a sine bridge followed by a cosine bridge. Subsequently, we manually synchronized the zero crossings using shift operators, as illustrated in Fig. 34a. These synchronized signals were then utilized for the angle computation, as defined by the following equation:

$$\theta = \arctan\left(\frac{2A_{\sin}\sin(\alpha+\phi)+\text{offset}_{\sin}}{2A_{\cos}\cos(\alpha)+\text{offset}_{\cos}}\right). \quad (10)$$

In this equation, θ denotes the measured angle, and α represents the rotational angle of the magnet with respect to the sensor. $2A_{\sin}$ and $2A_{\cos}$ represent the maximum sine and cosine amplitudes, respectively. ϕ denotes the phase error between the sine and cosine waveforms. The $\text{offset}_{\sin}$ and $\text{offset}_{\cos}$ terms denote the deviations in the amplitudes of the sine and cosine signals, respectively. Fig. 34 shows the angle calculation and absolute error obtained from the fully differential TMR signals, the TMR sensor positioned

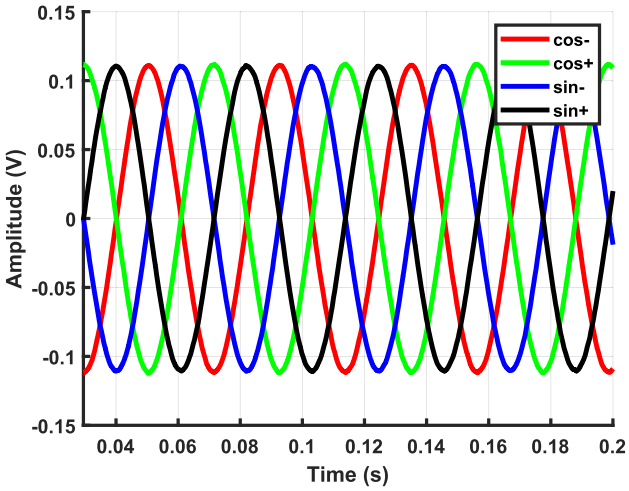

FIGURE 32. Outputs from the TMR sensor were recorded at a distance of 4 mm.

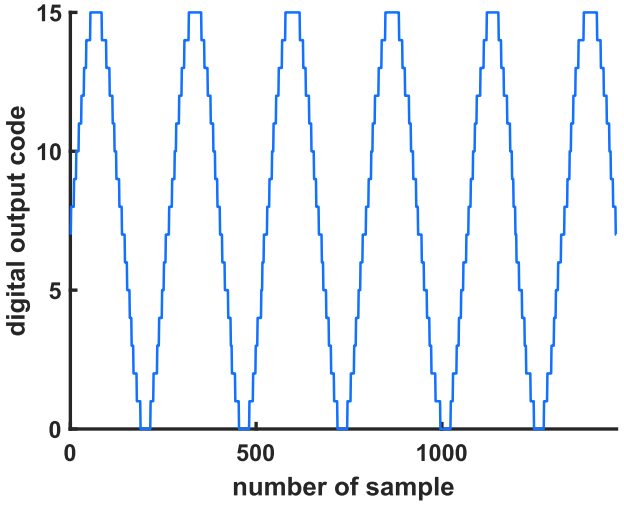

FIGURE 33. Demonstrating the functionality of the neuromorphic spiking sensory system, we observed its response to the differential outputs of the TMR sensor, which were applied to V1 and V2. It was recorded when the TMR sensor was positioned 4 mm away.

at a distance of 4 mm. For the current design phase, the highest absolute deviation is noted to be 12.89°, computed by subtracting the actual angle computed from the ideal best-fit line. Considering the limitations of the 4-bit ADC, the theoretical best angle resolution for the current prototype is 360 ° divided by the number of steps in one period, which is 32 steps (16 levels per half cycle), resulting in an error of 11.25 °.

For the next test, the TMR sensor was relocated to a position 7 mm away to investigate the impact of the reduction in the amplitude of the signal on the calculation of angle errors. As shown in Fig. 35, the TMR sensor produces differential outputs of approximately 0.104 Vp-p. Throughout this process, the ASSC synapse weights were maintained, with the up counters set at 255 and both vs1 and

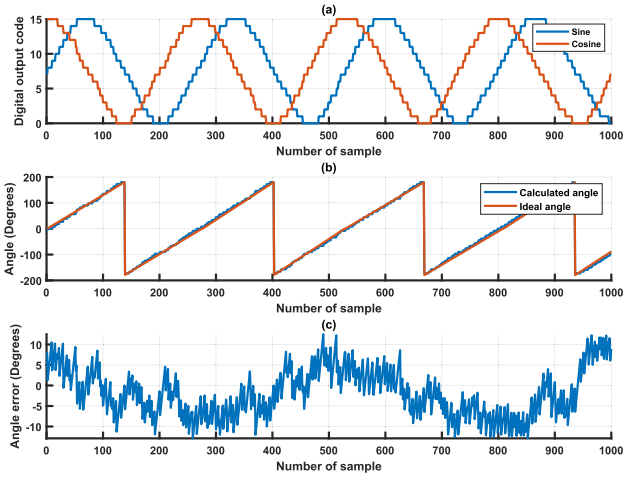

FIGURE 34. Angle calculation using a TMR sensor positioned 4 mm away from the motor shaft, (a) showing fully differential sine and cosine signals. (b) Evaluation of the computed angle compared to the ideal angle. (c) Absolute error in angle measurement.

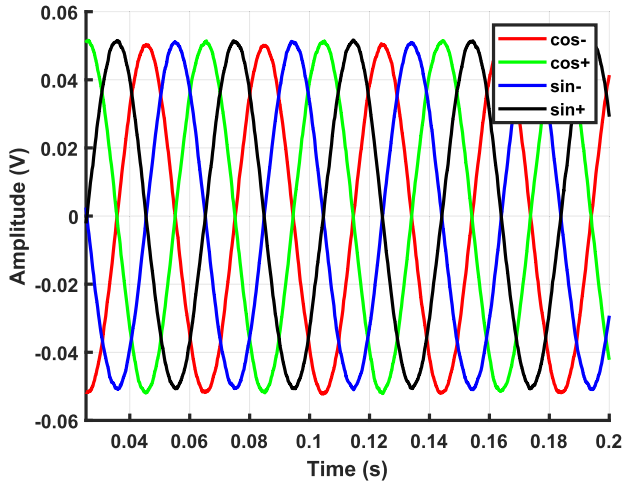

FIGURE 35. Outputs from the TMR sensor were recorded at a distance of 7 mm.

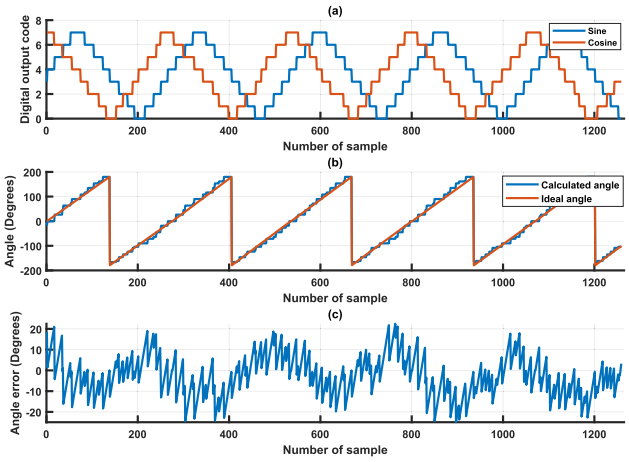

FIGURE 36. Angle calculation was performed using a TMR sensor positioned 7 mm away from the motor shaft. The ASSC synapse weights remained the same as in the previous experiment when the TMR sensor was positioned at 4 mm, with the up counters set at 255 and both vs1 and vs2 set to 1.8 V. (a) Illustrating fully differential sine and cosine signals. (b) Evaluating the computed angle compared to the ideal angle. (c) Absolute error in angle measurement.

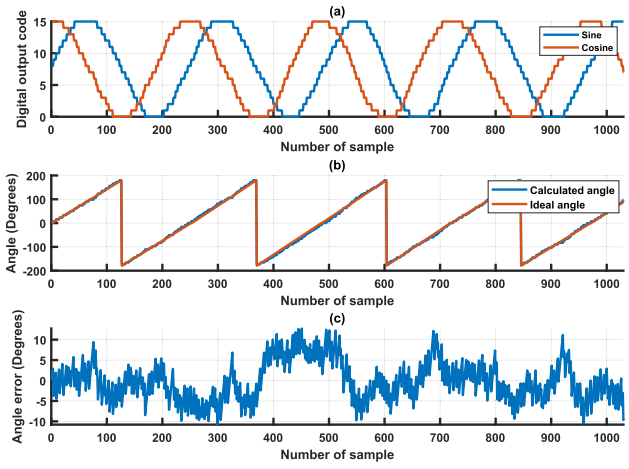

FIGURE 37. Angle calculation was performed using a TMR sensor positioned 7 mm away from the motor shaft. The ASSC synapse weights were adjusted, with the up counters set at 255 and both vs1 and vs2 set to 2.1 V. (a) illustrating fully differential sine and cosine signals, (b) evaluating the computed angle compared to the ideal angle, and (c) presenting the absolute error in angle measurement.

vs2 adjusted to 1.8 V. Fig. 36 illustrates the calculation of angles and absolute error with the TMR sensor positioned 7 mm away. The highest absolute deviation is noted to be 24.95°. Based on the experimental outcomes, the TMR signals induced time delays in the ASSC outputs, denoted as out1 and out2. The time delays ranged from -55 ns to +55 ns, which did not cover the complete input conversion spectrum of SA-SRC. According to the experimental observations, the SA-SRC cell generated eight unique spike-order codes within this range, corresponding to a 3-bit binary representation of the encoded information as shown in Fig. 36.

Adjustments were made to the synapse weights of the ASSC to align both the sensor and SA-SDC spans to utilize the full input conversion range of SA-SRC. In this adjusted configuration, the upper counters were set to 255, and both vs1 and vs2 were adjusted to 2.1 V. The neuromorphic spiking sensory system operated at a sampling frequency of 7.7 kHz. The following modifications to the synaptic weights, the TMR signals introduced temporal delays in the ASSC outputs ranging from -120 ns to +120 ns. This interval comprehensively spans the entire input conversion spectrum of the SA-SRC. Experimental observations indicate that within this range, the SA-SRC cell produces 16 distinctive spike-order codes, equivalent to a 4-bit binary representation of the encoded information. The overall system output, presented in Fig. 37 a, visually represents the sample number on the x-axis and the digital output data on the y-axis. Fig. 37 illustrates the calculation of the angles and absolute error with

the TMR sensor positioned 7 mm away after adjustments were made to the synapse weights of the ASSC to align both the sensor and SA-SDC spans. The highest absolute deviation is noted to be 12.72°.

The outcomes obtained with the sensor positioned at both 4 mm and 7 mm from the magnetic detector demonstrate the system's proficiency in converting the sensor signal into a digital format. Furthermore, the results highlight the efficacy of the ASSC block in aligning the sensor and SA-SDC block. It is noteworthy that in both scenarios, the full hardware capacity of the SA-SDC block, comprising four bits, was utilized in the current design. Moreover, the results illustrate the system's ability to adapt and reduce the absolute error in the angle measurement from 24.95° to 12.72° during this phase of the study.

VI. CONCLUSION

The creation of a successful application system relies on the integration sensors and suitable sensor electronics, thereby linking the system to the physical world. Our aim was to develop an adaptive neuromorphic spiking sensory system with key features, including noise resilience, power efficiency, scalability compatibility, and low-voltage operation. Furthermore, it is imperative to highlight that one of the key features of our approach is the ability to increase the yield without requiring labor-intensive 'pick-and-place' operations for individual calibration or trimming, which is continuously repeated during the circuits operation and life cycle. The selected information representation method relies on the spike domain, which is inspired by the biological sensor systems. This project focused on the measurement and characterization of a neuromorphic spiking sensor chip. Our chip, produced using XFAB CMOS 0.35 μm technology through EUROPRACTICE, encompasses the following essential components: neuron, synapse, ACD, and SA-SRC. The ASSC, which is the primary component of our sensor system, involves a design comprising two synapses and two neurons. The implementation required two chips, each housing one neuron and one synapse. The ASSC demonstrated its capability to correct offsets through modifications to synapse weights, and gain modulation was achieved by tuning synaptic weights. The measurement depicts the transfer function of the ASSC across various gains, where adjusting the gain increases the attainable MNoB_{ASSC} to approximately 11.98 bits. Subsequently, we interconnect the ASSC with the SA-SDC to characterize the entire system holistically. The constraints observed in the test outcomes, which limit the generation of 16 unique spike-order codes or four bits in our present model, arise from the chip's constraints, rather than the fundamental concept of information processing. Performance evaluation encompasses key parameters such as INL, DNL, ENOB, and NOMCs, yielding values of 0.3 LSB, 0.41 LSB, 3.82 bits, and zero missing codes. In this experiment, we conducted a comprehensive hardware-level assessment of our adaptive neuromorphic spiking sensory system and TMR sensor. The primary goal of this prototype demonstration was to confirm the functionality of the electrical interface in real sensor applications, emphasizing the importance of sensor readout digitization. Regarding power usage, the system consumes 321 μw. The decision to employ the 0.35 μm technology and implement the 4-bit version was influenced by financial factors and was intended to showcase the viability of the solution. It is essential to highlight that the concept is not restricted to these specifications and holds the potential for expansion in both bit capacity and the technology employed. To demonstrate the characteristics of our proposed design, which are characterized by their technology-agnostic attributes, for the next stage of the work, we began implementing the design using the FinFET 12 nm from Global Foundries and finalizing the levels of adaptation along with potential enhancements to both the neuron circuits and the adaptation approach.

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