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RESEARCH ARTICLE

Real-Time Emulation of Reversible Solid Oxide Electrolyzer's Electrical Behavior for Rapid-Prototyping of Power Electronics

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ABSTRACT Hydrogen production is predicted to increase, and a promising solution for energy-efficient hydrogen electrolysis is reversible solid oxide cell stacks. Given the complexity and costliness of reversible solid oxide electrolysis cell stacks, this study develops a novel emulator capable of replicating their electrical behavior. By doing so, the study aims to enhance accessibility for rapid prototyping of power electronic systems. In this paper, initially, three different techniques for real-time emulation of the electrical dynamics for a reversible solid oxide electrolysis cell stack are investigated and evaluated for rapid prototyping of power electronic converter systems. An analog circuit approach is chosen as the most suitable for real-time emulation based on a multiple-criteria decision analysis. An equivalent circuit model is utilized for the analog circuit approach, following the indications of previous work using electrochemical spectroscopy data for parameterization. Furthermore, experiments were conducted to compare the electrical dynamics of the developed emulator to a mathematically validated model of a commercial reversible solid oxide electrolyzer cell stack in static, dynamic, and cyclic operation. Finally, the emulator's effectiveness as a tool for rapid prototyping of the interfacing power electronic system is conclusively demonstrated in a case study. Specifically, the emulator is utilized to successfully prototype a bidirectional Buck-Boost converter and its accompanying control system for cyclic operation.

INDEX TERMS Electrolysis, emulation, power electronics, rapid prototyping, solid oxide cell (SOC).

I. INTRODUCTION

Hydrogen is a versatile fuel with feedstock, fuel, and long-term energy storage applications. In 2022, it was primarily produced from fossil fuels, resulting in nearly 900 Mt of CO_2 emissions [1]. To decarbonize the growing hydrogen demand, a potential solution is the production of green hydrogen using electrolysis and renewable energy resources. Various electrolyzer technologies exist for hydrogen production, with the three most common being alkaline, proton exchange membrane, and solid oxide cells. Alkaline and proton exchange membrane electrolyzers are mature technologies employed in large-scale plants, while Solid Oxide Electrolyzer Cell (SOEC) technology is less mature. Compared to other electrolyzer technologies, the SOEC exhibits several unique advantages, such as very high

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efficiency and scalability. However, it has certain disadvantages, including the need for high operating temperatures, low commercial maturity, and a high degradation rate [2].

The SOEC technology can perform steam electrolysis for H_2 production, CO_2 electrolysis for CO production, and co-synthesis of steam and CO_2 to produce syngas. This versatility enables the SOEC technology to produce fuel or feedstock for other valuable products [3], [4]. Furthermore, a unique operational method of the SOEC that promotes its use is its ability to operate in reverse mode as a fuel cell to generate electricity. This is denoted as a Reversible Solid Oxide Electrolyzer Cell (RSOEC). The reverse operation as a fuel cell, combined with hydrogen storage, enables the RSOEC to act as a renewable power generator. It can provide valuable utility grid services such as peak load or backup power production [5].

Previous studies [6], [7] have proposed methods to reduce degradation at the cell level. Cycling between electrolysis and fuel cell mode at an hourly interval can significantly reduce degradation, as shown in [6]. Additionally, a new electrothermally balanced operation mode for RSOEC (Denoted as AC:DC operation) was proposed in [7], utilizing reversible operation mode to reduce degradation further, albeit with much shorter cycle times. The cyclic current operation of an RSOEC stack was experimentally shown to mitigate temperature variations in the stack, which cause uneven cell degradation and reduce the RSOEC stack lifetime. Furthermore, the AC:DC operation mode demonstrated an increased tolerance towards impurities and a reduction of nickel migration and agglomeration. This novel electrothermally balanced operation could result in a cost-effective approach to extend the lifetime of the RSOEC and ease scale-up possibilities. Efficient and reliable design of power electronics converters and associated control methods are imperative before implementing cyclic operation mode for large-scale grid-connected plants. However, there is a need to accelerate the development process to mature this technology. Rapid prototyping of power electronic converters and control methods can expedite this. Rapid prototyping accelerates the transition from simulation to physical implementation, which is often challenging due to its time-consuming, expensive, and facility-intensive nature. To apply rapid prototyping for maturing bidirectional power electronics converter systems needed for the cyclic operation of the RSOEC stack, an emulator for the RSOEC stack electrical dynamics is essential as this can facilitate the initial process of physical testing.

The research presented in this paper explores the design, development, and application of an emulator for the RSOEC stack electrical dynamics within the context of rapid prototyping interfacing DC-DC converter systems. In conducting a thorough review of the existing literature, it became apparent that there is a gap in the available research concerning this particular aspect. By examining the existing body of literature related to our research, it was observed that there has been conducted research within the design and usage of an emulator for other types of fuel cells and electrolyzers; this is presented in section III-A.

This paper hypothesizes that the proposed emulation techniques and design methodology for an RSOEC stack emulator will effectively support the rapid prototyping of power electronic converters and their associated control algorithms. The emulator should be able to replicate the electrical behavior of the RSOEC stack near a single operating point, in terms of temperature, age, and gas flow compositions. This paper's novelty lies in analyzing different emulation techniques and proposing a suitable design method for an RSOEC stack emulator representing its electrical dynamics. The method is validated by conducting a case study, where an RSOEC stack emulator for a commercial-scale RSOEC stack is developed. The RSOEC stack emulator is experimentally validated through a comparison of steady-state, frequency, and dynamic responses. At last, a case study for rapid prototyping of a bidirectional Buck-Boost converter with a Proportional, Integral, and Derivative with first-order Filter on the derivative term (PIDF) controller is tested experimentally. The primary purpose of the emulator is to be a tool for the rapid prototyping of power electronic converters and their associated control algorithms for SOEC stacks or RSOEC stacks in cyclic current operation mode.

Section II presents the operation, dynamics, and different modeling methods for the RSOEC stack. Section III analyzes different emulator design methods for the RSOEC. The chosen emulator design method for the RSOEC stack used in this paper is then discussed. Section IV validates the emulator's performance experimentally in both the time and frequency domain. In section V, the bidirectional buck-boost converter system is designed and validated experimentally using the emulator in cyclic operation mode. Finally, Section VI concludes the paper.

II. REVERSIBLE SOLID OXIDE ELECTROLYZER CELL

A Solid Oxide Cell (SOC) consists of three primary components: the cathode, the anode, and the electrolyte. The SOEC is characterized by an oxide ion-conducting electrolyte made of ceramic oxide. Steam electrolysis is performed at high temperatures, typically in the range of 600°C to 900°C. The high efficiency of the SOC is attributed to the high operating temperatures, which reduce electrochemical losses.

The basic operation of a SOEC involves feeding high-temperature steam to the cathode and applying a voltage potential to the cell. The electrolysis reactions at the anode and cathode can be seen in (1)

$$\begin{aligned} \text{Anode: } & O^{2-} \rightarrow O_2(g) + 2e^- \\ \text{Cathode: } & H_2O(g) + 2e^- \rightarrow H_2(g) + O^{2-} \end{aligned} \tag{1}$$

From these reactions, it can be observed that on the cathode side, added electrons reduce H_2O, producing H_2 and O^{2-}. The oxygen ions migrate to the anode through a solid electrolyte, where O_2 is produced. The SOEC can be operated as a fuel cell by reversing the process, feeding H_2 at the

cathode side and O_2 at the anode side. To operate an RSOEC plant at a larger scale, individual SOC cells are connected in series to provide a higher operating voltage. This is necessary because the SOC is only a few millimeters thick, providing a low cell voltage. Multiple cell connections in series are often referred to as a stack.

To facilitate the high-temperature electrochemical reactions for an RSOEC stack, an experimental test platform with several external components, such as pumps, compressors, buffer tanks, heaters, flow measurement, and control units, is required. An example of an RSOEC stack testing platform can be visualized using a process flow diagram in Fig. 1. Therefore, it might be challenging to have access to these facilities at power electronic research institutions.

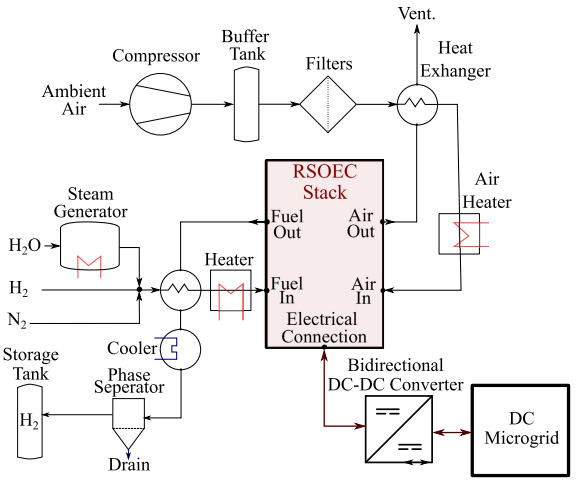

FIGURE 1. An example of a process flow diagram for an RSOEC stack testing platform.

III. METHODS

The main objective of the emulator designed in this paper is to provide accessible real-time emulation of the electrical dynamics of an RSOEC stack for experimental verification of power electronic converters and control methods prior to their deployment in real-world scenarios.

A. STATE OF THE ART

In this section, the state of the art is widened from only considering RSOEC technology to including all electrochemical hydrogen device technologies. Three different approaches exist for reproducing the electrical behavior of an electrochemical hydrogen device in real-time: Scaled models, real-time simulation, and analog emulators.

Scaled models are useful for downscaling plants for prototype testing in laboratories. This method can provide very detailed accuracy of the full-scale system. However, it still requires the use of specialized laboratory facilities for hydrogen experimentation. Furthermore, scaled model construction is often very costly and complex. Although the scaled-model approach has been widely used to investigate material and performance testing in a single-cell experimental setup. In [8], a full-scale stack emulation method is presented for PEM fuel cells, which uses a power amplifier for scaling up the voltage of a single cell.

Real-time simulation utilizes a real-time simulator platform to perform real-time simulation using a mathematical model. A common real-time simulation approach is Hardware In the Loop (HIL), which involves external interfacing of hardware, such as actual physical components, to be connected to the real-time simulator. A HIL real-time simulation involving power transfer is known as Power Hardware In the Loop (PHIL). In PHIL, a mathematical model of the RSOEC stack could be implemented on a real-time simulator, which could be used to control an external power amplifier, reproducing the electrical behavior in real-time. The accuracy of this method depends on the model's complexity and the computing performance of the real-time simulator. However, the price of the HIL approach is not high, as the cost is mainly from the real-time simulator and external power amplifier. Therefore, there is no requirement for special laboratory facilities. PHIL has been used for emulators for both alkaline [9], [10], [11] and PEM [12], [13], [14] technologies. The function of these PHIL emulators is mainly to match the real part of the impedance. This is due to the intended usage of these PHIL emulators, which is to study their integration into power systems. In [10], an analysis of the design of a high-frequency DC/DC converter and real-time simulator is presented, which has a time constant much lower than the plant. A simple modeling method using the Equivalent Circuit Model (ECM) is implemented on the real-time simulator. This method is experimentally validated to provide highly dynamic load emulation.

The analog circuit approach uses the fact that the dynamics of an electrochemical system can be described by an ECM. The ECM approach has been widely used to describe the frequency domain dynamics of fuel cells and electrolyzers using frequency domain data obtained from Electrochemical Impedance Spectroscopy (EIS). The ECM method can be parametrized with ideal and non-ideal components. For emulation purposes, the ideal component models are usable, the price of these components is low, the equivalent circuit is simple to construct, and there is no requirement for special facilities. However, restricting the use of ideal components gives the emulator limited accuracy. The analog circuit approach has been used in [15] to emulate a PEM electrolyzer. It is based on an equivalent passive circuit whose components reproduce the physical behavior of the PEM. In addition, it adopts a linear circuit to correct the I-V static characteristic and to retrieve the internal voltage. A dynamic comparison between a commercial PEM electrolyzer and the emulator shows that it provides a satisfactory dynamic response.

B. CHOICE OF EMULATOR APPROACH

To decide which of the emulator approaches is most suitable to fulfill the main objective of the emulator, a Multiple-Criteria Decision Analysis (MCDA) is conducted.

The four criteria for evaluating the emulator and their respective weightings are as follows:

- Accuracy (40%)
- Accessibility (30%)
- Price (20%)
- Simplicity (10%)

The criteria are defined as: Price is the cost of the emulator model. Accuracy is the emulator's ability to represent the electrical dynamics of the RSOEC stack, simplicity is the measure of the emulator's construction complexity, and accessibility is the requirement for special laboratory facilities. A high weighting for accuracy and accessibility is chosen, whereas price and complexity are less important.

To perform the MCDA, the qualitative measures of the different emulator approaches to fulfill the defined criteria are represented by a point system. The point-system measure goes from very bad (0) to very good (100). For the weighting selection and scoring of the emulators, a direct method has been utilized, with the authors as decision-makers.

The weighting of the four criteria is based on a compromise that the emulator approach should have sufficient accuracy of the RSOEC stack dynamics for power electronic system testing. Therefore, this criterion is given the highest weighting. Furthermore, the emulator approach should be assessable for all power electronic system engineers having a standard power electronic laboratory. Therefore, this criterion is also given a high weighting. For the method of using an emulator to be useful, the price and complexity of the emulator should also be considered. These two criteria are given a lower weighting.

The accuracy of using a scaled model is given a very good score, and as it emulates the electrical dynamics very precisely during different operating conditions, a high score is given. However, the HIL approach accuracy depends on the mathematical model of the RSOEC stack, and therefore, HIL could potentially also achieve good accuracy. The accuracy of the analog circuit is not that good, as it is limited to a single operating area and is therefore given a very low score.

The accessibility for a scaled model is given a very low score due to the need for special laboratory facilities. The accessibility for both the HIL and analog circuit approach is given an equally high score, as both just require the facilities of a power electronic laboratory.

The price for a scaled model is given a very low score due to the need for special laboratory equipment and an RSOEC. The price for HIL given a low score, due to the requirement of a fast real-time simulation device. Whereas the analog circuit just requires of the shelf electrical components, the score for the price is high. The simplicity of a scaled model is given a very low score due to the need to set up all the associated equipment for operating an RSOEC and electronics for scaling the power produced. The price for HIL given a decent score, this is due to the requirement of still having to get an adequate model of the RSOEC stack and develop the power electronics for interfacing the DC-DC converter. Meanwhile, an analog circuit just requires an assembly of electrical components. Therefore, the score for simplicity is high.

TABLE 1. MCDA for the emulator design approach.

Criteria	Weighting	Scaled model	HIL	Analog circuit
Accuracy	0.4	70	20	10
Accessibility	0.3	0	50	50
Price	0.2	5	20	75
Simplicity	0.1	0	25	75
Score		23.8	34.8	43.5

Table 1 presents the MCDA weighted-sum model for selecting the emulator design approach. The weighted scores indicate that the analog circuit design approach is the most suitable choice for achieving a satisfactory real-time hardware emulation of the electrical dynamics of an RSOEC stack in alignment with the specified criteria outlined in this paper. The main problem for the analog circuit approach, outlined from the MCDA is the low accuracy. However, it should be noted that the change in operating conditions for a commercially operated RSOEC stack is often very limited, and therefore, this approach is still useful in its ability to represent the electrical dynamics of the RSOEC stack.

C. DESIGN OF ANALOG CIRCUIT EMULATOR

The application of EIS is mainly as a tool for investigating the electrical and electrochemical properties of electrochemical devices. This is because there is often a correlation between the behavior of an actual system and that exhibited by an ECM composed of discrete electrical components. By fitting the impedance data obtained by EIS to an ECM, whose elements are representative of the physical processes taking place in the RSOEC stack, analogies between the circuit elements and electrochemical processes can then be made. The data fitting results can then be easily converted into a physical understanding of the internal processes in an RSOEC stack.

However, the authors have, in previous work [16], presented a lumped ECM for the representation of the electrical dynamics of a commercial RSOEC stack. The parameterization of the Voigt ECM is based on experimental data obtained from EIS on a commercial RSOEC stack, G8-80, from SolydEra SpA. This stack has a nominal capacity of 4.5 kW for electrolysis and 1.5 kW for fuel-cell operation. The averaged parameterization was conducted using a gray-box modeling approach from the EIS data at different gas flow mixtures, degradation stages, and temperatures. The developed ECM consisted of two RC elements and a single resistor in series, also denoted as a Voigt circuit configuration. The electrical dynamics of the presented ECM were simulated and compared to experimental data in cyclic operation at different degradation stages. The comparison showed that the nominal ECM adequately described the fundamental electrical dynamics of an RSOEC stack.

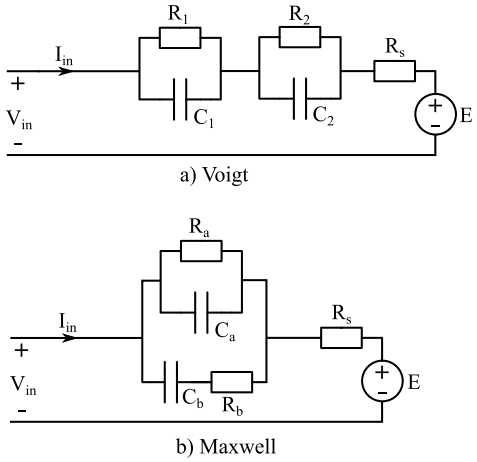

FIGURE 2. The impedance equivalent electrical circuit configurations for the emulator.

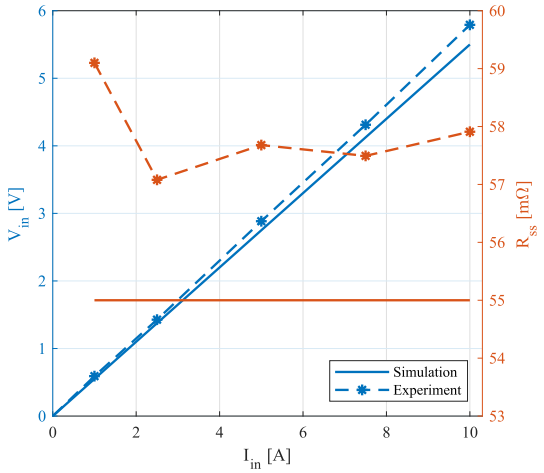

FIGURE 3. Experimental and simulated I-V curve and steady-state resistance for the emulator in the electrolysis mode.

TABLE 2. Electrical parameters for the analog electrical circuit for the RSOEC stack emulator at an operating temperature of 750°C [16].

	C_1 [μF]	C_2 [mF]	R_1 [Ω]	R_2 [Ω]	R_s [Ω]	E [V]
Voigt	470	610	0.21	0.15	0.20	62
	C_a[μF]	C_b [mF]	R_a [Ω]	R_b [Ω]	R_s [Ω]	E [V]
Maxwell	470	210	0.36	0.26	0.20	62
Emulator	487	218	0.35	0.25	0.20	58

The parameterization of the ECM in the Voigt circuit configuration exhibits a large capacitor. Therefore, this paper uses an equivalent circuit approach to reduce the capacitor size by converting the Voigt circuit into a Maxwell circuit configuration [17]. The electrical circuit of the Voigt and Maxwell ECM can be seen in Fig. 2. The ideal Voigt and Maxwell equivalent analog circuits parameters for their lumped components for an operating temperature of 750°C, given in Table 2. The developed emulator is based on the Maxwell ECM and can be seen in Fig. 9. The components are attached to a custom-developed 2-layer PCB for easy installation. The power paths are primarily located on the bottom layer of the PCB and are not shown in the figure. It should be noted, however, that the circuitry could have been constructed more simply, for example, using a breadboard. It should be noted that due to utilizing off-the-shelf components, a small discrepancy between the nominal Maxwell ECM and the developed emulator's parametrization can be seen in Table 2. To realize the rather large capacitance of the C_2 capacitor, several unipolar aluminum capacitors with a tolerance of 20% were utilized (TDK B41231). Due to the unipolarity of these capacitors, the emulator cannot be used for experiments where the emulation is only for fuel-cell mode or in cyclic operation where a predominant amount of time is spent in fuel-cell operation mode. The smaller capacitance of the C_1 is realized by using several bipolar multilayer ceramic capacitors with a tolerance of 20% were utilized (Samsung CL32). To realize the resistors in the ECM, several cemented wire-wound resistors with a tolerance of 5% were utilized (Vishay AC04). Furthermore, due to the power dissipation limit of the ceramic power resistors used for the emulator's resistors, only a maximum average current of 6 A can be applied. The Open Circuit Voltage (OCV), E, for the emulator, is reduced to 58 V to accommodate the voltage limit of the Power Supply Unit (PSU) used in the experimental setup.

IV. RESULTS AND ANALYSIS

A. EXPERIMENTAL APPARATUS

The performance of the developed emulator is experimentally investigated in different domains. The experimentally obtained results are compared to a simulation model using Maxwell ECM using the emulator's parameterization. The simulations were performed in MATLAB Simulink using Simscape Electrical. This model is denoted as the nominal model for the RSOEC stack. The nominal model is used for representing the electrical dynamics of an RSOEC stack. The simulation model was initialized with all initial conditions set to zero for consistency across all simulations. However, it's important to note that the simulation data presented reflects a settled state, indicating that the system has reached a stable condition regardless of the initial conditions. This approach ensures that the analysis focuses solely on the steady-state behavior of the system and does not consider any transient effects resulting from non-zero initial conditions. Only the passive components of the emulator are investigated in this section; therefore, no PSU is utilized, so the OCV, $E = 0$. The experimental data acquisition for this section is conducted using a Keysight DSOX3024T oscilloscope.

B. STATIC PERFORMANCE

The static performance of the emulator is validated by using a PSU and applying a fixed current, then measuring the steady voltage in electrolysis mode only. The current and voltage measurements are visualized utilizing an I-V curve in Fig. 3. The I-V curves show a very similar equivalent

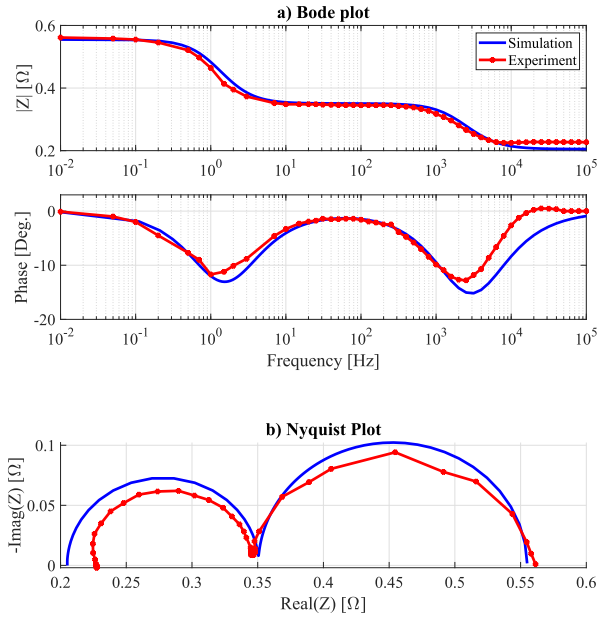

FIGURE 4. Comparison of the frequency response data between the nominal model and the emulator using: a) Bode plot and b) Nyquist plot.

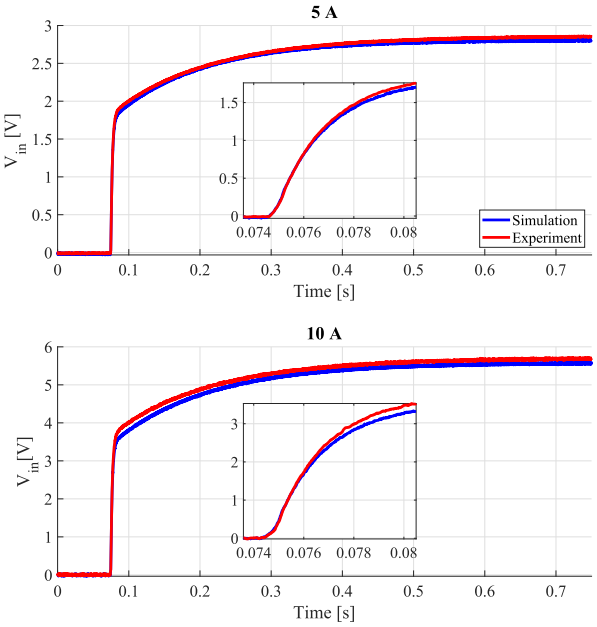

FIGURE 5. Comparison of the time-domain voltage response data between the nominal model and the emulator at two different applied current steps.

steady-state resistance, denoted as R_{ss}. However, a small mean discrepancy of around 27 mΩ was observed. The discrepancy is most likely due to the component tolerances and wiring; however, this is not thought to have an impact on the emulator's performance, as the discrepancy is less than 5% of the total steady-state resistance.

C. FREQUENCY DOMAIN PERFORMANCE

The performance of the emulator is compared to the nominal ECM model of the RSOEC stack in the frequency domain by conducting a Frequency Response Analysis (FRA). The frequency response describes how the circuit responds to different frequencies of input signals, representing the behavior in terms of amplification and phase shift across the frequency spectrum. The FRA is conducted using the built-in frequency response analyzer of the Keysight DSOX3024T oscilloscope, which measures the current to the emulator and calculates the gain and phase shift relative to the measured applied sinusoidal input voltage. However, to amplify the excitation signal from the oscilloscope, a power operational amplifier is utilized to amplify both voltage and current to drive the low-impedance emulator. The FRA was conducted in electrolysis mode only due to the unipolar capacitors. Therefore, the input signal to the emulator was offset by 500 mV and had a peak excitation voltage of 300 mV. A comparison of the frequency response between the nominal model and the RSOEC stack emulator, represented in both a Bode and Nyquist plot, can be seen in Fig. 4.

By comparing the frequency response data using the Bode Plot, it can be seen from the magnitude plot that the two impedance drops match quite well in magnitude and frequency occurrence. However, at high frequency, an impedance discrepancy of about 25 mΩ can be seen, which matches the discrepancy seen in the static I-V test in Fig. 3. The phase plot shows that the phase drop at the low frequency matches well in both phase and frequency occurrence. The phase drop at the high frequency matches well at the frequency occurrence; however, the experimentally measured phase drop is about 2 degrees less than the simulated phase drop and is narrower. This might indicate some parasitic resistance or inductance in the circuit.

The Nyquist plot shows that the frequency response data between the nominal model and the emulator seem to fit quite well. However, the simulated high-frequency arc is wider than the experimentally measured one. This could mean that the combination of components R_a, R_b, and C_a in the Maxwell representation has a slight deviation from their nominal value. However, this deviation could be caused by the tolerance of the components used for the emulator. The high-frequency arc deviation is relatively small, so it will not have a noticeable impact on the emulator's performance.

D. DYNAMIC PERFORMANCE

Initially, the dynamic performance of the RSOEC stack emulator is conducted by applying two different current amplitude steps to the emulator using a controllable PSU. It should be noted that for the current step excitation of the simulation model, the measured experimental current step data is utilized. Acquiring an idealized current step from a power supply proves challenging owing to inherent limitations within real-world electronic components and the limited bandwidth of the internal control loops of the PSU.

The time-domain voltage response data comparison between the nominal model and the emulator under two distinct applied current steps is shown in Fig. 5. By comparing

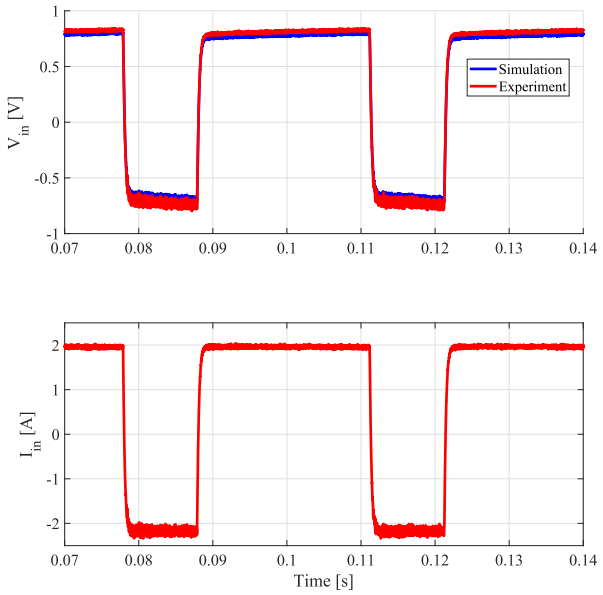

FIGURE 6. Comparison of the voltage response of simulation and emulator when an alternating current square wave signal is applied.

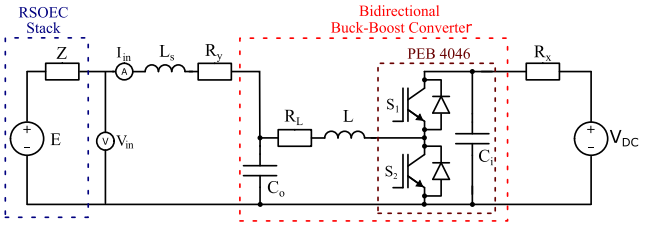

FIGURE 7. Schematic of the experimental setup of the bidirectional Buck-Boost converter connected to RSOEC stack emulator.

TABLE 3. Parameters of the bidirectional buck-boost converter.

Description	Symbol	Value
Switching frequency	f_{sw}	25 kHz
Sampling frequency	f_s	25 kHz
Input voltage	V_{DC}	200 V
Input capacitor	C_i	1.2 mF
Output capacitor	C_o	100 μF
Inductor	L	480 μH
ESR Inductor	R_L	10 mΩ
DC-bus wire resistor	R_x	75 mΩ
Stack wire resistor	R_y	150 mΩ
Parasitic inductor	L_s	60 nH

the step responses, it can be seen that simulation and experimental results are very similar. In both cases, there is only a slight difference in the rise time, less than 0.1 ms. The steady-state voltage response fits well, with only a slight deviation caused by the increased resistance in the emulator, which was also found in the previous experiments.

To compare the dynamic performance of the RSOEC stack emulator in cyclic operation mode, the emulator is driven by an alternating current square wave signal from a waveform generator using a power operational amplifier. Again, it should be noted that the measured cyclic current is used to excite the simulation model.

The voltage response from the simulation and experiment when an alternating current square wave is applied can be seen in Fig. 6. The alternating square wave current has a frequency of 30 Hz, with a duty cycle of 0.7. The transient voltage response fits well in both directions, with similar rise times. There is only a slight deviation in the steady-state voltage response due to the increased resistance in the emulator, as found in the previous experiments.

V. APPLICATION: RAPID-PROTOTYPING OF BIDIRECTIONAL CONVERTER SYSTEM

In this section, the developed emulator will be utilized for the experimental verification of a bidirectional Buck-Boost converter operating in constant conduction mode (CCM). The control algorithm used is PIDF to track the cyclic output current reference. The schematic of the bidirectional Buck-Boost converter with the RSOEC stack emulator can be observed in Fig. 7, with the parameters listed in Table 3. The size of the components for the bidirectional Buck-Boost converters is determined by setting the limits of the current ripples allowed. The current limits were set to a maximum inductor current ripple of 30% of the average inductor current and a maximum input current ripple to the RSOEC stack of 5%.

A. CONTROL DESIGN

For the control design, an extended small signal averaged model based on the model derived in [18] is utilized. The small signal averaged model of the plant is presented in the general state-space form in (2)

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ y(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \end{aligned} \tag{2}$$

where $\mathbf{x}(t)$ is the state vector, $y(t)$ is the output, and $\mathbf{u}(t)$ is the input vector. The matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{D}$ are the state, input, output, and feedthrough matrices, respectively. The state space vectors and matrices for the plant are given in (3).

$$\mathbf{A} = \begin{bmatrix} \frac{-(R_a+R_b)}{C_a R_a R_b} & \frac{-1}{C_a R_b} & 0 & 0 & 0 & \frac{1}{C_a} \\ \frac{-1}{C_a R_b} & \frac{-1}{C_a R_b} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_i R_x} & 0 & \frac{-\bar{D}}{C_i} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_o} & \frac{-1}{C_o} \\ 0 & 0 & \frac{\bar{D}}{L} & \frac{-1}{L} & \frac{-R_L}{L} & 0 \\ \frac{-1}{L_s} & \frac{-1}{L_s} & 0 & \frac{1}{L_s} & 0 & \frac{-(R_s+R_y)}{L_s} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 & \frac{1}{C_i R_x} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_s} \\ 0 & 0 & \frac{-\bar{I}_L}{C_i} & 0 & 0 & \frac{\bar{V}_i}{L} \end{bmatrix}^\top$$

$$\mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{D} = \mathbf{0}_{3\times 3}$$

$$\mathbf{x}(t) = \left[\tilde{v}_{ca}(t)\ \ \tilde{v}_{cb}(t)\ \ \tilde{v}_i(t)\ \ \tilde{v}_o(t)\ \ \tilde{i}_L(t)\ \ \tilde{i}_s(t)\right]^\top$$
$$\mathbf{u}(t) = \left[\tilde{v}_{dc}(t)\ \ \tilde{E}(t)\ \ \tilde{d}(t)\right]^\top$$
$$y(t) = \tilde{i}_s(t) \tag{3}$$

The tilde notation in the states indicates small-signal quantities near the linearization point. Where, the voltages across the Maxwell ECM capacitors C_a and C_b are $\tilde{v}_{ca}$ and $\tilde{v}_{ca}$, respectively. The voltages across the input and output capacitor of the bidirectional Buck-Boost converter, C_i and C_o, are $\tilde{v}_i$ and $\tilde{v}_o$, respectively. Furthermore, the current through the inductor of the bidirectional Buck-Boost converter is denoted $\tilde{i}_L$. Whereas the current through the parasitic inductor of the RSOEC stack and the connection wires is denoted $\tilde{i}_s$. It should be noted that the current through the parasitic inductor I_s is equal to the input current to the RSOEC stack I_{in}.

The linearization point is indicated by the average values of the duty cycle, input capacitor voltage, and inductor current denoted $\bar{D}$, $\bar{V}_i$ and $\bar{I}_L$, respectively.

The small-signal averaged model is appropriate for control design, yet its precision diminishes at higher frequencies due to neglecting high-frequency dynamics. As a result, a common guideline is to refrain from using the small-signal averaged model beyond one-tenth or one-sixth of the switching frequency [19].

The frequency response of the duty-cycle perturbations effect on the input current to the RSOEC stack emulator can be extracted from the small-signal model of the bidirectional Buck-Boost converter supplying the Maxwell ECM representing the RSOEC stack at the nominal prototype operating point.

It was necessary to discretize the continuous open-loop plant models to design a digital control, and for this task, the Zero-Order-Hold (ZOH) method was employed. The frequency responses can be seen in Fig. 8 at the linearization point $\bar{D} = 0.29$, $\bar{V}_i = 200$ V, and $\bar{I}_L = 4$ A. By comparison of the continuous and discretized transfer function, a close similarity is seen at lower frequencies. Due to the ZOH discretization, a small magnitude discrepancy close to the Nyquist frequency is seen, and an increasing phase drop starts close to the desired crossover frequency. The phase drop is small near the crossover frequency and should not impact the closed-loop system response.

Furthermore, from the magnitude plot, it can be seen that the gain of the system is high, which means that a small duty cycle perturbation will cause a significant change in the input current to the RSOEC stack emulator. It is, therefore, important for the digital output of the Digital Signal Processor (DSP) for the PWM generation to have a sufficient resolution. In these experiments, a sufficient resolution was achieved by using a dSPACE MicroLabBox, which has a 10 ns resolution for PWM generation. This PWM resolution gives a theoretical maximum current resolution of approximately 60 mA at a 25 kHz switching frequency at the linearization point. The intended control system is

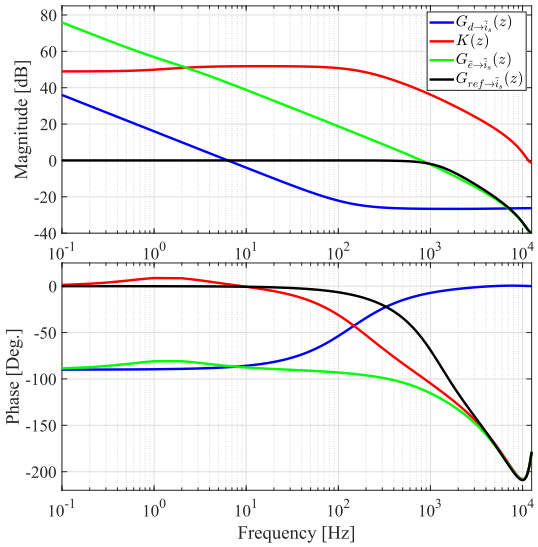

FIGURE 8. Bode plot for the discrete plant, PIDF controller, and open-loop and closed-loop system.

formulated to meet specific design requirements provided by the control system design engineer. In this paper, we outline the identified control system design requirements as follows:

- A cut off frequency f_{co} of the system placed in the range of $20 f_{cyclic} < f_{co} < f_s/20$
- A rise time within 10% of the minimum fuel-cell mode operating time.
- A 5% settling time within 20% of the minimum fuel-cell mode operating time.
- A limited overshoot of a maximum 10%.
- A steady-state error within 1%.
- A phase margin above 40 degrees.

The cut-off frequency needs to be sufficiently high to track the cyclic reference effectively. This paper sets an adequate threshold at 20 times the cyclic current reference frequency. Additionally, the cut off frequency should be low enough compared to the sampling frequency to accurately sample the current measurement and prevent aliasing distortion. For this, a suitable cut-off frequency limit is defined as 20 times less than the sampling frequency. To guarantee a certain amount of steady-state operation in each of the modes, a criterion is set such that the settling time should be within 20% of the minimum fuel-cell mode operating time, implying a maximum settling time of 0.54 ms. Furthermore, to ensure the RSOEC stack operates at the desired current level, the steady-state error should be within 1%. Overshoot must be constrained to avoid imposing unnecessary stress on the RSOEC within the stack. Therefore, the overshoot must not exceed 10%. The mathematical representation of the plant, in comparison to the experimental setup, exhibits a significant degree of uncertainty. Therefore, a phase margin of at least 40 degrees is desired to ensure stability. To fulfill these criteria, we employ a PIDF control algorithm. The choice of controller is based on that the proportional term ensures a fast rise time, the integral term will ensure zero steady-state error,

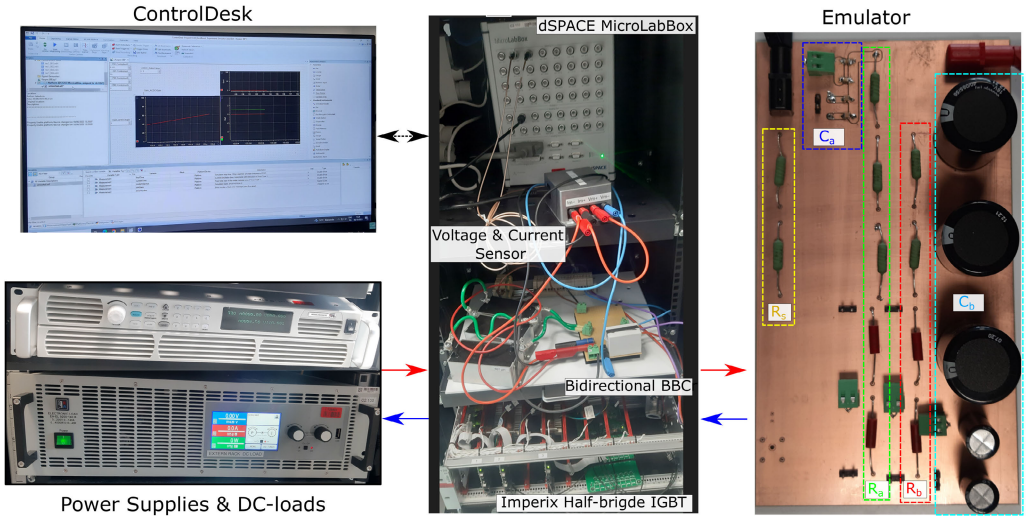

FIGURE 9. Experimental setup.

TABLE 4. Parameters of the discrete PIDF controller.

k_p	k_i	k_d	τ_F
47.1×10^{-3}	39.7	59.7×10^{-9}	45.2×10^{-6}

TABLE 5. Performance metrics for the designed PIDF controller.

GM [dB]	PM [Deg.]	f_{co} [Hz]	BW [Hz]
17.1	64.5	1000	1300

and the derivative term with a filter will improve the transient response, specifically lowering the overshoot caused by the integral term.

The general parallel transfer function representation of the discrete PIDF controller is implemented using the forward Euler method, as in (4)

$$K(z) = k_p + \frac{k_i T_s}{z-1} + \frac{k_d}{\tau_F + \frac{T_s}{z-1}} \tag{4}$$

where $K(z)$ is the discrete transfer function of the PIDF control algorithm. k_p and k_i are the proportional and integral gains.

As this paper mainly focuses on using emulators for rapid prototyping, the PIDF control algorithm is tuned using the Matlab Control Toolbox to fulfill the control design requirements. The open-loop and closed-loop system consist of the designed PIDF controller and the plant model and is given in (5)

$$\begin{aligned} G_{e\to\tilde{i}_s}(z) &= K(z)\, G_{\tilde{d}\to\tilde{i}_s}(z) \\ G_{ref\to\tilde{i}_s}(z) &= \frac{G_{e\to\tilde{i}_s}(z)}{1 + G_{e\to\tilde{i}_s}(z)} \end{aligned} \tag{5}$$

where $G_{e\to\tilde{i}_s}(z)$ is the discrete open-loop system describing the response from the error to the perturbation on the input current. $G_{ref\to\tilde{i}_s}(z)$ is the discrete closed-loop system describing the response from the reference to the perturbation on the input current.

The frequency response of discrete plant, PIDF controller, and open-loop and closed-loop system can be seen in Fig. 8.

To numerically evaluate the performance metrics from the Bode plot, such as the Gain margin (GM), Phase Margin (PM), cut-off frequency (f_{co}), and Bandwidth (BW) for the system, these are listed in Table 5.

B. VALIDATION

To validate the efficiency of the proposed method, the developed analog emulator is used for rapid prototyping of a bidirectional DC-DC converter, and a current feedback control algorithm. The method's efficiency is based on a comparison between the simulation and experiments for a case study. The experiments were conducted at the Renewable Energy Control Laboratory (RECL) at AAU Esbjerg; the experimental setup can be seen in Fig. 9.

The designed PIDF controller was implemented on a dSPACE MicroLabBox controller platform using ControlDesk. The bidirectional Buck-Boost converter was built with the values of the components listed in Table 3.

A half-bridge with IGBTs from an Imperix PEB4086 board was utilized for the switches.

However, to achieve the bidirectional power supply necessary for both the DC bus and the OCV of the RSOEC stack, a PSU operating in constant voltage mode is connected in parallel with a DC load set to operate in constant current mode. The sunk current by the constant current load is maintained at twice the level necessary for electrolyzer or fuel cell operation, ensuring that dynamic operation is not constrained. To validate the effectiveness of using the emulator for experimental validation of the designed control algorithm, a scenario where the bidirectional Buck-Boost

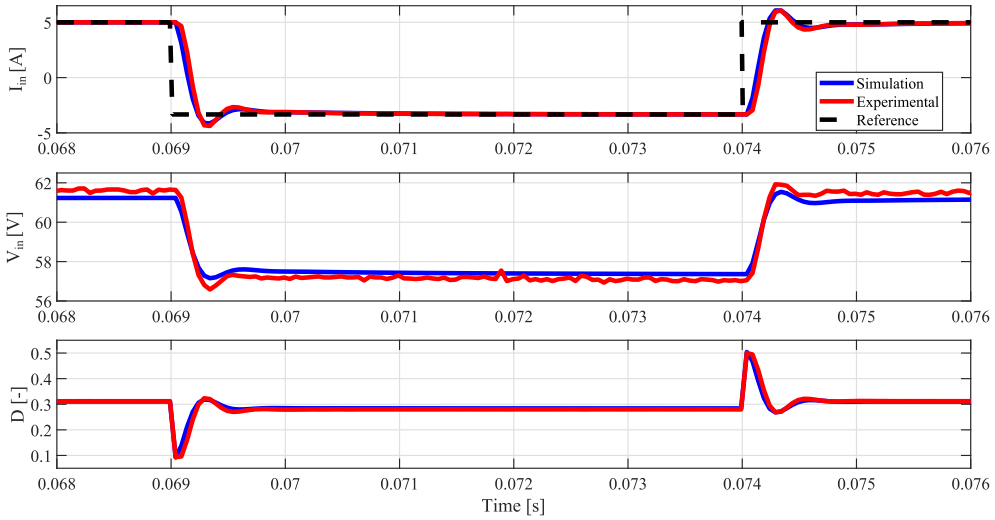

FIGURE 10. Comparison of time domain dynamics for the input current, input voltage, and duty-cycle from the simulation and experiment during cyclic current tracking operation.

converter system should be able to track the cyclic current reference at 40 Hz with electrolysis to fuel cell operation mode ratio of 0.8. The comparison between the simulated and experimental response can be seen in Fig. 10. By comparing the time domain performances for the output current, it can be seen that the two responses look similar. However, the simulation results show a slightly larger rise time, less than one sample time (50μs), and no overshoot as in the simulation. But, the 5% settling time is similar. The reason for the deviance between the responses may be caused by parameter uncertainties for the real circuit elements for both the converter and emulator. But also the usage of non-ideal PSU and DC loads. However, a very similar transient dynamic can be seen by comparing the two voltage responses. However, a steady-state voltage deviation can be seen. This voltage deviation is thought to be caused by the uncertainty of the resistors R_x and R_y, representing the interconnection wires and internal resistances of the PSU. But also the difference between the different components in the experimental setup. The validation of the case study using an emulator for testing the hardware in a real-world scenario, provided valuable insights into the effectiveness of the method, for ensuring successful implementation for the full-scale RSOEC stack.

VI. CONCLUSION

This paper introduced a novel analog emulator and evaluated its effectiveness in the rapid prototyping of power electronic converters and control systems for interfacing with RSOEC stacks. Recognizing the complexities and cost constraints of traditional setups, the study explored three real-time emulation techniques. Through MDCA, an analog circuit approach was identified as the most promising. Leveraging this approach, the emulator employed an ECM tailored for the rapid prototyping of power electronic converter systems. Experimental validation confirmed the emulator's ability to accurately replicate the scaled electrical dynamics of a mathematical model of a commercial RSOEC stack.

To validate the emulator's effectiveness for rapid prototyping, a bidirectional Buck-Boost converter, incorporating a PIDF control algorithm for cyclic current reference tracking, was meticulously designed and implemented. Comparative analysis of simulated and experimental time domain responses demonstrated significant alignment, with minor discrepancies attributed to inherent uncertainties in the physical system. Nevertheless, the experimental validation of the bidirectional Buck-Boost converter, coupled with the PIDF control algorithm, underscored its effectiveness in the rapid prototyping of interfacing power electronic systems enabling cyclic-operated RSOEC stacks.

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