IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 6 June 2024, accepted 18 June 2024, date of publication 24 June 2024, date of current version 30 August 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3418571

RESEARCH ARTICLE

A Single-Stage 0X/1X Regulating Rectifier With Improved Voltage Mode Delay Compensation for Wirelessly Powered Implantable Medical Devices

SILONG CHEN, (Student Member, IEEE), GUANGYIN SHI, XIN LIU, XINGCHEN XU, BIN WANG, AND ZHIQIANG LI, (Member, IEEE)

Institute of Microelectronics of the Chinese Academy of Sciences, Beijing 100029, China
University of Chinese Academy of Sciences, Beijing 100049, China
Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences, Beijing 100029, China

Corresponding authors: Xin Liu (liuxin@ime.ac.cn) and Zhiqiang Li (lizhiqiang@ime.ac.cn)

This work was supported by the Chinese Academy of Sciences (CAS) Youth Interdisciplinary Team under Grant JCTD-2022-07.

ABSTRACT This article presents a 6.78 MHz single-stage wireless power transfer (WPT) receiver (RX) using 0X/1X regulating rectifier with improved voltage mode (VM) delay compensation for implantable medical devices (IMDs). The regulation of 0X/1X modes is achieved through pulse width modulation (PWM), with the frequency set at 1/16 of the carrier clock to ensure circuit stability and enhance power conversion efficiency (PCE) under light loads. VM delay compensation has the advantage of power consumption. However, the traditional VM on-delay compensation may become ineffective because a large voltage pulse will occur on the RX side input when the circuit delays increase. Therefore, an improved VM on-delay compensation method is proposed. Coarse compensation for on-delays can be achieved by reusing the control signal generated from off-delay compensation loop, as off-delay compensation processes will not be influenced by on-delay compensation processes. It allows the on-delay compensation loop to function normally and finely compensate for on-delays. The proposed rectifier is designed in 0.18μm CMOS process. It can achieve output voltage management of 1.8V. Comparing with other regulating rectifier, the proposed rectifier has a fast transient response of 14 μs and a small chip area of 0.91 mm^2. The simulation results indicate that this rectifier can attain high PCE of 84.6% in light load (500Ω) and peak PCE of 93.5% in heavy load (50Ω). The high voltage conversion ratio (VCR) of over 93% is also achieved under the large circuit delays.

INDEX TERMS Implantable medical devices (IMDs), pulse width modulation (PWM), power conversion efficiency (PCE), single-stage regulating rectifier, voltage mode (VM) delay compensation, voltage conversion ratio (VCR), wireless power transfer (WPT).

I. INTRODUCTION

Wireless power transfer (WPT) technology has become widespread for charging a variety of devices, including portable electronics [1], electric vehicles [2] and especially implantable medical devices (IMDs) such as bionic systems [3], neural recording [4] and so on. In IMDs, the adoption of WPT techniques plays a pivotal role in eliminating the need for cumbersome batteries which often necessitates frequent replacements through surgical procedures [5]. A typical WPT system comprises a power transmitter (TX) and a power receiver (RX), as depicted in Fig.1(a). The TX side involves a primary coil driven by a power amplifier (PA). It transmits ac power to the secondary coil through resonant

The associate editor coordinating the review of this manuscript and approving it for publication was Valerio De Santis.

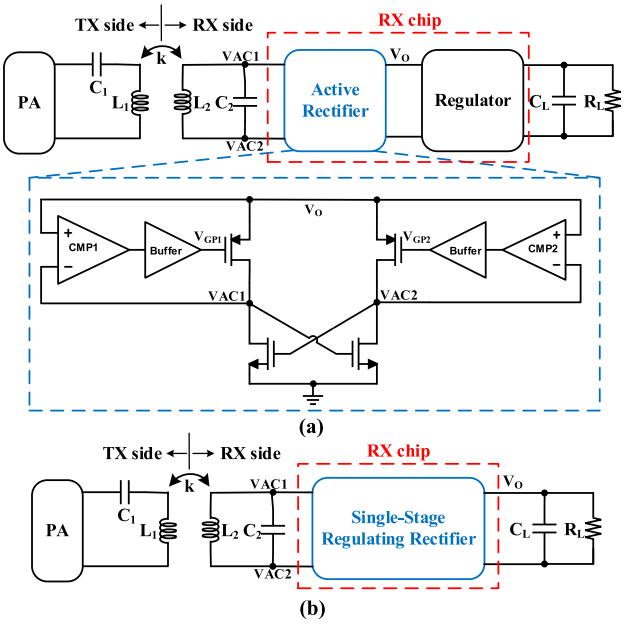

FIGURE 1. The structure of (a) typical WPT system and (b) single-stage regulating WPT system.

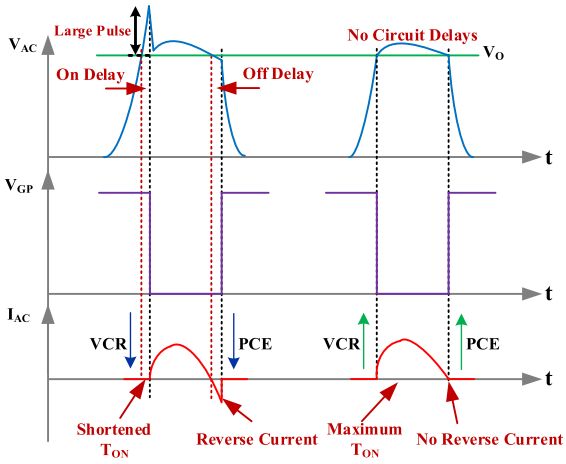

FIGURE 2. Impacts of on/off delays.

magnetic field. The resonant frequency is restricted according to the industrial, scientific and medical (ISM) bands. On RX side, the received ac power is rectified by active rectifier, followed by the application of a regulator to ensure a stable dc voltage for the connected loads. For the RX side, reducing the chip size is crucial because it need to be implanted inside the body. Additionally, achieving high PCE and VCR is important to minimize heating and improve the voltage utilization rate. So, current research focuses on two main areas: the ways of output voltage regulating and circuit delay compensation.

For output voltage regulating, a second-stage voltage regulator such as low dropout regulator (LDO) [6], [7] or switching regulator [8], [9], [10] is typically added. However, the efficiency of the LDO is constrained by the ratio of the output voltage to the input voltage. Moreover, the power loss in the LDO is large and can lead to heating issues. Efficiency enhancement is possible by employing a switching converter capable of maintaining high efficiency across a wide input and output range. However, this comes at the expense of requiring a bulky inductor, significantly increasing the chip area [11]. Therefore, integrating rectifier and regulator into a single stage and thus efficiently and space-savingly regulating output voltage is necessary, as shown in Fig.1(b). The common approaches for single-stage output regulating are switching among diode-closed(0X), half-bridge(1/2 X), full-bridge(1X), or voltage-double(2X) modes to ensure stable output voltage when coil coupling and output loads change. A 1X/1/2 X/0X reconfigurable rectifier is proposed in [11]. It has the fast transient response. However, it needs four active diodes which cause the silicon cost significantly increasing and the logic of switching among 1X/1/2 X/0X modes is complex. The 1X/2X mode rectifier proposed in [12] and [13] uses a combination of local and global adjustments to achieve output voltage management. It utilizes three active power transistors which may occupy a large chip area. In addition, this structure is only suitable for high-power outputs and its efficiency is low in light loads. In [14] and [15], a 1X/0X mode rectifier is introduced, where in the 0X mode, the losses are reduced by adjusting the input power at TX. Nonetheless, the receiver's transient response could be delayed as the feedback needs to pass through the transmitter to adapt the transferred power in response to changes in RX side load. Although these works have achieved single-stage output regulation, they still have shortcomings in terms of large chip area, complex regulating circuit, slow transient response or low efficiency in light load, making them unsuitable for using in IMDs.

For circuit delay compensation. The genetic active rectifier, depicted in Fig.1(a), is composed of cross-coupled NMOS transistors and PMOS transistors controlled by comparators (active diodes). Ideally, PMOS would switch once V_{AC} rises above (drops below) V_O. In practice, the existence of circuit delays will cause the PMOS to turn on/off late. The turn-on delays (on-delays) will lead to a reduction in conduction time T_{ON} and a large pulse. The turn-off delays (off-delays) will lead to large reverse current. They potentially undermine both VCR and PCE, as shown in Fig.2. Therefore, compensating for circuit delays is important. There are two commonly used methods for delay compensation: voltage mode (VM) delay compensation and current mode (CM) delay compensation. The compensation method employed in [16], [17], [18], and [19] is based on current-injection mode. The offset currents are directly injected into push-pull comparator and the comparator will trip early by using the unbalanced bias mechanism to eliminate circuit delays. The CM delay compensation has the advantages of wide compensation range and simple structure. Nevertheless, this mode requires additional injection of offset current, leading to increased power consumption. VM compensation method is employed in [20] and [21]. The MOS transistors operating in the linear region act as tunable resistors. Its resistance can be regulated by varying gate voltages

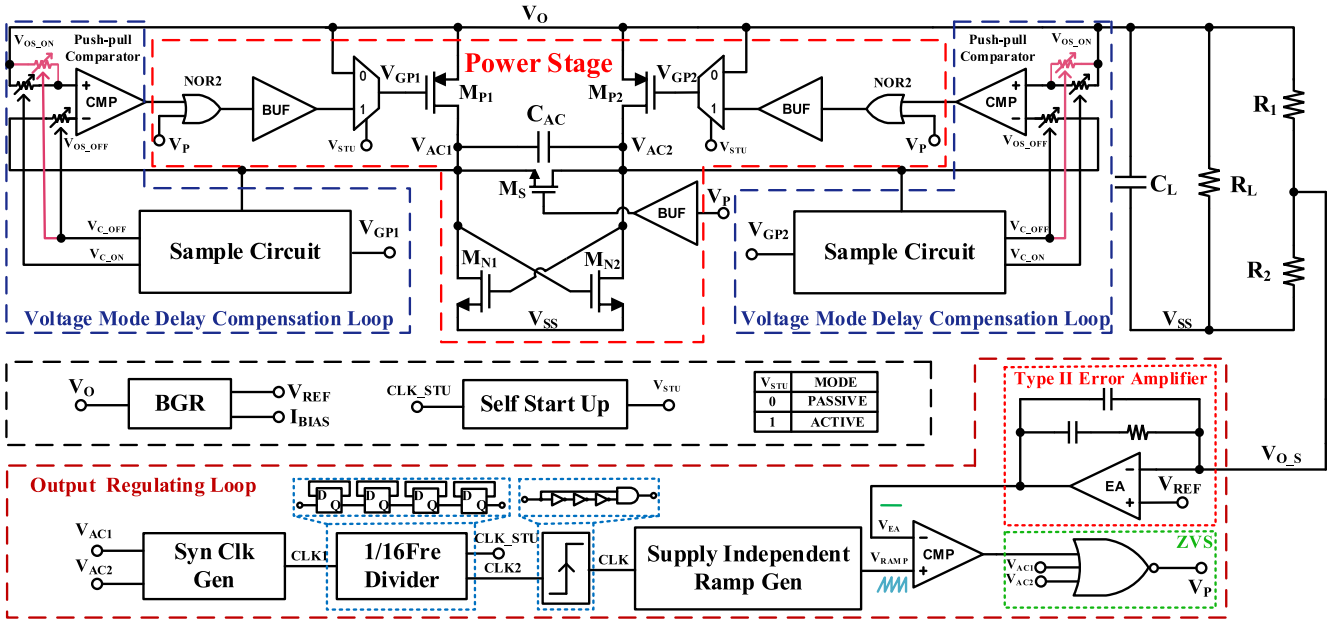

FIGURE 3. System architecture of the proposed single-stage regulating rectifier.

generated through feedback, directly creating a bias voltage at the input of the comparator to compensate for circuit delays. This mode, which need no additional current injection, demonstrates lower power consumption compared to the CM. However, when the circuit delays increase, V_{AC} may have a large pulse at the falling edge of V_{GP}. This large voltage pulse will result in a sampling failure for on-delays. Traditional VM on-delay compensation loop fails to operate effectively. Consequently, the on-delays can't be compensated and the VCR may significantly be reduced.

In this article, we proposed a single-stage 0X/1X regulating rectifier with improved VM delay compensation. There are two main contributions:

A: For single-stage output voltage regulating. We proposed a frequency-divided PWM local control method. The stable output is achieved by switching 0X/1X mode using PWM local control loop whose frequency is 1/16 of the carrier clock. It can improve the efficiency in light load as the switching loss is low. Meanwhile, due to the simple structure of the PWM local control loop, a small chip area and fast transient response can be achieved which is suitable for IMDs applications.

B: For delay compensation. We proposed an improved VM compensation method. Coarse on-delay compensation can be achieved by reusing the error signal produced from off-delay compensation loop. It can decrease the large pulse of V_{AC}, allowing the on-delay process to take effect and finely compensating for on-delays. This method can compensate for on/off delays effectively even though there is a large pulse in the RX side input due to the large on-delay.

The rest of this paper is organized as follows. Section II presents the proposed single-stage regulating rectifier in details, including the output regulating circuit, delay compensation circuit and self-start-up circuit. Section III shows the simulated results, including stability analysis, system-level transient waveforms and power loss analysis. Finally, the conclusion is drawn in Section IV.

II. PROPOSED SINGLE-STAGE REGULATING RECTIFIER

The system architecture of the proposed single-stage regulating rectifier is illustrated in Fig.3. It concludes the power stage, the output regulating loop, the improved voltage mode delay compensation loops, the bandgap reference (BGR) and the self-start-up module. The power stage mainly consists of two cross-coupled NMOS power transistors (M_{N1}, M_{N2}), a pair of comparator-based PMOS transistors (M_{P1}, M_{P2}), switch M_S, and buffers. The output regulating loop regulates the output voltage without the need for a second-stage regulator. The improved VM delay compensation loops are used to eliminate on/off delays. BGR provides a reference voltage and bias currents. The self-start-up module guarantees the normal operation of the receiver during the rising process of output voltage V_O. More details are introduced below.

A. OUTPUT REGULATING LOOP

The principle of output regulating loop is shown in Fig.3 and the relationships of the regulating signals are shown in Fig.4(a). The synchronous clock *CLK1* is generated from V_{AC1} and V_{AC2} by comparators. It undergoes a division by sixteen using four D flip-flops to produce *CLK2*. There exists a potential enhancement in efficiency under light loads when compared to regulating the output voltage in every cycle of the input signal, as the switching losses are small. *CLK2* is utilized to trigger the rising edge detector, subsequently generating a pulse signal denoted as *CLK*. This signal is then employed to generate the ramp signal V_{RAMP}. The slop of

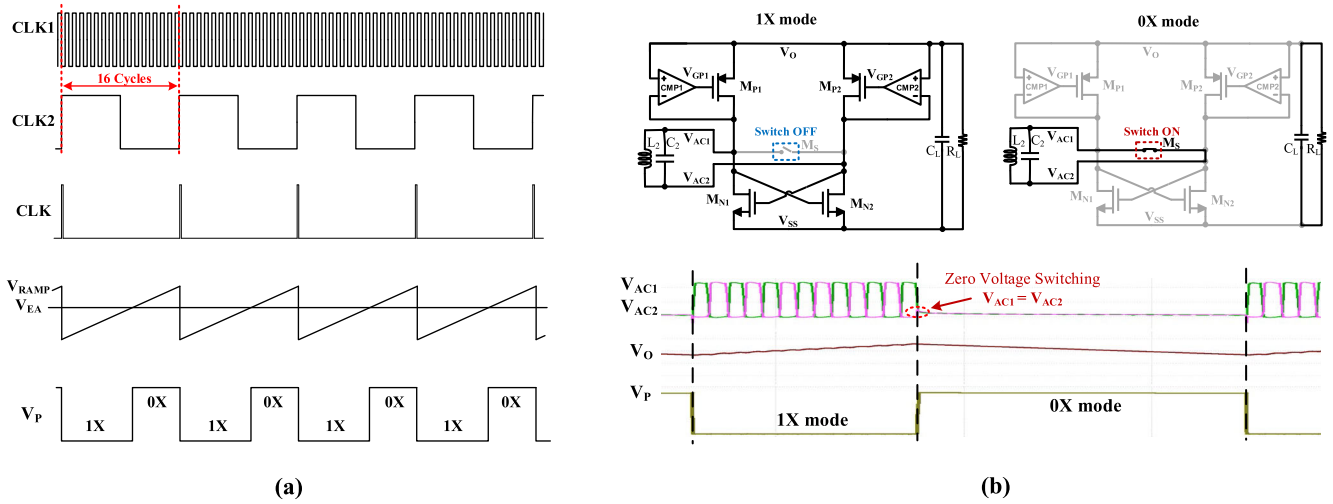

FIGURE 4. (a) The relationships of the regulating signals. (b) Equivalent structures and waveforms of the regulating rectifier in 1X/0X mode.

V_{RAMP} remains independent of the power supply due to the utilization of a supply independent bias current, as further illustrated later. When the sampled voltage V_{O_S} drops below (rises above) the reference voltage V_{REF}, the error voltage V_{EA} increases (decreases) and is compared to V_{RAMP}. This comparison leads to the generation of a corresponding PWM signal V_P, which is employed to regulate 0X and 1X modes. Fig.4(b) shows the equivalent structures and waveforms of 1X/0X mode. When V_P is low, the circuit is at 1X mode, switch M_S is turned off. It is a full wave bridge rectifier and the output voltage V_O will increase. When V_P is high, circuit is at 0X mode, switch M_S is turned on and the power transistors M_{P1}, M_{P2}, M_{N1}, and M_{N2} are turned off. C_L is discharged by R_L and V_O will decrease.

The duty cycle of 1X D_{1X} can be expressed as

$$D_{1X} = \frac{T_{1X}}{T_{1X} + T_{0X}} \tag{1}$$

where T_{1X} and T_{0X} are the duration of the 1X mode and 0X mode within one cycle of V_P. Under light load or high power input conditions, D_{1X} is small, resulting in less power being transferred to the load. However, D_{1X} becomes large under the heavy load or low power input conditions. This enables the stable output voltage across different loads or power input conditions.

Due to the presence of M_S, V_{AC1} and V_{AC2} will remain at a small value in 0X mode. It leads to the decrease in V_O and saves power consumption. However, the occurrence of shorting M_S may happen randomly at any phase in the switching cycle of V_P when the load changes. If M_S is shorted when there is a large voltage across the RX resonant capacitor C_2, the energy stored in C_2 will be dissipated, resulting in power loss. To mitigate this, a simple zero voltage switching (ZVS) circuit is employed. This circuit is implemented using a three-input NOR gate, as shown in Fig.3. The shorting of M_S happens only when V_{AC1} and V_{AC2} are at a low level and approximately the same which means the voltage across C_2 is approximately zero, as shown in Fig.4(b). It can reduce the energy loss on C_2 and improve PCE.

A constant ramp slope is desirable, as it is directly related to the system stability. The schematic of the supply independent voltage ramp generator is shown in Fig.5(a). The slope of ramp K_R can be given as follows

$$K_R = \frac{\Delta V_{RAMP}}{\Delta t} = \frac{I_B \cdot \Delta t / C_R}{\Delta t} = \frac{I_B}{C_R} \tag{2}$$

where V_{RAMP} is the output ramp voltage, C_R is the charging capacitor and I_B is the supply independent bias current. To achieve a stable bias current I_B, a negative feedback loop is introduced. The operational principle is as follows: as V_O increases, V_X also rises. Due to the common-source characteristics of transistor M_2, V_Y decreases, leading to a corresponding reduction at V_Z. Consequently, there is a decrease at V_X, ensuring its relative stability. The designed ramp signal in this article has a low frequency, indicating a small slope. Therefore, the bias current I_B can be set at the nanoampere (nA) level. It can lower power consumption. Transistors M_3 and M_4 operate in the sub-threshold region. Based on the expression for the drain-source current of a MOS transistor in the sub-threshold region, I_B is given as

$$I_B = \frac{\zeta V_T \ln K}{R_1} \tag{3}$$

where ζ is the sub-threshold slope factor, K is the ratio of sizes between M_3 and M_4. It can be observed from equation (3) that the bias current I_B is uniquely determined by R_1 and K. When V_O varies from 0.8V to 2.4V, the supply independent current source exhibits a variation of only 18 nA/V, whereas the peaking current source [16] shows a rate of change of 186 nA/V, as shown in Fig.5(b).

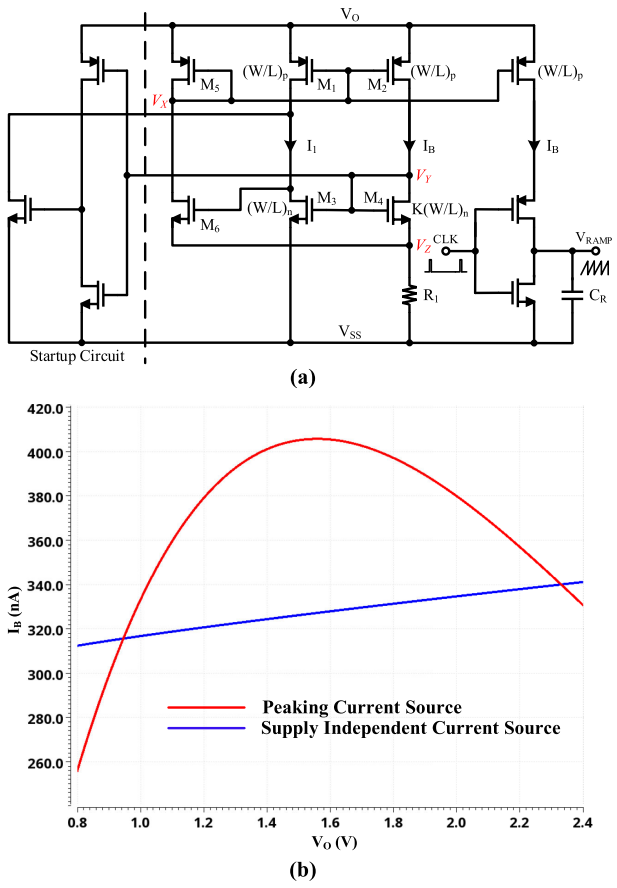

FIGURE 5. (a) The schematic of the supply independent voltage ramp generator. (b) The current variation of the peaking current source and the supply independent current source under different power supply voltages.

B. VOLTAGE MODE DELAY COMPENSATION LOOP

The voltage mode delay compensation loop includes sample circuit and push-pull comparator, as shown in Fig.3. The sample circuit for the half-side is shown in Fig.6. Consider the on-delay sample circuit as an example. V_O and V_{AC1} are level-shifted the same voltage to match the common-mode input voltage range of the error amplifier, labeled as V_{O_LS} and V_{AC1_LS}. They are then held by C_3 and C_4 at the falling edge of V_{GP1}, labeled as $V_{O\_S\_ON}$ and $V_{AC1\_S\_ON}$. Ideally, $V_{O\_S\_ON}$ and $V_{AC1\_S\_ON}$ should be equal. However, due to the presence of circuit delays, $V_{AC1\_S\_ON}$ will be larger than $V_{O\_S\_ON}$, resulting in an increase in the output of the error amplifier V_{C_ON}. It can introduce turn-on offset voltage V_{OS_ON} into push-pull comparator and let the comparator trip earlier. V_{OS_ON} will continue increasing until $V_{AC1\_S\_ON} \approx V_{O\_S\_ON}$, ultimately compensating for on-delays. The principle is similar to the off-delay sampling process. $V_{AC1}$and V_O are level-shifted by the level shifter and then sampled by C_1 and C_2. Initially, $V_{AC1\_S\_OFF}$ is smaller than $V_{O\_S\_OFF}$ due to the circuit delays and V_{C_OFF} increases. Then the increasing turn-off offset voltage V_{OS_OFF} is introduced to the comparator until $V_{AC1\_S\_OFF}$ equals $V_{O\_S\_OFF}$, thereby eliminating off-delays.

The concept of push-pull comparator with traditional voltage mode compensation is shown in Fig.7(a). The offset voltages $V_{OS\_ON/OFF}$ are directly injected into the input of comparator. By calibrating the control voltage $V_{C\_ON/OFF}$ of the transistors through the feedback loop, proper $V_{OS\_ON/OFF}$ can be introduced to remove the circuit delays. The switches SW_{ON} and SW_{OFF} are controlled by signals S_{ON} and S_{OFF}. S_{OFF} is derived from V_{GP1} in reverse. S_{ON} is generated by SR flip-flop and RC filter, as shown in Fig.7(b). During on-delay compensation process, S_{ON} remains high and S_{OFF} remains low, off-delay compensation is disabled. Similarly, during off- delay compensation process, S_{OFF} stays high and S_{ON} stays low, on-delay compensation is disabled. It ensures that off-delay compensation process will not be affected by on-delay compensation process. The push-pull comparator delay t_{cmp} can be given as [22]

$$t_{cmp} = \sqrt{\frac{C_{OUT}\,|VCR|}{\omega k_S \sqrt{2 I_B k_p \left(\frac{W}{L}\right)_{1-4}}}} \tag{4}$$

where C_{OUT} is the output capacitor of the comparator, $|VCR|$ is the value of voltage conversion ratio, ω is the angular resonant frequency, k_S is a scaling factor, I_B is the bias current, $k_p = \mu_p C_{ox}$. I_B and $(W/L)_{1-4}$ can be set to small values to reduce the power consumption and chip size. However, it will lead to an increase of circuit delays. Meanwhile, the circuit delays may become larger because of some no-ideal conditions (such as PVT and mismatch). The magnitude of V_{AC1} may be significant at the falling edge of V_{GP1} due to the large on-delays. This may potentially result in the sampled voltage $V_{AC1\_S\_ON}$ exceeding common-mode input voltage range ($V_{in,CM}$) of the error amplifier and V_{C_ON} will be as large as V_O. It will introduce a large V_{OS_ON}, causing the comparator to function unproperly because the transistors will not operate in the saturation region, ultimately resulting in the failure of on-delay compensation. This will significantly reduce the VCR. Fortunately, V_{AC1} does not drop significantly at the rising edge of V_{GP1} because it is clamped by the output voltage V_O. Therefore, $V_{AC1\_S\_OFF}$ is in the range of $V_{in,CM}$ and V_{C_OFF} stays at an appropriate value between V_O and V_{SS}, as shown in Fig.8(a). Off-delays can be effectively compensated. To compensate for on-delays reliably, we propose an improved VM compensation approach, as illustrated in Fig.7(c). The MOS transistors M_6, M_7, M_9, M_{10}, $M_{12}$and M_{13}operating in the linear region function as variable resistors, with their resistance directly proportional to the gate voltage $V_{C\_ON/OFF}$. When $V_{C\_ON/OFF}$ increases, the offset voltage also experiences an increasement. V_{C_OFF} is reused in the process of on-delay compensation. It controls transistors M_9 and M_{10} operating in parallel with transistors M_6 and M_7 controlled by V_{C_ON}. On-delay compensation process can be divided into three steps, as shown in Fig.8:

Step I: Owing to the large magnitude of V_{AC1} at the falling edge of V_{GP1}, the sampled voltage $V_{AC1\_S\_ON}$ exceeds the range of $V_{in,CM}$, thus causing V_{C_ON} to be as high as V_O.

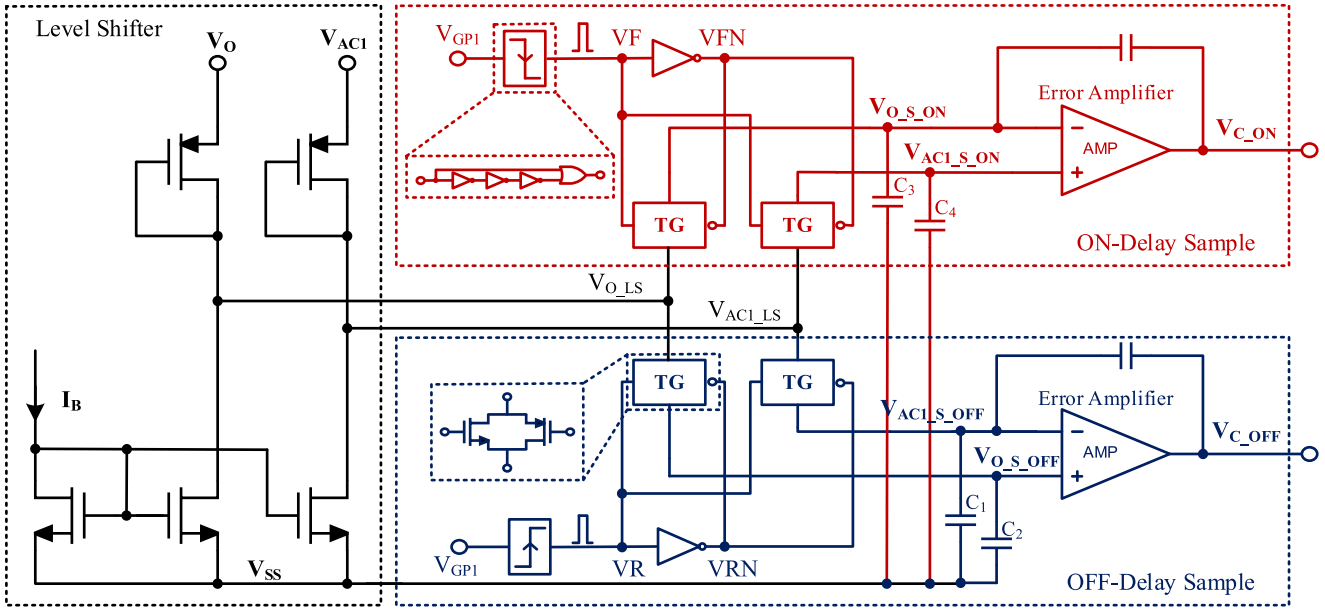

FIGURE 6. The half-side structure of the delay sample circuit.

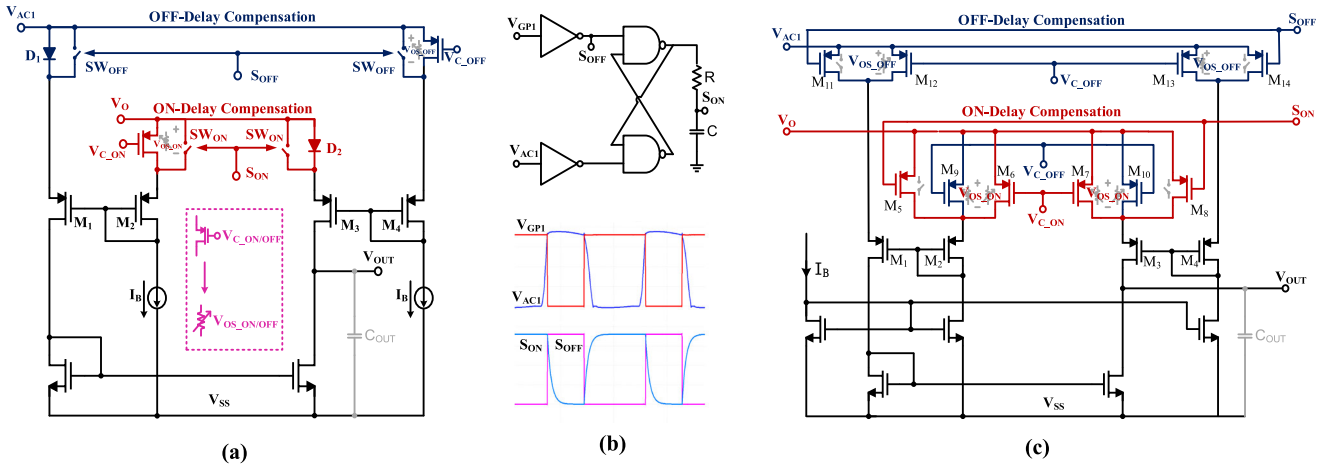

FIGURE 7. (a) Push-pull comparator with traditional voltage mode compensation. (b) The schematic and waveforms of half-side logic control circuit. (c) Push-pull comparator with improved voltage mode compensation.

M_6 and M_7 are closed and the on-delay compensation loop is inactive. Off-delay control signal V_{C_OFF} will provide coarse compensation for on-delay.

Step II: As V_{C_OFF} continues increasing, turn-on will be tripped prematurely. $V_{AC1\_S\_ON}$ is smaller than $V_{O\_S\_ON}$ and V_{C_ON} decreases. $V_{AC1\_S\_ON}$ enters the error amplifier's normal input common-mode range. On-delay compensation loop starts to function normally. V_{C_ON} provides fine compensation for on-delays.

Step III: Both on- and off-delays are well compensated.

By adopting this structure, effective compensation for circuit delays and high VCR has been achieved even in the presence of large pulse of V_{AC} due to the large circuit delays.

C. SELF-START-UP CIRCUIT

Fig.9(a) shows the self-start-up circuit of the rectifier. The resistors R_{S1} and R_{S2} are large to minimize the power dissipation in the circuit. Initially, V_{STU} is low. The gates of power transistors M_{P1} and M_{P2} are connected to V_O, causing the transistors to function as passive diodes. V_{STU} remains low until V_O reaches 1.35V, which is the sum of the threshold voltages of M_{SN1} and M_{SN2} in diode-connected configuration.

Then, V_{STU} becomes high, and the circuit will operate in active mode, as shown in Fig.9(b). A D flip-flop is employed to avoid potential multi-startup issues when the rectifier just becomes active mode.

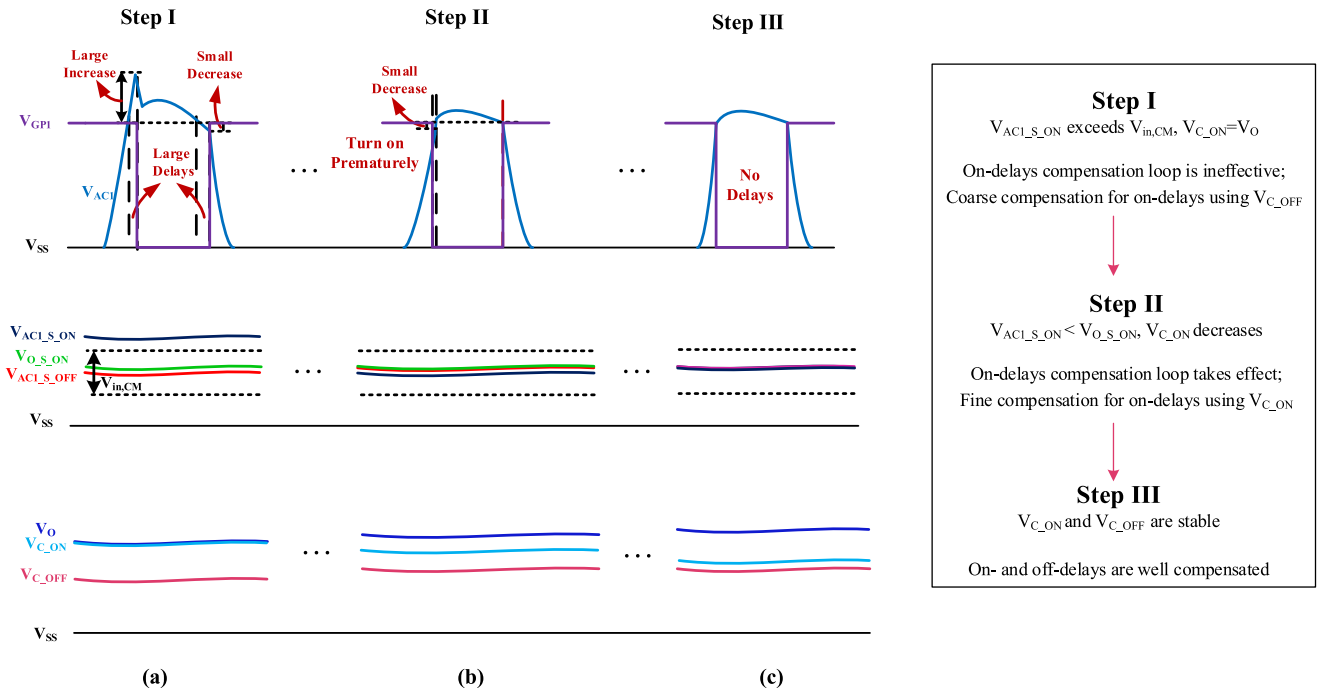

FIGURE 8. The (a)Step I, (b)step II and (c)step III of delay compensation using proposed push-pull comparator.

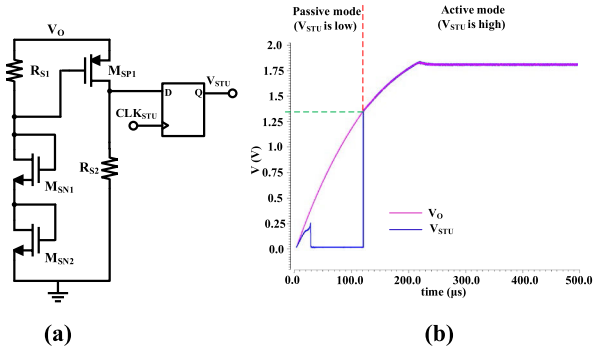

FIGURE 9. The (a) schematic and (b) waveform of self-start-up circuit.

III. SIMULATION RESULTS

The designed single-stage regulating rectifier is simulated using 0.18μm CMOS process. The layout of the chip, illustrated in Fig.10, occupies a small area of 0.91 mm^2. Fig.11 shows the simulation testbench. We performed post-layout simulations based on the platform of Cadence Virtuoso. On TX side, a series-resonant L_1C_1 tank is employed, and it is driven by a sinusoid voltage V_S with a frequency of 6.78 MHz in the ISM band. The RX side adopts a parallel-resonant L_2C_2 circuit because power transmission is in the milliwatt range. R_{P1}, R_{P2}, R_{P3}, L_{P1}, and L_{P2} are the simulated parasitic parameters of resonant modules. The coupling coefficient k can be defined as:

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{5}$$

where M is the mutual inductance, influenced by the relative distance and orientation of the resonant coils [23].

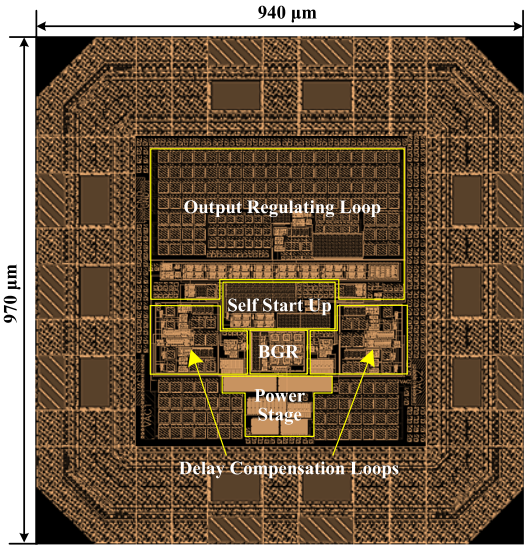

FIGURE 10. Layout of the proposed single-stage regulating rectifier.

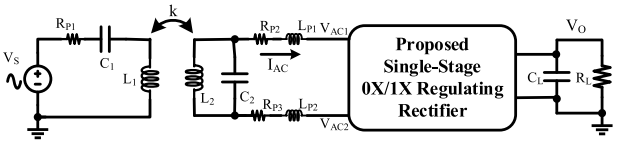

FIGURE 11. Simulated testbench.

In wireless power transfer for implanted devices, k typically ranges between 0.1 and 0.2 for loosely coupled coils. Normally, we set k as 0.2 for simulation. The load capacitor C_L is 1uF, and the load resistor R_L ranges from 50Ω to 500Ω.

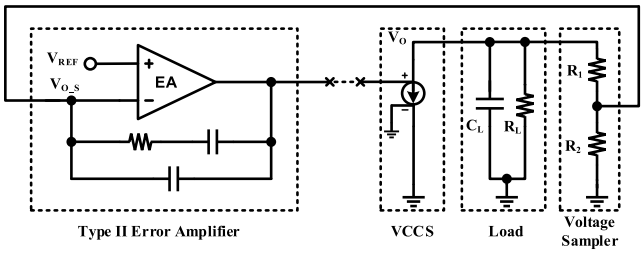

FIGURE 12. The equivalent small-signal model for stability analysis.

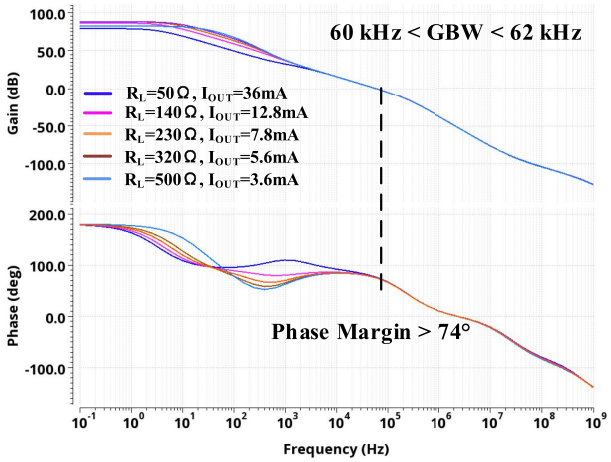

FIGURE 13. Bode plot of PWM loop under different loads.

A. STABILITY SIMULATION

To analyze the stability of the PWM loop, a simple small-signal model is depicted in Fig.12. The PWM controller utilizes an operational transconductance amplifier (OTA) as the error amplifier, incorporating type-II compensation to ensure the stability of the loop. The other components of the loop can be simplified to a voltage-controlled current source (VCCS) [24]. The bode plots of the loop under different loads from 50Ω to 500Ω are shown in Fig.13. The system achieves a large dc loop gain exceeding 80dB, along with a phase margin surpassing 74°. The loop bandwidth, approximately 60kHz, constitutes about 1/7 of the switching frequency (423 kHz). It ensures reliable stability for the system.

B. SYSTEM-LEVEL TRANSIENT SIMULATION RESULTS

Fig.14(a) depicts the waveforms of the proposed single-stage 0X/1X regulating rectifier with PWM-based control loop. During 0X mode, V_P is high. The received voltage V_{AC1} across the secondary resonant tank is shorted and remains at a small value. V_O decreases and the output load draws energy from C_L. During 1X mode, the circuit is in full-bridge rectification mode and V_O increases. In heavy load conditions, D_{1X} is large, the load will receive more power. In light load conditions, D_{1X} is small, and the output receives less power. The output voltage V_O can be regulated to 1.8V by adjusting D_{1X} based on the load conditions through feedback loop. When the load changes from heavy to light, the circuit demonstrates a transient response time of 14 μs, meaning that the circuit possesses a favorable transient response speed. Fig.14(b) shows the system response to changes in coil coupling. When k decreases from 0.2 to 0.1, the RX side will receive less energy, causing D_{1X} to increase in order to maintain a stable output voltage. Conversely, when k increases from 0.1 to 0.15, the RX side will receive more energy, causing D_{1X} to decrease to stabilize the output. It demonstrates that the output voltage can remain stable despite changes in the input.

Fig.15 represents the process of delay compensation with proposed VM compensation method. During step I, V_{AC1} has a large increase at the falling edge of V_{GP1} due to the large on-delays. V_{C_ON} remains high, resulting in failure of on-delay compensation loops. On-delays are coarsely compensated using V_{C_OFF}. During step II, V_{C_ON} decreases and on-delay compensation loops come into play. Fine compensation for on-delays has been achieved. During step III, both on- and off-delays are effectively compensated.

To verify the capability and robustness of proposed VM delay compensation method under various non-ideal conditions in silicon implementation, we performed PVT corners and Monte-Carlo mismatch simulations, as shown in Fig.16. In Fig.16(a), near-optimum On/Off delay compensation is guaranteed across different PVT corners. High PCE and VCR are achieved with minor variations. Fig.16(b) shows that the system's PCE is insensitive to mismatches under light and heavy loads. Therefore, the circuit delays of the proposed single-stage rectifier can always well-compensated under various PVT corners and mismatches, ensuring the feasibility and reliability of our idea. Here, the PCE of the rectifier is defined as

$$PCE = \frac{\frac{V_O^2}{R_L}}{\frac{1}{nT}\int_{t_0}^{t_0+nT} V_{AC}(t) I_{AC}(t) dt} \tag{6}$$

where T is the period of the V_{AC} and n is the count of V_{AC} cycles. The expression of VCR is defined as

$$VCR = \frac{V_O}{|V_{AC1} - V_{AC2}|} \tag{7}$$

where $|V_{AC1}$-$V_{AC2}|$ is the amplitude of the secondary side input voltage under 1X mode, V_O is the output DC voltage of the receiver [25].

C. POWER LOSS ANALYSIS

The frequency of switching 0X/1X mode is set to 1/16 of the resonant frequency. This can reduce the impact of switching loss on system efficiency, thereby improving PCE, especially under light load conditions. Fig.17(a) shows the power consumption breakdown of the system under different loads. Power stage always accounts for

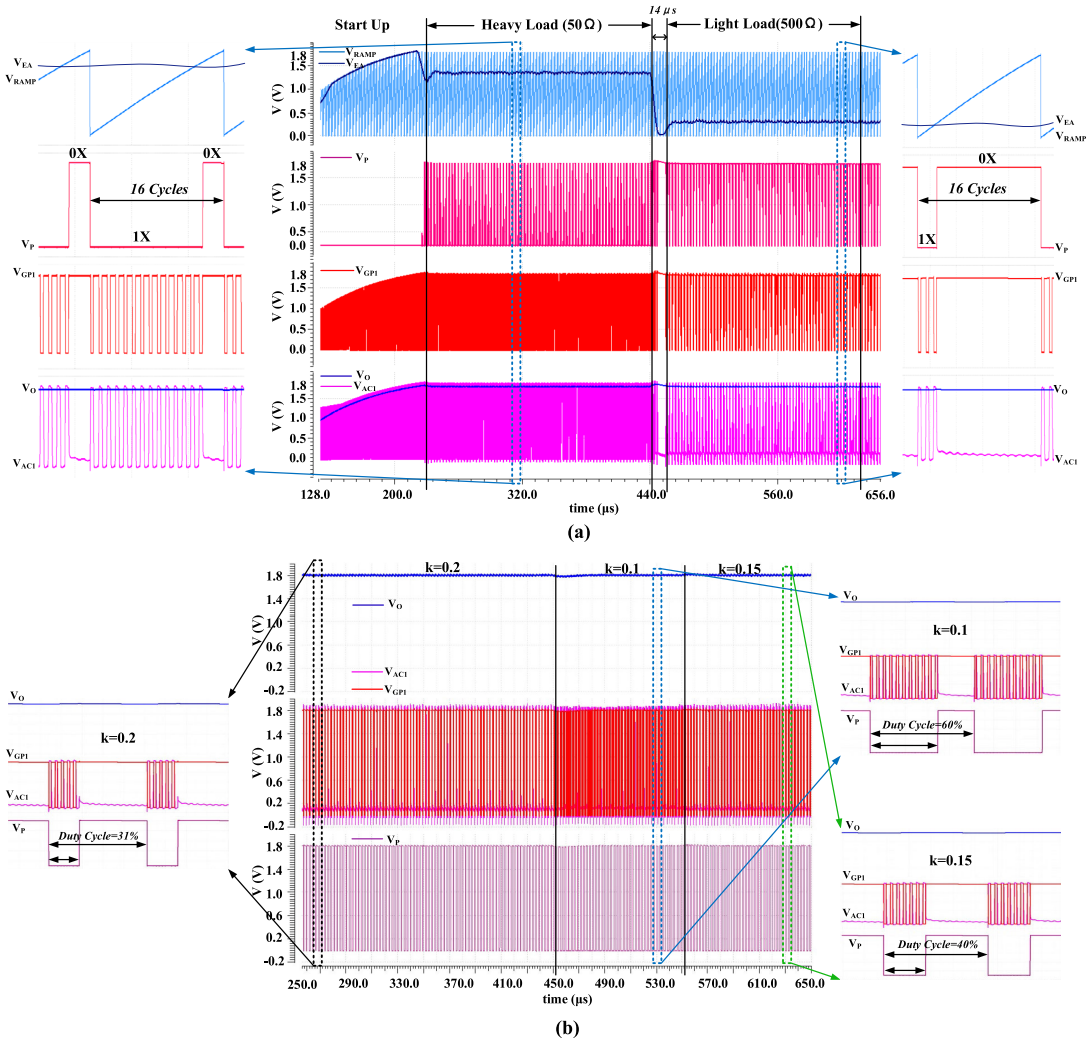

FIGURE 14. The waveforms of the proposed single-stage 0X/1X regulating rectifier with PWM-based control loop under (a) different loads (V_S = 4V, k = 0.2) and (b) variable k (V_S = 4V, R_L = 300Ω).

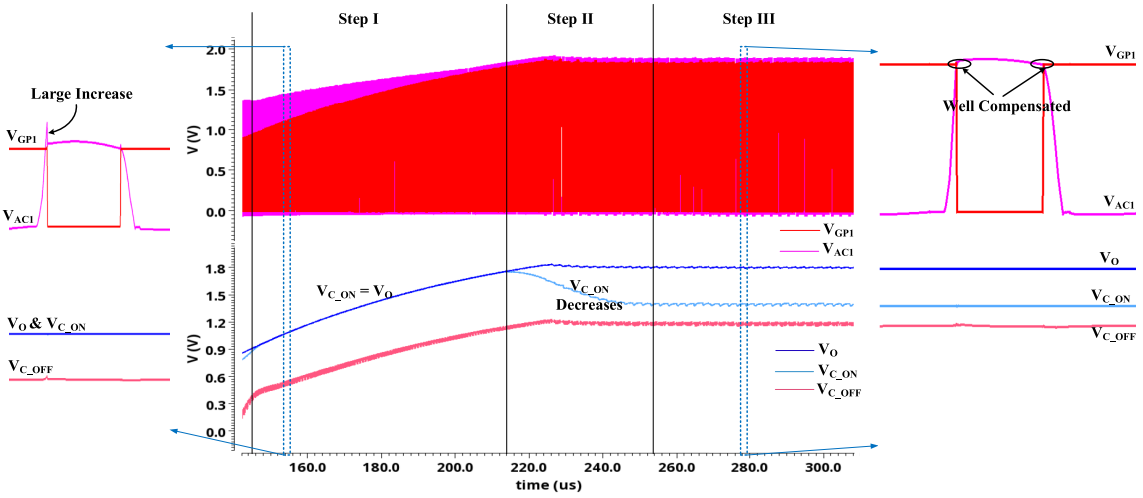

FIGURE 15. The process of delay compensation with proposed voltage mode compensation method.

the major consumption. The delay compensation loops and output regulation loop account for only 2.98% in heavy load and 7.18% in light load. Fig.17(b) shows the PCE of the rectifier under different D_{1X}. The efficiency of the

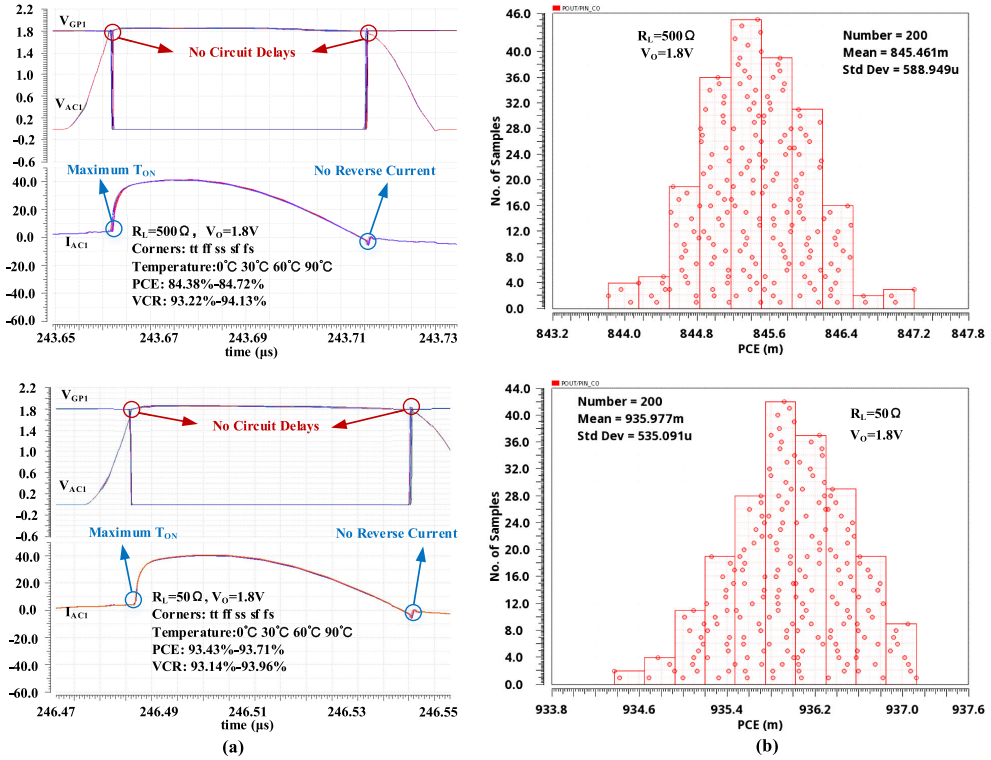

FIGURE 16. Simulation with (a) different PVT corners and (b) Monte-Carlo mismatches.

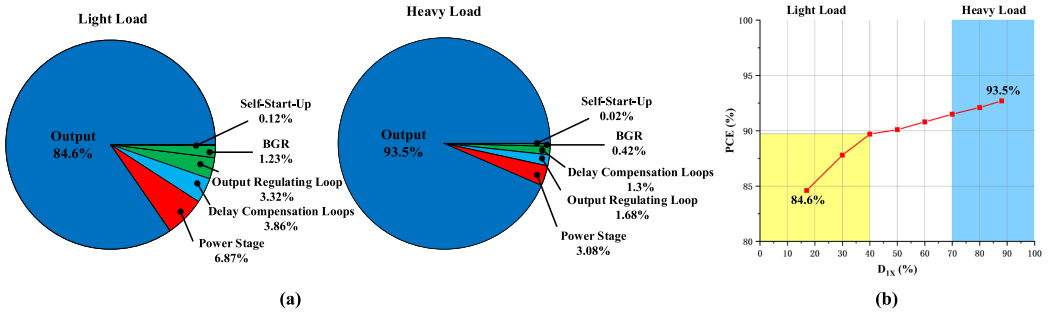

FIGURE 17. (a) Power consumption breakdown under different loads. (b) The PCE under different D_{1X}.

TABLE 1. Comparison with previous works.

	JSSC [26]	JSSC [11]	JSSC [12]	JSSC [14]	This work
Process	CMOS 0.35 μm	CMOS 0.35 μm	CMOS 0.35 μm	CMOS 0.25 μm	CMOS 0.18 μm
Frequency	2 MHz	6.78 MHz	13.56 MHz	6.78 MHz	6.78 MHz
Output Regulating Structure	LDO	Local 1X/½X/0X Mode PWM Control	Local 1X/2X Mode PWM Control+Global Control	0X/1X Mode Hysteresis Control+Global Control	Local 0X/1X Mode Fre-divided PWM Control
Number of Active Diodes	0	4	3	2	2
Delay Compensation Mode	N/A	N/A	Current Mode	Current Mode	Improved Voltage Mode
V_O	3 V	5 V	3.6 V	5 V	1.8 V
Maximum Output Power	1.45 W	6W	102 mW	400 mW	64.8 mW
Receiver Chip Area	4.8 mm^2	4.77 mm^2	3.06 mm^2	2.07 mm^2	0.91 mm^2
Off-chip Components	3 capacitors	1 capacitor	1 capacitor	1 capacitor	1 capacitor
PCE	76%**	81%-92.2% (P_{OUT}:0.5W-5W)	76%-92.6% (P_{OUT}:10mW-60mW)	72%-92.9% (P_{OUT}:5mW-400mW)	84.6%-93.5%* (P_{OUT}:6.5mW-65mW, V_S=4V)
Transient Response	N/A	16 μs (P_{OUT}:0.5W-5W)	130 μs (P_{OUT}:10mW→60mW)	820 μs (P_{OUT}:100mW→600mW)	14 μs* (P_{OUT}:6.5mW→65mW, V_S=4V)

* Simulation results ** For maximum P_{OUT}

circuit remains above 84.6%, with a peak efficiency of 93.5%. Table 1 summarizes and compares the performance of the proposed single-stage rectifier with previous regulating rectifiers.

IV. CONCLUSION

This paper presents a 6.78MHz single-stage 0X/1X regulating rectifier applying to wirelessly powered IMDs. By using the proposed improved VM delay compensation method, on- and off-delays can be well-compensated even though the circuit delays are large. Additionally, by setting the 0X/1X switching frequency to 1/16 of resonant frequency, the high PCE under light load and system stability have been achieved. This rectifier was designed in 0.18μm CMOS process and can regulate a 1.8V output voltage. Simulation results indicate that the proposed rectifier operates effectively with fast transient response of 14 μs. It occupies a small chip area of 0.91 mm^2. The high PCE of 84.6%-93.5% is achieved across the output power range from 6.5mW to 65mW. The high VCR of above 93% is achieved under the large circuit delays.

REFERENCES

[1] C.-G. Kim, D.-H. Seo, J.-S. You, J.-H. Park, and B. H. Cho, "Design of a contactless battery charger for cellular phone," *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1238–1247, Dec. 2001.

[2] J. Rahulkumar, R. Narayanamoorthi, C. Balaji, and A. Savio, "A dual receiver and inherent CC-CV operated WRIPT EV charging system with high misalignment tolerance couplers," in *Proc. IEEE Int. Transp. Electrific. Conf. (ITEC-India)*, Dec. 2023, pp. 1–8.

[3] M. W. Baker and R. Sarpeshkar, "Feedback analysis and design of RF power links for low-power bionic systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 28–38, Mar. 2007.

[4] S. B. Lee, H.-M. Lee, M. Kiani, U.-M. Jow, and M. Ghovanloo, "An inductively powered scalable 32-channel wireless neural recording system-on-a-chip for neuroscience applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 360–371, Dec. 2010.

[5] J. Moore, S. Castellanos, S. Xu, B. Wood, H. Ren, and Z. T. H. Tse, "Applications of wireless power transfer in medicine: State-of-the-art reviews," *Ann. Biomed. Eng.*, vol. 47, no. 1, pp. 22–38, Jan. 2019.

[6] C.-Y. Wu, X.-H. Qian, M.-S. Cheng, Y.-A. Liang, and W.-M. Chen, "A 13.56 MHz 40 mW CMOS high-efficiency inductive link power supply utilizing on-chip delay-compensated voltage doubler rectifier and multiple LDOs for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2397–2407, Nov. 2014.

[7] H.-M. Lee and M. Ghovanloo, "An adaptive reconfigurable active voltage doubler/rectifier for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 8, pp. 481–485, Aug. 2012.

[8] H.-G. Park, J.-H. Jang, H.-J. Kim, Y.-J. Park, S. Oh, Y. Pu, K. C. Hwang, Y. Yang, and K.-Y. Lee, "A design of a wireless power receiving unit with a high-efficiency 6.78-MHz active rectifier using shared DLLs for magnetic-resonant A4 WP applications," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4484–4498, Jun. 2016.

[9] P. S. Riehl, A. Satyamoorthy, H. Akram, Y.-C. Yen, J.-C. Yang, B. Juan, C.-M. Lee, F.-C. Lin, V. Muratov, W. Plumb, and P. F. Tustin, "Wireless power systems for mobile devices supporting inductive and resonant operating modes," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 780–790, Mar. 2015.

[10] J. Rahulkumar and R. Narayanamoorthi, "Power control and efficiency enhancement topology for dual receiver wireless power transfer EV quasi-dynamic charging," in *Proc. IEEE Int. Transp. Electrific. Conf. (ITEC-India)*, Dec. 2023, pp. 1–6.

[11] L. Cheng, W.-H. Ki, and C.-Y. Tsui, "A 6.78-MHz single-stage wireless power receiver using a 3-mode reconfigurable resonant regulating rectifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1412–1423, May 2017.

[12] X. Li, C.-Y. Tsui, and W.-H. Ki, "A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.

[13] X. Li, X. Meng, C.-Y. Tsui, and W.-H. Ki, "Reconfigurable resonant regulating rectifier with primary equalization for extended Coupling- and loading-range in bio-implant wireless power transfer," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 6, pp. 875–884, Dec. 2015.

[14] F.-B. Yang, J. Fuh, Y.-H. Li, M. Takamiya, and P.-H. Chen, "Structure-reconfigurable power amplifier (SR-PA) and 0X/1X regulating rectifier for adaptive power control in wireless power transfer system," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2054–2064, Jul. 2021.

[15] J. Fuh, F.-B. Yang, and P.-H. Chen, "A 69.3% efficiency, 6.78-MHz wireless power delivery system with 0X/1X regulating rectifier and reconfigurable power amplifier," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 37–38.

[16] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS active rectifier with switched-offset and compensated biasing for biomedical wireless power transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 334–344, Jun. 2014.

[17] C. Huang, T. Kawajiri, and H. Ishikuro, "A near-optimum 13.56 MHz CMOS active rectifier with circuit-delay real-time calibrations for high-current biomedical implants," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1797–1809, Aug. 2016.

[18] L. Cheng, W.-H. Ki, Y. Lu, and T.-S. Yim, "Adaptive on/off delay-compensated active rectifiers for wireless power transfer systems," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 712–723, Mar. 2016.

[19] Y. Ma, K. Cui, Z. Ye, Y. Sun, and X. Fan, "A 13.56-MHz active rectifier with SAR-assisted coarse-fine adaptive digital delay compensation for biomedical implantable devices," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 122–125, 2020.

[20] K. Noh, J. Amanor-Boadu, M. Zhang, and E. Sánchez-Sinencio, "A 13.56-MHz CMOS active rectifier with a voltage mode switched-offset comparator for implantable medical devices," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2050–2060, Oct. 2018.

[21] Y. Ma, K. Cui, Y. Sun, Z. Chen, and X. Fan, "A hybrid adaptive digital delay compensated active rectifier with PWM-based technique and resistor-array tuning for wireless power transmission," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11423–11435, Sep. 2022.

[22] L. Cheng, X. Ge, L. Hu, Y. Yao, W.-H. Ki, and C.-Y. Tsui, "A 40.68-MHz active rectifier with hybrid adaptive on/off delay-compensation scheme for biomedical implantable devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 2, pp. 516–525, Feb. 2020.

[23] U.-M. Jow and M. Ghovanloo, "Design and optimization of printed spiral coils for efficient transcutaneous inductive power transmission," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 193–202, Sep. 2007.

[24] R. Erfani, F. Marefat, and P. Mohseni, "A dual-output single-stage regulating rectifier with PWM and dual-mode PFM control for wireless powering of biomedical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1195–1206, Nov. 2020.

[25] Q. W. Low, M. Zhou, and L. Siek, "A single-stage direct-conversion AC–DC converter for inductively powered application," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 892–902, May 2018.

[26] M. Kiani, B. Lee, P. Yeon, and M. Ghovanloo, "A Q-modulation technique for efficient inductive power transmission," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2839–2848, Dec. 2015.

SILONG CHEN (Student Member, IEEE) received the B.S. degree from Jiangnan University (JNU), Jiangsu, China, in 2022. He is currently pursuing the master's degree with the Center of EDA, Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), Beijing.

GUANGYIN SHI received the B.S. degree from the School of Electronic and Information Engineering, Tiangong University, Tianjin, China, in 2019. He is currently pursuing the Ph.D. degree with the Center of EDA, Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), Beijing.

XIN LIU received the B.S. and Ph.D. degrees in circuits and systems from Jilin University, China, in 2004 and 2009, respectively. From 2009 to 2011, she was with the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS) for postdoctoral research. From 2011 to 2017, she was an Assistant Professor with IMECAS. Since 2018, she has been an Associate Professor with IMECAS. Her current research interests include wireless power transfer systems, RF energy harvesting, and power management ICs.

XINGCHEN XU received the B.S. degree from Hefei University of Technology, Hefei, China, in 2020. She is currently pursuing the Ph.D. degree with the Center of EDA, Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), Beijing.

BIN WANG received the B.S. degree from Shandong Normal University, Shandong, China, in 2015, and the Information Engineering degree from Hebei University, Hebei, China, in 2018. He is currently pursuing the Ph.D. degree with the Center of EDA, Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), Beijing.

ZHIQIANG LI (Member, IEEE) received the B.S. degree in microelectronics from Jilin University, Changchun, China, in 2004, and the Ph.D. degree in microelectronics from the University of Chinese Academy of Sciences, Beijing, China, in 2009. From 2015 to 2016, he was a Visiting Professor of electrical and computer engineering with the University of California at Santa Barbara, Santa Barbara, CA, USA. He is currently a Professor with the Institute of Microelectronics of the Chinese Academy of Sciences, Beijing. His current research interests include semiconductor device and process simulation electronic design automation (EDA) tools and radio frequency integrated circuits design.