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RESEARCH ARTICLE

Variable Window Size Moving Average Filter for Phase-Locked-Loop Synchronization

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ABSTRACT Efficient grid synchronization is crucial for integrating renewable energy sources and Flexible AC Transmission systems (FACTs) into power grids. This paper addresses the challenges faced by Synchronous Reference Frame Phase-Locked Loops (SRF-PLLs) in harmonic-polluted grids and proposes a novel solution employing Moving Average Filters (MAFs). The conventional MAF-PLL with a fundamental period window size provides harmonic rejection but slows down the dynamic response. To enhance MAF-PLL performance under harmonic-polluted grid conditions, we introduce a Variable Window Size (VWS) MAF. The proposed VWS-MAF adapts its window size based on the dominant frequency of oscillation in the dq frame, determined using Short-Time Fourier Transform (STFT). The proposed method ensures minimum window size, based on grid conditions, which improves the dynamic response while maintaining harmonic rejection capabilities. The proposed method offers improved adaptability and promising performance in elimination of integer harmonics, DC offset, interharmonics, and negative sequence component. Simulation and experimental studies are presented that demonstrate the effectiveness of VWS-MAF, positioning it as a noteworthy advancement in PLL technology for robust grid synchronization.

INDEX TERMS Grid synchronization, harmonic rejection, moving average filters (MAFs), phase-locked loops (PLLs), short-time Fourier transform (STFT), variable window size (VWS).

ABBREVIATIONS

The following is a list of abbreviations used in this paper.

DFT	Discrete Fourier Transform.
FACT	Flexible AC Transmission system.
FFT	Fast Fourier Transform.
LF	Loop Filter.
MAF	Moving Average Filter.
PI	Proportional-Integral.
PID	Proportional-Integral-Derivative.
PD	Phase Detector.
PLL	Phase-Locked Loop.
RTC	Real-Time Controller.
SFT	Sliding Fourier Transform.
SRF	Synchronous Reference Frame.
STFT	Short-Time Fourier Transform.
VCO	Voltage-Controlled Oscillator.
VSC	Voltage-Source Converter.
VWS	Variable Window Size.

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I. INTRODUCTION

Grid synchronization is pivotal for integrating renewable energy sources and Flexible AC Transmission systems (FACTs) into power grids [1], [2]. It ensures stable and efficient integration by precisely matching the phase, frequency, and amplitude of generated power with the grid [3], [4], [5], [6], [7]. Phase-Locked Loops (PLLs) emerge as a vital method for synchronization, employing three essential components: Phase Detector (PD), Loop Filter (LF), and Voltage-Controlled Oscillator (VCO) [6], [8], [9]. PLLs play a crucial role in accurately synchronizing renewable energy sources and FACTs with the grid, enabling their seamless operation and optimal power transfer [10], [11], [12].

Phase-Locked Loops (PLLs) operate by using a PD to generate an error signal proportional to the phase difference between input and VCO output. This error signal is then filtered by an LF, often a Proportional-Integral (PI) controller, controlling the VCO to produce a sinusoidal signal aligning with the input and minimizing phase error [13]. Synchronous Reference Frame Phase-Locked Loops (SRF-PLLs), shown in Figure 1, serve as effective mechanisms for transforming grid voltages into reference frames, employing PI or PID controllers to accurately estimate phase angles and frequencies in balanced, harmonics-free grid conditions [14], [15]. However, their performance falters in harmonic-polluted grids, manifesting distortion when faced with unbalanced voltages, harmonics, or DC offset [16], [17]. These limitations restrict the PLL's capability to reject disturbances such as DC offsets, harmonics, interharmonics, and imbalances prevalent in polluted grid environments. Despite their widespread use and simplicity, the need for further refinement of SRF-PLL persists to ensure robust and accurate synchronization, particularly in adverse grid conditions [18], [19]. To improve the performance of SRF-PLL under non-ideal grid conditions, different pre-loop and in-loop filters have been incorporated [20].

The utilization of Moving Average Filters (MAFs) within PLL structures has garnered significant attention in recent literature, particularly in the context of grid-connected applications [2], [4], [8], [17], [21], [22]. MAFs are linear-phase finite-impulse-response filters that exhibit effective blocking of harmonics under specific conditions. Several PLL schemes, including the SRF-PLL with integrated MAF, have been proposed to enhance harmonic filtering capabilities [8], [9], [19]. However, the incorporation of MAFs introduces a notable trade-off by significantly slowing down the dynamic response due to the induced phase delay [19], [22], [23]. Despite their ability to eliminate unwanted harmonics, DC offset, and unbalanced voltages, MAF-PLLs face challenges related to open-loop bandwidth reduction, impacting overall dynamic performance [24]. Various studies explored methods to mitigate these issues and improve the dynamic behavior of MAF-based PLLs while maintaining their harmonic-filtering advantages [5], [8], [9], [11], [12], [16], [19], [23], [24], [25], [26].

The window size (T_w) of MAF plays a crucial role in determining the dynamic performance and filtering capability of PLLs [12], [24]. A larger T_w results in slower detection dynamics, and the MAF introduces a delay equal to its window width [27]. The choice of T_w is essential for balancing response speed and filtering effectiveness. For instance, a larger T_w eliminates certain harmonics but slows down the PLL's response, while a smaller T_w improves dynamic response but may not filter all harmonics effectively [19]. Some approaches suggest adapting T_w to the lowest order harmonic, and for unknown harmonic content, selecting T_w equal to the fundamental period is recommended [14], [22]. The MAF's delay and response time become critical factors, impacting PLL performance, and careful consideration of

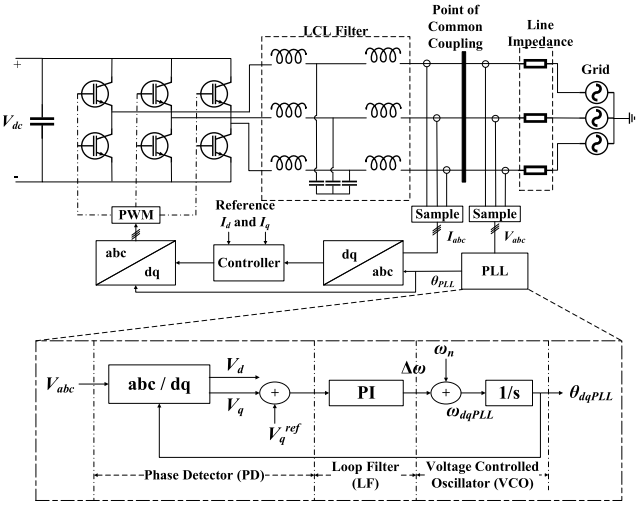

FIGURE 1. SRF-PLL setup for a grid-tied Voltage-Source Converter (VSC).

T_w is essential for optimal trade-offs between filtering and dynamic response. Many filtering improvements have been proposed to improve the dynamic performance of MAF and reduce its window size while maintaining its harmonic rejection advantages [7], [9], [12], [16], [19], [20], [24], [26], [28], [29], [30], [31].

Moreover, the static nature of conventional MAFs and lack of frequency adaptability, leads to suboptimal performance during significant frequency deviations [23], [27]. To address this limitation, researchers have proposed frequency-adaptive MAF-based PLLs [9], [30].

These adaptive schemes dynamically adjust the MAF window size based on the grid frequency, ensuring improved performance under varying conditions [1], [4], [7], [19], [23]. The adaptive MAFs show promising results in harmonics elimination, noise reduction, and negative sequence component cancellation. While the adaptive approaches offer benefits, challenges like discrete sampling errors and trade-offs between dynamic response and steady-state accuracy persist [3]. Recent developments focus on refining adaptive mechanisms and addressing the impact of frequency drift and harmonics in distorted grid environments, showcasing advancements in PLL technology for better grid synchronization [9], [25], [32], [33].

The contribution of present work is as follows. We propose a Variable Window Size (VWS) for the PLL's MAF based on the dominant frequency of the oscillation in the *dq* frame using Short-Time Fourier transform (STFT). The dominant frequency of oscillation determines the harmonic content of the voltage, based on which the window size of MAF is changed in real time. This method can be utilized in any PLL structure using *dq*-based MAF to shorten the MAF's window size during DC offset or harmonics. The dominant frequency of the oscillation changes, based on the type of harmonic observed in the grid. The window size is therefore altered adaptively to remove the harmonics based on the grid condition. Since the calculated window size is not always an

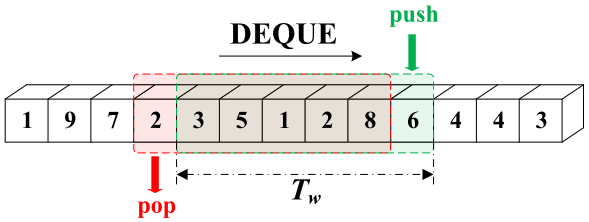

FIGURE 2. Moving window of an MAF.

integer multiple of the time step, interpolation is used to count for the sampling error. To improve the harmonic rejection capability of the MAF, discretization is done based on the trapezoidal rule instead of backward Euler integration [25], [34]. Using the method proposed in this paper, the window size of MAF is minimized while maintaining PLL's harmonic rejection capabilities.

The rest of this paper is organized as follows: In Section II, the formulations for MAF and MAF-PLL are presented along with a discussion of the impact of MAF's window size on its delay and harmonic rejection characteristics. The VWS-MAF is proposed in Section III and its functionality is demonstrated using simulation scenarios. In Section IV, several simulation and experimental scenarios are presented to verify the performance of proposed synchronization method. Conclusions are presented in section V.

II. MOVING AVERAGE FILTER (MAF)

MAF is a low-pass finite-impulse-response filter which, despite its simplicity, is optimal for reducing random noise while retaining a sharp step response [35]. As shown in Figure 2, in MAF, a window of specified length, T_w, moves over the data, sample by sample, and the average is computed over the data in the window.

The expression of MAF in continuous time-domain is given by

$$\langle x(t)\rangle = \frac{1}{T_w}\int_{t-T_w}^{t} x(\tau)d\tau \tag{1}$$

Thus, the transfer function of MAF in the s-domain is given by

$$G_{MAF}(s) = \frac{1-e^{-sT_w}}{sT_w} \tag{2}$$

Hence, the magnitude and phase characteristics of MAF are given by [3]

$$|G_{MAF}(j\omega)| = \frac{2\left|\sin\left(\frac{\omega T_w}{2}\right)\right|}{\omega T_w} \tag{3}$$

$$\angle G_{MAF}(j\omega) = -\frac{\omega T_w}{2} \tag{4}$$

From (3), it is concluded that the MAF is zero whenever the following condition is satisfied [27]

$$\frac{T_w}{T} = k \text{ for } k = 1, 2, 3, \ldots \tag{5}$$

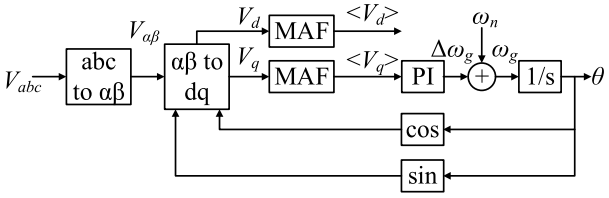

FIGURE 3. Block diagram of MAF-PLL.

TABLE 1. *ABC-DQ* harmonic transformation.

***abc* harmonics**	1^+	1^-	$(6k+1)^+$	$(6k-1)^-$
***dq* harmonics**	DC	2^-	$(6k)^+$	$(6k)^-$

MAF completely eliminates any oscillation that is a multiple of the frequency for which it is designed [27]. The application of the MAF is widespread in enhancing the disturbance rejection capacity of PLLs. This is crucial for the stable operation and grid integration of power electronic converters within electric power systems. The MAF method stands out as the most favored and widely adopted approach due to its straightforward digital implementation, minimal computational complexity, and efficiency in addressing grid disturbances [2].

A. MAF-PLL

Schematic diagram of MAF-PLL is provided in Figure 3 [19], [22].

After performing the Park transformation [36], [37], the *abc* frame variables are changed into the *dq* frame as follows:

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\hat{\omega}t) & \sin\left(\hat{\omega}t-\frac{2\pi}{3}\right) & \sin\left(\hat{\omega}t+\frac{2\pi}{3}\right) \\ \cos(\hat{\omega}t) & \cos\left(\hat{\omega}t-\frac{2\pi}{3}\right) & \cos\left(\hat{\omega}t+\frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{6}$$

For a three-phase voltage in the *abc* frame, with frequency ω and Park transformation based on rotating frame speed $\hat{\omega}$, the *abc* and *dq* voltages are given by

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_{pk}\sin(\omega t+\varphi_0) \\ V_{pk}\sin\left(\omega t-\frac{2\pi}{3}+\varphi_0\right) \\ V_{pk}\sin\left(\omega t+\frac{2\pi}{3}+\varphi_0\right) \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} V_{pk}\cos(\omega t-\hat{\omega}t+\varphi_0) \\ V_{pk}\sin(\omega t-\hat{\omega}t+\varphi_0) \\ 0 \end{bmatrix} \tag{8}$$

Referring to (8), the *dq* voltages have a different oscillation frequency compared to the *abc* components. The DC offset values are also transformed as follows:

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{V_{pk}}{3}\begin{bmatrix} \alpha\sin(\hat{\omega}t+\theta) \\ \alpha\cos(\hat{\omega}t+\theta) \\ v_{a,dc}+v_{b,dc}+v_{c,dc} \end{bmatrix} \tag{9}$$

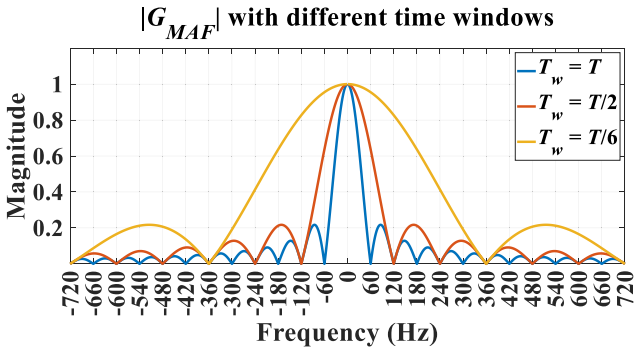

FIGURE 4. MAF's transfer function magnitude.

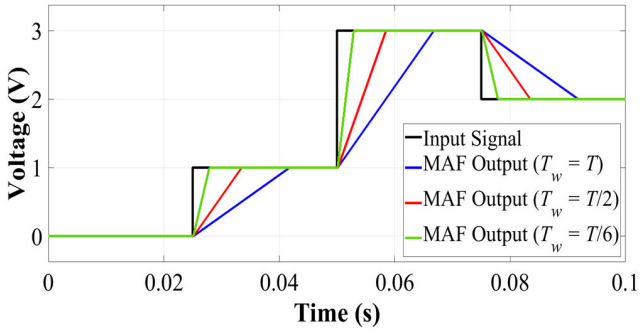

FIGURE 5. MAF's response delay based on the window size.

TABLE 2. Harmonic rejection capability of MAF.

MAF Window size	T	$T/2$	$T/6$
Harmonics to be rejected	0, -1, ±2, ±3, ±4, …	-1, ±3, ±5, ±7, …	-5, +7, -11, +13, …

where

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}(v_{c,dc} - v_{b,dc})}{2v_{a,dc} - v_{b,dc} - v_{c,dc}}\right) \tag{10}$$

$$\alpha = 2\sqrt{v_{a,dc}^2 + v_{b,dc}^2 + v_{c,dc}^2 - v_{a,dc}v_{b,dc} - v_{a,dc}v_{c,dc} - v_{b,dc}v_{c,dc}} \tag{11}$$

The phase sequence transformation after Park transformation from *abc* to *dq* frame is summarized in Table 1 [23]. Figure 4 displays the transfer function magnitude of MAF for three different window sizes: T, $T/2$, and $T/6$. The harmonic rejection capability of MAF based on its window size is summarized in in Table 2 [12].

A crucial aspect in designing a MAF lies in the selection of the window size, T_w, as it profoundly influences the response speed and filtering capability of MAF-PLL. Typically, when DC offset is disregarded, T_w is set to half the fundamental period to eliminate the negative sequence second harmonic which is a consequence of fundamental negative sequence voltage. However, it is recommended to set T_w to the full period when considering DC offset, as it can induce ripple at the fundamental frequency. Additionally, the window size of the MAF is chosen as one-sixth of the fundamental grid period to selectively eliminate non-triplen odd harmonics, thereby expediting the response of the PLL [7], [24].

MAF-PLL with a window size equal to the input fundamental period can remove all the harmonics, but the response delay is drastically increased due to the MAF's large window size. Longer filter delay times worsen the inverter's susceptibility to transient instability during significant grid disturbances compared to the traditional SRF-PLL [38].

By narrowing the window size of the MAF, the dynamic response performance is significantly improved [19]. As shown in Figure 5, the response delay of MAF is reduced with narrower time windows.

B. SIMULATION RESULTS

The following scenarios are simulated MATLAB/SIMULINK to study the impact of MAF's time window on PLL's performance under adverse grid conditions:

- 5-10 s: $\pi/6$ radian phase jump
- 15-20 s: 20% voltage swell
- 25-30 s: Odd harmonic injection (3^{rd}: 30%, 5^{th}: 30%, 7^{th}: 15%, 9^{th}: 20%)
- 35-40 s: DC offset (V_a: −5 V, V_b: −10 V: V_c: −15 V)
- 45-50 s: 2 Hz frequency jump
- 55-60 s: Even harmonic injection (2^{nd}: 30%, 4^{th}: 30%, 6^{th}: 20%, 8^{th}: 20%)
- 65-70 s: 30% negative sequence injection
- 75-80 s: 33 Hz inter-harmonics injection
- 85-90 s: Negative-sequence odd harmonic injection (3^{rd}: 30%, 5^{th}: 30%, 7^{th}: 15%, 9^{th}: 20%)
- 95-100 s: Non-triplen harmonics (5^{th}: 25%, 7^{th}: 10)

Three-phase voltages during contingencies are shown in Figure 6. V_q, depicted in Figure 7, shows an oscillatory behavior which can be fully removed when MAF with T_w equal to full fundamental period is used (as shown in Figure 8 (a)). As shown in Figure 8 (b) and (c), MAF with a smaller time window can remove some of the oscillations based on the harmonic rejection capability of MAF shown in Table 2.

Oscillations observed in the *dq* frame have different frequencies based on the existing harmonics. All oscillations have a zero average over fundamental period. Therefore, MAF with fundamental period window size can filter the oscillations. Smaller window size MAFs have the capability to filter the oscillations due to odd and non-triplen harmonics. This simulation shows that based on grid voltage's type of non-ideality, MAF's window size could be adjusted to filter the harmonics in the *dq* frame.

In next section, we show how we can adjust the window time of the MAF based on the oscillation frequency of V_q so that the harmonics are rejected while MAF operates with the minimum time window for any grid condition.

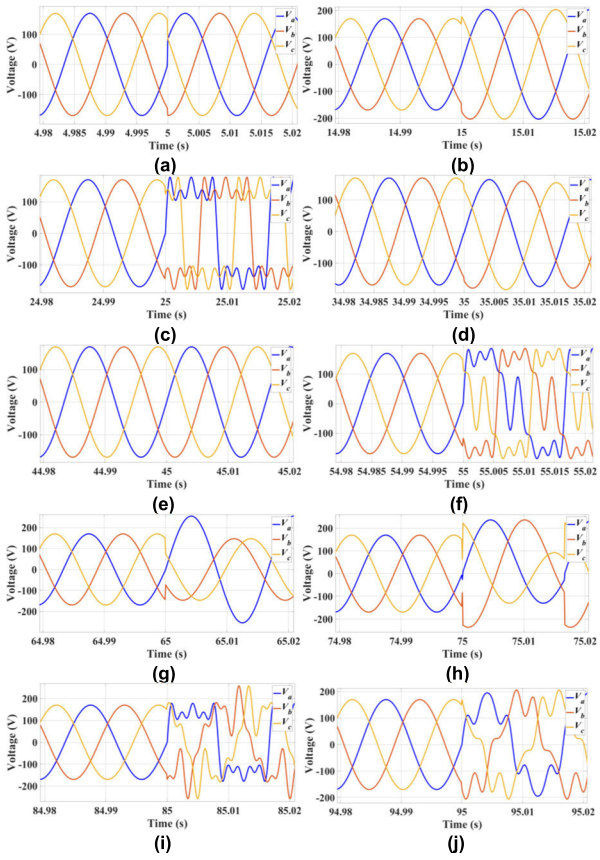

FIGURE 6. Simulation scenarios: (a) phase jump, (b) voltage swell, (c) odd harmonics, (d) DC offset, (e) frequency jump, (f) even harmonics, (g) negative sequence, (h) interharmonics, (i) negative-sequence odd harmonics, and (j) non-triplen harmonics.

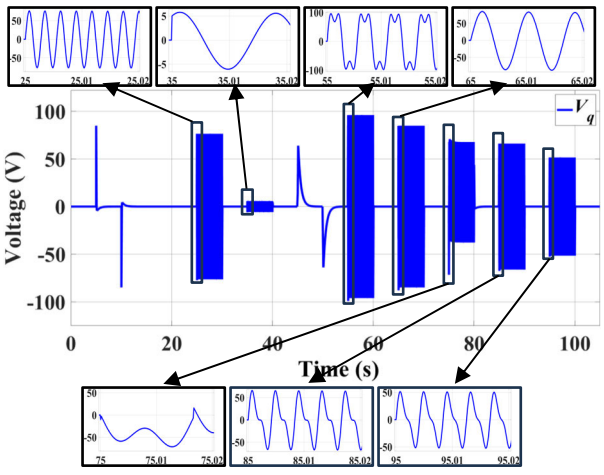

FIGURE 7. Simulated V_q and its oscillations.

III. PROPOSED SOLUTION

Existence of harmonics, inter-harmonics, and DC offset leads to oscillations with different frequencies in the *dq* frame after Park transformation as previously shown in Table 1. MAF with a time window equal to fundamental period can reject these oscillations, however some harmonics can be cancelled with smaller time windows as shown in Table 2. Since V_q has

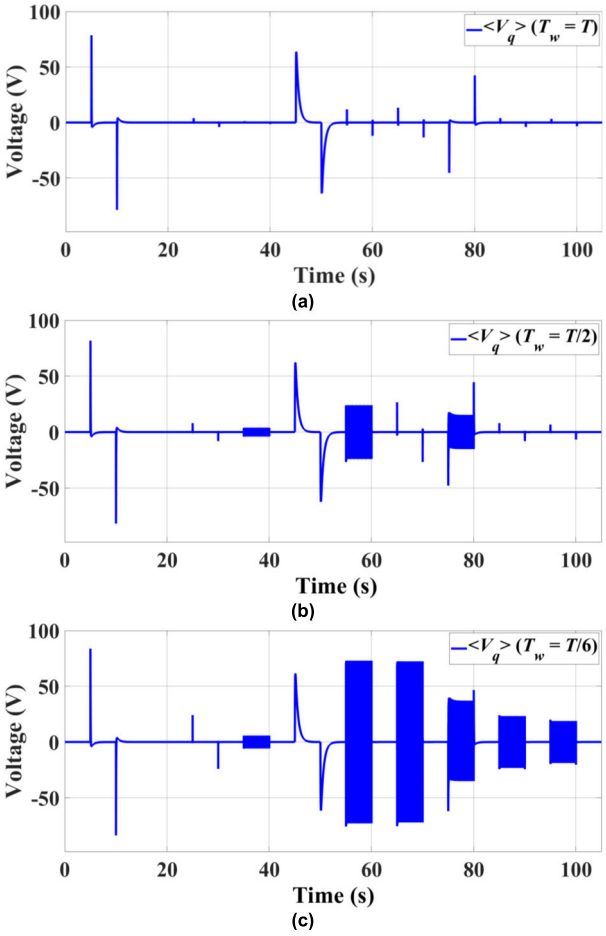

FIGURE 8. Oscillation rejection of MAF based on its window size. (a) $T_W = T$, (b) $T_W = T/2$, and (c) $T_W = T/6$.

no DC offset value, signal's average over the fundamental frequency should be zero. This means that the optimum size for MAF's window size depends on the frequency of oscillation in the *dq* frame. If V_q has no oscillation as is the case of no harmonics, MAF's time window can be reduced to only one sample per window. For integer harmonics, the frequency of oscillation will be multiple of the grid's nominal frequency. Choosing the time window based on V_q's oscillation frequency makes sure that MAF's window size is the minimum possible value based on grid conditions while rejecting all the harmonics in the output.

A. DISCRETE FOURIER TRANSFORM (DFT)

In this work, to find the fundamental frequency of the harmonic polluted V_q signal we used Discrete Fourier Transform (DFT). The application of DFT algorithm for frequency analysis is well-established [39], [40], [41]. However, the application of it in MAF-PLLs to identify the *dq* signal's oscillation frequency and optimizing the MAF's window size is a novel contribution of this work. Algorithm 1 shows the pseudocode for fundamental frequency detection of the signal using Fast Fourier Transform (FFT). Figure 9 displays the results of applying this method to a noisy signal.

Algorithm 1 Fundamental Frequency Detection

```
y = fft(bufferMean); % Compute the FFT
n = length(bufferMean);
fs = 1e4; % Sampling frequency
sp2 = abs(y/n); % Two-sided spectrum
sp1 = sp2(1:n/2+1); % Single-sided spectrum
sp1(2:end-1) = 2*sp1(2:end-1);
% Frequency axis
f = fs*(0:(n/2))/n;
% Find the peak in the spectrum
[~, idx] = max(sp1);
OscFreq = f(idx + 1);
```

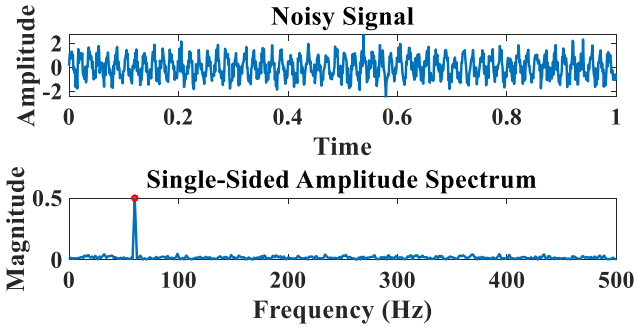

FIGURE 9. Fundamental frequency detection using DFT.

Other methods such as zero-crossing or peak detection could not accurately find the fundamental frequency in a harmonic-polluted signal. Addition of frequency-locked loops to estimate the frequency also makes the system highly nonlinear and increases the complexity of implementation [12]. Therefore, DFT is the most effective method to approximate *dq* oscillations.

The least complex, yet accurate, way to implement frequency estimation using FFT involves without additional windowing has a time complexity of O(N.log(N)), where N is the length of the input signal.

B. SHORT-TIME FOURIER TRANSFORM (STFT)

Due to the high computation time of FFT, we used Short-Time Fourier Transform (STFT) [42] for faster PLL operation. STFT is a powerful signal processing tool for noisy input signals which computes the amplitudes and phase of the localized signal frequency components [43]. STFT-based algorithms have superior computing speed and harmonic-rejection characteristics [44]. STFT decomposes the signal into short-term portions by windowing, and DFT is calculated for each window. The window slides along the signal, and the DFT results for each portion are entered into a matrix to represent the signal in terms of frequency, amplitude, and time [45]. The STFT of a signal $x[n]$ is defined as [46]:

$$X[k,n] = \sum_{m=0}^{R-1} x[n-m]\, w[m] e^{-j2\pi km/N} \tag{12}$$

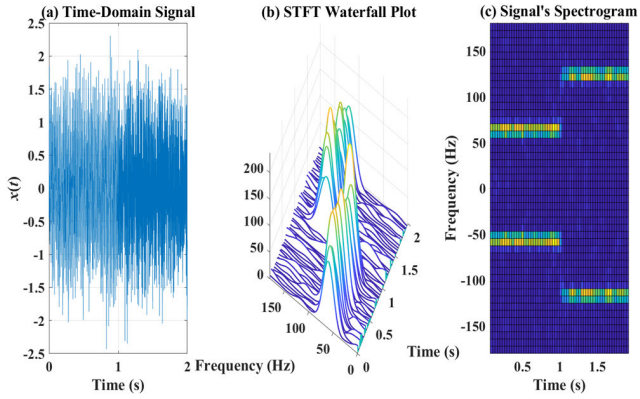

FIGURE 10. Frequency detection of a noisy signal using STFT.

where $w[n]$ is a window of length R, and k is the harmonic order.

The Goertzel algorithm can be used to compute DFT spectra over short time sections of the signal [47]. Goertzel algorithm is an alternative method for evaluating DFT which saves computation time as well as storage memory and reduces the number of operations to only $N+1$ multiplications and $2N+2$ additions [48]. Therefore, the computation complexity is reduced from O(N.log(N)) for the general FFT to O(N) using the Goertzel-algorithm-based STFT [49]. In the Goertzel algorithm, a set of N signal samples is transformed into a set of N frequency coefficients based on the following equation [50]:

$$Xy[k] = \sum_{n=0}^{N-1} x[n]\, e^{-j2\pi nk/N} \tag{13}$$

Figure 10 shows a noisy time-domain signal and its STFT-based DFT results. The time-domain signal, shown in Figure 10 (a), has a fundamental frequency of 60 Hz from 0 to 1 s and 120 Hz from 1 to 2 s. The waterfall and spectrogram plots in Figure 10 (b) and (c) show the efficacy of STFT in finding the fundamental frequency of oscillation, despite the existing noise, in a time-efficient manner.

While the fundamental concept of STFT-based frequency estimation is not new, the approach's adaptation and presentation within the context of PLL offer novel insights. Implementing this method on resource-constrained hardware platforms, such as microcontrollers (e.g. Microchip's *dsPIC*), highlights its applicability in real-time scenarios with limited computational capabilities. Employing specialized Digital Signal Processing (DSP) libraries, the algorithm efficiently computes the DFT of the windowed signal. Leveraging optimized STFT algorithms tailored for microcontroller platforms, this step minimizes computational complexity while maximizing speed, rendering it ideal for real-time applications. The implementation of STFT and Gertzel algorithm on a *dsPIC* microcontroller (from Microchip, Inc.) is displayed in the Appendix.

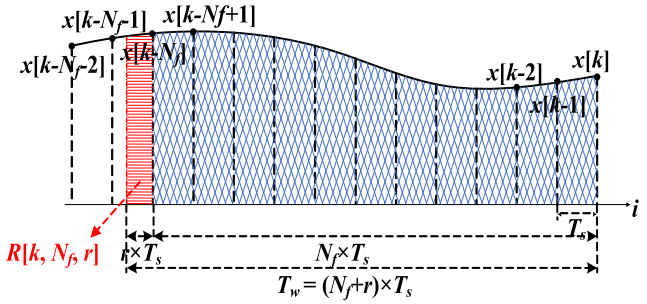

FIGURE 11. MAF discretization using trapezoidal integration.

Once the oscillation frequency is identified, window size is set to $T_w = 1/f$. In this work, we utilize the trapezoidal rule for the discretization of MAF (as shown in Figure 11) due to its higher accuracy, better harmonic rejection, and lower time delay when compared to other methods such as the backward Euler integration method [25], [34]. An issue of the discretized MAF is that T_w must be equal to an integer multiple of the sampling time, T_s. Otherwise, the effectiveness of MAF in eliminating the harmonic content is reduced [9]. To deal with this issue, interpolation method adopted in [34] is used to calculate the remainder area. The formulation for implementing MAF in the discrete form is given by (14).

$$y[k] = \frac{T_s}{T_w}\left\{\left(\sum_{i=0}^{N_f-1} x[k-i]\right) + \frac{x[k-N_f] - x[k]}{2} + R[k]\right\} \tag{14}$$

where $N_f = \text{floor}(\frac{T_w}{T_s})$, $r = \frac{T_w}{T_s} - N_f$, and

$$R[k] = \frac{1}{2}\left\{r^2 x[k-N_f-1] + \left(2r - r^2\right) x[k-N_f]\right\} \tag{15}$$

IV. RESULTS

A. SIMULATION RESULTS

The same scenarios explained in Section II-B are simulated using a variable window size algorithm. Oscillation frequency of V_q is estimated using STFT and MAF's window size is adjusted accordingly. The dq oscillation frequency and MAF's window size (number of samples) are shown in Figure 12 (a) and (b). Figure 12 (c) illustrates the frequency output of the PLL which rejects all the harmonic oscillation similar to the case when $T_w = T$. The main contribution of this work is achieving the same harmonic rejection capability of MAF with fundamental period window size with a minimum size window such that there are no oscillations in the output of MAF-PLL.

B. EXPERIMENTAL RESULTS

Further examination was conducted utilizing a prototyping system (from Triphase) designed for rapid testing of

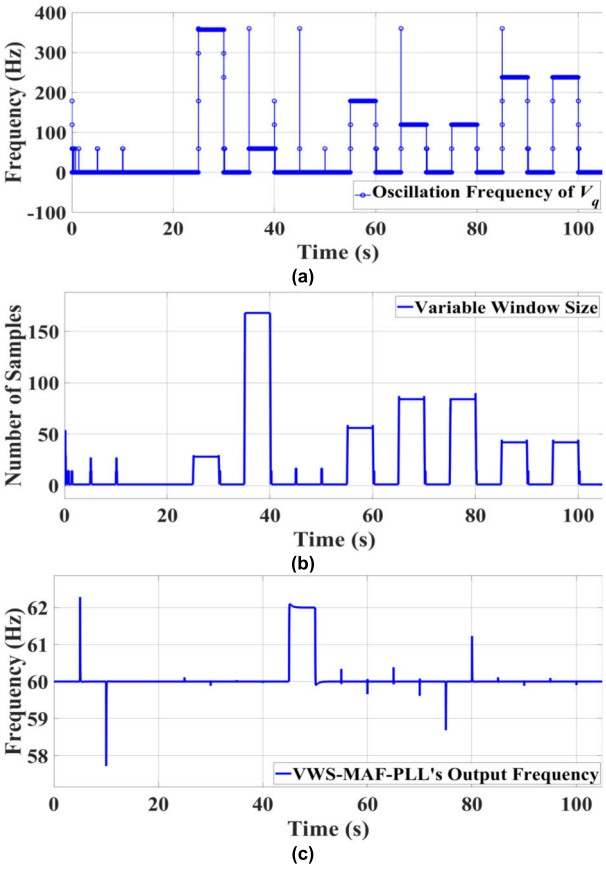

FIGURE 12. Simulated scenarios with a variable MAF, (a) oscillation frequency of V_q, (b) number of samples in MAF, (c) PLL's output frequency.

control systems. Illustrated in Figure 13, this system comprises a real-time controller (RTC), a standard x86/AMD64 PC operating on Linux. The operating system allows the execution of compiled C code, generated through MATLAB Simulink's automatic code generation, in real-time. The primary hardware component is a VSC, an industrial-grade variable-frequency-drive controlled by the RTC. A data acquisition panel is integrated, featuring six isolated voltage and three current measurement ports that can transmit data back to the workstation for control or visualization. The isolated inputs on the data acquisition panel can measure voltages up to 1000 V and current up to 15 A.

The experimental arrangement, shown in Figure 13, incorporates a fiber-optic communication system facilitating communication at a speed of 250 Mbps among the VSC, RTC, and the data acquisition block. Information and commands exchanged with the RTC are time-synchronized and organized for scheduled data exchange with the workstation PC through a standard Ethernet connection. Data logging occurs at a sampling rate of 16 kHz.

Two abnormal conditions were created and tested using this experimental setup. The ratio of the reference signal's amplitude to that of carrier, known as amplitude modulation index (m_a), was varied to generate different

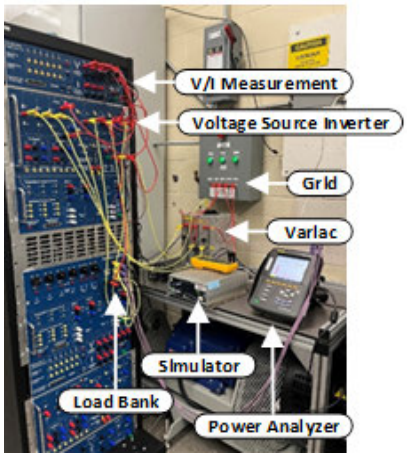

FIGURE 13. Experimental setup.

TABLE 3. Oscillation frequency and MAF's number of samples for experimental cases.

Case #	I	II
Oscillation Freq. of V_q (Hz)	57.14	80
T_w (Number of Samples)	175	125

harmonic-polluted non-ideal voltage signals. Scenarios for the inverter producing different harmonic contents are case (a) under-modulation ($m_a = 0.9$) and case (b) over-modulation ($m_a = 1.3$).

Figure 14 shows the inverter's input DC and three-phase output AC voltages as well as the harmonic content captured by the power analyzer. PLL's frequency and phase outputs as well as V_q and its average are shown for both scenarios.

Referring to Figure 14, one can observe that the VWS-MAF-PLL algorithm successfully can identify the frequency of the fundamental component and the phase angles in both harmonic-heavy scenarios. Table 3 shows the frequency of oscillation and MAF's window size (number of samples) for each case.

Furthermore, addition of a delay signal cancellation operator as explained in a previous work by the authors [20], and shown in Figure 15, can halve the window size of MAF while maintaining its harmonic rejection capabilities. Moreover, performance of the proposed PLL could be further improved by tuning the PI controller's parameters using symmetrical optimum method [4]. Figure 16 shows the improvement in overshoot and settling time values after tuning PLL's PI parameters.

C. COMPARATIVE ANALYSIS

To verify the accuracy of the VWS-MAF method proposed in this paper, we compared the performance of MAF PLL with a time window of one cycle and VWF-MAF PLL for six different contingencies:

1) $\pi/6$ radian phase jump
2) Odd harmonics (3rd: 30%, 5th: 30%, 7th: 15%, 9th: 20%)

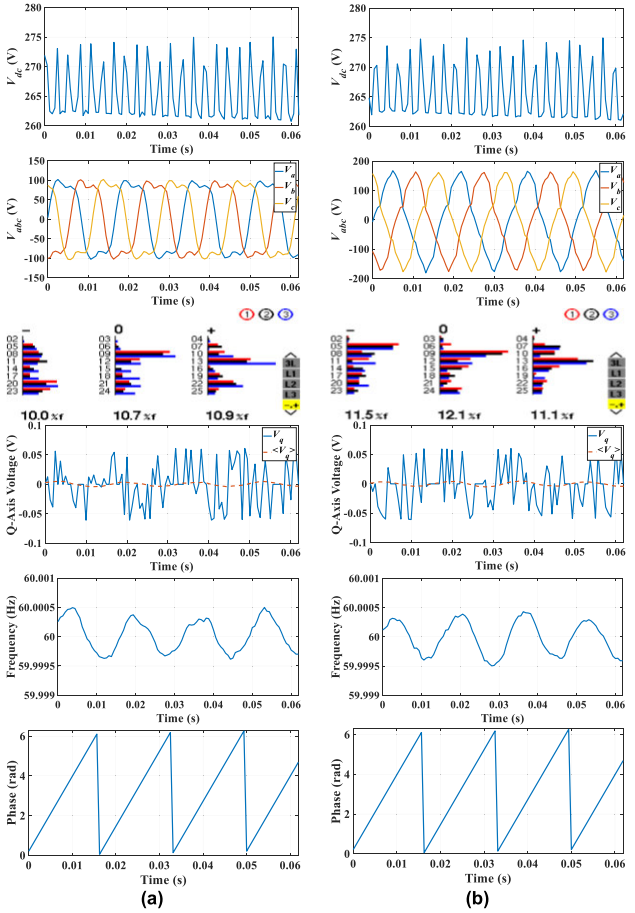

FIGURE 14. Inverter's V_{dc} and V_{abc}, harmonic content, V_q and $<V_q>$, and PLL's output frequency and phase (a) Case I, $m_a = 0.9$ and (b) Case II, $m_a = 1.3$.

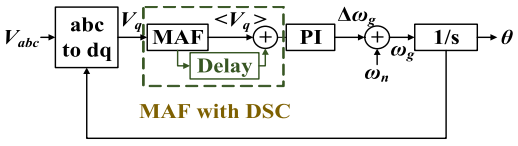

FIGURE 15. PLL based on MAF with embedded delay.

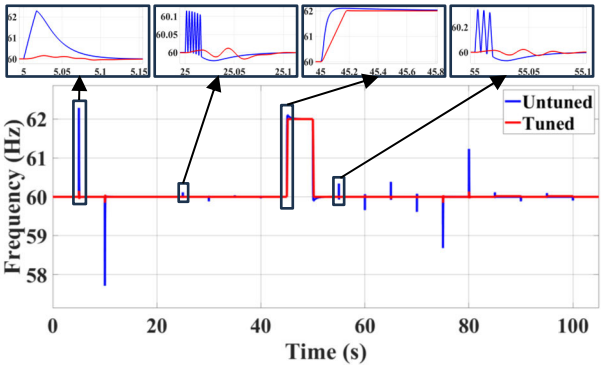

FIGURE 16. PLL's performance with tuned PI.

3) 2 Hz frequency jump
4) 30% negative sequence injection
5) Negative-sequence odd harmonics (3rd: 30%, 5th: 30%, 7th: 15%, 9th: 20%)

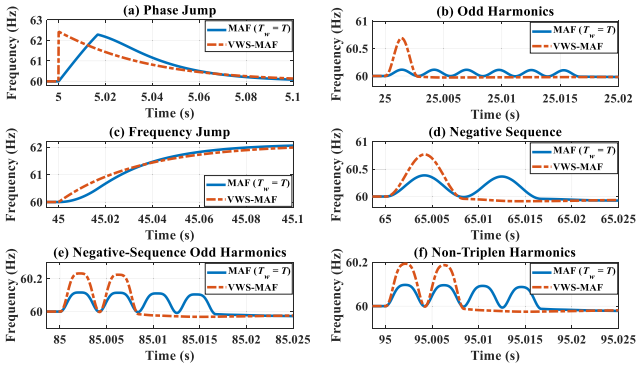

FIGURE 17. Performance comparison of PLL with fixed time-window MAF ($T_w = T$) with VWS-MAF PLL.

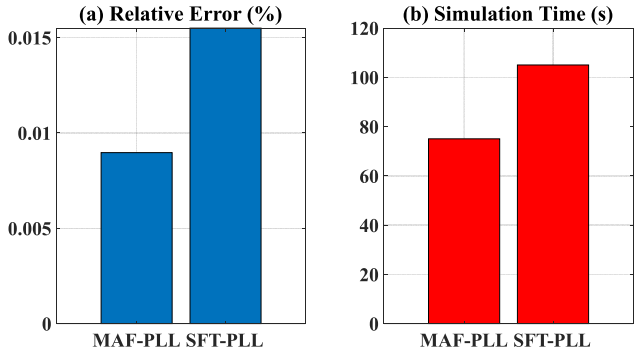

FIGURE 18. Performance comparison of VWS-MAF PLL and SFT-PLL.

6) Non-triplen harmonics (5^{th}: 25%, 7^{th}: 10)

As shown in Figure 17, for frequency and phase jump scenarios, VWS-MAF shows a faster transient response while for harmonic-injection scenarios faster damping and less oscillations are observed in the PLL's transient response.

Furthermore, we implemented another PLL algorithm based on Fourier transform, and compared its accuracy and runtime for the simulated abnormal grid conditions with our proposed MAF-based PLL algorithm. The Sliding Fourier Transform (SFT) method [51] is a recursive algorithm based on DFT which can serve as a potential tool for phase angle estimation, boasting robust immunity against harmonic interference. Scenarios presented in Section III were simulated using both algorithms and their average relative error and simulation time were compared in Figure 18. Results show a smaller average relative error for the estimated frequency and a shorter simulation time for the MAF-based PLL method.

V. CONCLUSION

This paper contributes to the field of grid synchronization, with a primary focus on addressing the challenges encountered by MAF-PLL with a fundamental-period window size. This configuration effectively achieves harmonic rejection, at the price of slowed dynamic response. The innovation presented in this paper is the development and application of a Variable Window Size (VWS) Moving Average Filter (MAF) within the PLL architecture. The adaptive nature of the VWS-MAF, determined by identifying the dominant frequency of oscillation in the *dq* frame through Short-Time Fourier Transform (STFT) analysis, addresses the trade-off by dynamically adjusting the window size. This ensures improved dynamic response while maintaining harmonic rejection capabilities, a substantial advancement in the quest for efficient grid synchronization. The experimental validation, simulation results, and comparative analysis presented in the paper affirm the effectiveness of the proposed VWS-MAF in calculating frequency and phase of a three-phase system accurately and efficiently.

Algorithm 2 STFT using Goertzel algorithm

```
float** STFT(float* in, int len, int wSize, int hSize, float rate, float
freq, int* numW) {
  *numW = (len - wSize) / hSize + 1;
  float window[wSize];
  for (int i = 0; i < wSize; ++i) {
    window[i] = 0.54 - 0.46 * cos(2 * PI * i / (wSize - 1));
  }
  float** stftMatrix = (float**)malloc(*numW * sizeof(float*));
  for (int i = 0; i < *numW; ++i) {
    stftMatrix[i] = (float*)malloc(sizeof(float));
  }
  for (int i = 0; i < *numW; ++i) {
    float power = 0.0;
    for (int j = 0; j < wSize; ++j) {
      float sample = in [i * hopSize + j] * window[j];
      power += goertzel(&sample, 1, rate, freq);
    }
    stftMatrix[i][0] = power;
  }
  return stftMatrix;
}
```

Algorithm 3 Goertzel algorithm for a single-frequency bin

```
float goertzel(float* signal, int len, float samplingRate, float freq) {
  float s, s_pre = 0.0, s_pre2 = 0.0;
  float c = 2.0 * cos(2.0 * PI * freq / samplingRate);
  for (int i = 0; i < len; i++) {
    float sample = signal[i];
    s = sample + c * s_pre - s_pre2;
    s_pre2 = s_pre;
    s_pre = s;
  }
    return s_pre2 ^2 + s_pre ^2 - c * s_pre * s_pre2;
}
```

APPENDIX

Algorithms 2 and 3 show the STFT and Goertzel algorithm implementation in the *dsPIC* platform.

REFERENCES

[1] N. R. N. Ama, W. Komatsu, and L. Matakas Junior, "Single and three phase moving average filter PLLs: Digital controller design recipe," *Electric Power Syst. Res.*, vol. 116, pp. 276–283, Nov. 2014, doi: 10.1016/j.epsr.2014.06.019.

[2] Y. Han, M. Luo, C. Chen, A. Jiang, X. Zhao, and J. M. Guerrero, "Performance evaluations of four MAF-based PLL algorithms for grid-synchronization of three-phase grid-connected PWM inverters and DGs," *J. Power Electron.*, vol. 16, no. 5, pp. 1904–1917, Sep. 2016, doi: 10.6113/jpe.2016.16.5.1904.

[3] L. Wang, Q. Jiang, L. Hong, C. Zhang, and Y. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4538–4549, Oct. 2013, doi: 10.1109/TPEL.2012.2236848.

[4] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," *Renew. Sustain. Energy Rev.*, vol. 90, pp. 434–452, Jul. 2018, doi: 10.1016/j.rser.2018.03.086.

[5] N. Hui, Y. Feng, and X. Han, "Design of a high performance phase-locked loop with DC offset rejection capability under adverse grid condition," *IEEE Access*, vol. 8, pp. 6827–6838, 2020, doi: 10.1109/ACCESS.2020.2963993.

[6] A. Bamigbade, B. S. Umesh, V. Khadkikar, M. S. E. Moursi, H. H. Zeineldin, and M. A. Hosani, "Reduced-order generalized integrator-based phase-locked loop: Performance improvement for grid synchronization of single-phase inverters," *IEEE Trans. Power Del.*, vol. 37, no. 5, pp. 4382–4393, Oct. 2022, doi: 10.1109/TPWRD.2022.3169470.

[7] I. Smadi, H. Kreashan, and I. Atawi, "Enhancing the filtering capability and the dynamic performance of a third-order phase-locked loop under distorted grid conditions," *Energies*, vol. 16, no. 3, p. 1472, Feb. 2023, doi: 10.3390/en16031472.

[8] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014, doi: 10.1109/TPEL.2013.2273461.

[9] W. Luo and D. Wei, "A frequency-adaptive improved moving-average-filter-based quasi-type-1 PLL for adverse grid conditions," *IEEE Access*, vol. 8, pp. 54145–54153, 2020, doi: 10.1109/ACCESS.2020.2981426.

[10] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Electron.*, vol. 59, no. 6, pp. 2718–2731, Jun. 2012, doi: 10.1109/TIE.2011.2166236.

[11] C. Liu, J. Jiang, J. Jiang, and Z. Zhou, "Enhanced grid-connected phase-locked loop based on a moving average filter," *IEEE Access*, vol. 8, pp. 5308–5315, 2020, doi: 10.1109/ACCESS.2019.2963362.

[12] J. Li, Q. Wang, L. Xiao, Y. Hu, Q. Wu, and Z. Liu, "An $\alpha\beta$-frame moving average filter to improve the dynamic performance of phase-locked loop," *IEEE Access*, vol. 8, pp. 180661–180671, 2020, doi: 10.1109/ACCESS.2020.3028237.

[13] L. Feola, R. Langella, and A. Testa, "On the effects of unbalances, harmonics and interharmonics on PLL systems," *IEEE Trans. Instrum. Meas.*, vol. 62, no. 9, pp. 2399–2409, Sep. 2013, doi: 10.1109/TIM.2013.2270925.

[14] D. Vukadinović, T. D. Nguyen, C. H. Nguyen, N. L. Vu, M. Bašić, and I. Grgić, "Hedge-algebra-based phase-locked loop for distorted utility conditions," *J. Control Sci. Eng.*, vol. 2019, pp. 1–17, Mar. 2019, doi: 10.1155/2019/3590527.

[15] S. Wang, A. Etemadi, and M. Doroslovački, "Adaptive cascaded delayed signal cancellation PLL for three-phase grid under unbalanced and distorted condition," *Electric Power Syst. Res.*, vol. 180, Mar. 2020, Art. no. 106165, doi: 10.1016/j.epsr.2019.106165.

[16] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, and J. Doval-Gandoy, "PLL with MAF-based prefiltering stage: Small-signal modeling and performance enhancement," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4013–4019, Jun. 2016, doi: 10.1109/TPEL.2015.2508882.

[17] I. Ullah and M. Ashraf, "Comparison of synchronization techniques under distorted grid conditions," *IEEE Access*, vol. 7, pp. 101345–101354, 2019, doi: 10.1109/ACCESS.2019.2930530.

[18] P. Kanjiya, V. Khadkikar, and M. S. El Moursi, "Adaptive low-pass filter based DC offset removal technique for three-phase PLLs," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 9025–9029, Nov. 2018, doi: 10.1109/TIE.2018.2814015.

[19] Z. Wang, P. Fu, L. Huang, X. Chen, S. He, X. Zhang, and J. Yang, "Performance improvement of a three-phase PLL under distorted grid conditions based on frequency adaptive hybrid pre-filtering," *IET Power Electron.*, vol. 15, no. 13, pp. 1429–1440, Oct. 2022, doi: 10.1049/pel2.12314.

[20] P. Taheri, J. Amini, and M. Moallem, "Improving performance of three-phase MAF-PLL under asymmetrical DC-offset condition," *IEEE Access*, vol. 11, pp. 111200–111211, 2023, doi: 10.1109/ACCESS.2023.3322430.

[21] D. I. Brandão and F. P. Marafão, "Digital processing techniques applied to power electronics," in *Modeling Power Electronics and Interfacing Energy Conversion Systems*. Hoboken, NJ, USA: Wiley, 2017, ch. 12, pp. 279–320, doi: 10.1002/9781119058458.ch12.

[22] W. Liu and F. Blaabjerg, "Phase-locked loops and their design," in *Control of Power Electronic Converters and Systems*. New York, NY, USA: Academic, 2021, ch. 10, pp. 269–301, doi: 10.1016/b978-0-12-819432-4.00013-5.

[23] M. Mellouli, M. Hamouda, J. B. H. Slama, and K. Al-Haddad, "A third-order MAF based QT1-PLL that is robust against harmonically distorted grid voltage with frequency deviation," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1600–1613, Sep. 2021, doi: 10.1109/TEC.2021.3061027.

[24] J. Wang, J. Liang, F. Gao, L. Zhang, and Z. Wang, "A method to improve the dynamic performance of moving average filter-based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5978–5990, Oct. 2015, doi: 10.1109/TPEL.2014.2381673.

[25] T. Premgamone, J. Kortenbruck, E. Ortjohann, A. Schmelter, D. Holtschulte, and S. D. Varada, "Real-time harmonic component decomposition for LV grids using heterodyne method with adaptive moving average filters," in *Proc. IEEE 11th Int. Workshop Appl. Meas. Power Syst. (AMPS)*, Cagliari, Italy, Sep. 2021, pp. 1–6, doi: 10.1109/AMPS50177.2021.9586030.

[26] S. Golestan, J. M. Guerrero, and A. M. Abusorrah, "MAF-PLL with phase-lead compensator," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3691–3695, Jun. 2015, doi: 10.1109/TIE.2014.2385658.

[27] E. Robles, S. Ceballos, J. Pou, J. L. Martín, J. Zaragoza, and P. Ibañez, "Variable-frequency grid-sequence detector based on a quasi-ideal low-pass filter stage and a phase-locked loop," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2552–2563, Oct. 2010, doi: 10.1109/TPEL.2010.2050492.

[28] L. Du, M. Li, Z. Tang, L. Xiong, X. Ma, and G. Tang, "A fast positive sequence components extraction method with noise immunity in unbalanced grids," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6682–6685, Jul. 2020, doi: 10.1109/TPEL.2019.2959672.

[29] S. Golestan, J. M. Guerrero, A. M. Abusorrah, and Y. Al-Turki, "Hybrid synchronous/stationary reference-frame-filtering-based PLL," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5018–5022, Aug. 2015, doi: 10.1109/TIE.2015.2393835.

[30] M. Mirhosseini, J. Pou, V. G. Agelidis, E. Robles, and S. Ceballos, "A three-phase frequency-adaptive phase-locked loop for independent single-phase operation," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6255–6259, Dec. 2014, doi: 10.1109/TPEL.2014.2328657.

[31] I. Carugati, S. Maestri, P. G. Donato, D. Carrica, and M. Benedetti, "Variable sampling period filter PLL for distorted three-phase systems," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 321–330, Jan. 2012, doi: 10.1109/TPEL.2011.2149542.

[32] H. Xue, M. Ruan, and Y. Cheng, "A fixed length adaptive moving average filter-based synchrophasor measurement algorithm for P class PMUs," *Energies*, vol. 12, no. 21, p. 4168, Nov. 2019, doi: 10.3390/en12214168.

[33] D. D. S. Mota and E. Tedeschi, "On adaptive moving average algorithms for the application of the conservative power theory in systems with variable frequency," *Energies*, vol. 14, no. 4, p. 1201, Feb. 2021, doi: 10.3390/en14041201.

[34] A. J. Roscoe and S. M. Blair, "Choice and properties of adaptive and tunable digital boxcar (moving average) filters for power systems and other signal processing applications," in *Proc. IEEE Int. Workshop Appl. Meas. for Power Syst. (AMPS)*, Aachen, Germany, Sep. 2016, pp. 1–6, doi: 10.1109/AMPS.2016.7602853.

[35] S. W. Smith, "Moving average filter," in *The Scientist and Engineer's Guide to Digital Signal Processing*. San Diego, CA, USA: California Technical Publishing, 1997.

[36] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765–778, Feb. 2013, doi: 10.1109/TPEL.2012.2204276.

[37] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, and J. Doval-Gandoy, "A quasi-type-1 phase-locked loop structure," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6264–6270, Dec. 2014, doi: 10.1109/TPEL.2014.2329917.

[38] C. Zhang, J. Chen, and W. Si, "Analysis of phase-locked loop filter delay on transient stability of grid-following converters," *Electronics*, vol. 13, no. 5, p. 986, Mar. 2024, doi: 10.3390/electronics13050986.

[39] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, 3rd ed. Chennai, India: Pearson, 2009.
[40] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 4th ed. Chennai, India: Pearson, 2006.
[41] J. W. Cooley and J. W. Tukey, "An algorithm for the machine calculation of complex Fourier series," *Math. Comput.*, vol. 19, no. 90, p. 297, Apr. 1965.
[42] S. K. Mitra, *Digital Signal Processing: A Computer-Based Approach*, 2nd ed. New York, NY, USA: McGraw-Hill, 2001.
[43] R. S. Dasari, "Phase locked loop based signal processing approach for the health monitoring of power systems through their RF emissions," M.S. thesis, College Eng. Polym. Sci., Univ. Akron, Akron, OH, USA, 2018.
[44] R. K. Mai, Z. Y. He, L. Fu, B. Kirby, and Z. Q. Bo, "A dynamic synchrophasor estimation algorithm for online application," *IEEE Trans. Power Del.*, vol. 25, no. 2, pp. 570–578, Apr. 2010, doi: 10.1109/TPWRD.2009.2034293.
[45] A. Yılmaz and G. Bayrak, "Real-time disturbance detection using STFT method in microgrids," in *Proc. 7th Intl. Symp. Innovative Technol. Eng. Sci. (ISITES)*, Şanlıurfa, Turkey, Nov. 2019, pp. 1115–1121, doi: 10.33793/acperpro.02.03.124.
[46] J. R. de Carvalho, C. A. Duque, M. V. Ribeiro, A. S. Cerqueira, T. L. Baldwin, and P. F. Ribeiro, "A PLL-based multirate structure for time-varying power systems harmonic/interharmonic estimation," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 1789–1800, Oct. 2009, doi: 10.1109/TPWRD.2009.2027474.
[47] J.-H. Kim, S.-W. Lee, S.-R. Lee, T.-W. Lee, and C.-Y. Won, "Power quality control using the Goertzel algorithm for grid-connected system," in *Proc. 31st Int. Telecommun. Energy Conf.*, Incheon, South Korea, Oct. 2009, pp. 1–3, doi: 10.1109/INTLEC.2009.5351931.
[48] S. Karvekar and D. Patil, "Comparison of reference current generation for shunt active power filter using Goertzel algorithm and enhanced PLL," in *Proc. Int. Conf. Circuits, Power Comput. Technol. (ICCPCT)*, Nagercoil, India, Mar. 2014, pp. 620–625, doi: 10.1109/ICCPCT.2014.7054757.
[49] M. Covell and J. Richardson, "A new, efficient structure for the short-time Fourier transform, with an application in code-division sonar imaging," in *Proc. Int. Conf. Acoust., Speech, Signal Process. (ICASSP)*, vol. 3, Toronto, ON, Canada, Apr. 1991, p. 2041, doi: 10.1109/ICASSP.1991.150805.
[50] A. Vitali, "The Goertzel algorithm to compute individual terms of the discrete Fourier transform (DFT)," ST Microelectron., Geneva, Switzerland, Tech. Rep. DT0089 Rev. 1, Dec. 2017.
[51] A. M. Mansour, O. M. Arafa, M. I. Marei, I. Abdelsalam, G. A. A. Aziz, and A. A. Sattar, "Hardware-in-the-Loop testing of seamless interactions of multi-purpose grid-tied PV inverter based on SFT-PLL control strategy," *IEEE Access*, vol. 9, pp. 123465–123483, 2021, doi: 10.1109/ACCESS.2021.3110013.

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