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RESEARCH ARTICLE

Effect of the Conduction Resistance of SiC MOSFET on the Harmonics of Inverter Voltage in Wireless Power-Transfer Systems for Electric Vehicles

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ABSTRACT This paper describes the effects of power device characteristics on the harmonics of the inverter output voltage and magnetic field leakage in a wireless power transfer system for electric vehicles with phase shift control and the suppression method of the haemonics. Even when the phase shift angle is theoretically set to minimize harmonics, the experimental results have confirmed the existence of the remaining harmonics, which have dead-time dependence. Harmonics with dead-time dependence include those caused by changes in the pulse width depending on the dead time, which have been conventionally compensated for by dead-time compensation. However, the targeted harmonics have a dead-time dependence even when the pulse widths are matched. Therefore, we focused on the difference between the dead-time period and other periods. Further, as the conduction resistance differs between these two periods, we performed a circuit analysis, also considering the conduction resistance. From the results, it was theoretically clarified that harmonics are generated because of the difference in resistance in the forward and reverse directions of power devices. Furthermore, the theoretically calculated dead time dependence of the device-induced harmonics was confirmed by experimental measurements of the harmonics of the inverter output voltage waveform and the magnetic field leakage. This confirms that one of the factors responsible for the harmonics is the difference in the device conduction resistance before and after the dead-time period. The main contributions of this paper are the revelation of unconventional dead-time-dependent harmonics and the proposal of a method for suppressing them.

INDEX TERMS Diodes, harmonics, inverters, MOSFET, power semiconductors, silicon carbide (SiC), wireless power transfer.

I. INTRODUCTION

The performance of power electronic systems is highly dependent on the characteristics of the power devices within them [1], [2], [3], [4], [5], [6]. For example, the efficiency and energy density of a power system can be improved by decreasing the on-resistance and increasing the switching speed of the power devices used [1], [2], [3]. However, these improvements of power devices do not always reduce the electromagnetic (EM) noise emanating from the power

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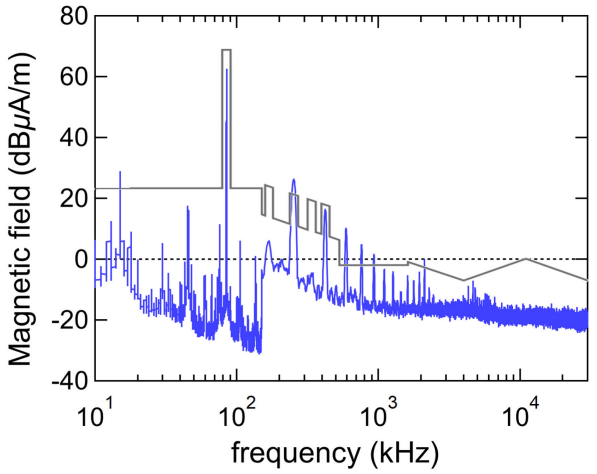

FIGURE 1. A comparison of the 10 m-radiated emissions test result for a WPT system with a fundamental period of 85 kHz (operation power: 7 kW) with the regulation values of the Japan Radio Act.

systems [7]. In reality, the high output power of power systems and the high switching speed of their power devices generally exacerbate EM noise. Wireless power transfer (WPT) systems for electric vehicles (EVs), which have received significant research interest in recent years as effective tools for improving the safety of EV charging and extending the cruising range, contribute minimally to reducing EM noise [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. This is because WPT systems for EVs transmit large power (several tens of kW) and employ a relatively high switching frequency (85 kHz) for the power devices based on the SAE J2954 standard [20]. In addition, the power-transmitting coils are expected to be installed outdoors. EM noise is legally regulated, for example, by Comité international spécial des perturbations radioélectriques (CISPR)) and Japan Radio Act [21], [22]. Accordingly, engineers need to solve the EM noise problem of WPT systems for EVs.

Fig. 1 shows a comparison of the experimental results of the 10 m-radiated emission test applied to a WPT system with a fundamental period of 85 kHz (operation power: 7 kW) with the regulation standards of the Japan Radio Act. It can be observed that the third-order harmonic is above the regulation values. The experimental conditions are described below.

Today, phase-shift control is widely employed as a suppression method using circuit control [23], [24], [25]. It theoretically eliminates the harmonics of the specific frequency that vanishes in the full-bridge configuration; it is also applied in WPT systems for EVs. However, experimental results confirm that harmonics with dead time dependence remain. A dead time compensation is proposed to solve the dead time dependent harmonics caused by pulse-width changes depending on the current direction during the dead time in pulse-width-modulation inverters for motors [26], [27]. However, the same countermeasure does not work for the WPT system with phase-shift control because, as detailed in the following sections, the dead time dependent harmonics in our experiment are generated even when the pulse width does not vary with the dead time. This indicates the presence of another factor, which previous works might have overlooked. The primary research questions of this paper are to analyze the origin of harmonics that remain even after phase-shift control and propose a suppression method.

Dead time is when an off signal is input to both series-connected devices in a full-bridge inverter circuit in a WPT system. The dead time prevents both devices from turning simultaneously, the so-called short circuit, with alternating input on signals due to the switching delay of the power devices. Although the dead time has some disadvantages, such as a slight increase in loss, the loss in a short circuit is much more significant; therefore, the dead time cannot be eliminated to achieve high efficiency. Furthermore, WPT systems for EVs, which output large power, require large-area devices, increasing the dead time, and the carrier frequency is higher at 85 kHz. Thus, the ratio of dead time in one cycle is relatively large. Consequently, the dead-time-dependent harmonics in this study are also relatively large. In the future, when the output power of WPTs is further increased, the problem of dead-time-dependent harmonics might also increase. Therefore, it is crucial to clarify the mechanism of the dead-time-dependent harmonics and propose a method to suppress them to prevent magnetic field leakage in WPT systems.

This paper is organized as follows. Section II describes the role of switching devices in phase-shift-controlled WPT systems, along with their operating mode specifications. Section III describes the harmonics simulated based on the circuit simulation results. The results show that the dead time settings do not result in zero amplitude for certain harmonics. In Section IV, we describe the inverter voltage waveforms by Fourier series expansion (including the effect of device-conduction resistance), confirm the dependence on DT, and describe the harmonic-generation mechanism. Additionally, we propose a method for reducing harmonics based on the dead time dependence. Section V describes the experiments conducted using a WPT circuit, which shows that the amplitude of the third harmonic component of V_p depends on DT and that the proposed method of adjusting the phase shift can reduce the harmonics and magnetic field leakage. The conclusions of this study are summarized in Section VI.

II. WPT INVERTER CIRCUIT AND OPERATION MODE INCLUDING DEVICE CONDUCTION RESISTANCE

The circuit diagram of a WPT system with a T-type equivalent circuit of power transmission coils is illustrated in Fig. 2. The circuits enclosed in green and red lines represent a full-bridge inverter and a power transmission circuit, respectively. Q1–Q4 are SiC MOSFETs employed as switching devices in the inverter, and R_g denotes the gate resistance. In the power-transmission part, L and C denote the inductance and capacitance, respectively, and the associated subscripts, "p" and "s", represent the primary and secondary

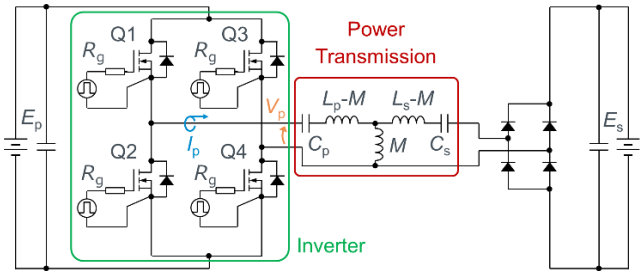

FIGURE 2. Circuit diagram of the WPT system with a T-type equivalent circuit of power transmission coils.

TABLE 1. List of simulation parameters.

Symbol	Quantity	Value
L_p	Inductance in the primary side	219.54 μH
L_s	Inductance in the secondary side	85.29 μH
M	Mutual inductance	19.87 μH
C_p	Capacitance in the primary side	14.6 nF
C_s	Capacitance in the secondary side	33.3 nF
R_p	Series resistance in the primary coil	68.9 mΩ
R_s	Series resistance in the secondary coil	25.1 mΩ
E_p	Power supply in the primary side	500 V
E_s	Battery in the secondary side	500 V
R_{on}	On-resistance of the switching device	6 mΩ
R_{di}	Differential resistance of the diode	15.6 mΩ
f	Fundamental frequency	85 kHz
α	Phase-shift angle	π/3 rad
R_g	Gate resistance of the switching device	4.7 Ω
DT	Dead time	250 ns
V_{gs}	Gate-source voltage of MOSFET	–
V_p	Inverter output voltage	–
I_p	Inverter output current	–

sides, respectively. M denotes the mutual inductance between the primary and secondary transmission coils. E_s and E_p represent the power supply and battery, respectively.

The circuit-simulation waveforms of the WPT system with phase-shift control, obtained using SIMetrix (SIMetrix Technologies), are presented in Fig. 3. The parameters employed in this simulation are listed in Table 2. The values of L_p, L_s, M, C_p, C_s, R_s, and R_p were measured using an LCR meter (IM 3533, HIOKI). The transmission coils described in Section V were arranged in a T-type equivalent circuit to obtain a dynamic WPT system [6]. The transistor model is an ideal switch model equipped with a series resistor with the on-resistance (R_{on}) of the transistor, whereas the diode model is an ideal diode model serially connected with the differential resistance of a diode (R_{di}). R_{on} and R_{di} adopt the static characteristic values of the devices used in the experiments described in Section V [28]. As depicted in Fig. 3, DT was set between the gate-on signals to prevent a short circuit. Thus, based on the combination of the gate signals, the circuit operation can be segmented into three modes (A, B, and C), as described below.

[Mode A] "Q1 and Q3" or "Q2 and Q4" are in the on-state simultaneously.

[Mode B] Only one transistor is in the on state (DT).

[Mode C] "Q1 and Q4" or "Q2 and Q3" are in the on-state simultaneously.

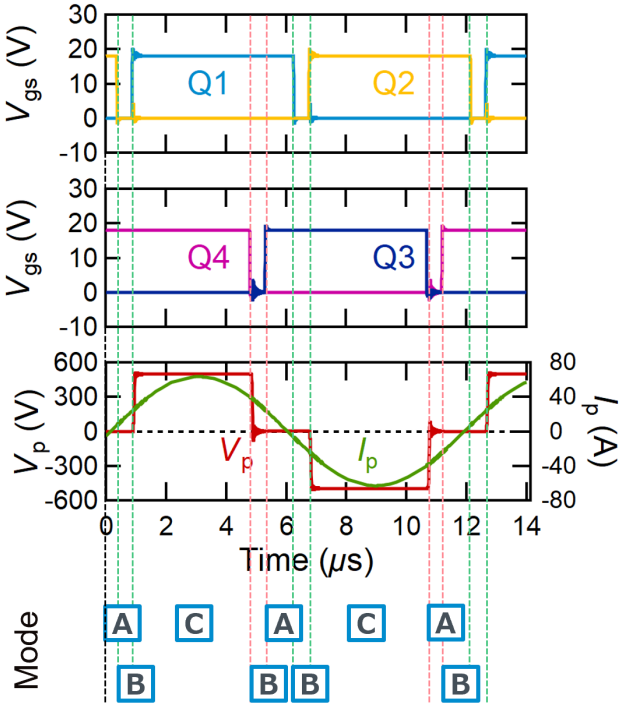

FIGURE 3. Simulated V_{gs}, V_p, and I_p waveforms of the WPT system.

The patterns of the current flow corresponding to these operation modes are respectively denoted by the arrows in Fig. 4(a). Fig. 4(b) presents a voltage waveform, showing the magnified waveform only near $V_p = 0$ to easily observe the effect of the device characteristics. Figures A, B, and C indicate the operation modes.

However, Fig. 5 shows the ideal V_p ($V_{p,ideal}$) waveform using phase-shift control without considering device characteristics, where ω denotes the angular frequency of the WPT system. The difference between the waveforms shown in Fig. 4(b) and Fig. 5 is that the one shown in Fig. 5 assumes that the switching device is an ideal switch, whereas the one shown in Fig. 4(b) considers the conduction resistance of the switching device. Therefore, as depicted in Fig. 4(b) and 5, the fundamental variations are observed in near-zero V_p. If the transistors are employed as an ideal switch, i.e., where they presume zero resistance in their on state, V_p follows the plot displayed in Fig. 5. However, the waveform near $V_p = 0$ deviates from zero because of the finite resistance of the transistors, as displayed in Fig. 4(b). Notably, a distinction is observed between R_{on} and R_{di} in the A and B portion of Fig. 4(b). Considering this scenario, the circuit equations were obtained as follows:

[Mode A] "Q1 and Q3" are in the on state, and the current flows through two MOSFETs and excludes E_p. Therefore, the circuit equation is expressed in (1):

$$0 = V_p + 2R_{on}I_p \tag{1}$$

[Mode B] Q3 is switched off, and the current flows through the body diode of Q3. Thereafter, the diode characteristics are expressed in (2) using a linear approximation, where V_{di}, I_{di},

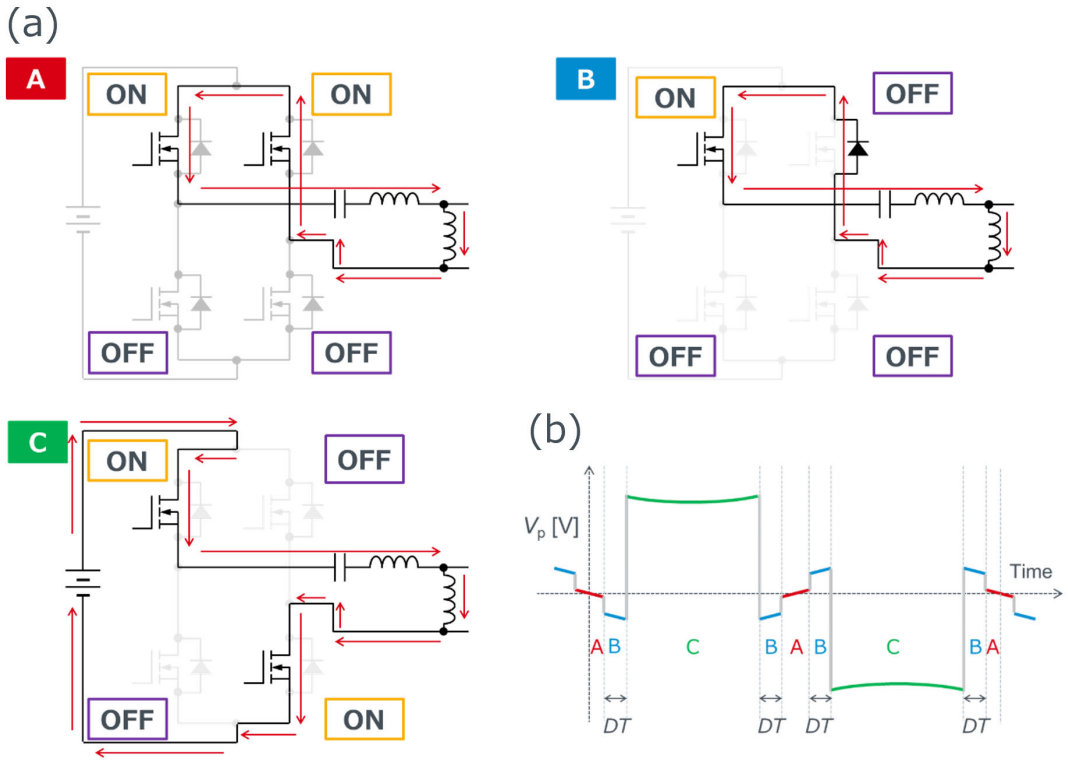

FIGURE 4. (a) Current flows in the first three operation modes of the WPT system with the on/off state of the switching devices; (b) image of the V_p waveform with phase shift control, emphasizing the effect of the conduction resistance of the switching devices.

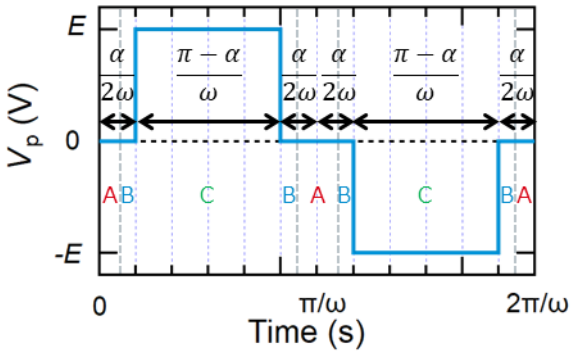

FIGURE 5. Ideal V_p waveform in phase-shift control.

and V_{f0} denote the voltage between the anode and cathode of the diode, diode current, and diode threshold voltage, respectively.

$$I_{di} = \frac{1}{R_{di}}(V_{di} - V_{f0}) \qquad (V_{di} > V_{f0}) \tag{2}$$

Therefore, the circuit equation is expressed in (3)

$$0 = V_p + (R_{on} + R_{di})I_p + V_{f0} \tag{3}$$

[Mode C] Q4 is switched on, and the current flows through the two MOSFETs: Q1 and Q4. Consequently, the power supply is connected to the current path, and the circuit equation is expressed in (4):

$$E_p = V_p + 2R_{on}I_p \tag{4}$$

The V_p waveform was obtained from the assembly of modes A, B, and C, and its inverted signature version of the voltage was obtained. The durations of modes A and B were determined using the phase-shift angle (α) and DT, whereas the duration of mode C was determined using α. Modes A and C were affected by only R_{on}, whereas mode B was influenced by both $R_r mon$ and R_{di}. Generally, R_{di} is larger than R_{on}, and the voltage variation in V_p is larger in mode B than in mode A, as indicated in Fig. 4(b).

The turn-on characteristics of the left leg comprising Q1 and Q2 contributed to the variations in V_p from 0 to E_p or $-E_p$, whereas the right leg comprising Q3 and Q4 contributed to the variations in V_p from E_p or $-E_p$ to 0. Hereinafter, the left and right legs are referred to as the rise leg and fall leg, respectively.

III. SIMULATION

The FFT results of V_p, simulated with DT values of 500 ns (blue curve) and 250 ns (purple curve), are presented in Fig. 6. In this simulation, the DT for the gate pulse was set following the stated described herein. As the harmonic components vary significantly with the pulse width of V_p, determined by the phase-shift angle (α), the pulse width of V_p must be set even if DT is altered. As described in Section II, the variations in V_p from 0 to E_p or $-E_p$ were determined by the turn-on characteristics of the switching device in the rise leg, whereas those from E_p or $-E_p$ to 0 were evaluated based on the turn-off characteristics of the switching device in the

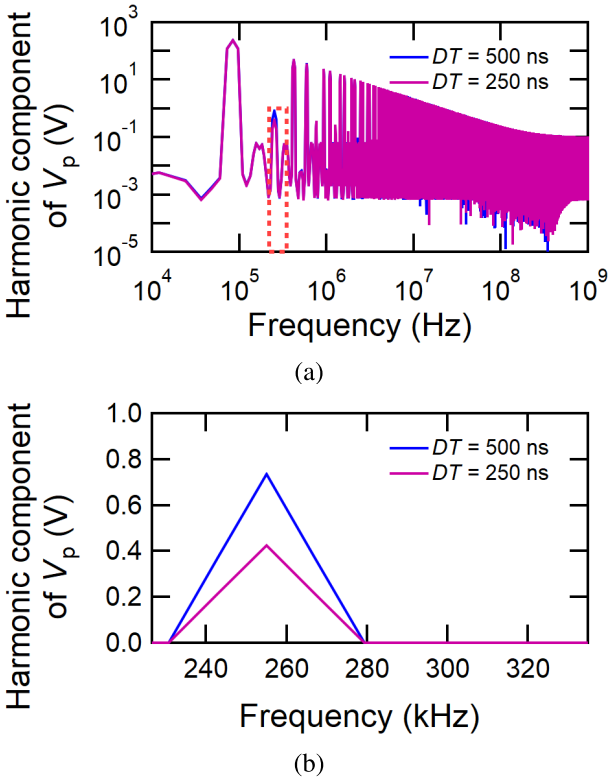

FIGURE 6. Simulated harmonic component of V_p with $DT = 250$ ns and 500 ns (a) up to 1 GHz and (b) around 3rd harmonic.

fall leg. Therefore, the rise duration of the rise leg and the fall period of the fall leg must be set. In addition, DT was set by reducing the gate signal of each leg on the opposite side of the fixed side. This DT setting method is also employed in the experiments described below.

Here, the DT setting was employed, and α was set to $\pi/3$ in this circuit simulation. Although the standard phase-shift theory predicted that the third-order harmonic component of V_p at $3f = 255$kHz should be zero, it was not zero for the simulation conducted in this section. This result suggests that the theory should be revised. Moreover, in Fig. 6, even though the pulse width is set such that it does not change with DT, it can be confirmed that the third harmonic varies with the DT.

We explained the reason for the dependence on DT (Fig. 6).

IV. FORMULATION AND PROPOSED METHOD

A. CONVENTIONAL FORMULATION OF THE DEPENDENCE OF THE HARMONIC COMPONENTS

In the conventional $V_{p,ideal}$ waveform using phase shift control without considering device characteristics, as shown in Fig. 5, $V_{p,ideal} = 0$ for Modes A and B, and $V_{p,ideal} = E$ or $-E$ for Mode C. Therefore, $V_{p,ideal}$, with phase-shift control, was expressed as the Fourier series containing the n-th harmonics, where n denotes a non-negative integer. $V_{p,ideal}$ represents an odd function, and $n = 2k - 1$ (where k is also a nonnegative integer) is sufficient for constructing the Fourier series of $V_{p,ideal}$, which eventually derives into (5) [29].

$$V_{p,ideal} = \sum_{k=1}^{\infty} \frac{4E}{(2k-1)\pi} \cos\frac{(2k-1)\alpha}{2} \sin(2k-1)\omega t \quad (5)$$

As seen in (5), for the conventional $V_{p,ideal}$, when $\alpha = \pi/(2k-1)$, the nth-order harmonics of V_p is zero.

B. PROPOSED FORMULATION OF THE DEPENDENCE OF THE HARMONIC COMPONENTS

However, as described below, when $\alpha = \pi/3$ in the experiment, the third-order harmonics of V_p do not equal 0. Since one of the factors contributing to this difference was considered to be the effect of device conduction resistance, we used (1), (3), and (4), which account for the device conduction resistance, to derive the Fourier series of V_p. As depicted in Fig. 3, V_p denotes an odd function; therefore, it is adequate to consider the half cycle for the Fourier expansion. Based on (1), (3), and (4), V_p is expressed as follows:

$$V_p = \begin{cases} -2R_{on}I_p & 0 \le t < \dfrac{\alpha}{2\omega} - DT \\ -(R_{on}+R_{di})I_p - V_{f0} & \dfrac{\alpha}{2\omega} - DT \le t < \dfrac{\alpha}{2\omega} \\ E_p - 2R_{on}I_p & \dfrac{\alpha}{2\omega} \le t < \dfrac{2\pi-\alpha}{2\omega} \\ -(R_{on}+R_{di})I_p - V_{f0} & \dfrac{2\pi-\alpha}{2\omega} \le t < \dfrac{2\pi-\alpha}{2\omega} + DT \\ -2R_{on}I_p & \dfrac{2\pi-\alpha}{2\omega} + DT \le t < \dfrac{\pi}{\omega} \end{cases} \quad (6)$$

I_p is approximately expressed as a sine wave. If I_0 and θ denote the amplitude of I_p and the phase deviation angle between V_p and I_p, respectively, then

$$I_p = I_0 \sin(\omega t - \theta). \quad (7)$$

The n-th harmonic component in the Fourier series of V_p ($V_{pJ}^{(n)}$) is expressed in (8)–(13), where"J" denotes operation mode A, B, or C. In (8), $|X|$ indicates the absolute value of X. As expressed in (9)–(13), only the terms including $\cos\frac{(2k-1)\alpha}{2}$ vanish for $\alpha = \pi/(2k-1)$. Therefore, unlike the ideal case represented in (5), $\alpha = \pi/(2k-1)$ generated nonzero terms, several of which include DT in (9) and (10).

$$V_p^{(n)} = \left| V_{pA}^{(n)} + V_{pB}^{(n)} + V_{pC}^{(n)} \right| \quad (8)$$

$$V_{pA}^{(n)} = A\cos\theta \left[\frac{1}{k-1} \sin\{(k-1)(\alpha - 2\omega DT)\} - \frac{1}{k} \sin\{k(\alpha - 2\omega DT)\} \right] \quad (9)$$

$$V_{pB}^{(n)} = B\cos\theta \left[-\frac{1}{k-1} \sin\{(k-1)(\alpha - 2\omega DT)\} + \frac{1}{k} \sin\{k(\alpha - 2\omega DT)\} + \frac{1}{k-1} \sin\{(k-1)\alpha\} - \frac{1}{k} \sin(k\alpha) \right]$$

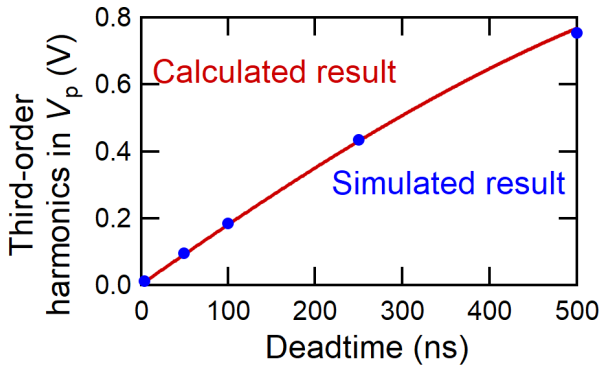

FIGURE 7. Dead time dependence of the third-order harmonic ($V_p^{(3)}$).

$$+\frac{4V_{f0}}{(2k-1)\pi}\left\{\cos(2k-1)(\omega DT-\frac{\alpha}{2})-\cos(2k-1)\frac{\alpha}{2}\right\} \quad (10)$$

$$V_{pC}^{(n)}=\frac{4E_p}{(2k-1)\pi}\cos(2k-1)\frac{\alpha}{2}-A\cos\theta\left\{\frac{1}{k-1}\sin(k-1)\alpha-\frac{1}{k}\sin k\alpha\right\} \quad (11)$$

$$A=\frac{2R_{on}I_o}{\pi} \quad (12)$$

$$B=\frac{(R_{on}+R_{di})I_o}{\pi} \quad (13)$$

From (9) – (11), the term including DT in (9) and (10) becomes 0 under the following two conditions: $DT = 0$ and $A = B$ and $V_{f0} = 0$. The first condition means no mode B period, and mode A continues without a step near 0 V, as shown in Figure 4(b). The second condition means that the voltage drop in modes A and B is equal, and there is no step between them in Figure 4(b). Thus, the residual harmonics are caused by the presence of a dead time in Mode B and the steps in the waveform near 0 V caused by the change in conduction resistance during the dead time.

C. METHOD FOR SUPPRESSING THE HARMONIC COMPONENTS

In Fig. 7, the influence of DT on $V_p^{(3)}$, characterized using (8)-(13) and the simulated results for $DT = 5$, 50, 100, 250, and 500 ns using the simulation circuit described in Section III are plotted as a red line and blue marker, respectively. Fig. 7 shows that the theoretical calculation results correlate well with the simulation results. Moreover, $V_p^{(3)}$ monotonically increases for $DT = 0-500$ ns. To reduce $V_p^{(3)}$, $DT = 0$ ns is preferable; however, this condition causes a short circuit in practice. Therefore, when operated under conditions considering short-circuit protection, DT generates a specific number of harmonics. Then, the harmonics are minimized when set at the lower limit of the DT value required for short-circuit protection.

Fig. 8 clarifies the relationship between the dead time and the harmonics in more detail by showing the DT dependence

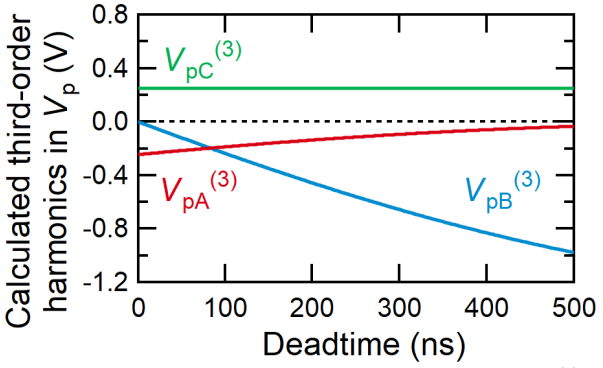

FIGURE 8. Dead time dependence of the third-order harmonics: $V_{pA}^{(3)}$, $V_{pB}^{(3)}$, and $V_{pC}^{(3)}$.

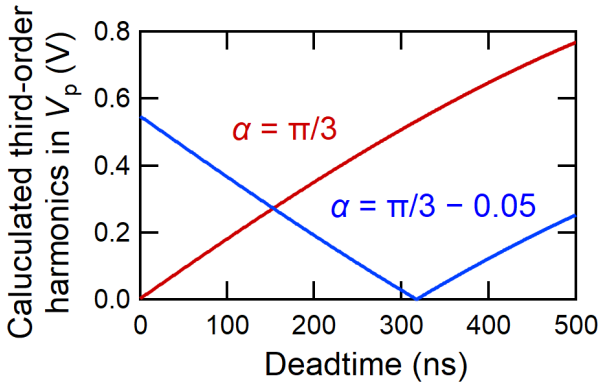

FIGURE 9. Variance in the dead time dependence with α.

of the components of $V_p^{(3)}$–$V_{pA}^{(3)}$, $V_{pB}^{(3)}$, and $V_{pC}^{(3)}$–. The mode categories shown in Fig. 4 and Equations (8)–(13) show that $V_{pA}^{(3)}$, $V_{pB}^{(3)}$, and $V_{pC}^{(3)}$ are related to the R_{on} of the MOSFET, diode conduction resistance, and phase-shift angle (α), respectively. As observed in Fig. 8, $V_{pA}^{(3)}$ and $V_{pB}^{(3)}$ are negative but depend on DT, whereas $V_{pC}^{(3)}$ is positive and almost independent of DT. More specifically, $V_{pA}^{(3)}$ and $V_{pB}^{(3)}$ are not freely adjusted because they depended on the device characteristics: R_{on} and the conduction resistance of the diode. Therefore, $V_{pC}^{(3)}$ is an appropriate candidate for reducing $V_p^{(3)}$, and it can be adjusted using α, as indicated in Eq. (11).

The variations in $V_p^{(3)}$ as a function of DT by setting α in the simulation are presented in Fig. 9, wherein the calculated DT dependence of $V_p^{(3)}$ at $\alpha = \pi/3$ is expressed as a red line and that at $\alpha = \pi/3 - 0.05$ is expressed as a blue line. This finding signifies that $V_p^{(3)}$ can be appropriately minimized using α and DT within a realistic range.

V. EVALUATION

Furthermore, we conducted experiments to confirm the calculated results obtained in Section IV-C. The same experimental circuit depicted in Fig. 2 was employed. The inverter circuit and the transmission coils employed are presented in

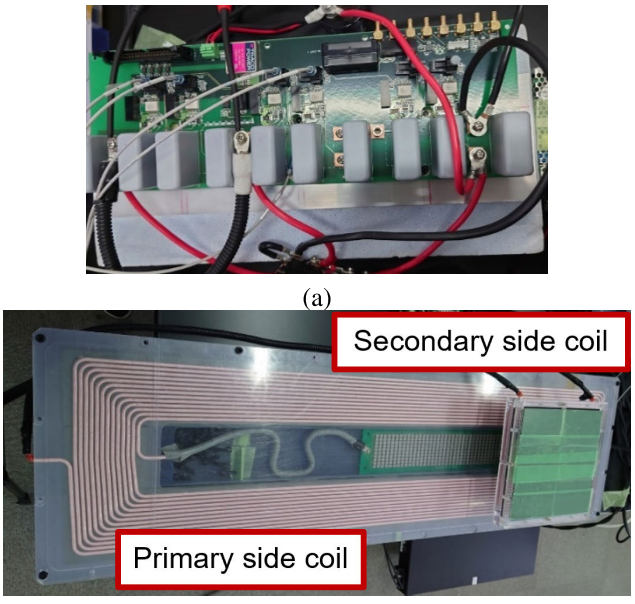

FIGURE 10. Measurement setup:(a) full bridge inverter and (b) transmission coils.

TABLE 2. List of parameters for measurement.

Symbol	Value	Symbol	Value
L_p	219.54 μH	P	3 kW
L_s	85.29 μH	E_p	210 V
M	19.87 μH	E_s	210 V
C_p	14.6 nF	R_g	4.7 Ω
C_s	33.3 nF	f	83.35 kHz
R_p	68.9 mΩ	α	$\pi/3$ rad
R_s	25.1 mΩ		

Figs. 10 (a) and (b), respectively. The circuit parameters are listed in Table 2, where P denotes the transmission power at the coil. In addition, two transfer-molded modules were employed in a half-bridge configuration with four SiC bare dies S4103 (ROHM) in parallel on one arm. An oscilloscope MSO58 with high-voltage differential probes TMDP0200 and current probes TCP0150 (Tektronix) was employed as the measurement equipment. The gate signal was generated by PE Expert4 (Myway plus), and the power supply was provided by biATLAS HBPS-A2D525-502 (headspring). Fig. 1, in Section I, shows the results of a 10 m-radiated emission test in an electromagnetic anechoic chamber, using the same experiment described in this section with $\alpha = 0$.

V_p was measured at several DT values. The experimental DT inevitably deviated from the set value because of a nonnegligible delay in the field-programmable gate array (FPGA) used to generate the timing signals for gate driving. Accordingly, the DT values were extracted from the measured waveforms. In the current experiment, the DT values were 135, 300, 430, and 600 ns. The method for setting the DT in the gate pulse was the same as that in the simulation described in Section III.

The measured V_{gs}, V_p, and I_p waveforms generated under the aforementioned DT conditions are illustrated in Fig. 11, which displays only the V_{gs} waveform for DT set to 430 ns.

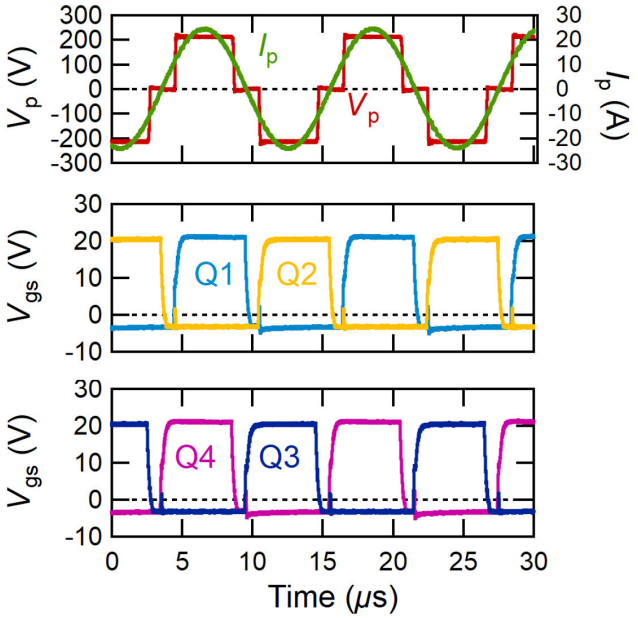

FIGURE 11. Waveforms of the gate-source voltage in each leg, V_p, and I_p.

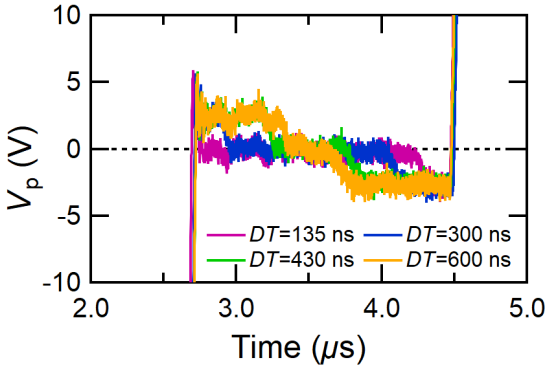

FIGURE 12. Waveforms of V_p around dead time for circuit operations with various dead times.

The V_p and I_p waveforms with all the DT values overlap. The results demonstrate that the pulse width of the V_p remains unaltered, regardless of the DT value. In the experiment, α was set to $\pi/3$. However, it is not exactly $\pi/3$ due to the switching characteristics and the FPGA clock. In this measurement, α was $\pi/3-0.05$ from the measured waveform shown in Fig. 11 described above.

A comparison of the V_p waveforms with various DT values around $V_p = 0$ V is presented in Fig. 12, where the V_p waveforms around the DT region exhibit various shapes depending on the DT value.

The FFT results of the experimental V_p waveform with various DT values up to 10 MHz and around the third order harmonics are shown in Fig. 13(a) and (b), respectively, and the influence of the DT on the third-order harmonic is shown in Fig. 13(c). Fig. 13(c) also shows the dead time dependence of harmonics from theoretical calculations at $\alpha = \pi/3-0.05$, which was the phase shift angle in the measurement.

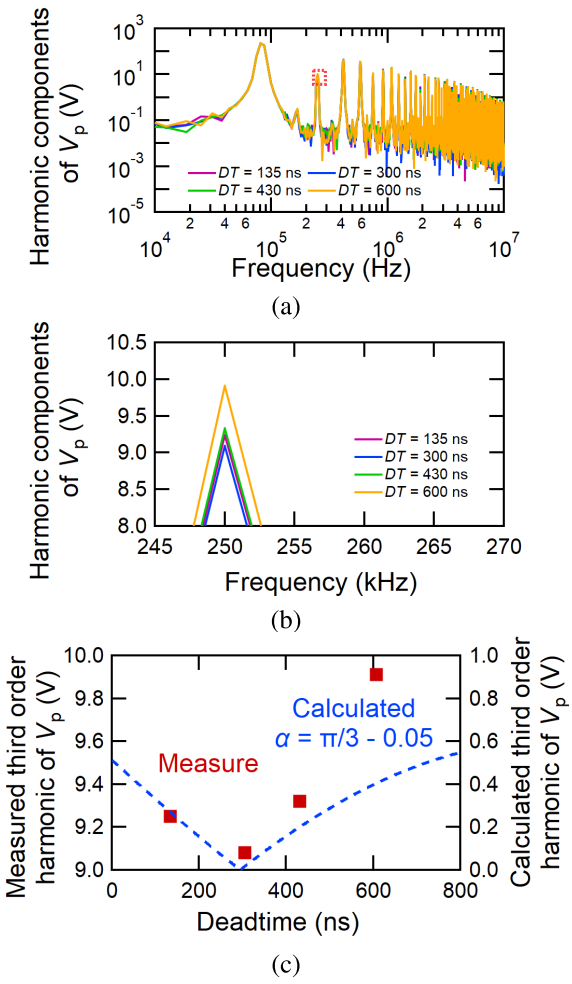

FIGURE 13. Comparison of the FFT results at the third-order harmonic for the experimental waveforms with various dead times (a) up to 10 MHz and (b) around the third-order harmonic; (c) dead time dependence of the third-order harmonic.

Figs. 13(a) and (b) show that the FFT results of the measured waveforms indicate that the third-order harmonics have dead-time dependence, as in the theoretical calculation. Fig. 13(c) shows that the harmonics reach a minimum value at DT, which is close to the theoretical calculation. Furthermore, the harmonics increase before and after the minimum value. Furthermore, two points of difference occur when comparing the measured and calculated results in Fig. 13(c). First, the dead-time-dependence slope of the harmonics differs. This result indicates that the diode resistances determining the dead-time dependence vary. The reason is that in the theoretical equation, a linear functional equation that considers the threshold value approximates the diode model. A more accurate calculation would require a more complex diode model. Second, the dead-time dependence of harmonics in the experiments has been confirmed to be approximately 9 V, even at the minimum value. This result is due to the effect of the switching characteristics of the device, which is not considered in the current theoretical equation; however, we are considering this as an area for further studies.

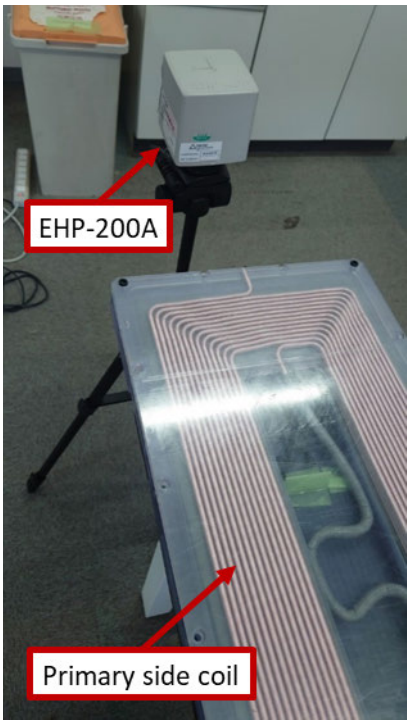

FIGURE 14. Setup for magnetic field leakage measurement.

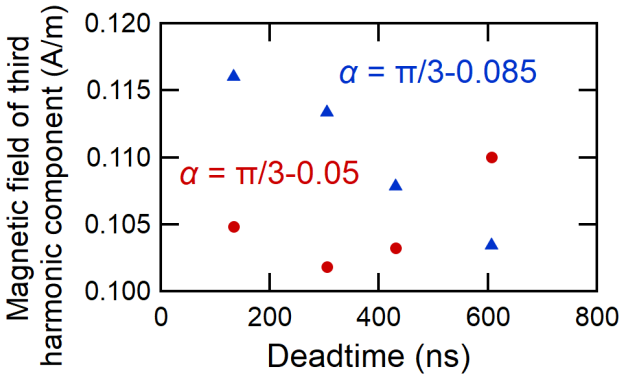

FIGURE 15. The measured *DT* dependence of the magnetic field leakage.

Finally, B_{leak} was measured by placing the EHP-200A (NARDA) equipment around the primary coil to minimize the influence of the magnetic fields from other components, as illustrated in Fig. 14. The *DT* dependences of the magnetic field leakage were measured at $\alpha = \pi/3$ and $\alpha = \pi/3 - 0.035$, which are displayed in Fig. 15 as red and blue dots, respectively. According to the FFT results of the experimental V_p, B_{leak} at $\alpha = \pi/3$ was minimized for a *DT* of 300 ns. More importantly, the results of the shifted α validated the theoretical analysis in Section IV-C because the measurement results shifted toward the right, as predicted in Fig. 9.

The experimental results show that harmonics and leakage magnetic fields caused by conduction resistance are dead-time dependent and can be reduced by adjusting the phase-shift angle at a realistic dead-time value without a short circuit. However, this method is unsuitable for cases where a significant reduction in harmonics is desired because the

harmonics due to dead time are not sufficiently large. Furthermore, two problems remain with the proposed method. First, since the diode characteristics are approximated linearly in the equation, the quantitative accuracy of the dead-time dependence is low. Second, switching characteristics are not considered device characteristics, and the harmonics resulting from this cannot be discussed. As a future study, the theoretical equation should be improved to improve the quantitative accuracy. Furthermore, the effect of the switching characteristics should be analyzed to clarify the generation factors of the harmonics that remained even after the suppression by the proposed suppression method.

VI. CONCLUSION

This study reveals that one of the causes of the nonzero harmonic components in phase-shift-controlled WPT inverters is the influence of the power device characteristics. Specifically, we found that the harmonics are caused by the distortion of the inverter output voltage (V_p) due to the change in the conduction resistance of the transistor during the DT period. The Fourier series expansion of V_p considering the transistor operation mode in DT highlights the DT dependence of V_p. Therefore, by exploiting this dependence and adjusting the phase-shift angle (α), the DT at which the amplitude of the harmonics of V_p is minimized can be set within a practical range. To confirm these theoretical results, V_p and the magnetic field leakage were measured during the WPT operation, finally confirming the theoretical predictions experimentally.

This study reveals the mechanism of dead-time-dependent harmonics. In high power transmission applications, such as those for EVs, reduction of magnetic leakage field is required, and consideration of harmonic components is also essential. Although the effect of reducing magnetic leakage field by adjusting the dead time is small, the proposed method is effective for realizing safer WPT systems. Moreover, in the future, the dead-time-dependent harmonics are considered to increase due to the longer dead-time caused by the higher output of WPT systems and the increase in the difference in the resistance values in the forward and reverse directions caused by the increased integration of devices. Therefore, this result will contribute to the future evolution of WPT systems and power devices.

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