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APPLIED RESEARCH

A Low-Phase-Noise and Area-Efficient Quad-Core VCO Based on Stacked Two-Port Inductors

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ABSTRACT In this paper, a quad-core oscillator is presented, which exploits a novel stacked two-port inductor topology to couple four oscillator cores. The topology guarantees excellent low-phase-noise performance, while overcoming the drawbacks of multi-core oscillators in terms of power consumption and silicon area occupation. Three different 19.125-GHz quad-core VCOs were designed in a fully depleted silicon on insulator CMOS technology to demonstrate the high design flexibility of the proposed solution that allows power consumption and area occupation to be traded off according to the specific requirements. Although the quad-core VCO design was aimed at 77-GHz automotive radar, the proposed topology can be profitably exploited in RF/mm-wave wireless communication systems.

INDEX TERMS CMOS integrated circuits, fully depleted silicon on insulator, stacked inductors, FD-SOI, phase noise, quad-core oscillator.

I. INTRODUCTION

Radio frequency (RF) and mm-wave applications, such as radar (radio detecting and ranging) and 5G, require the generation of frequency-modulated signals that are typically realized by a voltage-controlled oscillator (VCO), driven by a modulator, inside a phase-locked-loop (PLL). The VCO is the key block, especially in applications needing stringent phase noise performance. For instance, accuracy and resolution of a radar sensor are strictly related to the phase noise, thus a low-phase-noise oscillator is mandatory to achieve the highest possible target discrimination [1], [2]. In this context, LC resonant VCOs are highly preferred at the cost of a large silicon area consumption, mainly due to the tank inductor [3]. Traditionally, RF/mm-wave ICs are implemented in BiCMOS or CMOS technologies [4], [5], [6], [7], [8], [9], [10], [11]. Despite several advantages of BiCMOS over CMOS in terms of noise (i.e., lower flicker noise corners), thicker back-end-of-line (BEOL) [13], higher transistor breakdown voltage (BV), and higher transconductance, g_m, at a given current level, CMOS is becoming the reference process since it is highly suitable for system-on-chip (SoC) integration, which is pursued by microelectronic industries to reduce chip cost and size [14] Unfortunately, the transition from BiCMOS to CMOS affected IC design for almost all main RF/mm-wave front-end blocks [15]. In the last few years, several techniques have been developed to minimize phase noise and improve the overall performance of CMOS VCOs. Specifically, *multi-core* techniques that consist in coupling multiple in-phase oscillators, are theoretically powerful solutions for CMOS low-phase-noise VCO design. However, current implementations achieved significant reduction of the phase noise at the expense of power and/or silicon area consumption, which have hindered their exploitation in actual applications. This paper presents a recently patented multi-core oscillator topology [16] that allows phase-noise to be minimized, while trading-off power and area consumption according to the specs of the application.

This paper is organized as follows. A brief review of phase noise theory is provided in Section II to introduce the

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advantages of the multi-core technique. Section III presents an overview of current state-of-the-art quad-core oscillator implementations. In Section IV, the proposed quad-core topology is described. Section V presents the quad-core oscillator design in a 28-nm fully depleted silicon on insulator (FD-SOI) CMOS technology, along with a comparison with state-of-the-art quad-core solutions. Finally, the main conclusions are drawn in Section VI.

II. PHASE NOISE REVIEW AND MULTI-CORE VCOs

According to the well-known Leeson-Cutler model the phase noise can be expressed as follows [17] and [18]

$$\mathcal{L}(\Delta f) = 10 \cdot \log \left\{ \frac{2FkT}{P_{osc}} \left[1 + \left(\frac{f_0}{2Q_T \Delta f} \right)^2 \right] \left(1 + \frac{\Delta f_c}{|\Delta f|} \right) \right\} \tag{1}$$

where F is an empirical parameter called *device excess noise number*, which accounts for the active device noise and how it is upconverted, k is Boltzmann constant, T is the absolute temperature, P_{osc} is the average oscillator output power, f_0 is the oscillation frequency, Δf is the offset frequency with respect to the carrier, Q_{T} is the tank quality factor and Δf_{c} is the offset corner frequency between the $1/f^3$ (flicker) and $1/f^2$ (thermal) phase noise regions [19]. Some effective design considerations can be made by simplifying (1) in the thermal phase noise region, while expressing the oscillation output power, P_{osc}, in terms of the output voltage amplitude, A_0, and the tank equivalent parallel loss resistance, R_{p}, thus resulting in the following equation.

$$L(\Delta f) = 10 \cdot \log \left[\frac{FkT}{A_0^2} \frac{R_p}{Q_T^2} \left(\frac{f_0}{\Delta f} \right)^2 \right] \tag{2}$$

According to (2), the phase noise decreases with the square of the output amplitude, A_0, which is in contrast with the supply voltage reduction trend of nanometer CMOS technologies. Moreover, CMOS transistors exhibit worse F factor values compared to bipolar ones. The working frequency, f_0, has also a significant influence on the parameters of (2), thus indirectly affecting phase noise performance, as in-depth analyzed in [20]. Lastly, the ratio $R_{\text{P}}/Q_{\text{T}}^2$ must be minimized, which is the main target of the proposed work. It can be easily further expressed as follows,

$$\frac{R_{\text{p}}}{Q_{\text{T}}^2} = \frac{\omega_0 Q_{\text{T}} L}{Q_{\text{T}}^2} = \frac{\omega_0 L}{Q_{\text{T}}} \tag{3}$$

to highlight that specifically the L/Q_{T} ratio has to be minimized. Thus, the best design strategy for phase noise minimization is to use low inductance values, while maintaining a sufficiently high tank quality factor, Q_{T}. On the other hand, according to (3), low inductance values also imply low R_{p} values (i.e., higher losses in the tank), which means that optimizing the phase noise performance is at odds with power consumption optimization.

Unfortunately, since the quality factor of a spiral inductor degrades with its value, the L/Q_{T} ratio minimization design strategy requires a tradeoff between the inductance value, L, and the resulting tank quality factor, Q_{T}. Finally, other two aspects must be kept in mind. First, an excessively low inductance value would be highly susceptible to the parasitic inductances of the layout path connections. Second, given the operating frequency, as inductance decreases the overall required capacitance increases, which would have intrinsically a lower quality factor, Q_{C} with a consequent Q_{T} degradation. Given the integration technology, these constraints set a limit to the minimum phase noise that a single oscillator can achieve.

An effective way to pursue the L/Q_{T} ratio minimization design strategy is adopting a *multi-core technique*. It consists in coupling multiple oscillators together, by connecting them through a generic impedance network, so that their output voltages are in phase. Each single oscillator is called *core*; hence the whole oscillator takes the name of multi-core oscillator. In an ideal coupled system, at steady state, no current flows through the coupling network, and all outputs are virtually shorted. This virtual short is not physically implemented. Rather, it is the consequence of the outputs being in phase. The coupling network can be resistive, capacitive, or inductive. In general, a complex impedance network can be realized. A thorough theoretical analysis on the different types of coupling and their impact on the oscillator performance is available in [21]. Two main guidelines must be followed to achieve a robust coupling design:

- The coupling impedance must be low-Q to guarantee enough suppression of undesired oscillation modes.
- The coupling impedance must be as low as possible to guarantee a strong coupling between the cores.

The effect of an ideal multi-core coupling on the oscillator phase noise can be easily analyzed as follows. Let us suppose having an initial oscillator using an inductance, L_1, a capacitance, C_1, with a tank quality factor, $Q_{\text{T},1}$. From (2), being $R_{P,1} = Q_{T,1}\sqrt{L_1/C_1}$, the phase noise of the initial oscillator can be written as follows.

$$\begin{aligned} \mathcal{L}(\Delta f)_1 &= 10 \log \left[\frac{FkT}{A_0^2} \frac{R_{P,1}}{Q_{T,1}^2} \left(\frac{f_0}{\Delta f} \right)^2 \right] \\ &= 10 \cdot \log \left[\frac{FkT}{A_0^2 Q_{\text{T},1}} \sqrt{\frac{L_1}{C_1}} \left(\frac{f_0}{\Delta f} \right)^2 \right] \end{aligned} \tag{4}$$

When two identical oscillators are coupled (i.e., dual-core oscillator), the tank impedances are connected in parallel, which leads to an equivalent inductance, $L_{1,2}$, and an equivalent capacitance, $C_{1,2}$, halved and doubled in comparison with L_1 and C_1, respectively. Since the equivalent tank quality factor, $Q_{\text{T},1,2}$, remains constant and equal to $Q_{\text{T},1}$, the phase noise of the dual-core oscillator is ideally halved, as calculated in (5).

$$\mathcal{L}(\Delta f)_{1,2} = 10 \cdot \log \left[\frac{FkT}{A_0^2 Q_{\text{T},1}} \sqrt{\frac{L_{1,2}}{C_{1,2}}} \left(\frac{f_0}{\Delta f} \right)^2 \right] = \frac{\mathcal{L}(\Delta f)_1}{2} \tag{5}$$

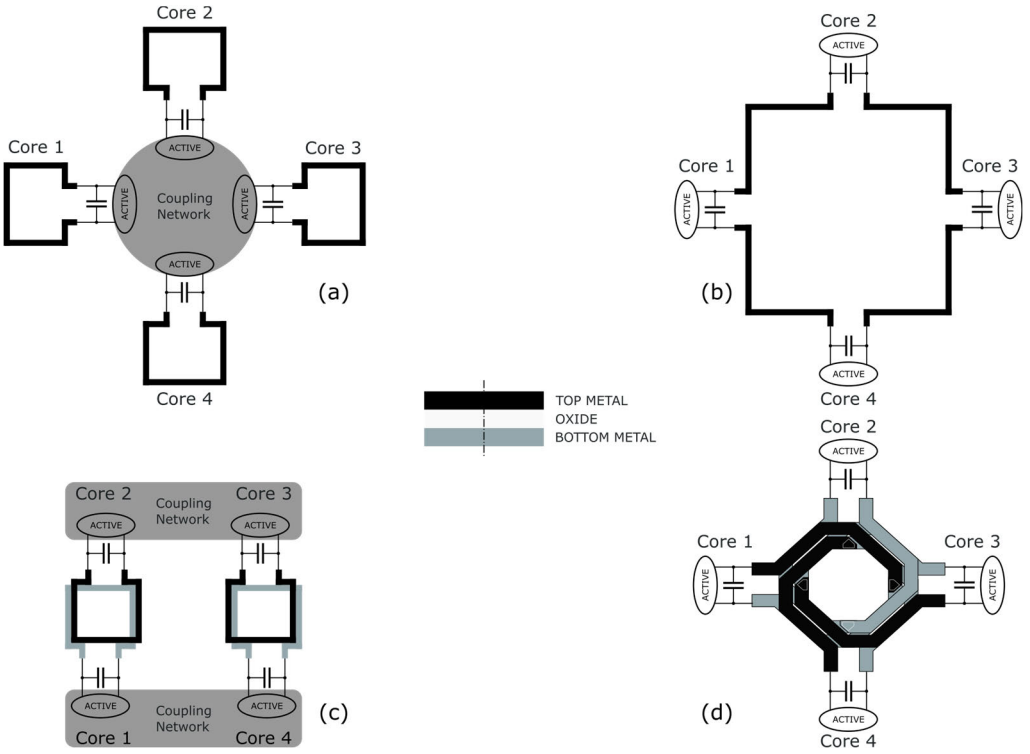

FIGURE 1. State-of-the-art implementations of RF/mm-wave quad-core oscillators: classical approach (a), multi-port inductor (b), stacked inductors (c), interstacked transformer (d) [30].

Therefore, the phase noise ideally decreases by a factor of two by coupling two identical cores. In general, coupling N identical cores allows ideally reducing the phase noise by a factor N. Equivalently, it can be said that coupling N cores lowers the phase noise of $10 \cdot \log(N)$ dBc/Hz. Approximately, a 3-dB reduction occurs every time the number of cores is doubled. It is worth mentioning that coupling between multiple cores allows for a parallel connection of their parasitics, as well. Thus, multi-core oscillators can achieve low inductance values with reduced impact of parasitics on the tank impedance.

Unfortunately, the multi-core technique has two serious drawbacks i.e., an increment by factor N of power consumption and silicon area occupation in comparison with the single oscillator core. Moreover, the higher the number of coupled cores, N, the higher the complexity of overall oscillator, which can degrade the phase-noise benefit. Therefore, quad-core solutions typically represent the optimum balance between reasonable complexity and remarkable phase noise reduction.

III. QUAD-CORE OSCILLATOR IMPLEMENTATIONS

This Section describes state-of-the-art implementations of RF/mm-wave quad-core oscillators, namely classical approaches, multi-port inductor, stacked inductors, and interstacked transformer represented in Fig. 1, while comparing pros and cons.

A. CLASSICAL APPROACH

A classical and simple method to implement a quad-core oscillator is to couple four cores, each one with its own inductor, by means of pure resistive network, as proposed in [22]. A centrosymmetric layout is adopted, where the active parts are placed in the central area and the inductors are spread apart as much as possible. This arrangement carries two main advantages. Firstly, coupling interconnections are easily realized and resistive paths minimized. Secondly, since inductors are spread apart, their magnetic coupling is reduced to a minimum, and this helps in minimizing proximity effect, which would inevitably lower inductor quality factors. The downside of this approach is the high area occupation. Such a classical approach is widely adopted thanks to its simplicity, but it is not suited to optimize and tradeoff the various oscillator performance parameters, such as the phase noise, the power consumption, and the silicon area occupation. On the other hand, the following two techniques (i.e., multiport inductor and stacked inductors) allow improving the tank Q-factor or reduce the VCO area consumption by adopting inductive coupling between cores by means of custom-made inductive structures.

B. MULTI-PORT INDUCTOR

Electromagnetic (EM) coupling between conductors produces increasing losses at higher frequencies due to the current crowding effect i.e., skin and proximity effect

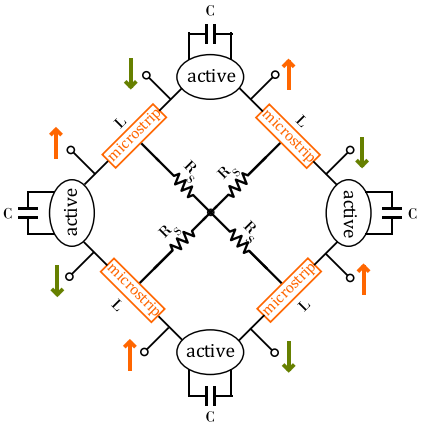

FIGURE 2. Circular geometry VCO exploiting a four-port inductor.

superimposition [23], [24], [25]. This phenomenon gets more accentuated as the EM coupling increases. Specifically, the proximity effect arises between the segments on the opposite sides of single-turn spiral inductors, typically used at mm-wave frequencies. As the inner diameter of the inductor is shrunk down, the increasing RF coupling between the traces reduces the inductor quality factor. For this reason, for low inductance levels, it would be more convenient to use microstrips in place of spiral inductors since they would not suffer from proximity effect and would have a higher Q-factor. However, for geometrical reasons, microstrips are rarely used in single-core integrated oscillators, as pointed out in [26].

On the other hand, multi-core oscillators allow the adoption of the so-called *circular geometry*, whose simplified scheme is shown in Fig. 2. This technique consists in connecting the VCO cores by means of microstrips in a circular configuration. The deriving inductive structure is a coil with four ports connected to the cores and can be regarded as a *four-port* inductor. The arrows in Fig. 2 show the phase of the voltage at the corresponding terminals for the desired mode of oscillation. Thanks to this arrangement, it is possible to increase the inner diameter at a given inductance level, thus resulting in a higher inductor Q-factor [21], [26], [27]. Compared to the classical approach, this inductor can be used in place of the four single coils whose diameter is four times smaller (i.e., lower quality factor). The EM coupling between cores is guaranteed by the inductive coupling and therefore no additional resistive network is needed. As shown in Fig. 2, the microstrips are connected in their middle points by means of high-resistance traces, R_S, to prevent latching and undesired oscillation modes that otherwise may occur. A *two-port* version of the *multi-port* inductor can be found in [28]. The constraint to avoid latching is $|G_M| < 2 / R_S$, where G_M is the conductance of the active part and R_S is the resistance of one of the high-resistance central traces. The choice of R_S value is a tradeoff between contrasting requirements. Indeed, it should be sufficiently small to prevent latching, but large enough to suppress the undesired oscillation modes.

TABLE 1. Multi-core oscillator techniques.

Multi-core technique	Advantages	Disadvantages
Classical approach	Low complexity	High area occupation
Multi-port inductors	Highest Q, undesired modes suppression	High area occupation
Stacked inductors	Low area occupation	Low Q
Interstacked transformer	Very low area and current consumption	Moderately high phase noise

C. STACKED INDUCTORS

The multi-port inductor approach is aimed at enhancing the inductor Q-factor to achieve both lower phase noise and power consumption. However, this is achieved at the cost of high area occupation without any significant advantages with respect to the classical approach. On the other hand, silicon area (along with power consumption) is often the parameter that limits the adoption of a circuit topology in a commercial product. A common practice to reduce area occupation is to use a stacked transformer as coupling network. Indeed, the magnetic coupling, k, between the stacked coils allows obtaining higher inductance values for the same area occupation. In other words, for a given inductance level, less silicon area is required. This advantage, though, is paid in terms of transformer winding Q-factor due to the current crowding, as pointed out earlier. An example of application of such a technique within a quad-core VCO is provided in [29], where two pairs of stacked coils are exploited to couple four cores.

D. INTERSTACKED TRANSFORMER

A recent implementation of quad-core oscillators was published in [30] and represented in Fig. 1(d). It is based on a high-k symmetric transformer configuration, namely interstacked, which has been mainly proposed for mm-wave frequency applications [31], [7]. Specifically, an interstacked transformer is made of two spirals of different metal layers, using complementary geometries for primary and secondary windings. Indeed, the outer (inner) spiral of primary winding is stacked to the outer (inner) spiral of the secondary winding and interleaved with the inner (outer) spiral of the secondary winding at the same time, thus exploiting both interleaved and stacked magnetic couplings [32]. The quad-core oscillator based on a four-port interstacked transformer shown in Fig. 1(d) can be considered an evolution of the stacked inductors solution described in Section III(c), enabling for lower area consumption and better winding Q-factor thanks to its higher magnetic coupling factor, k. As a recap, Table 1 reports advantages and disadvantages of the multi-core techniques seen so far.

IV. THE PROPOSED SOLUTION: STACKED TWO-PORT INDUCTORS

A new quad-core VCO topology is proposed, which is based on an original inductor structure [16]. The proposed solution

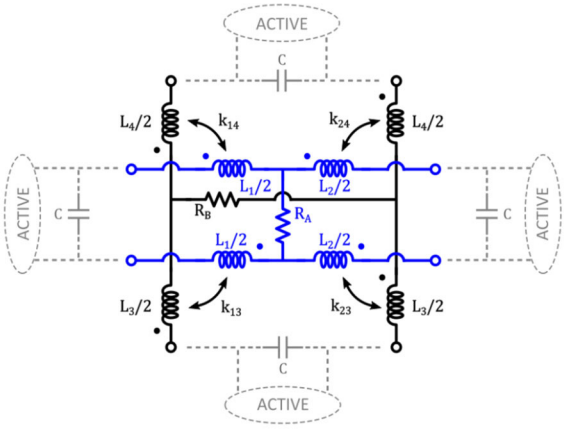

FIGURE 3. Proposed quad-core VCO solution using two magnetically coupled two-port inductors as coupling network.

enables the optimization of both the phase-noise and the power consumption, while trading off the silicon area occupation by means of a compact high-Q inductor. Indeed, the inductive part of the oscillator tank is the main responsible for both tank Q-factor and VCO area consumption, at the targeted working frequency, i.e., 20 GHz. The basic idea of the proposed solution is represented in the equivalent circuit shown in Fig. 3. A quad core VCO is formed by using two multi-port inductive structures, (represented in blue and black, respectively) that are magnetically coupled. In this way, it is possible to exploit the area-saving property of magnetic coupled structures and the Q-factor enhancement guaranteed by multi-port inductor approach, as well.

One of the possible implementations of such a solution is shown in Fig. 4(a), in which the two-port inductors are stacked on top of each other to maximize their magnetic coupling. To better understand the inductor layout, Figs. 4(b) and 4(c) show the two separate two-port inductors which the whole structure is made up with. These two-port inductors are a modified version of the two-port inductor in [28], properly adapted to be stacked for high magnetic coupling. No patterned ground shield (PGS) is implemented [33]. Figs. 4(b) and 4(c) also show the currents flow for the desired oscillation mode. Theoretical currents (in green) show that current cancellation occurs in the central path, resulting in a net currents flow (in red) through the wide high-Q traces. As a consequence, the central resistive trace has no impact on the desired oscillation mode performance. Conversely, the undesired modes generate a net current flow through it, resulting in a low-Q-factor operation.

Fig. 5 helps in understanding the different oscillation modes of the stacked two-port inductors. On the left-hand side of the picture, the voltage phases at each terminal are indicated, along with the flow of the currents for each of the four excitation modes. On the right-hand side of the picture, the current flow direction is represented (i.e., clockwise, or anticlockwise), thus highlighting if coupled currents are in-phase or out of phase.

In the first oscillation mode (i.e., mode 1 in Fig. 5(a)), all the net currents flow through the wide metal traces and in a clockwise direction that leads to a constructive magnetic coupling between the overlapping two-port inductors depicted in Figs. 4(b) and 4(c). All these factors together contribute to the high Q-factor associated with this oscillation mode that is the desired one for the quad-core VCO.

On the other hand, oscillation mode 2 shown in Fig. 5(b) is strongly asymmetric. Indeed, it is the only asymmetric excitation mode among them all. This means that the impedances seen at each port are different from each other. Furthermore, the net currents in one of the two-port inductors flow through the central low-Q metal path, resulting in a very low-Q oscillation mode.

Oscillation mode 3 represented in Fig. 5(c) is similar to mode 1. Indeed, current cancellation in the central trace occurs, and the net currents flow through the wide high-Q traces only. However, a destructive (out of phase) magnetic coupling between the two coils results in both a lower equivalent inductance and lower Q-factor.

Finally, oscillation mode 4 depicted in Fig. 5(d) exhibits the lowest Q-factor since both two-port inductors have net current flowing through the central trace.

As is well known, the VCO must have an appropriate nonlinear characteristic and satisfy the startup condition to produce stable oscillation. Specifically, the negative

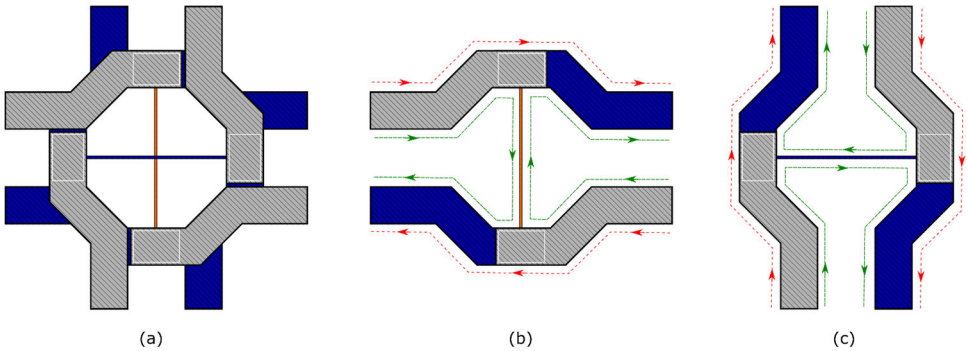

FIGURE 4. (a) Stacked two-port inductors (b-c) view of the two separate two-port inductors which the whole structure is made up with.

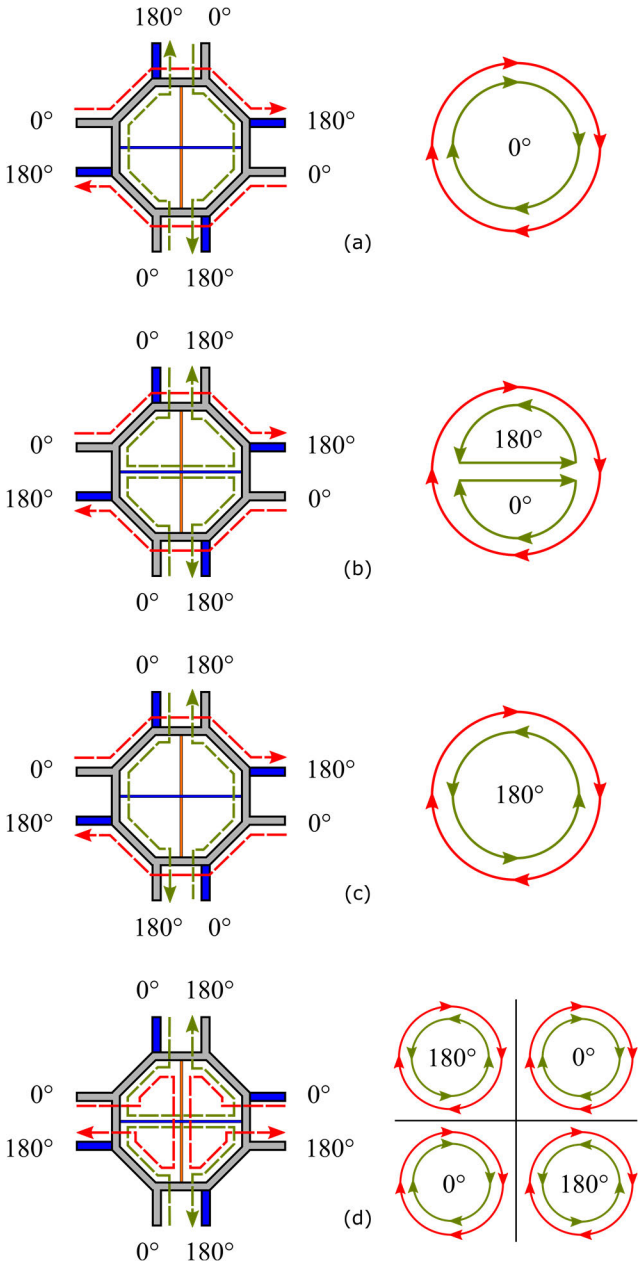

FIGURE 5. Oscillation mode representation. Currents and voltage phases on the left-hand side, phase difference between coupled currents on the right-hand side: (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4.

conductance provided by the active part must compensate for the *LC* tank losses, that is:

$$G_{\mathrm{A}}(0) < -\frac{1}{R_p} \tag{6}$$

where $G_A(0)$ is the active negative conductance evaluated at zero oscillation amplitude and is proportional to the transconductance g_m of the transistors, and R_p is the tank parallel loss resistance. In practical application a rule of thumb is sizing the active core to obtain a $G_A(0)$ at least twice the minimum value reported in (6). When different oscillation modes are physically possible, the oscillator will trigger on the mode

TABLE 2. Parameters of stacked two-port inductors.

Parameters	Small	Medium	Large
Inductance @ 19.125 GHz [pH]	50.4	80.2	112
Q-factor @ 19.125 [GHz]	17.8	24.1	28.8
Coil width [µm]	18	18	18
Inner diameter [µm]	44	71	96
Area [mm^2]	0.015	0.023	0.031

TABLE 3. Oscillation modes for stacked two-port inductors.

	Small		Medium		Large	
Mode	L [pH]	Q	L [pH]	Q	L [pH]	Q
1	50.4	17.8	80.2	24.1	112	28.8
2	-	-	-	-	-	-
3	26.2	12.4	33.2	13.5	40.0	13.9
4	105	4.74	162	6.58	231	6.84

with the highest Q-factor (mode 1 for the proposed structure), thus oscillating at the frequency associated with such mode and rejecting all the other ones.

In the following, a simplified analysis is reported to find a simple expression for both inductance and Q-factor seen at each port of the proposed structure for the dominant oscillation mode (i.e., mode 1). To this aim, let's consider the equivalent circuit of the stacked two-port inductor of Fig. 3 and calculate the impedance when all the in-phase terminals are connected, as shown in Fig. 6(a). It is possible to rearrange the components to visually declutter the connections, as shown in Fig. 6(b), while including the parasitic resistances (i.e., R_1, R_2, R_3, and R_4) of the wide high-Q traces to allow the calculation of the equivalent Q-factor. The layout implementation of the stacked two-port inductors in Fig. 4(a) is symmetric and thus the equivalent circuit in Fig. 6(b) can be further simplified by setting all inductances, resistances and magnetic coupling factors equal (i.e., $L_{1-4} = L$, $R_{1-4} = R$; $k_{14} = k_{13} = k_{23} = k_{24} = k$). Therefore, a symmetrical current distribution occurs in the schematic of Fig. 6(a) and the impedance seen at each of the four ports, Z_{in}, is simply equal to

$$Z_{\mathrm{in}} = 4\frac{V_0}{I} \tag{7}$$

while the equivalent inductance, L_{eq} and Q-factor, Q_{eq}, at each port can also be easily drawn as follows:

$$L_{\mathrm{eq}} = (1+k)L \tag{8}$$

$$Q_{\mathrm{eq}} = (1+k)\frac{\omega L}{R} \tag{9}$$

Although this topology generally results in slightly lower quality factors compared to the four-port inductor designed in [28], it significantly decreases the area occupation to a level comparable, or even better, to the one achieved in [29], where two pairs of stacked inductors are used.

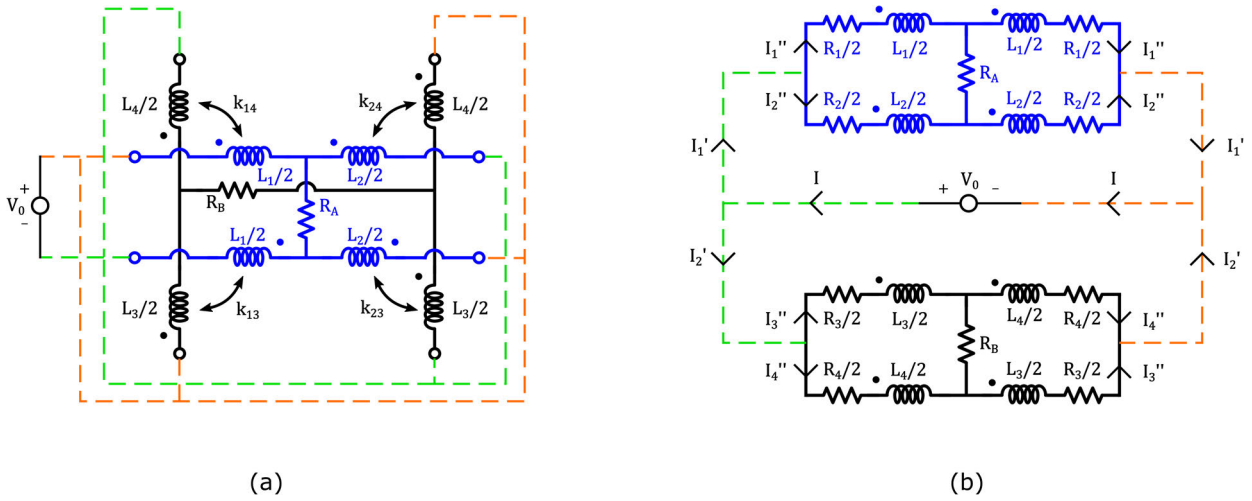

FIGURE 6. (a) Equivalent circuit of the stacked two port inductor for impedance calculation for oscillation mode 1; (b) rearranged equivalent circuit with parasitic resistances R_1, R_2, R_3, R_4.

V. QUAD-CORE VCO DESIGN BASED ON STACKED TWO-PORT INDUCTORS

Stacked two-port inductors were exploited in a 19.125-GHz quad-core VCO to be used in a narrowband 77-GHz CMOS radar system for automotive applications [14], [34], [35], [36], [37]. The VCO was designed in 28-nm fully depleted silicon on insulator (FD-SOI) CMOS technology by STMicroelectronics, providing low-V_T transistors, which exhibit a f_T as high as 270 GHz [38]. The process features a general-purpose BEOL with eight Cu-metal layers and a top aluminum one [13].

Three differently sized inductors were designed to search for the better trade-off among the VCO performance parameters, i.e., phase-noise, power consumption and silicon area. Table 2 reports the inductance and Q-factor seen at each port of the three inductors at the desired mode of oscillation, obtained by means of 2.5D EM simulations. Table 2 also contains the main geometrical parameters of the components. As expected, the higher the inductance the better the Q-factor. Hence, choosing an extremely low inductance with the purpose of minimizing phase noise may not be the best option, since the benefit of reaching a low inductance is cancelled by the poor Q-factor. Fig. 7 reports the frequency characteristics of small, medium and large inductors. The self-resonance frequency is beyond 100 GHz for all the designed structures. Let us note that the reported inductance value is the equivalent inductance seen at each port. Once the oscillation starts, the voltages at all the four ports are in phase and the impedances are virtually in parallel. Thus, the equivalent tank total inductance is a quarter of the ones reported in Fig. 7.

Since the proposed stacked two-port inductors can oscillate according to different modes, as discussed in Section IV, a dedicated analysis is required. Specifically, among the possible four oscillation modes reported in Fig. 5, mode 2 is inherently asymmetrical and therefore the analytical estimation of the impedances for each port is not straightforward.

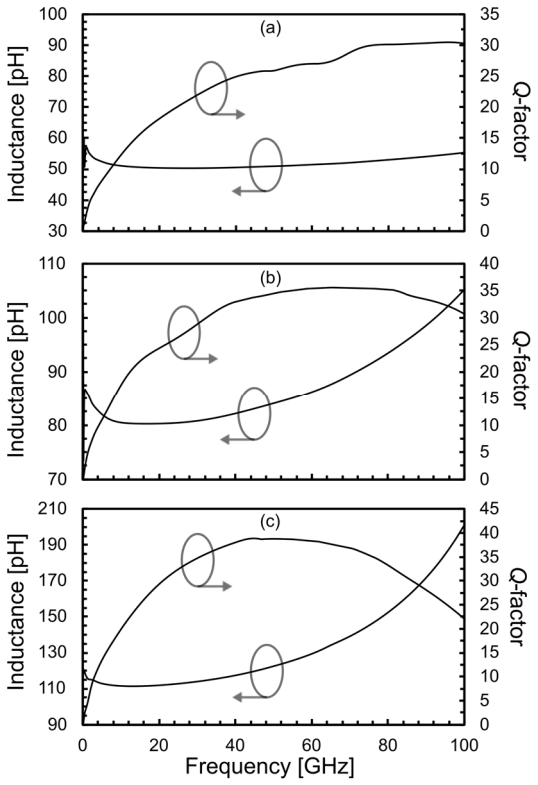

FIGURE 7. Inductance and Q-factor as a function of frequency for small (a), medium (b), and large (c) inductors.

However, mode 2 can be skipped in the analysis since the VCO will not reasonably trigger due to mode intrinsic asymmetry and consequently poor Q-factor (see the current flow in Fig. 5(b)). For the remaining oscillation modes, Table 3 reports the inductance and Q-factor, at 19.125 GHz, which further confirms that mode 1 is the dominant one.

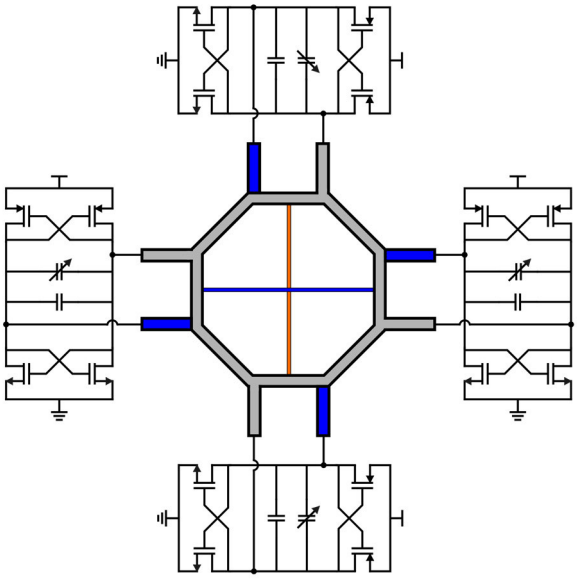

FIGURE 8. Schematic of the proposed quad-core VCO with stacked two-port inductor.

As far as the circuit topology is concerned, a complementary cross-coupled oscillator was adopted since it is well-suited to the proposed stacked two-port inductor, which is intrinsically asymmetrical and does not provide a center tap for the power supply. Moreover, no tail current was used to maximize the output voltage swing. Fig. 8 shows a complete schematic of the quad-core VCO. A supply voltage, V_{DD}, of 1.2 V was chosen. The quad-core VCO was designed by using the three inductive structures of Table 3 to look for the better trade-off among main oscillator performance parameters. The transconductance, g_m, of the cross-coupled transistors was set three times the minimum required one to guarantee Barkhausen criterion to obtain a robust startup along with achieving an oscillation amplitude of about 1 V. Finally, 63-nm and 90-nm channel lengths have been used for the PMOS and the NMOS transistors, respectively, to minimize the flicker and thermal noise, without excessively increasing their parasitic capacitances. The ratio $(W/L)_P$ / $(W/L)_N$ was chosen to set the dc output voltage at $V_{DD}/2$.

Fig. 9 shows the simplified layout floorplan of the proposed quad-core VCO, which highlights main connections of the stacked two-port inductors to transistors (gm), varactors, capacitors (MOM), power supply (VDD), ground (GND) and decoupling capacitors (decoupling cap). The layout has been developed to guarantee full symmetry for the four cores along with the minimization of RLC parasitics. Distributed power supply/ground planes are also used, thus obtaining a very compact layout with an overall area lower than 0.1 mm^2.

Achieved performances for the three designed quad-core oscillators are summarized in Table 4. They have been obtained by means of circuit simulations along with electromagnetic (EM) data of two-port stacked inductors along with main RLC layout parasitics (see Fig. 9) in order to fairly demonstrate the benefits of the proposed topology. The results are also compared in terms of well-known figures of merits (FoMs), whose expressions are reported below for the sake of clarity,

$$\mathrm{FoM} = \mathrm{PN} - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) + 10\log_{10}\left(P_{\mathrm{DC,mW}}\right), \tag{10}$$

TABLE 4. Simulated performance comparison of the quad-core VCOs.

	Small	Medium	Large
Technology	28-nm FD-SOI CMOS		
Frequency [GHz]	19.125		
Tuning range [%]	21	21	21
PN (*) @ 1 MHz [dBc/Hz]	−118.7	−118.7	−117.6
V_{DD} [V]	1.2	1.2	1.2
Current [mA]	62	27	18
Silicon area [mm^2]	0.08	0.09	0.105
FoM [dBc/Hz]	−185.6	−189.3	−189.8
FoM$_T$ [dBc/Hz]	−192.0	−195.7	−196.2
FoM$_A$ [dBc/Hz]	−196.6	−199.8	−199.7

(*) PN is normalized at 77 GHz.

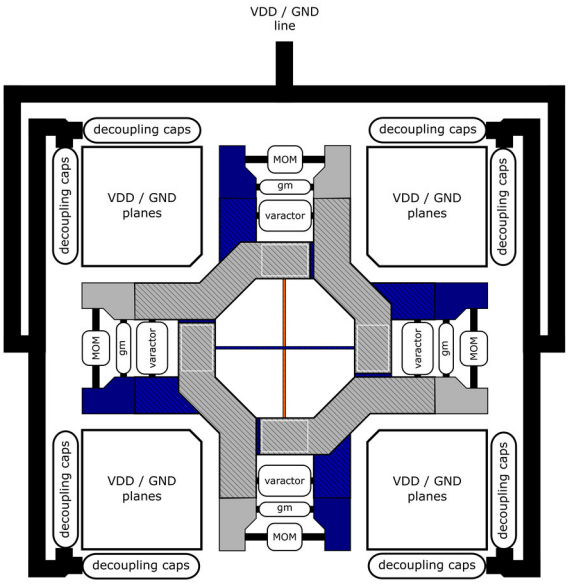

FIGURE 9. Simplified layout of the proposed quad-core VCOs with stacked two-port inductors.

TABLE 5. Corner analysis of the medium-size quad-core VCO.

	SSA	TYP	FFA
Frequency [GHz]	18.080	19.125	20.601
Current [mA]	24	27	29
PN @ 1 MHz [dBc/Hz]	−119.0	−118.7	−117.4

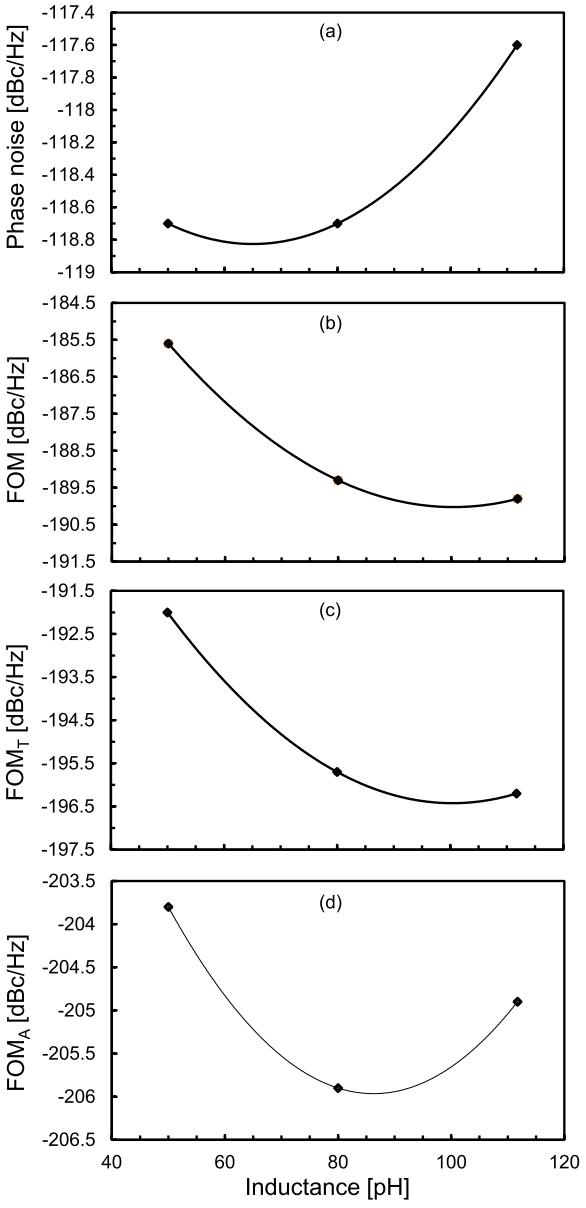

FIGURE 10. PN at 1-MHz from the carrier (a), FoM (b), FoM$_T$ (c) and FoM$_A$ (d) versus the inductance value of the stacked two-port inductor.

$$\mathrm{FoM_T} = \mathrm{FoM} - 20\log_{10}\left(\frac{\mathrm{TR}}{10}\right), \tag{11}$$

$$\mathrm{FoM_A} = \mathrm{FoM} + 10\log_{10}\left(\mathrm{Area_{mm^2}}\right), \tag{12}$$

where PN is the phase noise, f_0 is the oscillation frequency, Δf is the offset frequency from the carrier at which phase noise is measured, $P_{\mathrm{DC,mW}}$ is the dc power consumption expressed in mW, TR is the frequency tuning range and $\mathrm{Area_{mm2}}$ is the area consumption expressed in mm^2.

The dependence of the phase noise and the three FoMs from the inductance value, at 19.125 GHz, is reported in Fig. 10. The curves are based on the simulation results of the three quad-core VCOs reported in Table 4 using polynomial interpolation. It is apparent that the "*small inductor*" design does not carry any advantage over the "*medium inductor*" solution. Rather, its performance is significantly worse since the PN remains unchanged, but the power consumption increases exponentially. On the other hand, the "*medium*" and "*large*" inductor designs show excellent

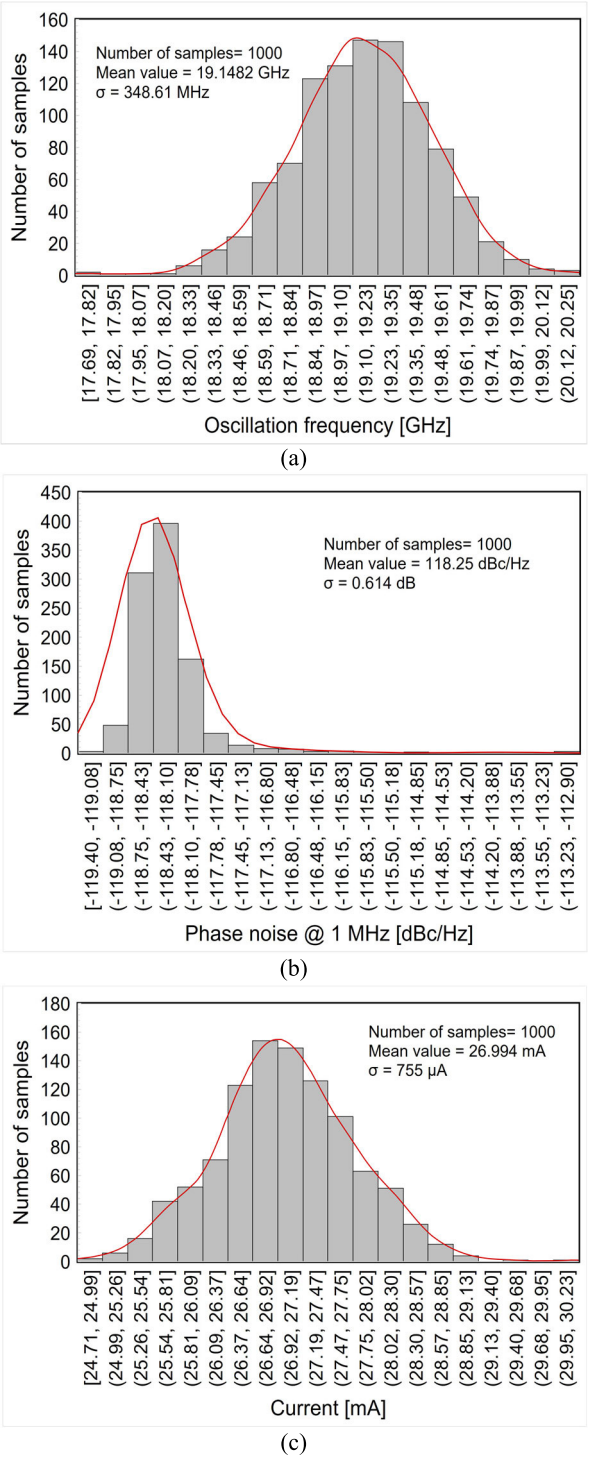

FIGURE 11. Montecarlo analysis of the medium-size quad-core VCO: oscillation frequency (a), PN (b), current consumption (c).

TABLE 6. Performance comparison with the state-of-the-art quad-core VCO.

	[22]	[28]	[29]	[30] (Simulated)	This work (Simulated)
Inductor topology	Single-turn	Four-port	Stacked	Interstacked	Stacked two-port (medium / large-size)
VCO topology	Class-B, NMOS-only, tail filtering	Complementary cross-coupled, $4f_0$ tail filtering	NMOS-only, tail filtering, push-push	Complementary cross-coupled	Complementary cross-coupled
Technology	55-nm BiCMOS	40-nm CMOS	45-nm PD-SOI CMOS	28-nm FDSOI CMOS	28-nm FD-SOI CMOS
Frequency [GHz]	20	26.45	60.5	19.125	19.125
Tank inductance [pH] [(1)]	~300 @ 20 GHz	59.2 @ 30.1 GHz	~225 @ 30.0 GHz	90.8 @ 19.1 GHz	80.2 / 112 @ 19.1 GHz
Inductor *Q*-factor	~20 @ 20 GHz	27.7 @ 30.1 GHz	~25 @ 30.0 GHz	21 @ 19.1 GHz	24.1 / 28.8 @ 19.1 GHz
Tuning range [%]	15	26	19	20	21
Tuning range type	analog and discrete	analog and discrete	analog-only	analog and discrete	analog and discrete
PN @ 1 MHz [dBc/Hz]	−118.5	−109.5	−101.7	−112.6	−118.7 / −117.6
PN @ 1 MHz from 19.125 GHz [dBc/Hz]	−118.9	−112.3	−111.7	−112.6	−118.7 / −117.6
Vdd [V]	1.2	0.95	1	1.2	1.2
Current [mA]	36	17	40	6	27 / 18
Power [mW]	43	16	40	7.2	32 / 22
Area [mm^2] [(2)]	2.4	0.1	0.044	0.025	0.09 / 0.105
FoM [dBc/Hz]	−188.2	−186.8	−181.3	−189.6	−189.3 / −189.8
FoM$_T$ [dBc/Hz]	−191.7	−195.0	−186.9	−195.6	−195.7 / −196.2
FoM$_A$ [dBc/Hz]	−190.4	−196.8	−194.9	−205.6	−199.8 / −199.7

[(1)] The tank inductance is referred to the one seen by each core.

[(2)] Total area occupied by the quad-core VCO.

performance. It is worth noting that silicon area consumption and phase noise can be traded by properly sizing the inductor. Notice also that FoM$_A$ has a minimum at around 80 pH. Therefore, this inductance value represents the best design choice for the most compact and lowest-PN quad-core VCO at 19.125 GHz based on the structure of Fig. 4 in the adopted CMOS technology. Let us mention that there is still room to improve the single-core oscillator performance by using other advanced techniques, like a class-C topology or tail filtering. However, the main claim of this paper is the novel approach based on stacked two-port inductors.

A corner analysis was performed on the "*medium*" design (i.e., 80-pH inductance) by applying the fast-fast-analog (FFA) and slow-slow-analog (SSA) corners, as reported in Table 5. Similar results are expected for other inductance values. The current does not change significantly and PN stays abundantly below the minimum requirement of −112 dBc/Hz given by the targeted application (i.e., 77-GHz automotive radar), thus confirming the robustness of both the proposed quad-core approach and design strategy. Finally, to further demonstrate the robustness of the proposed solution against process mismatches between cores, a Montecarlo simulation (with 1000 runs) was carried out. Fig. 11 summarizes the main outcomes of the Montecarlo simulations for the oscillation frequency, the phase noise, and the current consumption. The results align with those provided by the FFA/SSA corner analyses reported in Table 5. The variations of the current consumption are very low. The discrete frequency tuning effectively compensates for the variations in the oscillation frequency. Additionally, the phase noise is well below the target of −112.0 dBc/Hz, demonstrating the soundness of the proposed solution.

A comparison with the state-of-the-art quad-core solutions is made in Table 6. The proposed medium-sized quad-core VCO design achieves a comparable phase noise to that designed in [22], but has a 27x reduction of area occupation and a 25% decrease in the power consumption. On the other hand, the proposed large-sized design has a similar power consumption and area occupation to that designed in [28], but has more than 5.3 dB lower phase noise. Thanks to the stacked and interstacked topologies, the works in [29] and [30] achieve the lowest area consumption but at the cost of a higher phase noise than the proposed solution (of about 6 dB), which could be not compatible with the application. The proposed quad-core oscillator designs achieved better values of FoM and FOM$_T$ despite the lower power consumption of [30].

VI. CONCLUSION

A novel quad-core VCO design exploiting a stacked two-port inductor topology to couple the cores has been proposed. Expected results show excellent low-phase-noise performance at low power consumption and extremely low area occupation, which overcomes the typical drawbacks of multi-core oscillators and open new opportunities for their

exploitation in actual applications. The comparison with state-of-the-art quad-core approaches further confirms the strength of the proposed solution. Although the focus of the present work is 77-GHz radar, the field of application is wide and includes all modern wireless communication systems.

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