IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 21 May 2024, accepted 11 June 2024, date of publication 19 June 2024, date of current version 28 June 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3416834

RESEARCH ARTICLE

A Capacitor Voltage Balancing Hybrid PWM Technique to Improve the Performance of T-Type NPC Inverters

SHAHRIAR HOSSAIN[1], SHUVRA PROKASH BISWAS[2], (Graduate Student Member, IEEE), SUDIPTO MONDAL[1], (Student Member, IEEE), MD. RABIUL ISLAM[2], (Senior Member, IEEE), AND AFEF FEKIH[3], (Senior Member, IEEE)

[1]Department of Electronics and Telecommunication Engineering, Rajshahi University of Engineering and Technology, Rajshahi 6204, Bangladesh
[2]School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Keiraville, NSW 2522, Australia
[3]Department of Electrical and Computer Engineering, University of Louisiana at Lafayette, Lafayette, LA 70504, USA

Corresponding author: Afef Fekih (afef.fekih@louisiana.edu)

ABSTRACT Research into solar photovoltaic (PV) fed grid-tied multilevel inverters (MLIs) has increased in recent years due to their distinct features compared to two-level voltage source inverters (VSIs). However, maintaining the power quality of MLIs is a challenging problem that encompasses the reduction of total harmonic distortion (THD), dc-link voltage imbalance issues, power loss reduction and thermal stress mitigation; which are significantly affected by the applied pulse width modulation (PWM) technique. In order to tackle the above mentioned power quality problems, this work presents a modified hybrid PWM technique which combines a modified modulating signal with a modified carrier signal. The comparison between the proposed and the existing PWM techniques is performed under different conditions and using a wide range of modulation index variations. A grid-tied three-phase three-level T-type neutral point clamped (NPC) inverter is adopted for the power quality assessment. The proposed hybrid PWM offers 25.57% output line voltage THD and 11.8 V peak-to-peak dc-link capacitor voltage difference which are lower than existing PWM techniques. Additionally, by reducing the switching and conduction losses of the power switches, the proposed hybrid PWM technique offers lower thermal stress than existing PWM techniques. The comparative analysis between the existing and the proposed hybrid PWM technique is carried out using MATLAB/Simulink and PLECS simulation environments. The proposed hybrid PWM technique is further validated using a reduced scale prototype developed in our research laboratory.

INDEX TERMS Multilevel inverters, voltage source inverters, total harmonic distortion, dc-link voltage imbalance, pulse width modulation, T-type neutral point clamped inverter.

I. INTRODUCTION

Multilevel inverters (MLIs) are widely adopted in medium to high voltage applications as well as renewable solar photovoltaic (PV) systems due to several advantages over two level voltage source inverters (VSIs). This includes lower harmonic distortions, lower filter size, lower electromagnetic interference (EMI), high output waveform quality etc. [1], [2]. Cascaded H-bridge inverter (CHB), flying capacitor inverter (FC), and neutral point clamped inverter (NPC) are the three major topologies for the MLIs [3], [4], [5]. Among the topologies, NPC inverters have some appealing features over other topologies thus making them a smart choice for grid-tied solar PV applications. These features include higher efficiency, voltage handling capability, flexibility and better output voltage and current quality. T-type NPC inverters, however, which is a partial variant of the NPC inverter topology, can achieve greater efficiency than

The associate editor coordinating the review of this manuscript and approving it for publication was Ahmed Aboushady.

the NPC inverters in certain circumstances [6]. Though NPC inverters are well stablished and provide attractive power quality, there still remains some challenging issues and room for improvement. The major challenges are the total harmonic distortion, neutral point voltage imbalance, power loss, thermal stress etc. These challenges are greatly reliant on the applied PWM techniques. Hence, applying an appropriate and well controlled PWM technique has the potential to improve the inverter's harmonic distortion, voltage balancing performance, power loss and thermal stress. Various improved PWM techniques and control algorithms have been proposed in the literature to mitigate these problems [7], [8], [9], [10], [11], [12], [13], [14], [15], [16].

In [7], a sinusoidal pulse width modulation technique (SPWM) is applied to the nested T-type NPC inverter in order to balance the dc-link capacitor voltage. The SPWM technique is regarded as the easiest technique for the multilevel inverters due to its simplicity. A major drawback of this technique, however, is its high THD and poor power loss and the dc-link voltage balancing performance. A space vector pulse width modulation (SVPWM) is employed for NPC inverter and compared with SPWM in [8]. The obtained results showed that the SVPWM technique performs better than the SPWM technique in terms of THD. In [9], a detailed comparative analysis is conducted between the performance of a five-level diode clamped inverter, a sinusoidal PWM and a third harmonic injected PWM (THPWM). The performance of various types of medium voltage power converter topologies and their control techniques in increasing the efficiency for the grid integration of solar PV power plants is assessed in [10]. Comparative performance analysis between different PWM techniques such as SPWM, CSVPWM, THPWM, trapezoidal PWM (TRPWM), sixty-degree PWM (SDPWM) is examined in the literature. SDPWM based on the discontinuous modulating signal is known as bus clamping PWM. Among the BCPWM techniques, sixty-degree BCPWM and thirty-degree BCPWM are the most common and well suited PWM techniques for reducing switching loss. The third harmonic injected SDBCPWM and TDBCPWM techniques are considered in [11] for medium voltage grid-tied converters. They were shown to significantly reduce the switching losses and improve the output quality of the converter. By utilizing NPC inverter-based solar PV systems, a modified modulating signal-based PWM scheme is presented in [12], to improve the power quality of motor drive applications. It was also shown to mitigate the THD, switching losses, conduction losses and torque ripple by generating symmetrical and balanced gate pulses. In [13], a new current controller PWM scheme is proposed with a neutral point balancing technique in which a three level NPC inverter is utilized as a dual purpose of active shunt filtering and solar PV integration to distributed grid. To balance the dc-link capacitor voltages, a new step-up switch capacitor-based converter is introduced in a grid-tied seven level NPC inverter [14]. The additional converter needs separate control mechanism, thus making the system complex and bulky. In [15], a hybrid PWM strategy is proposed by combining space vector PWM and nearest level modulation for a five-level NPC inverter. The hybrid PWM offers lower THD at fundamental frequency and balances the unbalanced dc-link voltages. Using a multicarrier phase disposition PWM technique, a novel single-phase grid-tied five-level NPC converter is proposed in [16]. The proposed converter is shown to improve the grid current's power quality while simultaneously balancing the dc-link split capacitors. A major drawback of this topology, however, is the use of more power switches compared to conventional topologies.

In some literatures, PWM techniques are proposed to offer some specific improvements regarding a desired concern [17], [18]. However, none of them is able to simultaneously mitigate all the concerns. In [17], a carrier based discontinuous PWM technique is suggested utilizing a three level T-type converter for neutral point potential balancing. However, the THD and power loss of the inverter are not considered. In [18], a new PWM strategy is introduced to reduce the common mode voltage of the three phase three-level T-type NPC inverters by about 50%, thus alleviating the higher voltage stress and leakage current of the inverters. However, the total harmonic distortion of the output voltage is significantly higher than that of other existing PWM techniques.

In order to improve the power quality of multilevel converters, carrier-based PWM techniques such as multi carrier PWM, phase shifted PWM, and level shifted PWM are gaining popularity [19], [20]. Phase shifted PWM can be classified into other variants, such as phase disposition PWM, phase opposite disposition PWM, alternative phase opposite disposition PWM. Applying these PWM techniques in the multilevel converters, has some specific advantages and disadvantages based on the applications. A comparative analysis has been carried out with these PWM techniques for the NPC inverters in [21] and [22]. Combination of modulation techniques is known as hybrid PWM technique which is capable of combining their advantages together. A hybrid modulation technique is presented in [23] to balance the dc-link voltages and mitigate the lower order harmonics for NPC inverters by combining selective harmonic elimination and selective harmonic mitigation. The main obstacle in this technique is the complex nonlinear equations that is needed to be solved by different solving techniques. In [24], a hybrid PWM scheme is investigated for grid-tied T-type NPC inverter that is the combination of space vector PWM and selective harmonic elimination PWM. Through this technique, a smooth and quick transition is achieved which is desirable for the grid-tied inverter applications. However, neutral point voltage balancing arrangement is missing.

To alleviate the aforementioned limitations of the multilevel inverters, a well-balanced hybrid PWM technique consisting of a modified modulating signal and a carrier signal is proposed in this paper. The main attributes of the proposed hybrid PWM technique are as follows:

- It reduces the total harmonic distortion of the output line voltage the inverter;
- Improves the dc-link capacitor voltage balancing performance by reducing the peek-to-peek voltage difference;
- Reduces the switching and conduction losses of the power switches;
- Minimizes the total power loss thus resulting in lower junction temperature and reduced thermal stress;

It is worth noting that though various PWM techniques and control algorithms are proposed in different literatures, they all increase system complexity and require additional circuitry for hardware implementation. In contrast, modifying the modulating and carrier signals is a relatively easy approach to mitigate the crucial power quality concerns. Moreover, no additional circuitry is needed to implement it on the hardware and the behavior of the modified signals is well understood and predictable.

II. ADOPTED INVERTER TOPOLOGY

A grid tied three phase 3-L T-type neutral point clamped inverter is depicted in Fig. 1.

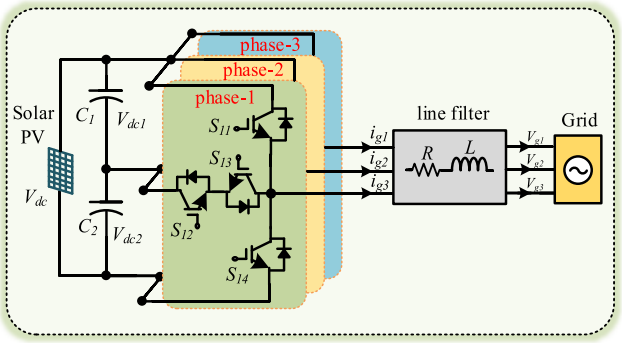

FIGURE 1. Solar PV fed grid-tied three-phase three-level T-type NPC inverter topology.

The inverter is fed by a solar PV and two dc-link capacitors (C_1, C_2) are used at the input side. The inverter consists a total of twelve power switches, namely (S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, S_{24}, S_{31}, S_{32}, S_{33}, S_{34}). For each phase, four power switches are necessary. Switch pairs (S_{11}, S_{13}) and (S_{12}, S_{14}) are known as each other's counterparts, thereby it's strictly prohibited to turn them on at the same time to avoid inverter failure. A RL line filter is used to connect the output side of the inverter to the grid and mitigate the harmonics of the current and line voltage.

III. CLOSED-LOOP CONTROL STRATEGY

Fig. 2 depicts a standard grid connected *dq* reference frame-based closed-loop control strategy for the adopted inverter topology, which is able to supply both active and reactive power to the grid. The three-phase AC current and voltage signals are converted into D (direct) and Q (quadrature) components which represent active and reactive power, respectively and are aligned with the grid voltage reference frame. The phase locked loop (PLL) determines α and β values with phase angle of the voltage and current by sensing the grid voltage (V_g) and grid current (i_g), respectively. The measured direct and quadrature axis components of the grid current are represented by i_d and i_q, respectively that can be used to control the active and reactive power individually. Then, i_d and i_q are compared with the reference quantity i_d^* and i_q^*, respectively and the measured errors are fed to the PI controller. At the output, two reference signals (M_d and M_q) are obtained in *dq* frame which are converted to the *abc* frame to produce the three phase reference signals. These reference signals are then further modified to produce the proposed modulating signal of the hybrid PWM technique.

The generation procedure of the proposed modulating signal is described in section V. The proposed modulating signal and carrier signal are then compared in order to produce the twelve gate pulses which are needed for the adopted three phase three level T-type NPC inverter.

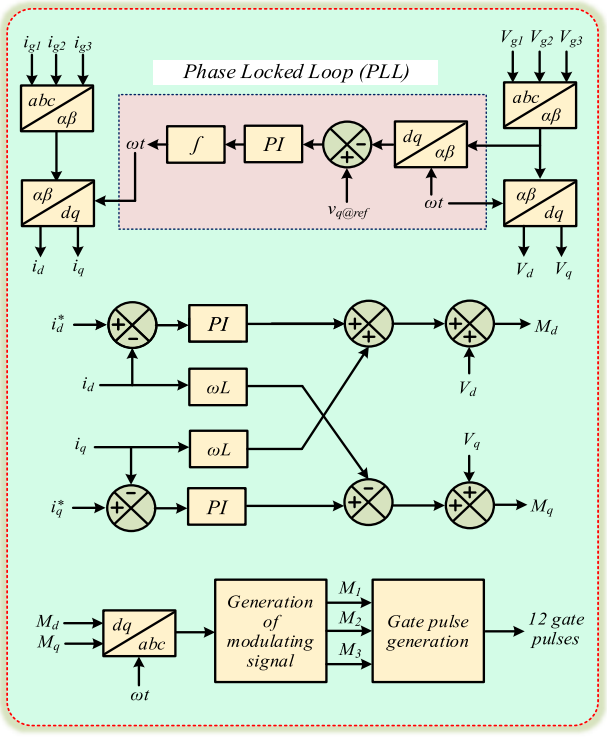

FIGURE 2. Closed-loop control strategy for the adopted inverter topology.

IV. GENERATION OF THE EXISTING PWM TECHNIQUES

All the existing PWM techniques, which can be applied to the MLIs, have some merits and demerits based on their applications. The most widely used PWM techniques applied to the MLIs are SPWM [7], CSVPWM [8], THPWM [9], SDPWM [10]. SPWM is the most common and simple PWM technique for MLIs. CSVPWM and THPWM are highly regarded for mitigating lower order harmonics and improving the power quality. On the contrary, the SDPWM technique is

well capable of reducing the switching loss compared to other PWM techniques.

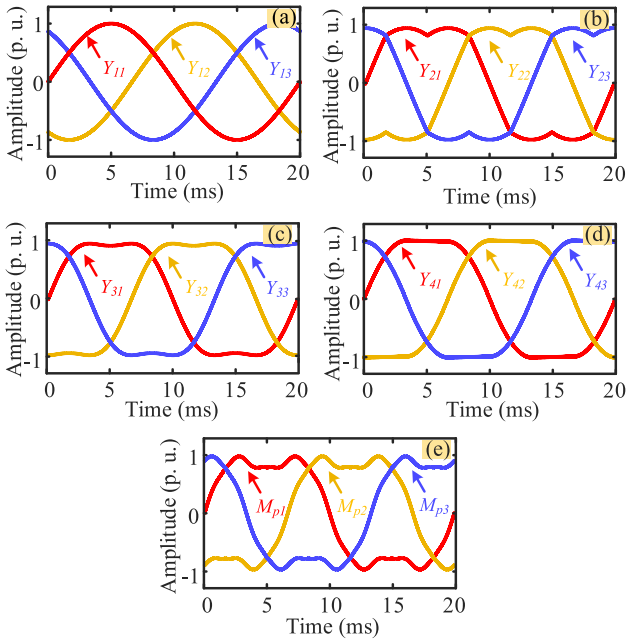

FIGURE 3. The modulating signals of (a) SPWM, (b) CSVPWM, (c) THPWM, (d) SDPWM and (e) the proposed hybrid PWM technique.

Table 1 depicts the mathematical representation of some well-known existing PWM techniques. Though these techniques offer balanced performance in terms of power quality, performance improvement is further possible by modifying the PWM technique. This means modifying the modulating signal along with the carrier signal. The modulating signals of existing SPWM, CSVPWM, THPWM, SDPWM techniques and the proposed modified hybrid PWM technique are sketched in Fig. 3.

V. DEVELOPMENT OF THE PROPOSED HYBRID PWM TECHNIQUE

The modified modulating signal and the carrier signal are the heart of the proposed hybrid PWM technique. This section provides a brief description of the steps involved in developing the proposed modified carrier signal and modulating signal, as well as the gate pulses required for the power switches.

A. GENERATING THE MODULATING SIGNAL

The proposed modified modulating signal is generated by combining three sinusoidal signals with different amplitude and a triangular signal. The generation procedure of the proposed modified modulating signal, M_p is illustrated in Fig. 4.

At first, a sinusoidal signal (P) is taken with three times larger frequency than the fundamental such that:

$$P = A\sin\ (3\,\omega\,t) \tag{1}$$

where, A and ω are the amplitude and angular frequency the signal, respectively. By using the sinusoidal signal (P),

TABLE 1. Mathematical representation of different PWM techniques.

PWM Technique	Mathematical Representation
SPWM [7]	$Y_1 = A\sin(\omega t+\theta)$ $[Y_{11}\quad Y_{12}\quad Y_{13}]=\left[Y_{1_{\theta=0^o}}\quad Y_{1_{\theta=-120^o}}\quad Y_{1_{\theta=120^o}}\right]$
CSVPWM [8]	$Y_2=\frac{2}{\sqrt{3}}\{A\sin(\omega t+\theta)\}-\frac{1}{2}\{\max(Y_{11},Y_{12},Y_{13})\}$ $+\frac{1}{2}\{\min(Y_{11},Y_{12},Y_{13})\}$ $[Y_{21}\quad Y_{22}\quad Y_{23}]=\left[Y_{2_{\theta=0^o}}\quad Y_{2_{\theta=-120^o}}\quad Y_{2_{\theta=120^o}}\right]$
THPWM [9]	$Z=cA\sin(\omega t+\theta)$ $Y_3=A\sin(\omega t+\theta)+Z$ $[Y_{31}\quad Y_{32}\quad Y_{33}]=\left[Y_{3_{\theta=0^o}}\quad Y_{3_{\theta=-120^o}}\quad Y_{3_{\theta=120^o}}\right]$
SDPWM [10]	$Y_4=\frac{2}{\sqrt{3}}[A\sin(\omega t+\theta)]+\frac{1}{2\pi}[A\sin(3\omega t+\theta)]$ $+\frac{1}{60\pi}[A\sin(9\omega t+\theta)]+\frac{1}{180\pi}[A\sin(15\omega t+\theta)]...$ $[Y_{41}\quad Y_{42}\quad Y_{43}]=\left[Y_{4_{\theta=0^o}}\quad Y_{4_{\theta=-120^o}}\quad Y_{4_{\theta=120^o}}\right]$

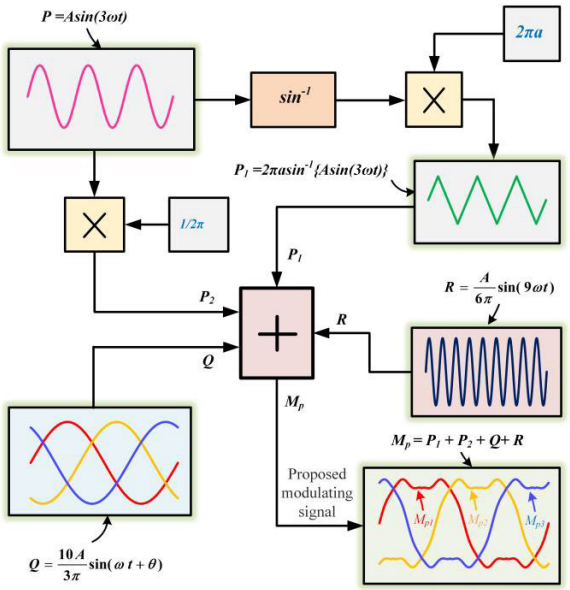

FIGURE 4. The generation procedure of the modulating signal of the proposed hybrid PWM technique.

a triangular signal (P_1) is generated that is expressed as:

$$P_1 = 2\pi a\sin^{-1}\{A\sin(3\omega t)\} \tag{2}$$

where, a is the amplitude constant. Then, another version of the signal (P) is generated as follows:

$$P_2 = \frac{A}{2\pi}\sin(3\omega t) \tag{3}$$

After that, a three-phase sinusoidal signal (Q) is taken such that:

$$Q = \frac{10A}{3\pi}\sin(\omega t + \theta) \tag{4}$$

$$\lfloor Q_1 \quad Q_2 \quad Q_3 \rfloor = \lfloor Q_{\theta=0^\circ} \; Q_{\theta=-120^\circ} \; Q_{\theta=120^\circ} \rfloor \tag{5}$$

where, θ defines the phase difference of the signal, Q. Then, another sinusoidal signal (R) with nine times larger frequency than the fundamental is generated such that:

$$R = \frac{A}{6\pi}\sin(9\omega t) \tag{6}$$

At last, the proposed modified modulating signal (M_P) is developed by adding the previously constructed signals P_1, P_2, Q and R as follows:

$$M_p = P_1 + P_2 + Q + R \tag{7}$$

$$\lfloor M_{p1} \; M_{p2} \; M_{p3} \rfloor = \lfloor M_{p_{\theta=0^\circ}} \; M_{p_{\theta=-120^\circ}} \; M_{p_{\theta=120^\circ}} \rfloor \tag{8}$$

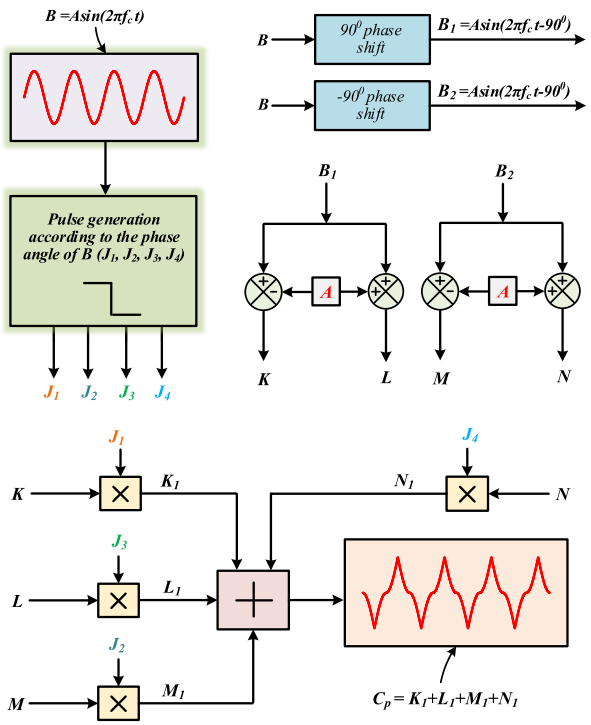

FIGURE 5. The generation procedure of the carrier signal of the proposed hybrid PWM technique.

B. GENERATING THE CARRIER SIGNAL

The proposed modified carrier signal is developed by using a sinusoidal signal by applying some changes in it. The development procedure of the proposed carrier signal is illustrated in Fig 5. To generate the proposed carrier signal, first a sinusoidal signal (B) is considered as follows:

$$B = A\sin(2\pi f_c t) \tag{9}$$

where, A and f_c represents the amplitude and the carrier frequency of the signal, respectively. Then, two intermediate signals (B_1) and (B_2) are constructed using the sinusoidal signal (B), as follows:

$$B_1 = A\sin(2\pi f_c t + 90^\circ) \tag{10}$$

$$B_2 = A\sin(2\pi f_c t - 90^\circ) \tag{11}$$

Now, according to the phase angle of the signal (B), four pulse signals J_1, J_2, J_3 and J_4 as follows:

$$B = \begin{Bmatrix} J_1; & if\ 0^0 \le \theta < 90^0 \\ J_2; & if\ 90^0 \le \theta < 180^0 \\ J_3; & if\ 180^0 \le \theta < 270^0 \\ J_4; & if\ 270^0 \le \theta < 360^0 \end{Bmatrix} \tag{12}$$

where, θ is the phase angle of signal (B). Now, four intermediate level shifted signals (K, L, M, N) are generated as follows:

$$K = B_1 - A \tag{13}$$

$$L = B_1 + A \tag{14}$$

$$M = B_2 - A \tag{15}$$

$$N = B_2 + A \tag{16}$$

Then, the newly generated level shifted signals (K, L, M, N) are multiplied by the previously generated pulse signals (J_1, J_3, J_2, J_4) to build the signals (K_1, L_1, M_1, N_1), respectively.

$$K_1 = KJ_1 \tag{17}$$

$$L_1 = LJ_3 \tag{18}$$

$$M_1 = MJ_2 \tag{19}$$

$$N_1 = NJ_4 \tag{20}$$

Finally, the discrete signals (K_1, L_1, M_1, N_1) are added together to develop the proposed carrier signal, C_p of the hybrid PWM technique.

$$C_p = K_1 + L_1 + M_1 + N_1 \tag{21}$$

C. GENERATING THE GATE PULSES

The modulating signal of Fig. 4 and the carrier signal of Fig. 5 together form the proposed hybrid PWM technique. The block diagram representation of the generation process of the gate pulses under the proposed modified hybrid PWM technique is depicted in Fig. 6. To generate the gate pulses for the IGBTs, the proposed modulating signal is compared with the proposed carrier signal. For generating three level output for each phase, two carrier signals ($Carrier_1$ and $Carrier_2$) are needed for S_{11}, S_{12}, S_{13} and S_{14}, respectively.

The gate pulse generation for IGBTs (S_{11}, S_{12}, S_{13}, S_{14}) is depicted in Fig. 7 for 0.8 kHz carrier signal. When amplitude of Carrier$_1$ is lower than M_{p1}, the IGBT S_{11} is turned on. Otherwise, the IGBT S_{11} is turned off. Similarly, when amplitude of Carrier$_2$ is lower than M_{p1}, the IGBT S_{12} is turned on.

TABLE 2. Switching states of the IGBTs for a single phase.

State	S_{11}	S_{12}	S_{13}	S_{14}	Output
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

The IGBTs S_{13} and S_{14} are the counterpart of S_{11} and S_{12}, respectively. That means, S_{13} and S_{14} must be turned off when S_{11} and S_{12} are turned on. The switching states of the IGBTs for a single phase is given in Table 2. The states P, O and N represent positive, neutral and negative state, respectively.

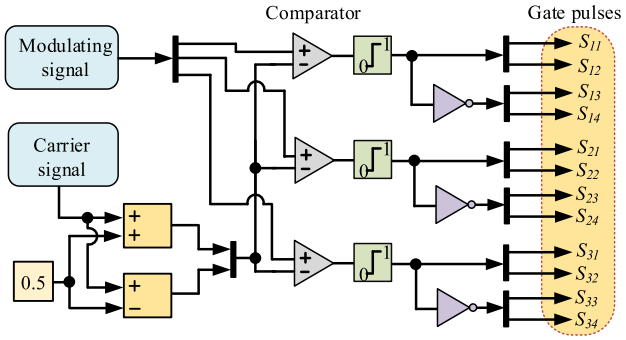

FIGURE 6. The gate pulse generation process for the adopted topology.

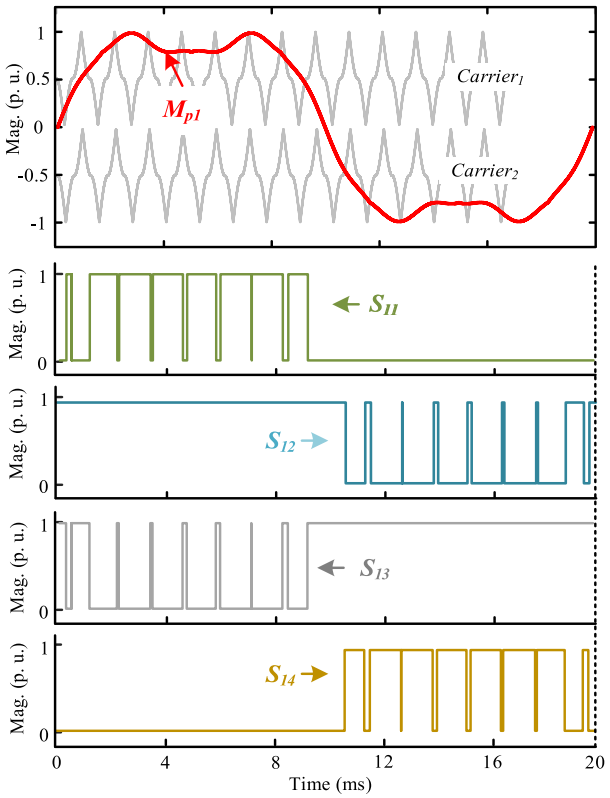

FIGURE 7. Gate pulse generation for a single phase under the proposed hybrid PWM technique.

D. MOTIVATION AND PROCESS OF FINDING OF THE PROPOSED HYBRID PWM TECHNIQUE

The main motivation of the proposed modified PWM technique comes from the shortcomings of existing PWM techniques which suffer from high THD, power loss leading to thermal stress and capacitor voltage balancing problems. The mitigation of THD, power loss and capacitor voltage balancing issue depend on the gate pulses used for switching the power semiconductor switches. The gate pulses obtained from the proposed modified PWM technique is symmetric and balanced compared to the gate pulses of existing PWM techniques which ensure lower THD, power loss and balanced capacitor voltages. These gating signals are only obtained if we use the proposed modified carrier and modulating signal together. The proposed hybrid PWM technique is developed using a process consisting of some methodical procedures during the generation of the gating signals for the NPC inverter.

The gate pulse generation procedure is the major part of the PWM technique, which significantly controls all the performance parameters such as THD, power losses, heat distribution and capacitor voltage balancing issue. Optimized and well-balanced gate pulses contribute to the overall improved performance of the MLIs. Hence, to generate the improved modified modulating and the carrier signals, at first the pulse sequences under the traditional PWM technique are analyzed. The investigated gate pulse sequences for six IGBTs (S_{11}, S_{12}, S_{21}, S_{22}, S_{31} and S_{32}) and the charging behavior of the dc-link capacitors under the SPWM technique is depicted in Table 3. Here, SPWM technique is utilized, as it is the simplest modulation strategy among the traditional techniques. In this case, low frequency carrier signal (about 50 Hz) is used so that the switching states of the IGBTs can be easily observed. S_{X1} and S_{X2} are the counter part of S_{X3} and S_{X4}, respectively. Hence, analyzing only two IGBTs from each leg of the inverter is sufficient. As a result, there are six IGBTs and 720 probable switching sequences that are needed to be analyzed. However, in this case, some common and repetitive switching sequences are investigated. From the switching sequences, it can be found that some sequences such as 1, 3, 5, 7, 10 and 13 are responsible for keeping the capacitor voltages constant. Repeating these sequences can be suitable for mitigating the dc-link capacitor voltage fluctuation issue.

After analyzing the pulse sequences, the proposed carrier signal is developed according to the process depicted in Fig. 5. The shape of the proposed carrier signal helps with supportive switch turn on and turn off sequence. Next step is to develop the proposed modulating signal which is depicted in Fig. 4. In this case, the generation idea is taken from the previous literatures where the modulating signals are constructed by adding some odd harmonic signals reflected

TABLE 3. Investigation of the behavior of the capacitor voltages under different switching sequences.

Switching sequence	Switching states of the IGBTs						Behavior of the capacitor voltages: charging (↑), discharging (↓), constant (−)	
	S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	V_{C1}	V_{C2}
1	OFF	ON	OFF	OFF	ON	ON	−	−
2	ON	ON	OFF	OFF	OFF	ON	↑	↓
3	ON	ON	OFF	OFF	OFF	OFF	−	−
4	OFF	ON	OFF	ON	OFF	OFF	↑	↓
5	OFF	ON	ON	ON	OFF	OFF	−	−
6	OFF	OFF	ON	ON	OFF	ON	↓	↑
7	OFF	OFF	ON	ON	ON	ON	−	−
8	OFF	OFF	OFF	ON	ON	ON	↑	↓
9	OFF	ON	OFF	ON	ON	ON	↓	↑
10	ON	ON	OFF	OFF	ON	ON	−	−
11	ON	ON	OFF	OFF	OFF	ON	↑	↓
12	ON	ON	OFF	ON	OFF	OFF	↓	↑
13	OFF	OFF	ON	ON	OFF	OFF	−	−

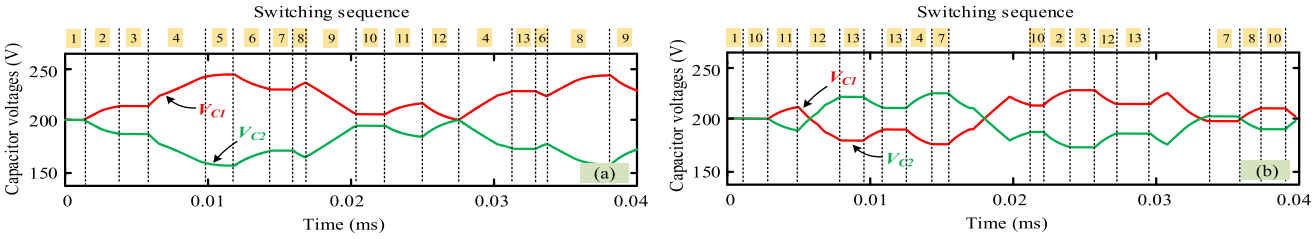

FIGURE 8. Response of the dc-link capacitor voltages for different switching sequences under (a) SPWM and (b) the proposed hybrid PWM technique.

in the development process of THPWM and SDPWM techniques. The amplitude constant of the harmonic signals of the proposed PWM technique is highly sensitive, as it directly affects the gate pulse pattern of the IGBTs. As different odd harmonic signals with different frequencies are added, there are chances that the amplitude may exceed the defined value A. The main consideration in this case is the amplitude of the modulating signal which is adjusted as follows for ensuring intermediate flatted top signal that can generate balanced and symmetric gating signals:

$$Amp.\ of\ M_P \leq Amp.\ of\ P_1 + Amp.\ of\ P_2 + Amp.\ of\ Q + Amp.\ of\ R \tag{22}$$

where M_P is the proposed modulating signal and P_1, P_2, Q, R are the intermediate signals, respectively as previously described.

At 0°, 180° and 360° phase angle the amplitude of M_P is surely less than A whereas at 90° and 270° phase angle, the amplitude of M_P is expressed as:

$$\begin{aligned} &Amp.\ of\ M_P \\ &= \pm\left\{A\left(\frac{10}{3\pi} - 2\pi\, a - \frac{1}{2\pi} + \frac{1}{6\pi}\right)\right\} \\ &= \pm\left\{A\left(\frac{10}{3\pi} - 0.02\pi - \frac{1}{2\pi} + \frac{1}{6\pi}\right)\right\} \quad [a = 0.01] \\ &= \pm 0.892A \end{aligned}$$

The amplitude of M_P is less than A. The amplitude constants are taken in a way that the maximum amplitude of M_P is achieved between 0° to 90° phase angle which is exactly match the defined amplitude A.

The response of the dc-link capacitor voltages for different switching sequences under SPWM and the proposed hybrid PWM technique is depicted in Fig. 8(a) and 8(b), respectively. Under the SPWM technique the constant voltage sequences are repeated after two or more than two sequences which gives more time to charge or discharge the capacitors, resulting high dc-link voltage fluctuation. Hence, if the constant

sequences can be repeated after every charge or discharge sequence, it will minimize the difference between the capacitor voltages. In order to maintain this, the modulating signals are adjusted so that the constant sequences can be repeated after every charge or discharge sequence. This process is demonstrated in Fig. 8(b), where the sequences are identified according the investigated sequences from Table 3. Form the Fig. 8(b), it can be seen that the constant voltage sequences are repeated after a signal charge or discharge sequence. In some cases, there are two sequences where they are different. That means, one sequence charges the capacitor and other discharge the capacitor. As a result of it, the capacitor voltages cross each other and the voltage difference is more minimized. There are other unmatched sequences such as, between (7^{th} -10^{th}) and (13^{th} -7^{th}) which can be ignored, because it can be easily seen that they show opposite behavior and cross each other.

Moreover, the proposed hybrid PWM technique offer balanced switch turn on and turn off which mitigate the unfiltered line voltage THD compared to the existing SPWM, CSVPWM, THPWM and SDPWM techniques. On the other hand, balanced switch turn on and turn off sequences also improve the number of switching and conduction period of the IGBTs which aid to minimize the power losses of the inverter.

VI. PERFORMANCE ANALYSIS AND COMPARISON

The comparative performance analysis between the existing PWM techniques and the proposed modified hybrid PWM technique in terms of THD, capacitor voltage balancing, power loss and thermal stress is conducted by using both simulation and experiment results.

A. SIMULATION RESULTS

The output line voltage (unfiltered) and the harmonic spectrum of the output line voltage under the proposed modified hybrid PWM technique are depicted in Fig. 9(a) and Fig. 9(b), respectively. The obtained THD of inverter line voltage (unfiltered) is 25.57%. The three-phase grid current and its harmonic spectrum under the proposed hybrid PWM are depicted in Fig. 9(c) and Fig. 9(d), respectively. The recorded grid current THD is 1.12% which is satisfactory, because according to the IEEE-519 standard THD must be less than 5%.

The peak-to-peak dc-link capacitor voltage difference under the existing SPWM, CSVPWM, THPWM, SDPWM techniques and the proposed hybrid PWM technique are depicted in Fig. 10(a), Fig. 10(b), Fig. 10(c), Fig. 10(d) and Fig. 10(e), respectively. From Fig. 10, it can be seen that the peak-to-peak capacitor voltage difference under SPWM, CSVPWM, THPWM, SDPWM and the proposed hybrid PWM techniques are 28.7 V, 13.6 V, 17.5 V, 20.6 V and 11.8 V, respectively. The highest peak-to-peak capacitor voltage difference is recorded under SPWM technique whereas the lowest is recorded under the proposed hybrid PWM technique. It is evident from Fig. 10 that the proposed hybrid PWM technique gives 16.9 V, 1.8 V, 5.7 V and 8.8 V less peak-to-peak capacitor voltage difference than the existing PWM techniques, respectively. So, the proposed hybrid PWM technique is better than the existing SPWM, CSVPWM, THPWM and SDPWM, respectively in terms of capacitor voltage balancing performance.

The bar graph of Fig. 11(a) showed unfiltered THD of the inverter output line voltage offered by the existing PWM techniques and the proposed hybrid PWM technique, respectively against modulation index variation (0.6∼1.4). Similarly, peak-to-peak dc-link capacitor voltage difference achieved by the existing PWM techniques and the proposed hybrid PWM technique against modulation index variation (0.6∼1.4) is illustrated in Fig. 11(b), respectively.

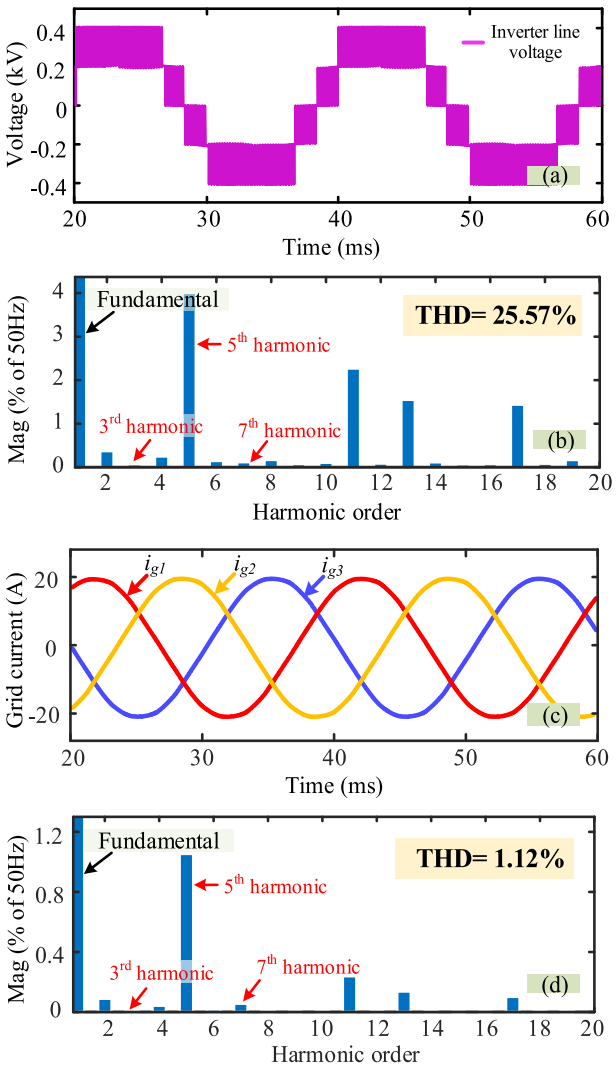

FIGURE 9. (a) Inverter output line voltage (b) THD spectrum of inverter output line voltage (c) grid current (d) THD spectrum of the grid current under the proposed hybrid PWM technique.

The detailed summary of the inverter output line voltage THD (unfiltered) and the peak-to-peak dc link voltage difference between the existing PWM techniques and the

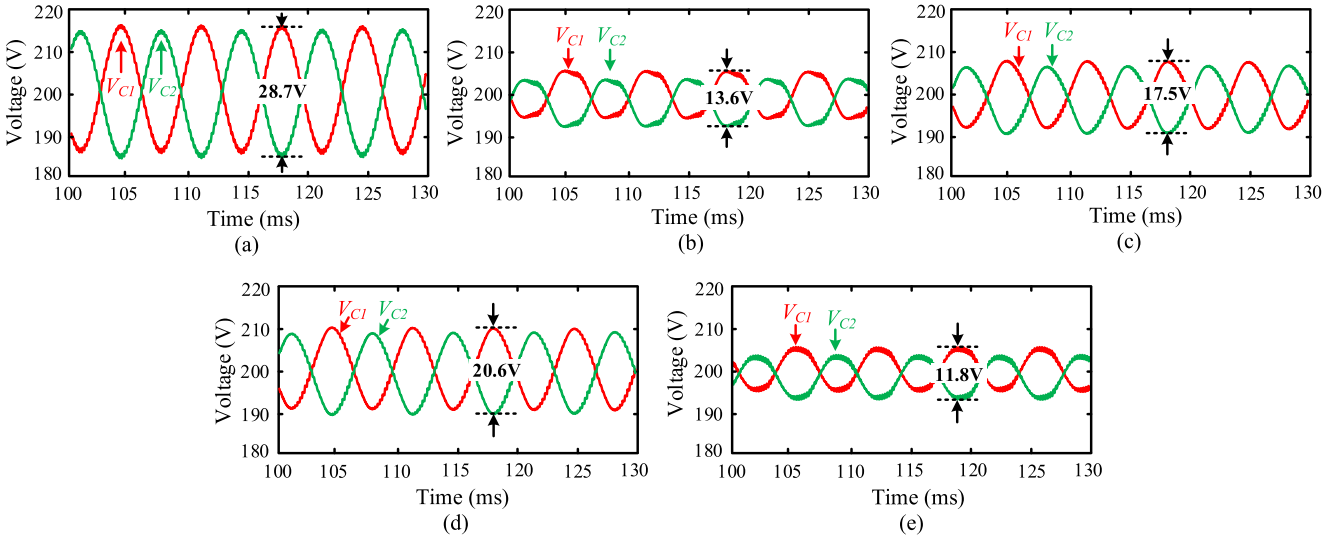

FIGURE 10. Dc-link capacitor voltage difference under (a) SPWM (b) CSVPWM (c) THPWM (d) SDPWM and (e) the proposed hybrid PWM techniques.

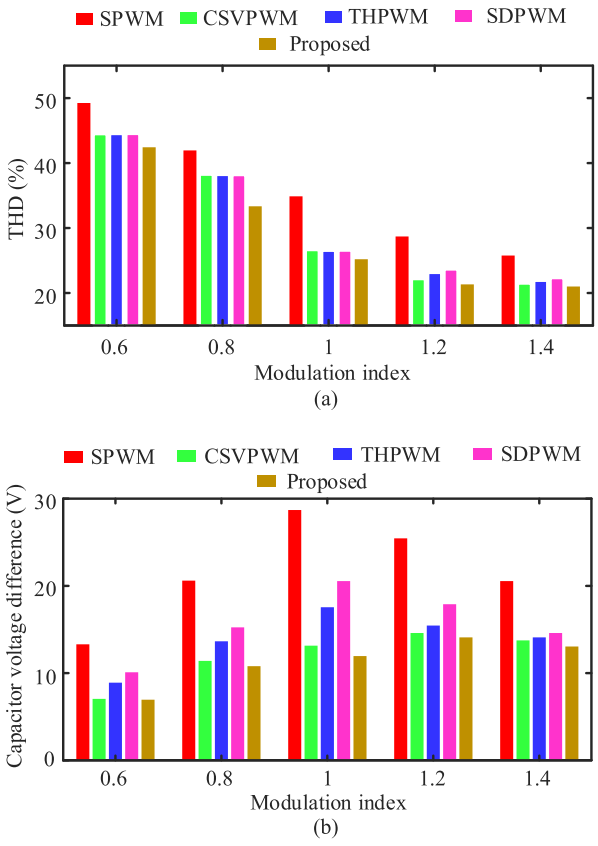

FIGURE 11. Comparative analysis between SPWM, CSVPWM, THPWM, SDPWM and the proposed hybrid PWM techniques against modulation index variation in terms of (a) inverter output line voltage THD and (b) capacitor voltage difference.

proposed hybrid PWM technique is depicted in Table 4. The THD of the inverter output line voltage obtained by the proposed hybrid PWM technique against modulation index 0.6, 0.8, 1, 1.2 and 1.4 are 43.42%, 34.01%, 25.57%, 21.56% and 21.22%, respectively, which are lower than the existing SPWM, CSVPWM, THPWM and SDPWM techniques. At modulation index 1, the proposed hybrid PWM offers 9.32%, 1.05%, 0.94% and 0.97% less inverter output line voltage THD than the existing PWM techniques, respectively. On the contrary, the peak-to-peak capacitor voltage difference obtained by the proposed hybrid PWM technique against modulation index 0.6, 0.8, 1, 1.2 and 1.4 are 7.1 V, 10.4 V, 11.8 V, 13.7 V and 13.1 V, respectively, which are lower than the existing PWM techniques, respectively. The proposed hybrid PWM technique gives 6.6 V, 0.2 V, 2.1 V and 3 V less capacitor voltage difference than the existing SPWM, CSVPWM, THPWM and SDPWM techniques, respectively, when modulation index is 0.6. For modulation index 0.8, the proposed hybrid PWM gives 10.1 V, 0.8 V, 3.4 V and 4.9 V less capacitor voltage difference than the existing PWM techniques, respectively. Similarly, for modulation index 1, 1.2, 1.4, the proposed hybrid PWM technique gives less capacitor voltage difference than the existing PWM techniques, respectively which is clearly noticeable from Table 4.

The power loss and thermal distribution of the proposed hybrid PWM technique for the IGBTs of phase-1 (S_{11}, S_{12}, S_{13}, S_{14}) are sketched in Fig. 12. The power loss and the junction temperature of the IGBTs are calculated in PLECS simulation software using IKW50N65F5 IGBT and diode from Infineon Technologies. The characteristic curve from the selected model is placed in PLECS block set to obtain the power loss and junction temperature. From Fig. 12(a), it can be seen that the power losses of S_{11}, S_{12}, S_{13}, S_{14} are 42.25W, 1.94 W, 1.94 W and 42.25 W which are 48%, 2%, 2% and 48%, respectively, of the total power loss of phase-1. Hence, for each phase the outer switches (S_{11} and S_{14}) consume more power loss than the inner switches (S_{12} and S_{13}), respectively. On the contrary, the junction

TABLE 4. THD and peak-to-peak capacitor voltage difference between different PWM techniques against modulation index variation.

PWM technique	THD (%) of inverter output line voltage (unfiltered) with the variation of modulation indices (0.6~1.4)					Capacitor voltage difference (V) with the variation of modulation indices (0.6~1.4)				
	0.6	0.8	1	1.2	1.4	0.6	0.8	1	1.2	1.4
SPWM [7]	49.25	41.95	34.89	28.71	25.77	13.7	20.5	28.7	25.4	20.7
CSVPWM [8]	44.46	38.22	26.62	22.15	21.47	7.3	11.2	13.6	14.6	13.5
THPWM [9]	44.49	38.19	26.51	23.11	21.89	9.2	13.8	17.5	15.3	14.1
SDPWM [10]	44.5	38.17	26.54	23.64	22.31	10.1	15.3	20.6	17.8	14.6
Proposed	43.42	34.01	25.57	21.56	21.22	7.1	10.4	11.8	13.7	13.1

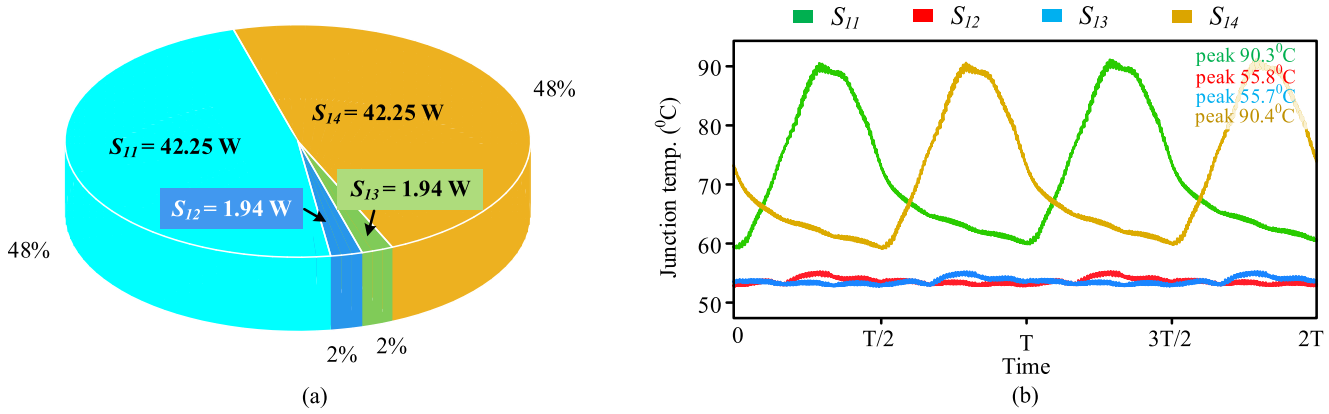

FIGURE 12. (a) Power loss and (b) thermal distribution of the proposed hybrid PWM technique for IGBTs (S_{11}, S_{12}, S_{13}, S_{14}).

temperature of the IGBTs (S_{11}, S_{12}, S_{13}, S_{14}) are illustrated in Fig. 12(b) for two operating cycles. The IGBTs of phase-1 (S_{11}, S_{12}, S_{13}, S_{14}) encounter peak temperature of 90.3°, 55.8°, 55.7° and 90.4°, respectively. The outer switches (S_{11} and S_{14}) face high junction temperature as well as thermal stress than the inner switches (S_{12} and S_{13}), respectively, that is seen from Fig. 12(b). Switching loss (S_L) and conduction loss (C_L) are considered as the major power loss of the inverter. A detailed pictorial representation of the switching loss (S_L), conduction loss (C_L) and total power loss (T_L) between SPWM, CSVPWM, THPWM, SDPWM and the proposed hybrid PWM techniques against modulation index variation (0.6∼1) is sketched in Fig. 13-15, respectively using 3D bar graph.

When the modulation index is near 1, inverter operates at high power rating resulting high power loss. Total power loss (T_L) under the proposed hybrid PWM technique for modulation index 0.6, 0.7, 0.8, 0.9 and 1 are 191.6 W, 223.1 W, 240.1 W, 259.4 W, 278.3 W, respectively that is lower than the other existing SPWM, CSVPWM, THPWM and SDPWM techniques. The proposed hybrid PWM technique shows 10.87% upgrade in terms of switching loss (S_L), 2.69% upgrade in terms of conduction loss (C_L) and 3.6% upgrade

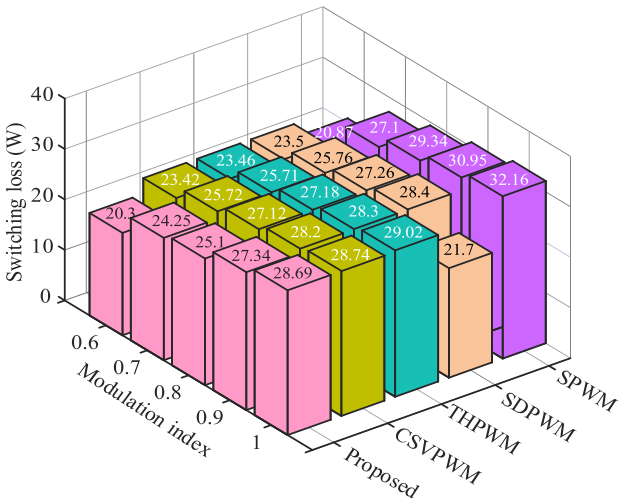

FIGURE 13. Switching loss comparison among different PWM techniques against modulation index variation.

in terms of total loss (T_L) than the SPWM technique that can be clearly seen from Fig. 13-15, respectively. Similarly, the proposed hybrid PWM technique shows around 2.73%

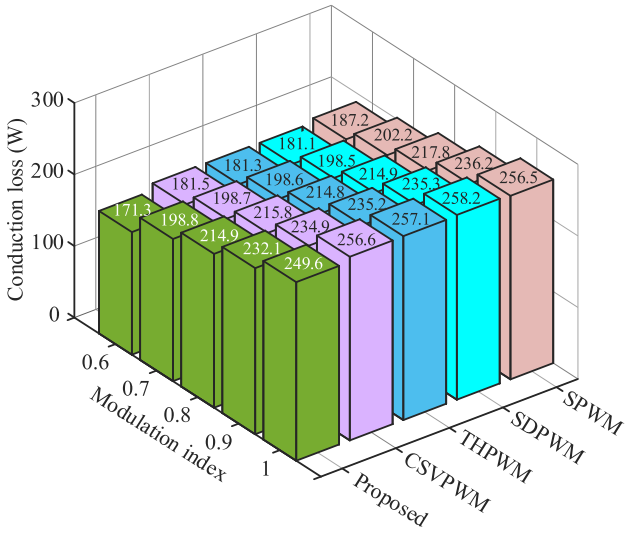

FIGURE 14. Conduction loss comparison among different PWM techniques against modulation index variation.

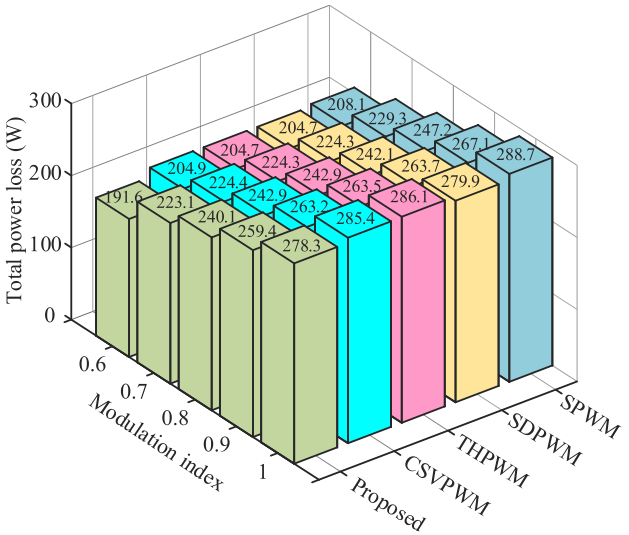

FIGURE 15. Total loss comparison among different PWM techniques against modulation index variation.

upgrade in terms of total loss (T_L) than both CSVPWM and THPWM techniques, respectively. On the contrary, the proposed hybrid PWM exhibits 24.4% worse result in terms of switching loss (S_L), 3.33% upgrade in terms of conduction loss (C_L) and 0.57% upgrade in terms of total loss (T_L) than the SDPWM technique for modulation index 1. The SDPWM technique is regarded as the best technique to reduce the switching loss of the inverter [11]. So, switching loss is greatly reduced in SDPWM technique than the proposed hybrid PWM technique when modulation index 1. However, with the decreasing modulation index the proposed hybrid PWM technique shows better result in terms of switching loss (S_L). Hence, the proposed hybrid PWM technique can surely outperform the existing SPWM, CSVPWM, THPWM and SDPWM techniques, respectively.

The close-loop reference current responses under the proposed hybrid PWM technique for both active and reactive power is demonstrated in Fig. 16 and Fig. 17, respectively. The voltage and current waveform for unity, lagging and leading power factor is demonstrated in Fig. 16(a), Fig. 16(b), and Fig. 16(c), respectively. At unity power factor, only resistive load is applied (3.25 kW, i_d^* = -20 A, i_q^* = 0 A) which keeps the voltage and current in same phase. At leading power factor, capacitive load is applied (3.25 kVAR, i_d^* = 0 A, i_q^* = -20 A) where current leads the voltage by 90°. On the contrary, at lagging power factor, inductive load is applied (3.25 kVAR, $i_d^* = 0$ A, $i_q^* = 20$ A) where voltage lead current by 90°. Fig. 17 demonstrates the inverter's step responses when applying active and reactive power under the proposed hybrid PWM technique. Two step changes are made at 60 ms and 120 ms, respectively. Initially, reactive power is applied (3.25 kW, i_d^* = -20 A, $i_q^* = 0$ A) to the grid. The grid current track the reference grid current (20 A) with no phase shift between the grid voltage and grid current.

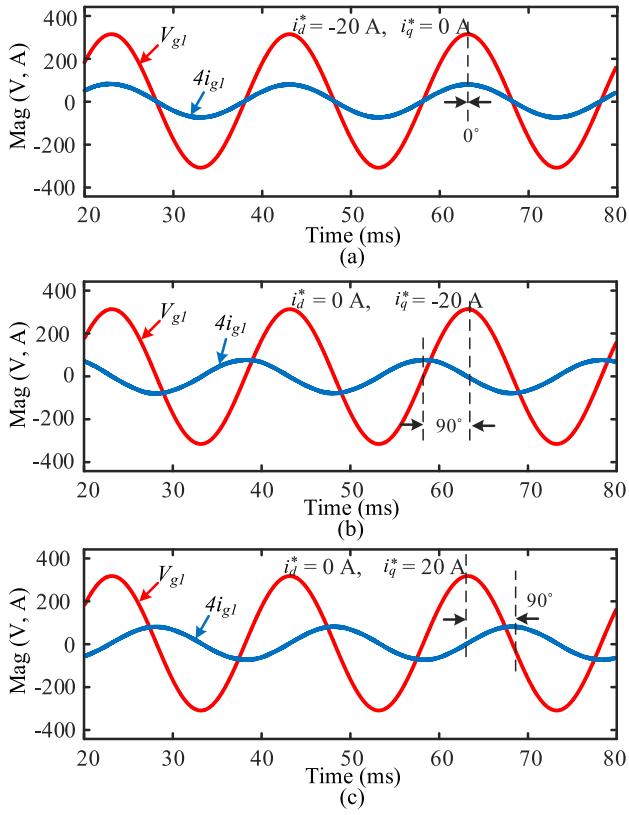

FIGURE 16. Grid voltage and grid current waveform at (a) unity (b) leading, and (c) lagging power factor.

At 60 ms, 1st step change is made by applying reactive power (3.25 kW, 3.25 kVAR, $i_d^* = -20$ A, $i_q^* = 20$ A) through inductive load to the grid. As a result, the grid current changed to 28.26 A which is expected as both active and reactive power is applied together. At 120 ms, 2nd step change

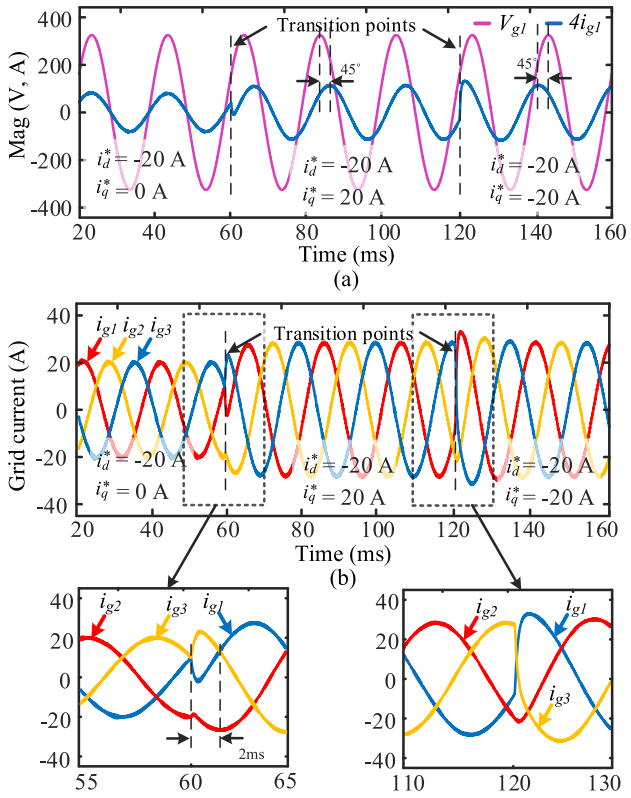

FIGURE 17. Step responses of the inverter under the proposed PWM technique while applying active and reactive power (a) single phase grid voltage and current (b) three phase grid current.

TABLE 5. Parameters used for performance analysis.

Parameter	Simulation	Experimental
DC-link voltage (V_{dc})	400 V	200 V
Grid voltage (V_g)	230 V (RMS)	120 V (RMS)
Grid frequency (f_{grid})	50 Hz	50 Hz
Inverter rating	8 kW	2 kW
Capacitor (C_1, C_2)	5000 uF	1600 uF
Carrier frequency (f_c)	5 kHz	5 kHz
Line filter (R, L)	2.5 mH + 0.04 Ω	1.2 mH + 0.1 Ω
Power switch (IGBTs)	IKW50N65F5	K50T60
Body diode	IKW50N65F5	DUNIA 10A10
DSP board	N/A	TMS320F28335
IGBT gate driver	N/A	TLP250

is made by applying reactive power (3.25 kW, 3.25 kVAR, $i_d^* = -20$ A, $i_q^* = -20$ A) through capacitive load to the grid. This time the grid current changed to 28.26 A, as same active and reactive power is applied. After the 2nd step change, the grid current leads the grid voltage by 45° which can be seen from Fig. 17(a). For the step changes, the controller tracks the reference grid current within 2 ms which is clearly seen from Fig. 17(b).

B. EXPERIMENTAL RESULTS

A 2kW reduced scale laboratory prototype is built in order to validate the proposed hybrid PWM technique. The parameters used in case study for both simulation and experiment are depicted in Table 5.

The photograph of the laboratory test platform is displayed in Fig. 18. To develop the adopted inverter topology total twelve IGBTs, two dc-link capacitors are needed. From the Infineon Technologies K50T60 IGBTs (650V, 80A) are used for constructing the laboratory prototype. Antiparallel body diode DUNIA 10A10 (10A, 1000V) is equipped with the IGBT to block the flow of reverse current. To produce the gate pulses for the IGBTs, TMS320F28335 DSP development board is utilized. The grid is considered in the laboratory using the California Instruments AMETEK CSW5550 programmable power supply. The gate pulses coming from the DSP board are insufficient for the IGBTs. Hence, the gate pulses of the DSP board are boosted up by a custom gate driver circuit which is designed by using TLP250 opto-couplers and B1212S-1W isolated dc-dc converters. Two dc power supply are used for powering up the system. In order to display the outputs, a four-channel oscilloscope (GDS-1104B) is used.

FIGURE 18. A photograph of the laboratory test platform.

The modulating signal and the carrier signal of the proposed hybrid PWM technique is depicted in Fig. 19(a) and Fig. 19(b), respectively. Comparing these two signals, gate pulses for the IGBTs of the adopted T-type NPC inverter are generated. The unfiltered line voltage and filtered three phase line current of the inverter under the proposed hybrid PWM technique are depicted in Fig. 20 and Fig. 21, respectively.

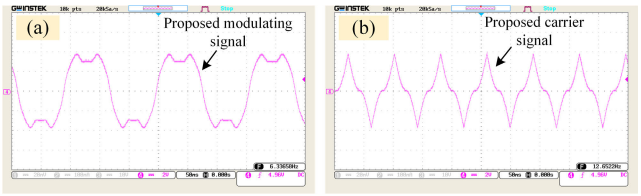

FIGURE 19. (a) Modulating signal and (b) carrier signal of the proposed hybrid PWM technique.

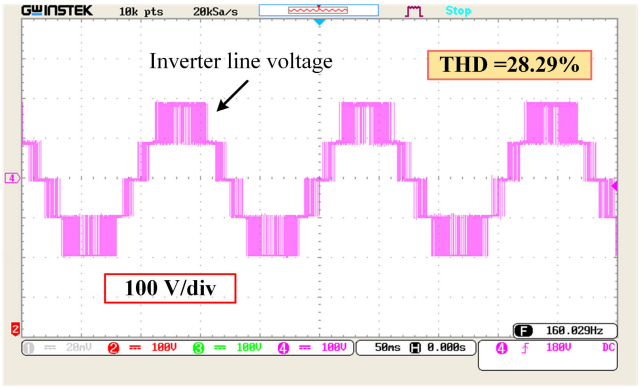

FIGURE 20. Unfiltered line voltage of the inverter under the proposed hybrid PWM technique.

28.29% unfiltered line voltage THD and 3.46% filtered line current THD are achieved by the experimental. On the contrary, the dc-link capacitor voltages are depicted in Fig. 22, which shows that 17.2 V maximum peak-to-peak capacitor voltage difference is achieved by the experiment.

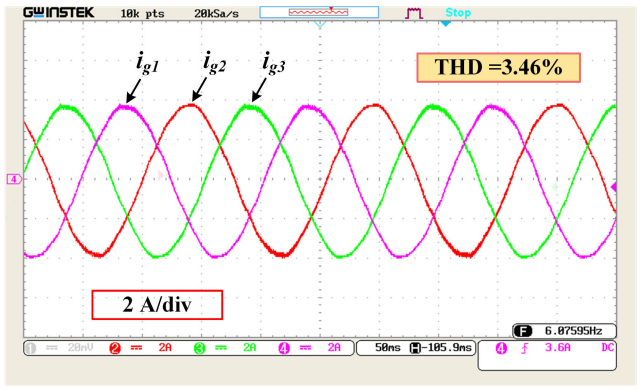

FIGURE 21. Filtered three phase line current under the proposed hybrid PWM technique.

The filtered three-phase grid voltage waveform under the proposed hybrid PWM technique is observed through the grid simulator, as depicted in Fig. 23. The grid voltage and grid current waveforms at unity, leading and lagging power factor condition are depicted in Fig. 24(a), 24(b) and 24(c), respectively. At unity power factor condition, the grid voltage and grid current are in same phase. At the leading power factor grid current leads the grid voltage by 90° whereas at the lagging power factor, the grid current lags the grid voltage by 90°.

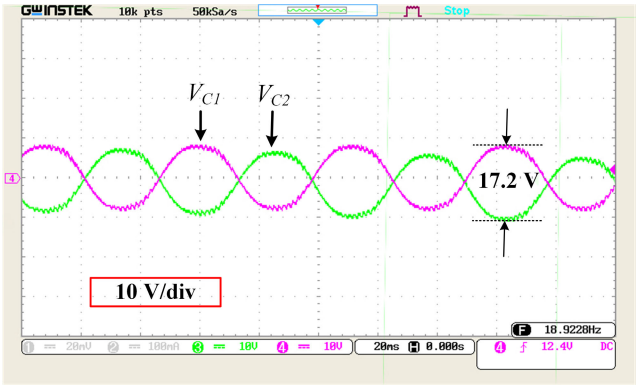

FIGURE 22. DC-link capacitor voltages under the proposed hybrid PWM technique.

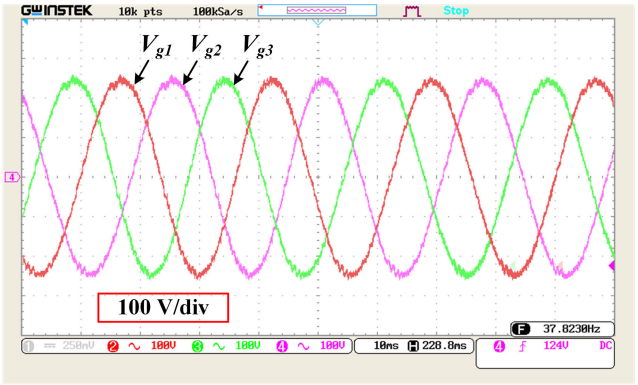

FIGURE 23. Three phase grid voltage (filtered) under the proposed hybrid PWM technique.

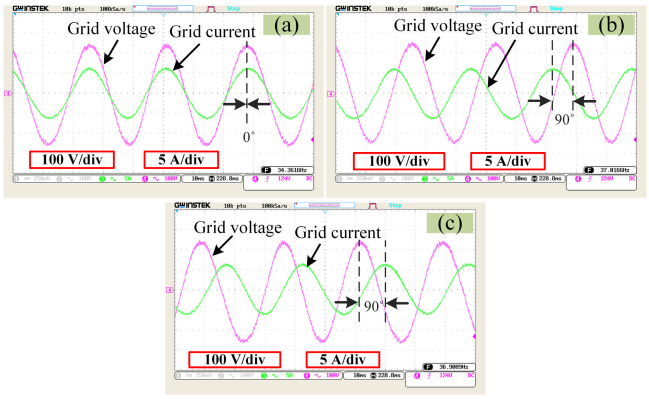

FIGURE 24. Grid voltage and grid current waveform at (a) unity, (b) leading and (c) lagging power factor under the proposed hybrid PWM technique.

Another important issue regarding the hardware implementation of the proposed PWM technique is associated with the computational burden of the DSP processor. The clock frequency of TMS320F28335 DSP control card is 150 MHz which is a constant term. By changing the counter maximum

value, a single operation execution time period can be easily tweakable. To generate only a 5 kHz carrier wave, it requires pre-scaling of the counter value, as it supports higher resolutions of the triangle wave.

Generating the proposed modified carrier wave in DSP control card, requires a sinusoidal function along with several arithmetic operations such as addition, multiplication and subtraction. A single instruction execution time for TMS320F28335 is 25ns. To generate a single period of proposed carrier wave, it takes 250ns worth of additional computing time compared to a conventional triangle wave. Considering only a 5 kHz carrier wave, the additional 250ns per instruction doesn't create any effect or additional computational burden on the DSP processor. Therefore, it can be said that there is not much computational burden associated with implementing the proposed hybrid PWM technique on DSP hardware.

VII. CONCLUSION

A hybrid PWM technique consisting of a modified modulating signal along with a modified carrier signal is suggested in this work to improve the performance of grid-tied T-type NPC inverter. The unfiltered output line voltage THD and the peak-to-peak dc-link capacitor voltage difference offered by the proposed modified hybrid PWM technique are 25.57% and 11.8 V, respectively which are lower than the existing SPWM, CSVPWM, THPWM and SDPWM techniques. Moreover, the total power loss of the proposed hybrid PWM technique is 278.3 W which is an upgrade of 3.6%, 2.73%, 2.74%, 0.57% than the existing SPWM, CSVPWM, THPWM and SDPWM techniques, respectively. Therefore, the proposed hybrid PWM technique can lower the thermal stress of the power switches by lowering the junction temperature generated through power loss. The total harmonic distortion of the output line voltage and the dc-link capacitor voltage difference obtained under the proposed modified hybrid PWM technique are 28.29% and 17.2 V, respectively, by experimental laboratory prototype which support the simulation results very well. Finally, it can be said that the well agreement between simulation and experimental results make the proposed hybrid PWM technique a better competitor in the field of solar PV fed grid-tied applications than other existing PWM techniques.

REFERENCES

[1] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan. 1999.

[2] A. Ahmed, S. P. Biswas, M. S. Anower, M. R. Islam, S. Mondal, and S. M. Muyeen, "A hybrid PWM technique to improve the performance of voltage source inverters," *IEEE Access*, vol. 11, pp. 4717–4729, 2023, doi: 10.1109/ACCESS.2023.3235791.

[3] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[4] S. Mondal, S. P. Biswas, M. R. Islam, and S. M. Muyeen, "A five-level switched-capacitor based transformerless inverter with boosting capability for grid-tied PV applications," *IEEE Access*, vol. 11, pp. 12426–12443, 2023.

[5] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[6] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[7] A. Bahrami and M. Narimani, "A sinusoidal pulsewidth modulation (SPWM) technique for capacitor voltage balancing of a nested T-type four-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1008–1012, Feb. 2019.

[8] S. Srivastava and M. A. Chaudhari, "Comparison of SVPWM and SPWM schemes for NPC multilevel inverter," in *Proc. IEEE Int. Students' Conf. Elect.,Electron. Comput. Sci. (SCEECS)*, Bhopal, India, Feb. 2020, pp. 1–6.

[9] W. Subsingha, "A comparative study of sinusoidal PWM and third harmonic injected PWM reference signal on five level diode clamp inverter," *Energy Proc.*, vol. 89, pp. 137–148, Jun. 2016.

[10] M. R. Islam, A. M. Mahfuz-Ur-Rahman, K. M. Muttaqi, and D. Sutanto, "State-of-the-art of the medium-voltage power converter technologies for grid integration of solar photovoltaic power plants," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 372–384, Mar. 2019.

[11] M. R. Islam, A. M. Mahfuz-Ur-Rahman, Md. M. Islam, Y. G. Guo, and J. G. Zhu, "Modular medium-voltage grid-connected converter with improved switching techniques for solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8887–8896, Nov. 2017.

[12] S. Haq, S. P. Biswas, M. K. Hosain, M. A. Rahman, Md. R. Islam, R. M. Elavarasan, and K. M. Muttaqi, "A modified PWM scheme to improve the power quality of NPC inverter based solar PV fed induction motor drive for water pumping," *IEEE Trans. Ind. Appl.*, vol. 59, no. 3, pp. 3019–3030, Jun. 2023.

[13] R. V. Chavali, A. Dey, and B. Das, "A hysteresis current controller PWM scheme applied to three-level NPC inverter for distributed generation interface," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1486–1495, Feb. 2022.

[14] A. Taghvaie, M. E. Haque, S. Saha, and Md. A. Mahmud, "A new step-up switched-capacitor voltage balancing converter for NPC multilevel inverter-based solar PV system," *IEEE Access*, vol. 8, pp. 83940–83952, 2020.

[15] A. Gopi, M. A. Kumar, J. Biswas, and M. Barai, "An optimized hybrid PWM strategy for five level NPC VSI with unequal DC-links in a PV system," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 3, pp. 766–776, Jul. 2022.

[16] J. Lara, L. Masisi, C. Hernandez, M. A. Arjona, and A. Chandra, "Novel single-phase grid-tied NPC five-level converter with an inherent DC-link voltage balancing strategy for power quality improvement," *Energies*, vol. 14, no. 9, p. 2644, May 2021.

[17] J. Zhou, J. O. Ojo, F. Tang, J. Haruna, and P. C. Loh, "A carrier-based discontinuous PWM for single and parallel three-level T-type converters with neutral-point potential balancing," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 5117–5127, Sep. 2021.

[18] T. D. Nguyen, D. Q. Phan, D. N. Dao, and H.-H. Lee, "Carrier phase-shift PWM to reduce common-mode voltage for three-level T-type NPC inverters," *J. Power Electron.*, vol. 14, no. 6, pp. 1197–1207, Nov. 2014.

[19] S. P. Biswas, S. Mondal, M. R. Islam, S. Haq, M. K. Hosain, and R. N. Shaw, "Advanced level shifted carrier based bus clamping PWM technique for a 54-pulse AC–DC converter fed MLI based induction motor drive," *IEEE Trans. Ind. Appl.*, vol. 60, no. 3, pp. 4109–4124, May 2024.

[20] S. Mondal, S. P. Biswas, M. R. Islam, M. K. Hosain, and R. Raad, "A seven-level switched-capacitor based transformerless inverter with modified PWM strategy to enhance the performance of grid-connected PV systems," *IET Power Electron.*, vol. 17, no. 7, pp. 855–868, May 2024.

[21] B. Chokkalingham, S. Padmanaban, and F. Blaabjerg, "Investigation and comparative analysis of advanced PWM techniques for three-phase three-level NPC-MLI drives," *Electric Power Compon. Syst.*, vol. 46, no. 3, pp. 258–269, Feb. 2018.

[22] V. Jayakumar, B. Chokkalingam, and J. L. Munda, "Performance analysis of multi-carrier PWM and space vector modulation techniques for five-phase three-level neutral point clamped inverter," *IEEE Access*, vol. 10, pp. 34883–34906, 2022.

[23] M. Sharifzadeh, H. Vahedi, A. Sheikholeslami, P.-A. Labbé, and K. Al-Haddad, "Hybrid SHM–SHE modulation technique for a four-leg NPC inverter with DC capacitor self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4890–4899, Aug. 2015.

[24] Y. Zhang, C. Yan, S. Zou, and D. Xu, "Hybrid PWM scheme for the grid inverter," in *Proc. IEEE 5th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Galway, Ireland, Jun. 2014, pp. 1–8.

SHAHRIAR HOSSAIN was born in Pabna, Bangladesh, in 2001. He received the B.Sc. degree in electronics and telecommunication engineering (ETE) from Rajshahi University of Engineering and Technology (RUET), Rajshahi, Bangladesh, in 2024. He is currently taking preparation for his master's degree admission. His main research interests include power electronics and applications, including multilevel inverters, PWM techniques, thermal stability and reliability of power converters, GaN devices, and grid integration of renewable energy sources.

SHUVRA PROKASH BISWAS (Graduate Student Member, IEEE) received the B.Sc. degree in electronics and telecommunication engineering (ETE) and the M.Sc. degree in electrical and electronic engineering (EEE) from the Rajshahi University of Engineering and Technology (RUET), Rajshahi, Bangladesh, in 2017 and 2021, respectively. He is currently pursuing the Ph.D. degree with the School of Electrical, Computer and Telecommunications Engineering (SECTE), University of Wollongong (UOW), Wollongong, NSW, Australia.

From December 2021 to February 2024, he was an Assistant Professor with the Department of ETE, RUET. He has authored and coauthored more than 95 technical papers and two book chapters. His research interests include power electronics, motor drives, renewable energy, advanced PLLs design for grid synchronization, integration of grid forming and grid following inverters, stability improvement of zero inertia power systems, and hardware implementation considerations of power converters and controls with MCU, DSP, and FPGA. He received the Best Paper Awards at ICECTE 2019, IEEE ASEMD 2020, IEEE IAS GUCON 2021, IEEE IAS ICCCA 2021, ICEEE 2022, ICECE 2022, IEEE ASEMD 2023, and EICT 2023. He was also a recipient of the Star Reviewer Award from IEEE TRANSACTIONS ON ENERGY CONVERSION, in 2022. He has served as a Reviewer for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON ENERGY CONVERSION, IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, IEEE SYSTEMS JOURNAL, and IEEE ACCESS.

SUDIPTO MONDAL (Student Member, IEEE) was born in Rajbari, Dhaka, Bangladesh, in 2002. He is currently pursuing the B.Sc. degree in electronics and telecommunication engineering (ETE) with the Faculty of Electrical and Computer Engineering, Rajshahi University of Engineering and Technology (RUET), Rajshahi, Bangladesh.

He has authored and coauthored more than 25 technical papers in international journals and conference proceedings. His current research interests include power electronics, power quality, electrical machines and drives, grid integration of renewable energy sources, hardware implementation of power electronic systems with various DSP processors, and smart micro-grids. He received the Best Paper Awards and the Best Presenter Awards at ICECE 2022, IEEE ASEMD 2023, and EICT 2023. He has served as a Reviewer for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, and IEEE ACCESS.

MD. RABIUL ISLAM (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Technology Sydney (UTS), Sydney, Australia, in 2014.

He is currently a Senior Lecturer with the School of Electrical, Computer, and Telecommunications Engineering (SECTE), University of Wollongong (UOW), NSW, Australia. He has received several funding from the Government and Industries, including in total $5.48 million from the Australian Government through the Australian Research Council (ARC) Discovery Project (DP) 2020 titled "A Next-Generation Smart Solid-State Transformer for Power Grid Applications" and the ARC Industrial Transformation Training Centre Project 2021 titled "ARC Training Centre in Energy Technologies for Future Grids." He has authored or coauthored more than 400 papers including more than 110 IEEE TRANSACTIONS/IEEE journal articles. He has written or edited nine technical books published by Springer and Taylor & Francis. His research interests include power electronic converters, renewable energy technologies, power quality, electrical machines, electric vehicles, and smart grids. He has received several Best Paper Awards including two Best Paper recognitions from IEEE TRANSACTIONS ON ENERGY CONVERSION, in 2020. He is serving as an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON ENERGY CONVERSION. As a lead Guest Editor, he has organized the first joint IEEE Industrial Electronics Society and IEEE Power and Energy Society Special Section titled "Advances in High-Frequency Isolated Power Converters." He is an Editor of the Book Series titled *Advanced Power Electronics Converters* (CRC Press, Taylor & Francis Group). He is the Vice-Chair of IEEE New South Wales (Australia) Joint Chapter IAS/IES/PELS. He is the Australia/Oceania Liaison Officer for the IEEE IAS Transportation Systems Committee. He has organized many international conferences in different countries. He was a keynote speaker for many international conferences. He is one of the Chief Investigators of the ARC Training Centre in Energy Technologies for Future Grids and the Theme Leader of the Australian Power and Energy Research Institute.

AFEF FEKIH (Senior Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the National Engineering School of Tunis, Tunisia, in 1995, 1998, and 2002, respectively. She is currently a Full Professor with the Department of Electrical and Computer Engineering and the Chevron/BORSF Professor of engineering with the University of Louisiana at Lafayette. She has authored or coauthored more than 200 publications in international journals, chapters, and conference proceedings. Her research interests include control theory and applications, including nonlinear and robust control, optimal control, and fault-tolerant control with applications to power systems, wind turbines, unmanned vehicles, and automotive engines. She is a member of the editorial board of the IEEE Conference on Control Technology and Applications, the IEEE TC on Education, and the IFAC TC on Power and Energy Systems.