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RESEARCH ARTICLE

A Power Dividing Rectenna System for High-Power Wireless Power Transfer for 2.45-GHz Band

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ABSTRACT There has been growing interest in the field of wireless power transfer (WPT), especially for a high-power (Watt-level) application. Rectifiers are essential components for WPT, as they convert incoming RF into DC power. However, conventional Schottky diodes used in WPT exhibit their highest efficiency at low power levels typically less than few Watts. To address this limitation, we introduce a power dividing rectenna system that can handle beyond several Watts of input RF power. The proposed rectenna consists of a single patch antenna integrated with a radial power divider, whose output ports are connected to rectifiers. In this way, incident RF power can be distributed into lower levels at which Schottky diode-based-rectifier can accommodate. Via simulation and measurement, we demonstrate that the input power (about 10 W) received through the proposed structure can be uniformly distributed to each output port of the divider to be rectified at lower power levels, which are then combined at DC to provide several Watts of DC power. The proposed rectenna can be utilized in WPT applications requiring beyond several Watts. Furthermore, by configuring the proposed structure into an array, even higher power handling can be achieved for applications that require hundreds of Watts.

INDEX TERMS Wireless power transfer (WPT), power divider, rectenna, energy harvesting (EH).

NOMENCLATURE

W_1	Width of each power-dividing line at center disk.
W_2	Diameter of center disk.
W_3	Width of each power-dividing line at output.
H_1	Substrate thickness of top layer.
H_2	Substrate thickness of bottom layer.
L_1	Diameter of substrate (laminate).
L_2	Diameter of center via.
L_3	Diameter of center hole.
L_4	Diameter of patch antenna.
N	Output port of power-dividing line.
H	Input port of horn antenna.
S_{NH}	Ratio between the power delivered to each output port and transmitted power from horn antenna.
P_r	Total received power by patch antenna.
P_N	Delivered power to each output port.
P_t	Transmitted power from horn antenna.
G_t	Gain of horn antenna.
G_r	Gain of patch antenna.
λ	Wavelength in free space.
R	Distance between horn antenna and patch antenna.

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I. INTRODUCTION

Recent years have seen active research in the field of wireless power transfer (WPT) and energy harvesting (EH), which provide wireless powering solutions for electronic devices [1], [2], [3], [4]. In the case of WPT, it can be

applied across a wide range of power levels, from low-power IoT and small electronic devices [5], [6] to mobile devices and drones requiring power in the several-Watt range [7]. Additionally, space solar power systems or satellites used for energy transmission require even higher power levels [8], [9]. While there is a growing demand for Watt-level WPT in high-power applications, stable rectification converting RF power to DC power remains a significant bottleneck due to the overwhelming received power. Since such excessive input power to the receiver can induce nonlinearity, distortion, and potential damage to the components, it would be desirable to have a robust RF-to-DC rectifier capable of withstanding high input power to obtain high DC power.

Most RF-to-DC rectifiers utilize Schottky diodes, known for their low voltage drop and fast switching characteristics, to achieve high rectification efficiency, especially at input powers below several tens of dBm [10], [11]. However, the input power levels compatible with Schottky diodes, which have low breakdown voltage, are not suitable for the aforementioned Watt-level WPT. Alternatively, GaN diodes with extremely high breakdown voltage can be employed to handle high input powers, but there are only a few commercially available products [12], [13], [14]. Another approach for dealing with high input power levels while using conventional Schottky diodes is to employ a power dividing network to distribute the received power before the rectification process. Here, the role of the power dividing network is to evenly distribute high input RF power to each rectifier connected to the output ports of the power divider, enabling the conversion of RF power into DC power at a lower level.

Various rectifier designs based on power dividing networks have been proposed in recent studies to mitigate the excessive input power at the rectifier stage, allowing stable operation and protection for the rectifier [15], [16], [17], [18], [19], [20]. In [15] and [16], a transformer-type architecture was adopted, and the system was designed to achieve maximum efficiency in delivering power to the rectifier by utilizing a microstrip line-based power dividing network. Additionally, one of the conventional divider configurations, such as the Wilkinson dividers [17] or T-junction dividers [18], [20] were used in the rectifiers. In [19], a rectenna array consisting of antennas, power distributing network, and rectifier array with an enhanced RF power distributing strategy was proposed. Although the rectifier designs using power dividing networks in these studies were validated to be effective in providing improved rectification efficiency even under high input power conditions, individual antennas, power dividing networks, and rectifiers are connected through cables or connectors.

In this paper, we present a novel power dividing rectenna system based on Schottky diodes, capable of receiving and rectifying high power in the range of several watts and beyond. The key concept of the proposed rectenna system lies in the integration of its main components, i.e. antenna and power dividing network, into a single structure on a double-stacked substrate platform, as shown in Fig. 1:

1) A circular patch antenna on the front side (bottom layer) for receiving RF power at 2.45 GHz band

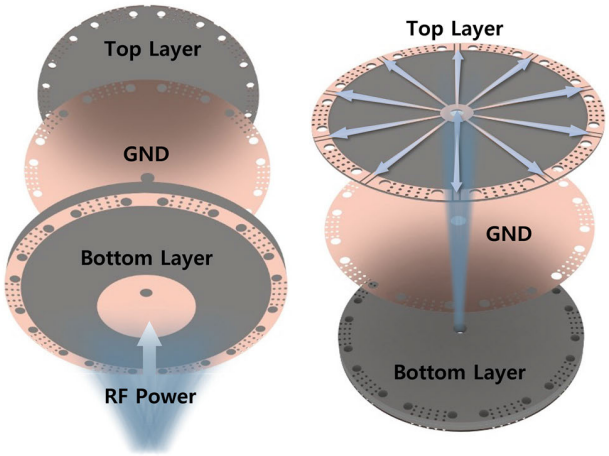

FIGURE 1. Illustration of the signal flow in the proposed integrated design.

2) A 10-way radial power divider on the back side (top layer) to evenly distribute the received high RF power which is fed to RF-to-DC rectifiers connected to the output port of power divider, whose output DC power are later combined

The circular patch antenna receives RF power, and the received power is distributed to each output port on the opposite side. Subsequently, Watt-level RF-to-DC rectifiers are connected to each output port of the 10-way power divider, and the divided power becomes the input power to these rectifiers. This unique configuration allows for an efficient handling of high input RF power at 10 Watts or more by distributing it into lower power levels, which can be effectively rectified using Schottky diodes. We demonstrate the proposed rectenna design via simulation and measurement.

This paper is organized as follows. In Section II, we present the design of the proposed rectenna system that integrates a patch antenna and power divider. Although the antenna and power divider are designed as a single integrated unit, the design method for each component is described separately. Section III describes the design of a Watt-level rectifier connected to each output port of 10-way power divider. The complete power-dividing rectenna system is realized by connecting the rectifiers to the power divider. In Section IV, the measurement results of the proposed power dividing rectenna system are presented. This section also demonstrates the uniformity of power distribution across the output ports of the power divider, as well as the rectification efficiency. Section V presents the expected layout of arranging the power-dividing rectenna system in an array configuration for scalability into a larger system. Finally, we conclude the paper in Section VI.

II. DESIGN OF POWER DIVIDING RECTENNA SYSTEM

Fig. 2 illustrates the design of the proposed power dividing rectenna structure before rectifiers are connected. A circular patch antenna and 10-way radial power divider are integrated in a via-coupled stacked-substrate configuration. One key

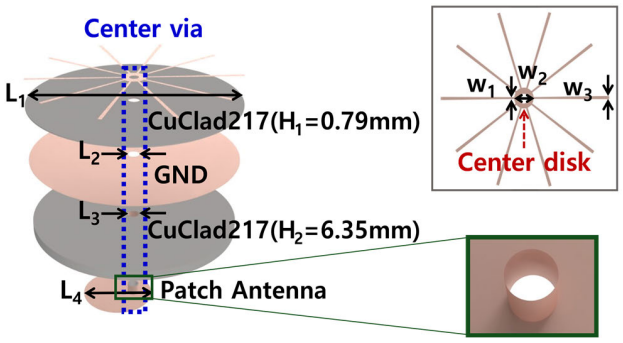

FIGURE 2. Layout of 10-way radial power divider integrated with patch antenna.

TABLE 1. Design parameters of 10-way power divider integrated with circular patch antenna.

Parameter	Description	Value (mm)
W_1	Width of each power-dividing line at center disk	1.35
W_2	Diameter of center disk	16
W_3	Width of each power-dividing line at output	2.36
L_1	Diameter of substrate (laminate)	140
L_2	Diameter of center via	8
L_3	Diameter of center hole	6.25
L_4	Diameter of patch antenna	50

element of the proposed design is the utilization of only a single antenna system capable of converting beyond several Watts. Such a configuration would be advantageous when employed in an array, as array elements can collectively handle much higher power if necessary. The radial power divider is designed to equally distribute the input power coupled through the center via [21]. To accommodate the radial configuration of the proposed structure, circularly cut PCB laminates with a diameter (L_1) of 140 mm are used. On the side of the stacked structure where the patch antenna is printed, a 6.35 mm-thick Rogers CuClad217 ($\varepsilon_r = 2.2$) is used. On the opposite side where the 10-way power divider is printed, the same laminate with a 0.79 mm thickness is used. Table 1 shows the design parameters of the integrated patch antenna and 10-way power divider, which are optimized to achieve impedance matching for the entire configuration, as described in the following paragraph. The process of the signal flow is as follows. The high power received by the patch antenna is coupled through the center via to the center disk on the 10-way power divider layer and then divided radially outward into ten output ports, where rectifiers will be connected.

To ensure the lossless transmission of the received signal from the patch antenna to the output ports, the impedance for the entire configuration should be accurately matched. The first consideration is the impedance of the microstrip lines of the divider, which are connected to the center disk in parallel.

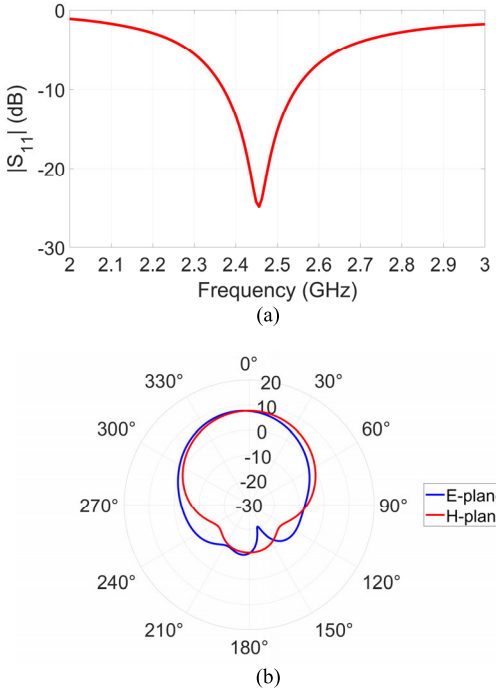

FIGURE 3. Simulated (a) reflection coefficient and (b) radiation pattern of the patch antenna.

To appropriately arrange ten output lines within the limited space of the center disk and prevent physical and electrical interference between the lines, the width of each line should be minimized. Therefore, the width of each radial line in contact with the center disk (W_1) is set to 1.35mm to have a characteristic impedance of 100 Ω. To match the output of each line at the edge of the substrate to 50 Ω for connection with rectifiers, an impedance transition is placed by linearly tapering its width to 2.36 mm (W_3). Given that the ten radial lines are in a parallel connection to the center disk, the port at the center disk is set to have an impedance of 10 Ω. Since the center via acts as a coaxial feed to the patch antenna, the diameter of the center hole (L_3) in the antenna substrate (through which the center via enters) is set to 6.25 mm, and the position of the via on the circular patch is adjusted to match the input impedance of the antenna to 10 Ω [22].

The design and optimization of the patch antenna and divider are carried out with CST Studio Suite. First, to evaluate the performance of the patch antenna, simulation is conducted with only the center via serving as the 10 Ω feed, excluding the divider layer. The simulated reflection coefficient of a single patch antenna is shown in Fig. 3 (a), where the impedance bandwidth is observed to be approximately 7 %. Additionally, the radiation pattern at 2.45 GHz is depicted in Fig. 3 (b), with the maximum gain of 7.84 dBi.

A fabricated structure combining the patch antenna and 10-way radial power divider is shown in Fig. 4. The top layer depicts the location of the output ports, while the patch antenna is positioned on the bottom layer. Simulation and measurement are conducted to verify whether this structure

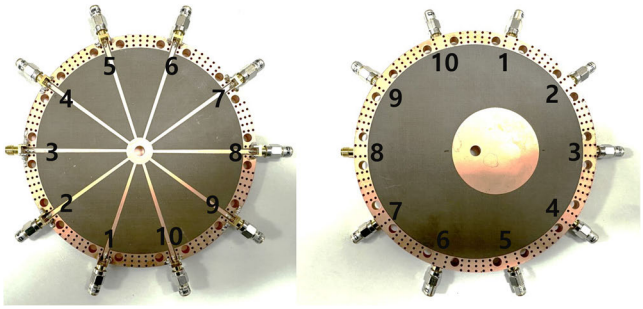

FIGURE 4. Photograph of the fabricated stacked structure: (a) the radial 10-way power divider on the top layer, and (b) the patch antenna on the bottom layer.

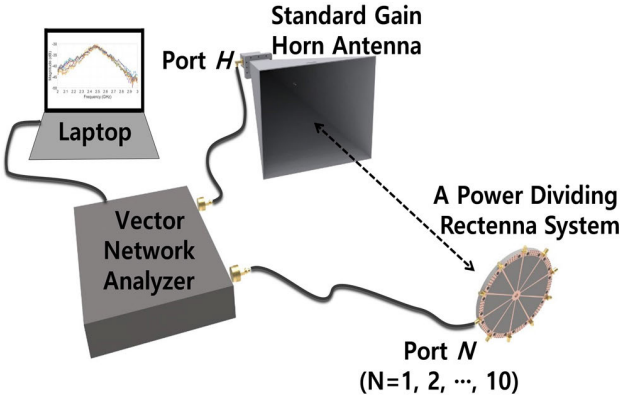

FIGURE 5. A measurement setup for power division verification with VNA.

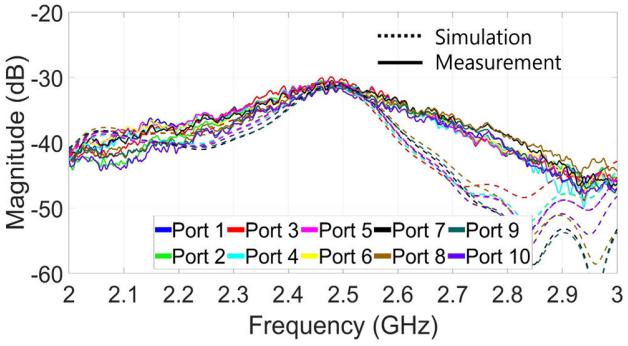

FIGURE 6. Measured (solid) and simulated (dashed) $|S_{NH}|$ at each output port of radial 10-way power divider.

effectively receives the power through the antenna at the target frequency and uniformly distributes it through the power divider. In the simulation, an incident plane wave is used as an input to the patch antenna and the power at each output port is probed. In the measurement, a standard gain horn is used as the transmitting antenna as shown in Fig. 5. An Anritsu MS46122B vector network analyzer (VNA) is used to measure the relative output level at each output port of the divider. In Fig. 6, the simulated and measured $|S_{NH}|$ are shown, where each $|S_{NH}|$ ($N = 1, 2, \cdots, 10$) corresponds to the ratio between the power delivered to each output port and the transmitted power from the horn antenna.

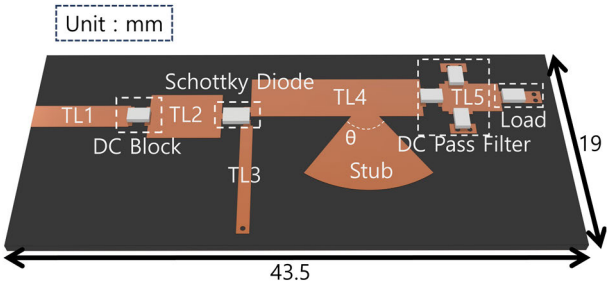

FIGURE 7. Illustration of the proposed rectifier.

The simulated and measured results show a good agreement, where the input power is uniformly distributed at the output ports while the magnitude is highest at the target frequency of 2.45 GHz. Note that the value of $|S_{NH}|$ is the relative level normalized to the transmitted power and it does not indicate any physical power, as the purpose of this measurement is to confirm the uniform distribution of the received power at the outputs.

Since the proposed structure has 10 output ports, it is difficult to directly measure the antenna gain of the fabricated structure. However, the Friis equation can be utilized to validate the gain of the antenna from the measured $|S_{NH}|$ in Fig. 5, which can be expressed as

$$\sum_{N=1}^{10} |S_{NH}|^2 = \frac{\sum_{N=1}^{10} P_N}{P_t} = \frac{P_r}{P_t} = \frac{G_t G_r \lambda^2}{(4\pi R)^2} \tag{1}$$

where P_r is the total received power by the patch antenna, P_N is the delivered power to each output port, P_t is the transmitted power from the horn antenna, G_t is the gain of the horn, G_r is the gain of the proposed structure, λ is the wavelength, and R is the distance between the antennas. Since the sum of $|S_{NH}|^2$ should be the normalized total received power and all other parameters are known, we can solve for G_r in (1), which in this case is obtained to be 7.25 dBi, showing a close agreement between the simulation and measurement.

III. RECTIFIER DESIGN

In the previous section, the design and performance of the combined structure of antenna and radial divider are presented. In this section, we present the design of a rectifier connected to each output port and finally complete the power dividing rectenna system. Since the purpose of the proposed rectenna system is to convert high RF power to DC power exceeding several watts, we aimed to design a rectifier that can handle power levels above 1 W. This ensures that the system can handle more than 10 W when connected to the radial divider. To this end, an HSMS-282C Schottky diode with a relatively high breakdown voltage of at least 15 V is utilized. As shown in Fig. 7, the rectifier is designed as a voltage doubler type, consisting of two diodes with a DC block, DC pass filter, inductor, and load resistor. The design process begins by verifying

TABLE 2. Numerical parameters of the designed rectifier.

	TL1	TL2	TL3	TL4	TL5	Stub (θ=70°)
Width (mm)	2.2	4.5	1	4	3	2.3
Length (mm)	8	6	10.2	14.3	5	6.9

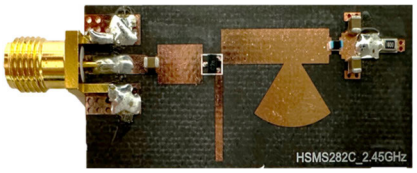

FIGURE 8. Fabricated 1W-level rectifier utilizing a Schottky diode.

the performance of the DC pass filter, which is in front of the load resistor. An inductor is positioned at the front end of the DC pass filter to operate as an RF choke. Since the rectifier inevitably generates harmonic distortion at the diodes that may lower the power conversion efficiency, a harmonic suppression approach is employed by connecting TL3 and TL4 to the rear of the diodes. The operating band is split into two half-bands, with f_1(1.9 GHz) and f_2 (2.8 GHz) being the center frequencies of the low half-band and high half-band, respectively. TL3 connected to the diode anode has a length equal to the quarter-wavelength of the second harmonic of f_1, ensuring the suppression of this harmonic. Similarly, TL4 connected to the diode cathode has a length equal to the quarter-wavelength of the second harmonic of f_2, effectively suppressing this harmonic [26]. Moreover, the length of TL3 and TL4 are optimized to reduce impedance variations over a wide frequency range in front of the diode, allowing a wide bandwidth of the rectifier. The numerical parameters of the rectifier are listed in Table 2.

The rectifier is then fabricated on a Rogers RT/Duroid 5880 substrate (thickness of 0.79 mm) as shown in Fig. 8. The reflection coefficient ($|S_{11}|$) of the proposed rectifier is evaluated with Advanced Design System (ADS), and the results are shown in Fig. 9. The simulated reflection coefficient in Fig. 9 is the result when input power level is at 31 dBm. It depends on the input power level due to the nonlinear characteristics of the diode. Here, a wide impedance bandwidth of 96.7 % (0.55 – 2.92 GHz) is achieved, safely covering the target frequency of 2.45 GHz. It is to be noted that the lack of vector network analyzer that can provide over 31 dBm prevented us from obtaining measured reflection coefficients. Nevertheless, the experimental verification of the rectifier can be confirmed in the rectification measurement.

The rectification performance of the fabricated rectifier is carried out with an Agilent E4436B signal generator and AR100S1G4 high power amplifier as the power source and a multi-meter at the output of the rectifier. Fig. 10 shows the simulated and measured rectification efficiency of the rectifier at the optimal load resistance of 160 Ω at the target frequency of 2.45 GHz. The simulated maximum efficiency

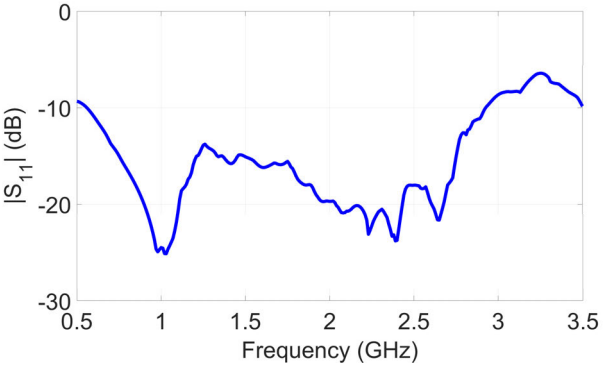

FIGURE 9. Simulated reflection coefficient of rectifier.

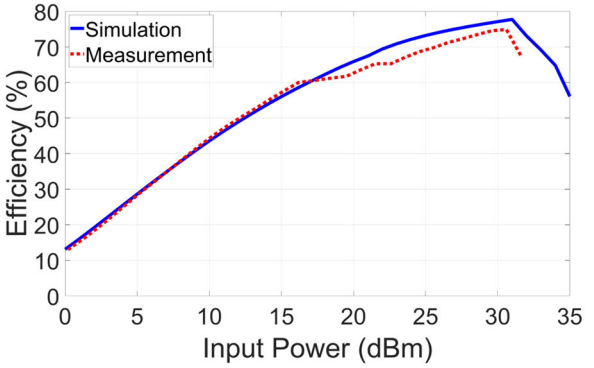

FIGURE 10. Simulated (solid blue) and measured (dashed red) power conversion efficiency of the proposed rectifier.

TABLE 3. Comparison between the proposed rectifier and other rectifiers that use the same Schottky diode (HSMS-282X).

Ref.	Diode	No. of Diode	Maximum Efficiency	Input Power
[18]	HSMS-282C	1	80.9 %	20 dBm
[23]	HSMS-282B	1	64.3 %	24 dBm
[24]	HSMS-282C	4	80 %	27 dBm
[25]	HSMS-2822	4	58 %	30 dBm
This work	HSMS-282C	2	74.9%	30.6 dBm

of 77.7 % occurs at 31 dBm of input power, while the measured maximum efficiency of 74.9 % occurs at 30.6 dBm of input power, showing a good agreement between simulation and measurement. Note that the purpose of the designed rectifier is to convert watt-level input power, enabling the rectenna system to handle high power efficiently. Table 3 presents a performance comparison between the proposed rectifier and other rectifiers that use the same Schottky diode model (HSMS-282X) and operate at 2.45 GHz. The proposed rectifier demonstrates a high rectification efficiency for input power levels above 1 W compared to other rectifiers using the same diode. Ten identical rectifiers are then fabricated for the proposed rectenna system.

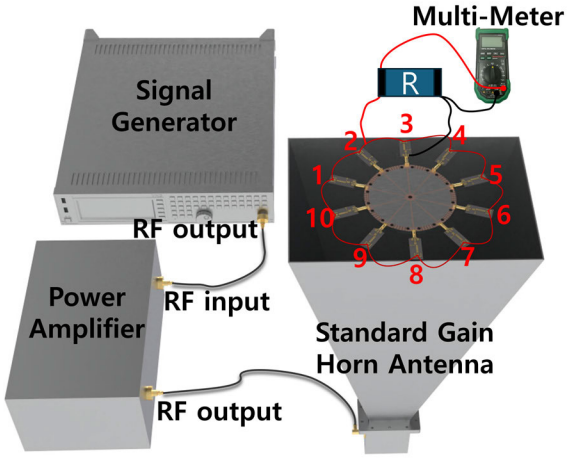

FIGURE 11. Measured setup for the overall power dividing rectenna system.

IV. VERIFICATION OF THE POWER DIVIDING RECTENNA SYSTEM

To validate the overall power dividing rectenna system, the rectifiers are connected to the output port of the radial power divider and the DC output ports are connected in parallel to have a single DC output. In lieu of high enough amplifier that can sufficiently deliver more than 10 W at a far-field distance, we have conducted the measurement by placing the rectenna in front of the horn aperture as shown in the Fig. 11. Even though such a setup places the rectenna in the near-field of the horn, the field distribution at the aperture of the horn (TE_{10} mode) can be regarded as a quasi-uniform plane wave especially towards the center where the rectenna is placed. Before measuring the power dividing rectenna system, we first measure the RF power delivered to each output port of the divider with the measurement setup shown in Fig. 11, while probing each port with an Agilent E4407B spectrum analyzer instead of connecting the rectifiers. The receiving patch antenna is positioned directly in front of the transmitting horn antenna, and the gain of the amplifier is adjusted to enable the receiving antenna to capture approximately 10 W of power. The measured results of RF power delivered to each output port are shown in Table 4. Even when the system is placed in front of the horn antenna aperture, the power delivered to each output port is quite uniform, and the sum of all power delivered to the output ports is 9.77 W.

After connecting the rectifiers to all output ports, the output DC power of the proposed rectenna system is measured. Since the rectifiers are connected in parallel to each output port, the load resistance value is varied to find the optimal value that yields the highest RF-to-DC power conversion efficiency. The measurement results shown in Fig. 12 demonstrate that the load resistance R (depicted in Fig. 11) is varied from 10 Ω to 22 Ω with an increment of 2 Ω. The highest RF-to-DC power conversion efficiency of 69 % is achieved at 18 Ω. When the rectification efficiency is measured individually, the maximum efficiency is achieved

TABLE 4. Power delivered to each output port when the power divider is placed in front of the horn antenna aperture.

Port	RF Power (W)	Port	RF Power (W)
P_1	0.97	P_6	0.98
P_2	1.02	P_7	1.00
P_3	0.94	P_8	0.93
P_4	1.02	P_9	1.02
P_5	0.98	P_{10}	0.90
$P_1+P_2+P_3+\cdots\cdots+P_{10} = 9.77$ W			

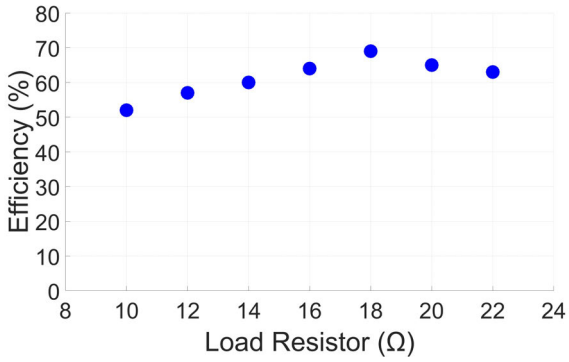

FIGURE 12. Measured power conversion efficiency of the proposed power dividing rectenna system.

at a load resistance of 160 Ω. However, when 10 rectifiers are connected in parallel, the optimal load resistance is found to be 18 Ω instead of 16 Ω (which would be one-tenth of 160 Ω) due to slight changes in the impedance values of the rectifiers. Ideally, if the power of 30.6 dBm at which the rectifier achieves its highest efficiency is delivered identically to each output port, the efficiency of the power dividing rectenna system in the parallel structure would be close to 74.9%, the maximum efficiency of a single rectifier. However, in practice, the power delivered to all output ports is lower than 30.6 dBm, resulting in a slightly reduced efficiency. Nevertheless, comparing the efficiency of the proposed power dividing rectenna system with the rectifier efficiency in Fig. 10 and the power delivered to each port in Table 4, it is evident that the system demonstrates a high efficiency.

V. DISCUSSION

In the previous section, we verify that approximately 10W of RF power is received through a single antenna, while rectification efficiency of 69 % is achieved when the rectifiers connected in parallel. In this section, we discuss the scalability of the proposed power dividing rectenna system. To further increase the amount of RF power to be rectified, the current structure can be modified to use an array configuration instead of a single antenna. By employing an array structure for receiving RF power, the proposed

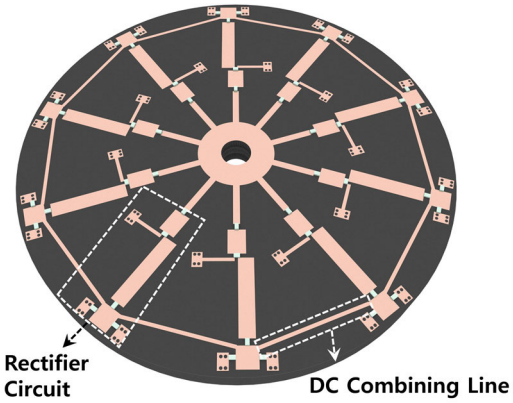

FIGURE 13. Illustration of the expected configuration when rectifier circuits are integrated onto the same substrate with the power divider.

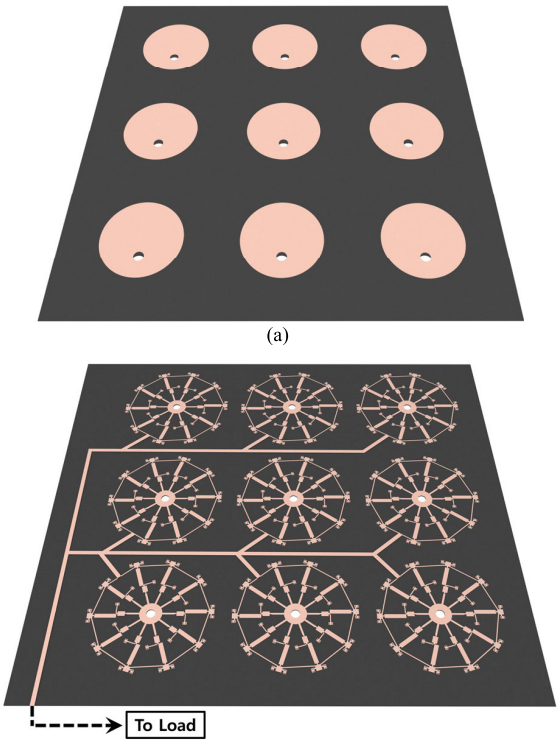

FIGURE 14. Expected configuration when the proposed power dividing rectenna system is arranged into a rectenna array (a) antenna layer, (b) output layer.

system can receive and rectify higher power incident level compared to a single antenna setup. To implement this array configuration, the spacing between the antennas of each power dividing rectenna system needs to be set at 0.5 λ. However, achieving this spacing between antennas requires reduction of overall form factor. One approach to minimize the form factor is to optimize the layout of the top layer (divider layer), particularly the length of the radial lines. By properly placing the output ports and minimizing the length of the radial lines, we can reduce the overall footprint of the system. Additionally, directly integrating the rectifier circuit at the end of the radial lines, as shown in Fig. 13, further contributes to the size reduction. These modifications not only enable the implementation of an array structure but also enhance the scalability and extendibility of the proposed power dividing rectenna system, allowing it to efficiently capture and rectify higher levels of incident RF power.

Assuming that the power dividing rectenna system is applied in a 3 × 3 array structure as shown in Fig. 14 (a), it is possible to receive up to 90 W of RF power. The expected configuration of the structure where each power dividing rectenna system connected in parallel can be seen in Fig. 14 (b). The parallel connection of these units ensures efficient combining of the rectified DC power. With its ability to scale up to a larger array, the proposed power dividing rectenna system presents a promising solution for harvesting substantial amounts of RF power and converting it into usable DC power.

VI. CONCLUSION

In this paper, a power dividing rectenna system capable of receiving and rectifying several-Watt level power is proposed and verified. The proposed rectenna consists of a single patch antenna integrated with a 10-way radial power divider in a stacked substrate configuration, where each output of the power divider is connected to a rectifier that can handle up to a few watts, thereby collectively handling about 10 W of incident RF power. Through simulation and measurements, it is confirmed that the power received through the proposed structure can be uniformly distributed to each output port of the power divider. Furthermore, the rectification measurement of the overall structure demonstrates the ability of the proposed rectenna to convert more than several Watts of RF power into DC power, overcoming the limitations of Schottky diode-based single rectenna that typically peak at less than few Watts. This scalable and extendable design opens up new possibilities for WPT and EH in various applications, ranging from low-power devices to high-power industrial and commercial systems.

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