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RESEARCH ARTICLE

A Fully Integrated, Switched-Capacitor DC–DC Buck Converter Featuring an Inverter-Based Comparator

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ABSTRACT A fully integrated ultra-low-power step-down DC-DC converter in 65nm is presented. The purpose of this converter is to convert battery voltage levels, in the range of 2.5-3V, to digital and mixed-signal voltage levels for low-power always-on domains. A down-conversion with a ratio of 5:1 is employed to provide a digital voltage level near the threshold voltage (Vth), which ranges from 0.55-0.6V. Higher voltage levels, such as 1.2V and 1.8V, are also made available for analog circuits. To achieve high-speed regulation at low power, an inverter-based comparator is utilized. Silicon results indicate an Efficiency-Enhancement-Factor (EEF) of 66% and a power density of 2.56 mW/mm^2 at an output power of 100µW. These parameters represent the state-of-the-art for this level of power. The DC-DC converter exhibits a fast transient response, leading to minimal droops and overshoots, even for a 50pF output capacitor.

INDEX TERMS DC–DC conversion, switched-capacitor, voltage regulator.

I. INTRODUCTION

Internet-of-Things (IoT) devices at the edge are required to operate at ultra-low average power levels of 10's of µW and lower [1]. To conserve power, IoT chips operate at a very low activity factor in most computing circuits. However, always-on circuits, such as wakeup circuits, reference voltages, real-time clocks, and the digital circuits controlling them can be greedy energy consumers in the system, despite the fact that they are low-power. The main voltage regulators of IC active circuits may have very poor efficiency at such light loads. Although a Low-Drop-Out linear regulator (LDO) can sometimes be utilized for low power modes, their main limitation lies in the fact that the LDO efficiency is limited by the ratio of the output to the input voltages. Therefore, an efficient on-die DC-to-DC converter is crucial to regulating power of the battery voltage for these low-power domains. In always-on applications, digital domains operate at or near the threshold voltage (Vth), typically 0.5-0.6V, while analog circuits require higher voltages (1.2-1.8V). There has been scant research dealing with on-die switched capacitor DC-DC converters in the 10-100µW domain [2], [3], [4], [5], [6], [7], [8].

The Efficiency-Enhancement-Factor (EEF) is an important parameter when comparing DC-DC buck converters, since it takes into account both the efficiency and the Voltage-Conversion-Ratio (VCR) [2]. EEF is defined as

$$EEF = 1 - \frac{\eta_{lin}}{\eta_{sw}} \tag{1}$$

where ηlin is the efficiency of an ideal LDO and ηsw is the efficiency of the DC-DC converter under consideration. For instance, a DC-DC converter with a VCR of 0.8 and an efficiency of 80% may not be useful, since it is similar to an LDO, thus resulting in an EEF of 0. Conversely, a DC-DC converter with an efficiency of 50% but a VCR of 0.2 would have an EEF of 60%, indicating better performance than an LDO. The VCR used for EEF calculation is the actual achieved ratio between Vout and Vin which is slightly lower than the topology VCR determined by the number of flying

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capacitors. The reason for that lies in the fact that "real" VCR takes into account additional IR drop that always exists at the output voltage. In the low-voltage domain, the speed of the DC-DC converter is crucial because any voltage droop caused by current surges can affect digital speed paths.

This paper describes a switched capacitor DC-DC converter for low power always-on domains and is a journal extension of the work reported in [9]. An inverter-based amplifier was used for loop regulation because it is low-power and high-speed which helps prevent droops and overshoots during load transients. In addition, the fast regulation loop allows the circuit to operate with a low output capacitance of 50 pF. The DC-DC converter operates at battery voltage levels, Vbat, of 2.5-3 V. The main output voltage (Vout=0.55V nominally) is generated for the digital circuitry as well as the intermediate voltage levels (VDD1=1.8V and VDD2=1.2V), which can be utilized for analog circuits. Combining several analog techniques (counter-phase cores, floating well circuit, and multi-level clocking) with a novel way of output voltage detection (inverter-based comparator) the proposed topology was able to achieve contribution in terms of EEF and Power Density. Additionally, a very fast transient response was accomplished.

II. ARCHITECTURE AND CIRCUIT DESIGN

A. CONTROL LOOP AND CLOCK GENERATION

Figure 1 illustrates a simplified block diagram of the DC-DC converter. Vout is monitored by an inverter-based comparator, which generates a rising edge when it detects that Vout < Vref. Simulated waveforms of the Vout and comparator output (V1) are shown in Fig. 2(a) and Fig. 2(b) respectively, where the output current (Iout) is set to 50µA. This rising edge changes the output state of the T-flip-flop (V2), as shown in Fig 2(c), and the clock signal is level-shifted and input into the Switched-Capacitor (SC) network (Vtp represents the trip point of the inverter used as a comparator). The SC network operates using clocks at three different voltage levels (L1, L2, and L3) for switching purposes. When the rising or falling edge of the clock triggers the SC network, a package of charge is delivered to Vout, which raises it above Vref, thus resetting the V1. A watchdog circuit is included as a failsafe feature but can also serve as a startup mechanism and is in standby mode during regular DC-DC operation, consuming only 135 nW. If a malfunction is detected, such as overcurrent, the watchdog kicks in and restarts the whole system. The reset signal generates the required intermediated voltages (1.2 and 1.8 V) as needed.

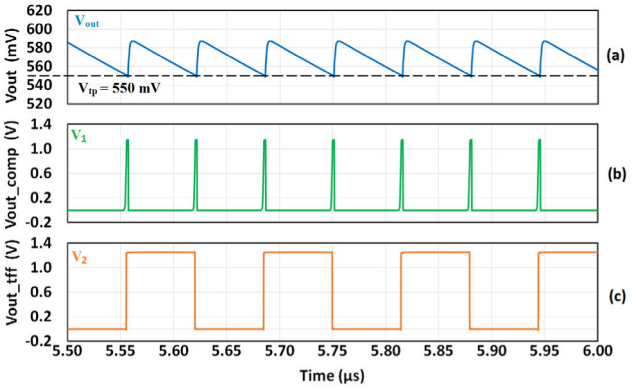

FIGURE 2. Simulated waveforms of the clock generation mechanism @ Iout = 50uA, (a) Vout, (b) V1, (c) V2 (Fig. 1).

B. SWITCHED-CAPACITOR NETWORK

Figure 3 illustrates the architecture utilized to achieve the necessary Voltage-Conversion-Ratio (VCR) is a dual-core Ladder-Star [10] architecture, also known as Dickson or Dickson Star [11]. Each core's flying capacitors (Cfly) comprise three 5pF Metal-Insulator-Metal capacitors (MIM-CAP). The two cores operate at orthogonal clock phases, which enables a lower ripple and provides access to the intermediate voltage levels. The internal voltages of the one core (Vx0, Vx1, and Vx2) are shown in Fig. 4. Since the second core's internal voltages are identical, but at an opposite phase, a floating well circuit (Fig. 5) can be used for intermediate voltage generation according to the following equations: VDD1 = max(Vx1,Vy1), VDD2 = max(Vx2,Vy2). The voltage supplies, VDD1 (∼1.8V) and VDD2 (∼1.2V), are produced by providing the opposite-phase internal voltages

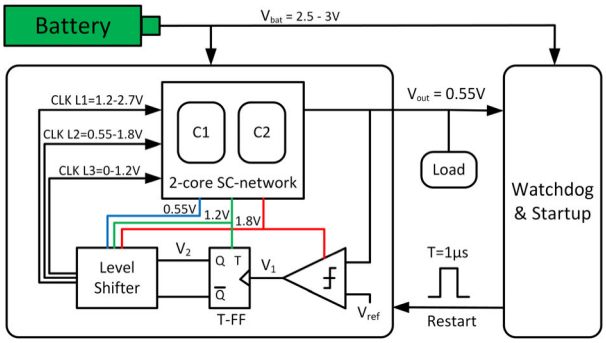

FIGURE 1. Block diagram.

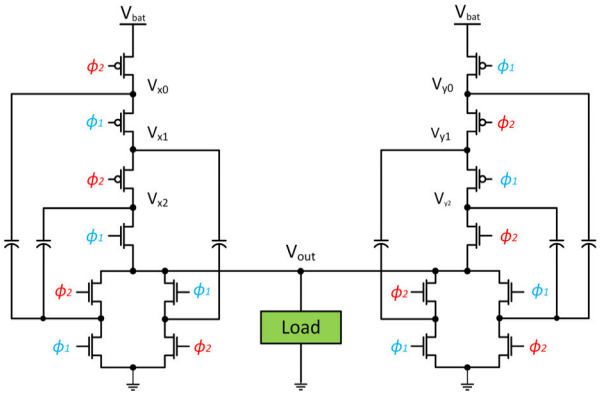

FIGURE 3. Two core ladder-star architecture.

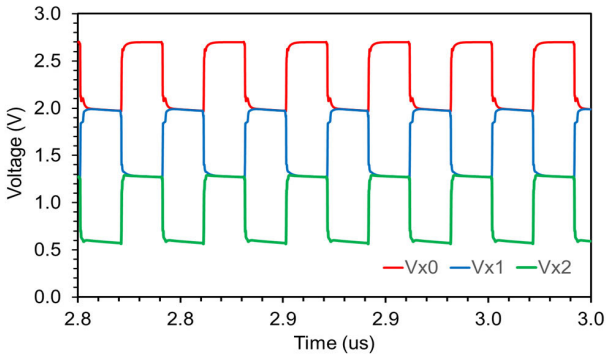

FIGURE 4. Simulated waveforms of one bank at a 130uA load.

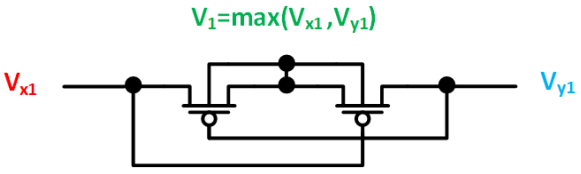

FIGURE 5. Intermediate voltage generator.

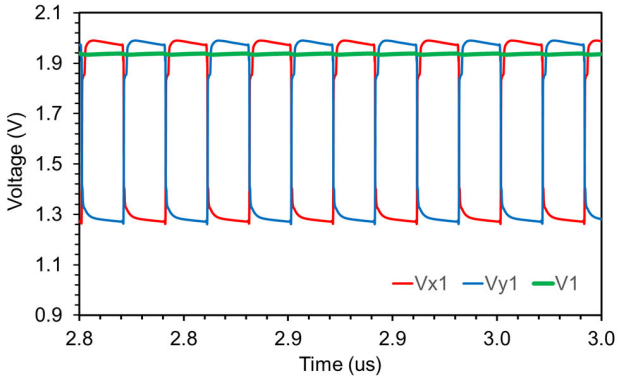

FIGURE 6. Simulated waveforms - Intermediate voltage generator.

(Vx1, Vx2, Vy1, and Vy2) to the intermediate voltage generation circuit. A waveform of VDD1, generated from Vx1 and Vy1, is presented in Fig. 6 as an example. VDD2 is generated in a similar manner. The intermediate voltages, along with the main output voltage (Vout), are used to generate three distinct clock-voltage levels that are applied to the corresponding NMOS and PMOS switches (see Fig. 7). The V2 signal is first level shifted up to the battery voltage level (Vbat = 2.7V).

Then, in order to reduce the charging losses, the clock signal is driven into three buffers which charge stages L3, L2, and L1 from 0 to 1.2V, 0.6V to 1.8V, and 1.2V to 2.7V respectively. Thus, each stage in the DC-DC can be driven to exactly the voltage required for the conversion. A detailed illustration of both DC-DC cores including the intermediate voltage generation and clock levels used for each stage is shown in Fig. 8. Note that each switch is toggled between its required minimum and maximum voltage levels.

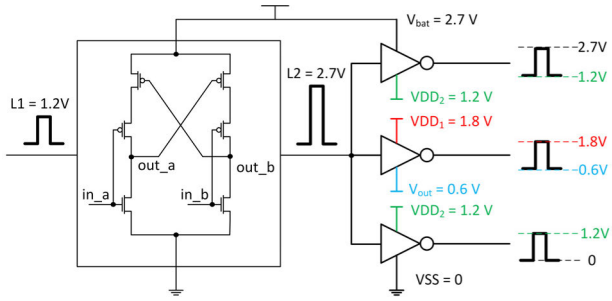

FIGURE 7. Level shifting concept.

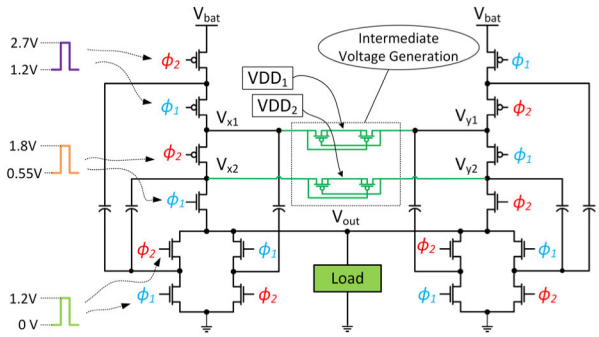

FIGURE 8. Two Core Ladder-Star with intermediate voltages and clock voltage levels.

C. INVERTER-BASED COMPARATOR

Inverter-based amplifiers are commonly used for their high-speed, low-power properties. However, they are subject to issues such as process-dependence and supply-voltage-dependent trip points. Despite these shortcomings, an inverter-based amplifier can be implemented as an efficient comparator if its disadvantages are overcome. To address this issue, the supply voltage (Vdd_inv) of the inverter is regulated such that its trip point is always at a fixed voltage level, as depicted in Fig. 9(a). The voltage reference (Vref) is supplied to the input of the Unity Gain Buffer (UGB), whose output is utilized as the supply voltage for the inverter. Therefore, the trip point of the inverter (Vtp) is approximately Vref/2, based on the ratio of the NMOS to the PMOS. The control loop causes Vout to track Vtp, and fine-tuning of Vref enables digital control of the output voltage. This feature can be realized with trimmable subthreshold reference voltage circuits that consume nW or sub-nW level power, such as the 2T based reference in [12], which can operate directly off Vbat. It can be observed that the inverter, when used as an analog circuit, has a bandwidth of 363 MHz (Fig. 9(b)) which enables a very fast response to the transient load changes. The Vtp point is nearly temperature- independent, as seen in simulations (Fig. 10). Since the UGB does not require very high-speed operation, it can function with very low bias currents (∼1.4 μA).

D. WATCHDOG MECHANISM

A watchdog mechanism was designed to reset the DC-DC converter in case of malfunction caused by overvoltage and

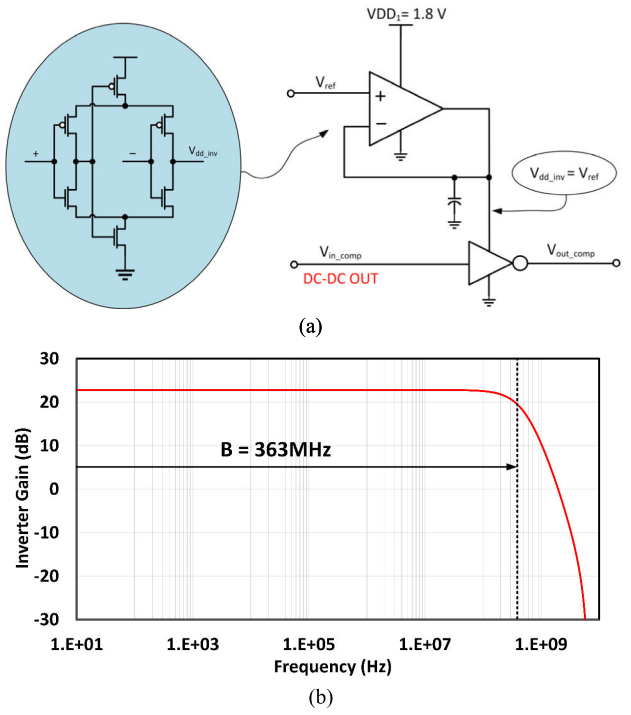

FIGURE 9. (a) Comparator with UGB. (b) Inverter bandwidth.

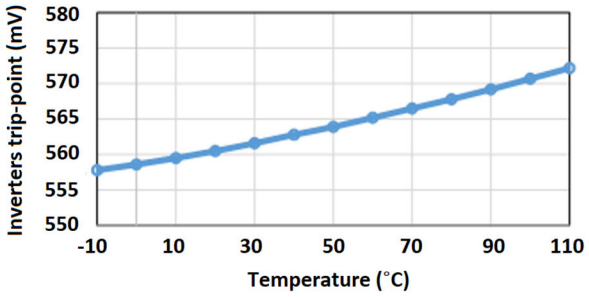

FIGURE 10. Inverter trip-point vs. Temperature.

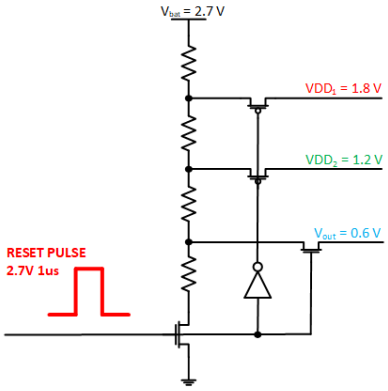

FIGURE 11. Startup circuit.

excessive current, but it can also be utilized as a trigger for the startup mechanism. A startup circuit using a resistor divider between Vbat and VSS, as depicted in Fig. 11, was used to initialize VDD1, VDD2, and Vout, and could be enabled by the external startup pulse or by the watchdog pulse.

The simplicity of the circuit provides considerable reliability and robustness since the reset and startup functions are crucial parts of the circuit's normal operation as well as the fail-safe mechanism. In order to secure the required voltage levels (VDD1, VDD2, and Vout), the startup circuit needs to be enabled for roughly 1 µs. Thus, the required length of the reset pulse is generated with the watchdog circuit as illustrated in Fig. 12. Inverter I1 has a lower trip point than Vtp (Fig. 9) and is thus used to detect situations where Vout is too low. The supply of I1 is generated by weak PMOS devices P1-P4 which operate off Vbat. Digital inputs Trim1 and Trim2 determine the voltage level at which a malfunction can be detected. If the DC-DC converter operates normally, Vout will be above this trip point, and the watchdog will consume minimal power. However, if Vout drops too low, a rising edge at node n1 is generated, which is level-shifted to the battery voltage level at node n2 and fed to the Edge-Triggered-Pulse-Generator (ETPG) that generates a restart pulse (T=1 µs). The restart pulse sets the voltage levels at the DC-DC core back to the normal range, resulting in falling edges at nodes n1 and n2. If the malfunction is due to a current spike or glitch, the DC-DC converter will continue to operate normally. The Edge-Triggered-Pulse-Generator is shown in Fig. 13.

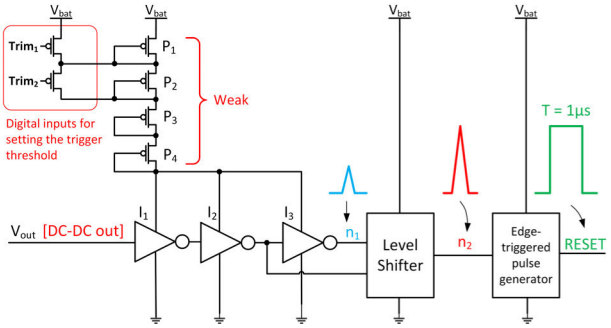

FIGURE 12. Watchdog circuit.

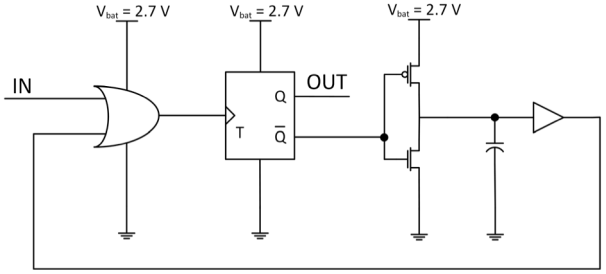

FIGURE 13. Edge-triggered pulse generator (Fig. 12).

E. INTERNAL LOAD SETUP

To measure the parameters of the DC-DC converter in an environment that was as close as possible to realistic operating circumstances, an internal load circuit (Fig. 14) was implemented on silicon next to the DC-DC converter. This setup enabled the measurement of circuit operations with a

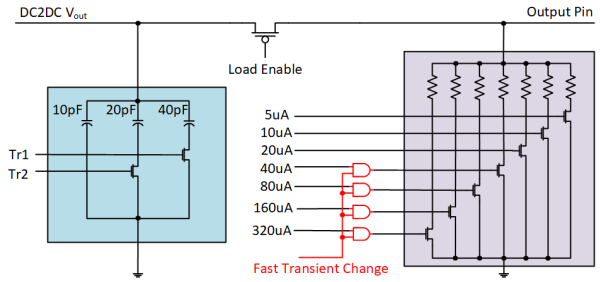

FIGURE 14. Internal load setup.

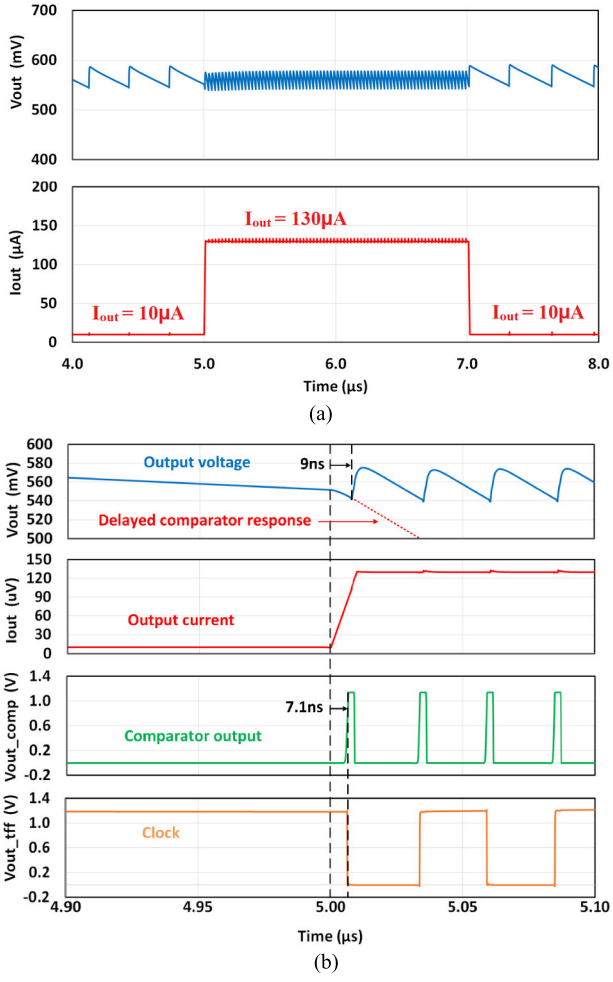

FIGURE 15. (a) Simulated transient load. (b) Relevant waves in the moment of transient load change.

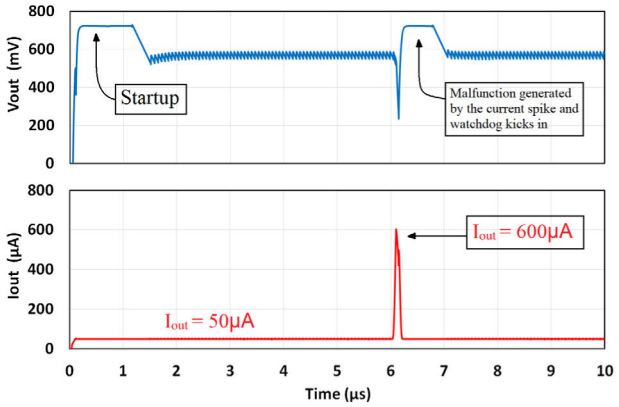

FIGURE 16. Simulated Startup & Watchdog.

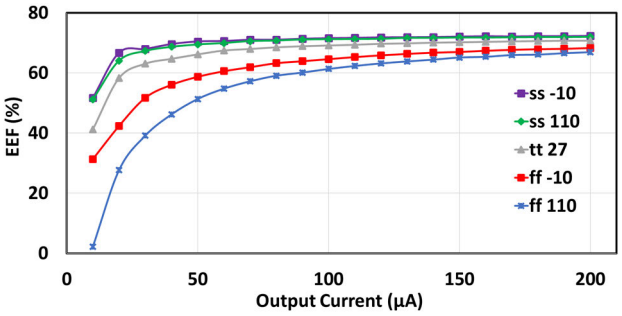

FIGURE 17. Simulated EEF vs Iout @ Vin = 2.7V, nominal and extreme (ss -10 ss 110, ff -10, ff 110).

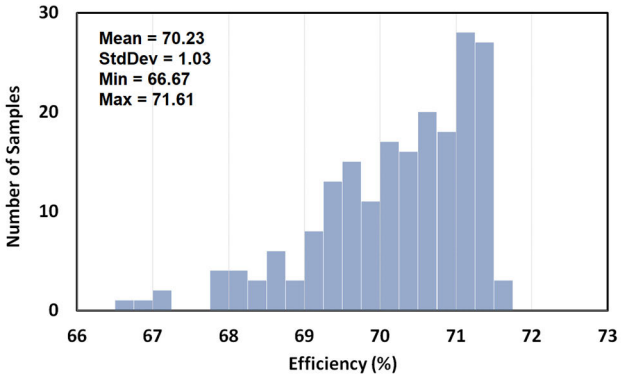

FIGURE 18. Monte Carlo Efficiency @ Iout = 160uA, 200 samples.

load capacitance as low as 50pF (including the oscilloscope probe). It also had a tunable resistor load across the required current range that enabled a fast internal current transient. This internal current step could be much quicker than an external step, which would be strongly affected by parasitic package inductances and capacitors.

III. SIMULATED RESULTS

Due to the complexity of the whole system and the limited capabilities of silicon measurements in different corners, the simulation results represent an important aspect for performance analysis. The results of the transient analysis, that simultaneously depict the Vout, Iout, as well as other relevant waveforms, are presented in Fig. 15a, Fig. 15b, and Fig 16. A fast response without voltage droops or overshoots can be observed in cases of fast transient load change (Fig. 15a and Fig. 15b). Figure 15b presents waveforms of signals relevant to the speedy transient response (Vout, Iout, Comparator output, and T-flipflop output) right around the moment of transient load change. It can be observed that the response from the comparator takes only 7.1ns from the load change (due to the inverter's high bandwidth). The pulse from the comparator results in an almost immediate change in the

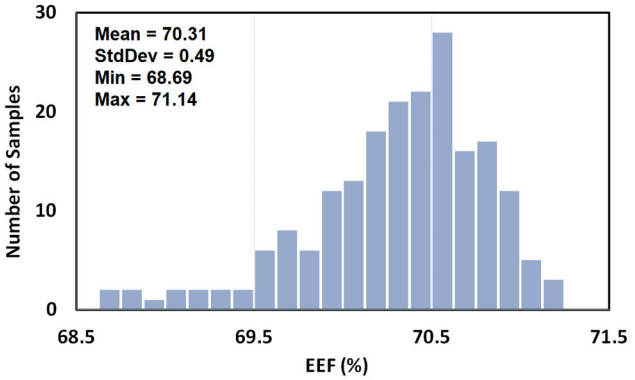

FIGURE 19. Monte Carlo EEF @ Iout = 160uA, 200 samples.

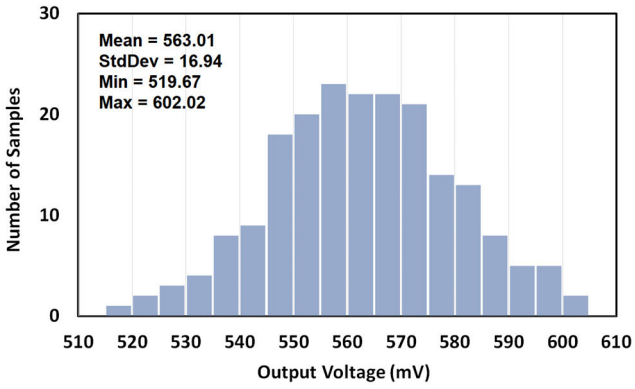

FIGURE 20. Monte Carlo Vout @ Iout = 160uA, 200 samples.

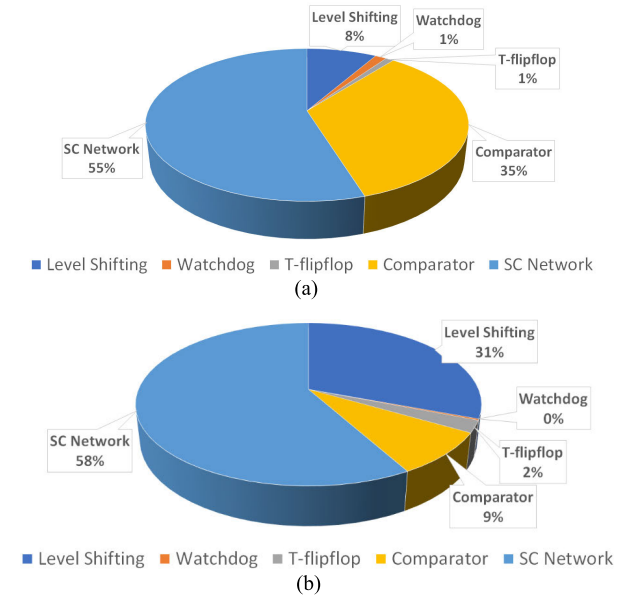

FIGURE 21. (a) Simulated sub-circuit energy consumption @ 5.5μW. (b) Simulated sub-circuit energy consumption @ 95μW.

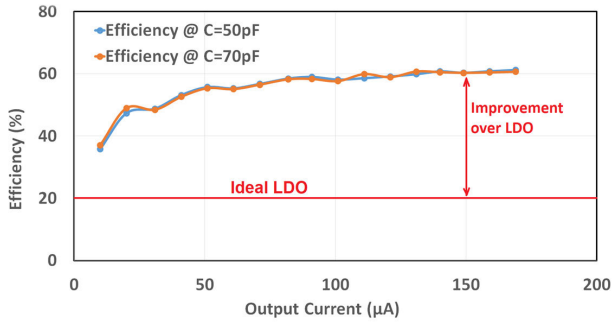

FIGURE 22. Measured Efficiency vs. Iout.

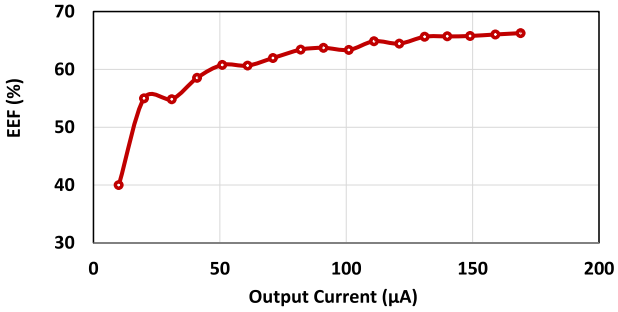

FIGURE 23. Measured EEF vs Iout.

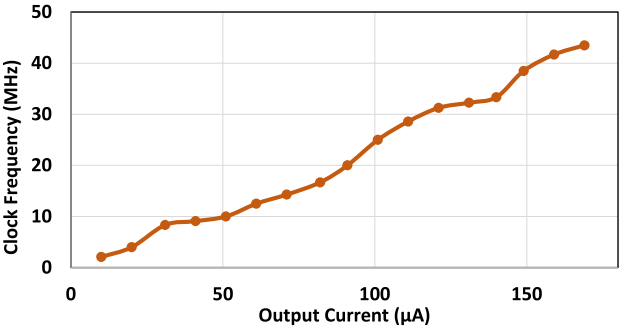

FIGURE 24. Measured clock frequency vs. Iout.

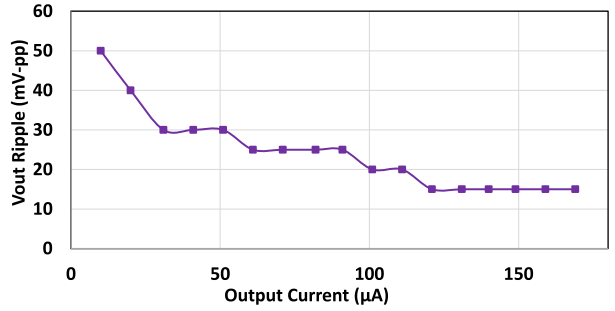

FIGURE 25. Measured vout ripple vs. Iout.

clock frequency which enables output voltage to spike up 9ns after load change, thus, preventing voltage droop or malfunction. A dashed red line presents a slope of Vout in case of delayed response from the comparator. Note that the minimum voltage in this transient was similar in the low current (10uA) and high current range (130uA). This is because at this voltage, the comparator tripped. At low current, a larger ripple was observed at a lower frequency.

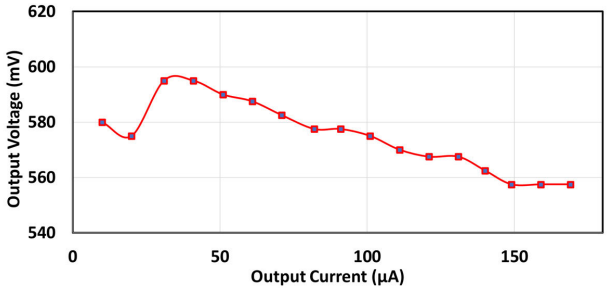

FIGURE 26. Measured vout vs Iout.

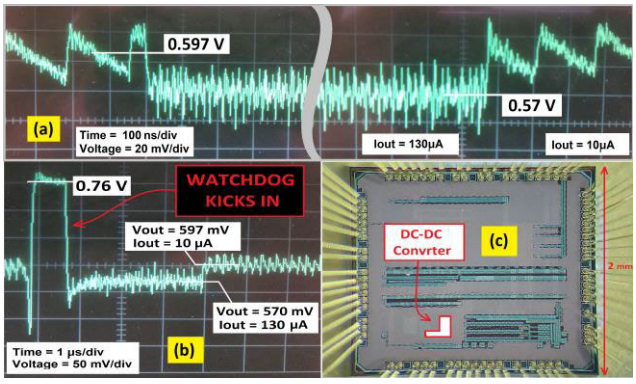

FIGURE 27. (a) Measured Load transient - 10uA -> 130uA -> 10uA, (b) Load transient as well as a watchdog operation, (c) Die photo.

A watchdog activation due to malfunction caused by an over-current is shown in Fig. 16. Note that the startup event in this case was triggered because the external pulse lasted a bit longer than the watchdog pulse. In the case of a lack of external pulse, the pulse from the watchdog could serve as a startup trigger as well.

Figure 17 shows simulated extreme cases of the EEF dependence on the Iout (process corners combined with extreme temperatures). As expected, a given drop in efficiency was associated with the fast corner due to leakage. The figure indicates that even for the worst-case scenario (ff, T=110 °C), the DC-DC converter could be utilized efficiently over the entire operating range, as indicated by the positive EEF.

Figures 18-20 show Monte Carlo variations (process and mismatch) on Efficiency, EEF, and Vout for nominal cases and Iout=160µA. Both Efficiency and EEF had very low dispersions with standard deviations equaling 1.03% and 0.49% respectively. Even though Vout had a slightly larger standard deviation of 16.94 mV, this does not constitute a problem since it can be calibrated if a trimmable Vref is utilized [12]. The energy consumption by the individual sub-circuits was analyzed for two different scenarios: a minimum power of 5.5µW (Fig. 21(a)) and maximum power of 95µW (Fig. 21(b)). The results show that the dominant energy consumer for both scenarios was the switched capacitor network, which is another indicator of relatively consistent efficiency over the entire operating range.

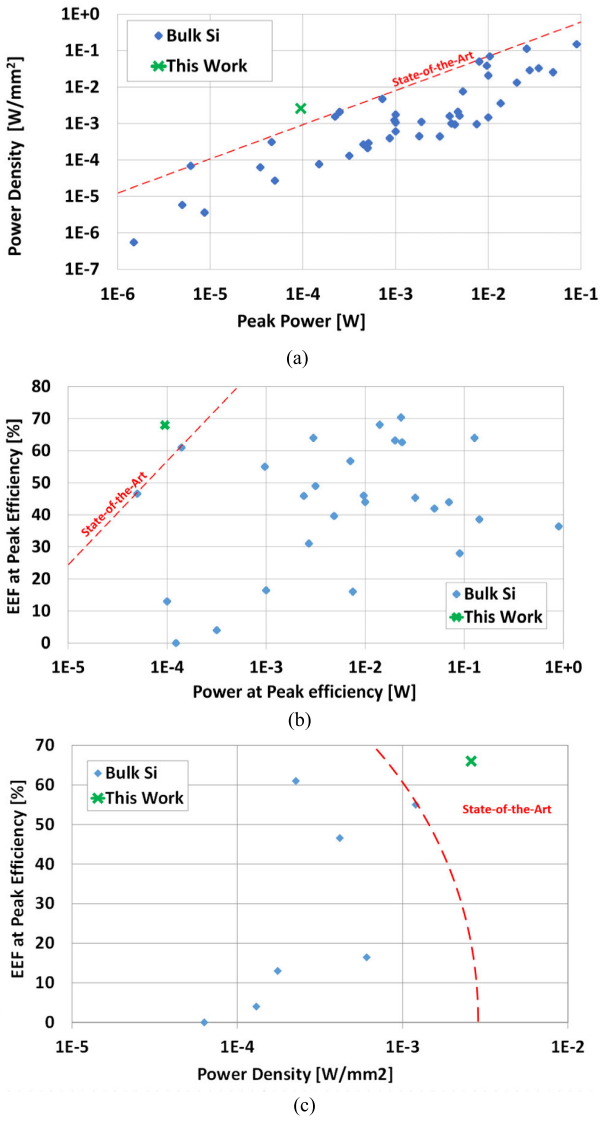

FIGURE 28. (a) Power Density vs. Peak Power for Bulk Si switched capacitor buck and boost DC-DC [8]. (b) EEF vs. Power at Peak Efficiency for Bulk Si switched capacitor Buck converters [8]. (c) Combined contribution of EEF and Power Density (EEF vs Power Density) for sub-mW converters.

The main difference between minimum and maximum power in terms of the energy consumption contribution emerged for the Comparator and Level Shifter. This can be attributed to the Comparator's power consumers that are not dependent on the clock frequency. For low-current converters, the overhead circuits contribute a larger percentage of the total power budget as compared to high-power converters. This is why the Efficiency and EEF were reduced at very low output currents (see Fig 17).

IV. MEASURED RESULTS

The DC-DC converter was fabricated using TSMC's 65nm technology node. In Fig. 22, the measured efficiency as a function of output current (Iout) is presented for a nominal

TABLE 1. Comparison to other on-die low power switched capacitor converters.

	This Work	[3]	[4]	[5]	[6]	[7]
Tech Node	65nm	180nm	180nm	65nm	130nm	180nm
Actual VCR (topology VCR)	0.2 (1/4)	0.23 (1/3)	0.225 (1/4)	0.83	0.32 (2/5)	(1/3)
C_fly	MIM 6x5pF	-	-	MIM 445pF	800pF	MIM
Power Density (mW/mm²)	2.56	1.2	0.266	1.3	0.055	0.038
Efficiency	62%	54%	58%	78%	65%	81%
EEF	66%	57%	61%	-7%	51%	44%
Vin	2.5 – 3 V	4.2 V	3.8 – 4.2 V	1.2 V	2.7 – 3.3 V	0.9 – 4 V
Vout	0.55/1.2/1.8 V	0.98 V	0.9/1.2/1.5 V	1 V	1.05 V	0.6/1.2/3.3 V
Max Power (mW)	0.095	0.97	0.45	0.35	0.1	9.7
Area (mm²)	0.037	0.79	1.7	0.27	1.82	0.25
Ripple peak-to-peak	15mV – 50mV	20 mV	-	40 mV	200 mV	-
C out	50 - 70 pF	1nF	-	1050 pF	-	3 nF
Droop Response	No Droops or Overshoots 10µA -> 130µA	Droop = 230mV Overshoot=200mV 10µA -> 100µA	Droop = 200mV Overshoot = 200mV 10µA -> 50µA	Droop = 50mV No overshoots 10µA -> 250µA	–	Droop=150mV Overshoot=150mV 10nA –> 1µA

output voltage of Vout=0.55V. The efficiency exhibited a peak value of 62% at the maximum Iout and remained close to the peak value over most of the operating range. The relationship between the Energy Efficiency Factor (EEF) and Iout is illustrated in Fig. 23, and also displays good consistency over the range. The nearly linear dependence of the clock frequency on Iout (Fig. 24) enables relatively high efficiency and EEF over the range. The Vout ripple is plotted against the output current in Fig. 25, assuming an output capacitance of 50pF. Figure 26 shows the DC level of Vout versus Iout. A DC load line of 37.5 mV was observed over the entire operating range, which was mainly associated with the delay in boosting after the comparator's trip. The ripple difference between light and heavy loads also contributed to some extent to the DC load-line since the regulated value is not a DC component of the Vout but the minimum Vout. In Fig. 27(a), the transient response of the converter is depicted when the current was suddenly changed from 10uA to 130uA and back to 10uA. Due to the fast speed of the inverter-comparator, no droops or overshoots were observed, despite the small Cout. A DC load-line of 27mV can be observed here as well. The activation of the watchdog circuit during an overcurrent event is also shown in Fig. 27(b). After approximately 1µs of reset time, the DC-DC converter resumed normal operation. Figure 27(c) depicts the silicon die photo with its corresponding dimensions and the DC-DC converter's location.

V. DISCUSSION

Table 1 compares the proposed on-die switched capacitor DC-DC converter to previous sub-mW DC-DC converters. Figures 28(a,b,c) show a graphical comparison of the power density and the Energy Efficiency Factor (EEF) for the bulk Si switched-capacitor DC-DC converters presented in [8]. The efficiencies and EEFs reported in Table 1 were evaluated near or at peak power, where they are typically at the optimal point. Figure 28 shows that both the power density and EEF tend to degrade at very low power, which can be partially attributed to current consumption in the regulation and support circuitry. The proposed DC-DC converter exhibited the best EEF and power density of all the sub-0.5mW DC-DC converters and was competitive with converters whose power was two orders of magnitude higher. A graphical presentation of other power density works (Fig. 28(b)) clearly indicates that achieving higher power density becomes increasingly more difficult in low-power domains, which is also the case with other indicators of quality. For this reason, only DC-DC converters in a similar power area should be compared or the parameters should be scaled with power. Figure 28(c) illustrates EEF vs. Power Density for sub-mW DC-DC converters. The upper right corner indicates higher performance. It can be observed that the proposed topology scores better than reported prior art DC-DC converters.

VI. CONCLUSION

The proposed topology employs a supply-regulated inverter, which is the foundation of a highly energy-efficient, high-speed comparator. Regulation is achieved by adjusting a reference voltage that determines the supply voltage of the inverter. This reference can be operated directly from Vbat, because it is assumed to consume nW-level power similar to other adjustable references reported in the literature [12]. Despite being low power, the inverter enables a fast response, thus allowing the proposed DC-DC converter to exhibit the

best transient recovery out of the circuits in Table 1, despite the small load capacitor. This prevents voltage droops that could result in timing failures.

Because the DC-DC converter is self-clocked, the efficiency and EEF remain relatively stable over most of the operating range. The main output voltage of 0.55V is suitable for always-on digital domains operating at near-Vth. In addition, voltage domains of 1.2V and 1.8V are available for analog circuits, and the DC-DC converter uses internally generated voltages to power its own circuits. The State-of-the-Art performance in terms of efficiency, speed, and power density of the proposed DC-DC converter makes it a promising solution for always-on circuits in IoT devices.

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