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RESEARCH ARTICLE

Data Path Nonlinearity Estimation for 200 Gbps PAM4 Serdes Receivers

ARCHIT JOSHI
Intel Corporation, Bengaluru 560103, India
e-mail: architjoshi1@gmail.com

ABSTRACT This paper presents a method to estimate the nonlinearity of the analog data path of Serdes receiver, in real time operation. The estimated nonlinearity can be used to adapt various receiver parameters to improve performance. The proposed method is demonstrated for a 200 Gbps ADC-Based receiver, in which, nonlinearity estimate is used to set Analog Front End (AFE) swing optimally, resulting in improved eye opening. The proposed method is also used to adapt decompressive characteristic optimally.

INDEX TERMS Serdes, nonlinearity, continuous time linear equalizer, variable gain amplifier, decision feedback equalization, feed forward equalization.

I. INTRODUCTION

As high-speed wireline serial link data rate keeps going up, the need for higher equalization in the Serdes receivers keep increasing. It is very common to have 3-4 analog equalization stages of Continuous Time Linear Equalizer (CTLE) and Variable Gain Amplifier (VGA) in receiver's Analog Front End (AFE). After VGA the data passes through analog summer, voltage buffer, track and hold sampling switches etc., depending on the receiver's architecture [1], [2]. As each analog stage has its own contribution to the total nonlinearity of the data path, the impact of nonlinearity is gaining significance. Technology scaling and heat dissipation demands lowering the power supply. This reduces the headroom available for analog circuits and increases the nonlinearity further. Nonlinearity degrades eye opening, Bit Error Rate (BER) and overall system performance [3]. Equalization techniques like Decision Feedback Equalization (DFE) and Feed forward Equalization (FFE) can correct the linear Inter-Symbol Interference (ISI). Nonlinearity cannot be corrected by traditional DFE and FFE.

Traditionally, to deal with nonlinearity, analog circuits are designed considering worst-case nonlinearity scenario (across corners, channel losses etc.), leading to overdesign for most of the operating conditions. In [4] the DFE tap weights change with bit patterns which would have large power penalty, and the proposal is limited only to Simulink model. Significant computation overhead is present in [5] and [6] and have not been proven for high-speed links at hundreds of Gbps data rates. A method to model the nonlinearity is presented in [7]. Analysis of distortion of histogram due to nonlinearity is presented in [2] but doesn't propose a solution to estimate the nonlinearity using the distortion. Determining the nonlinearity with histogram distortion is likely to be very inaccurate.

A method to estimate the nonlinearity during real time operation is presented in this work. Using this estimate, the analog circuits can be adapted, optimally across operating conditions. The proposed algorithm is implemented for a receiver whose architecture is adopted from a 224 Gbps ADC based Serdes [1].

II. NONLINEARITY OF DATA PATH

Consider the block diagram of a typical Serdes receiver (Fig. 1(a) and (b)) where multiple gain stages of CTLE and VGA perform equalization. The output of the VGA goes to summer and sampler for traditional receivers (Fig. 1(a)) [8] or to track-and-hold sampling switches (SW), ADC and digital FFE/DFE for ADC based receivers (Fig. 1(b)) [1].

Nonlinearity of the analog data path arises due to multiple reasons. Degradation of saturation margin of differential pair or tail device, cause gm and bias current to vary with signal voltage, causing nonlinearity. Capacitance of 'drain' node of the tail device gives frequency dependence to bias current

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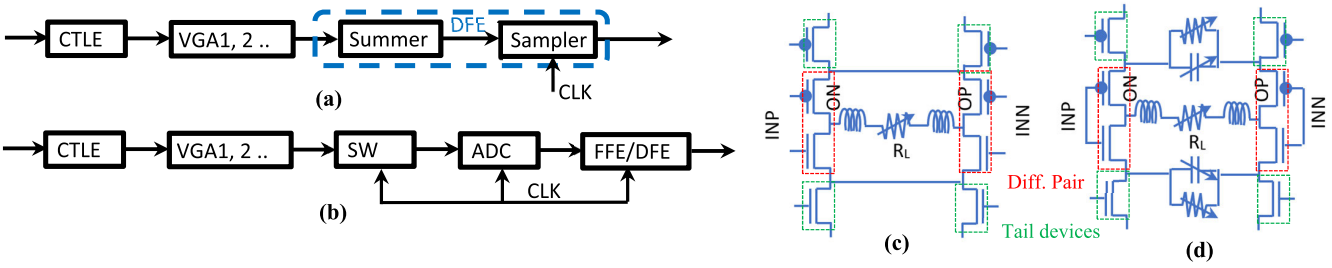

FIGURE 1. (a) Traditional, (b) ADC based receiver architectures, (c) VGA [1], (d) CTLE [1].

variation, making nonlinearity frequency dependent. The ON resistance of the sampling switches (SW) [1] vary with the signal voltage leading to nonlinearity.

Consider the example of a high loss link with say, 35dB channel loss at Nyquist frequency. The AFE boost will be targeted around 20-22 dB [1], [9] and rest of the equalization will be done by DFE/FFE. When the signal passes through the analog stages, it has much more low frequency content compared to that around Nyquist, the low frequency nonlinearity dominates even though the circuits themselves may be more nonlinear at higher frequencies.

The focus of this work is high channel loss links, and its nonlinearity analysis as high loss links are the main performance bottleneck compared to low loss links.

III. ESTIMATION OF NONLINEARITY

Consider input to AFE stage x_n with output y_n. The nonlinearity (NL) is modelled as being present at the AFE output (Fig. 2(a)). To make hand analysis feasible, consider the AFE output having only two dominant ISI terms. Since the continuous time output finally gets sampled, the linear AFE output is written as

$$\acute{y}_n = g_0 a_n + g_1 a_{n-1} + g_2 a_{n-2}, \tag{1}$$

where $g_0, g_1 \& g_2$ are cursor, 1st & 2nd post ISI coefficients. For a third order compressive nonlinearity with coefficient β, the output can be written as $y_n = \acute{y}_n - \beta \acute{y}_n^3$. Using (1), we get

$$\begin{aligned} y_n = {} & g_0 a_n + g_1 a_{n-1} + g_2 a_{n-2} \\ & - \beta \{g_0 a_n + g_1 a_{n-1} + g_2 a_{n-2}\}^3. \end{aligned} \tag{2}$$

For PAM4 encoded data, $a_n \in \pm 3A, \pm A$, where A is the bit amplitude. Let α_1, α_2 be the DFE coefficients from LMS (Least Mean Square) adaptation. The equalized data at the input to the data sampler (Fig. 2(a)) is given by

$$\begin{aligned} z_n = {} & g_0 a_n + (g_1 - \alpha_1) a_{n-1} + (g_2 - \alpha_2) a_{n-2} \\ & - \beta \{g_0 a_n + g_1 a_{n-1} + g_2 a_{n-2}\}^3. \end{aligned} \tag{3}$$

PAM4 eye diagram at the data sampler input is shown in Fig. 2(b) with different levels; H_3 and H_1 for upper side and L_3 and L_1 for lower side. For linear case ($\beta = 0$) the average value for level H_3 can be found using (3) as $E\{z_n \mid a_n = 3A\} = 3Ag_0$ assuming uncorrelated and

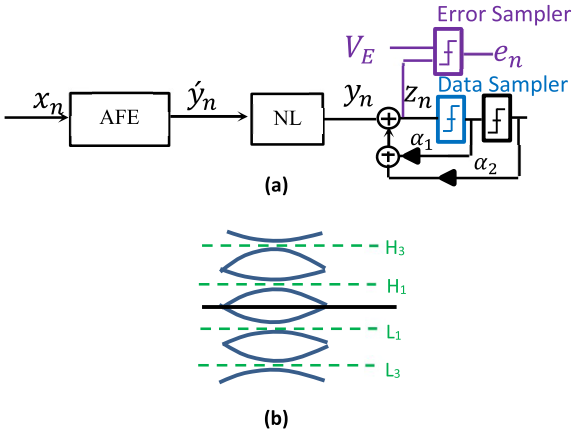

FIGURE 2. (a) Data path, (b) PAM4 eye at data sampler input.

equiprobable data bits. Here $E\{|\}$ is the conditional expectation operator using notation from [10]. Similarly, H_1 is obtained as $E\{z_n \mid a_n = A\} = Ag_0$.

For nonlinear case ($\beta \neq 0$), $E\{z_n \mid a_n = 3A\}$ is evaluated after solving for (3) as

$$\begin{aligned} E\{z_n \mid a_n = 3A\} &= 3Ag_0 - 3\beta A^3 g_0 \left(9g_0^2 + 15g_1^2 + 15g_2^2\right) \\ E\{z_n \mid a_n = A\} &= Ag_0 - \beta A^3 g_0 \left(g_0^2 + 15g_1^2 + 15g_2^2\right). \end{aligned} \tag{4}$$

The subtractive terms of (4) give reduction of the signal amplitude due to compressive nonlinearity. They are bigger for $E\{z_n \mid a_n = 3A\}$ compared to $E\{z_n \mid a_n = A\}$; because larger signal is more affected by nonlinearity.

For linear case the LMS in (3) will converge to $\alpha_1 = g_1$ and $\alpha_2 = g_2$ giving ideal ISI cancellation, $z_n = g_0 a_n$. Since the nonlinearity depends on signal's amplitude, the converged values of α_1, α_2 for $\beta \neq 0$ will depend on whether they are obtained by keeping the error sampler threshold V_E (Fig. 2(a)) at H_3 or H_1. The LMS converged coefficient solution for α_1 and α_2 for $V_E = H_3$ and $V_E = H_1$, after lengthy algebra, is obtained as

$$\begin{aligned} \alpha_1 | H_3 &= g_1 - g_1 A^2 (\beta/5) \left(41g_1^2 + 135g_0^2 + 75g_2^2\right) \\ \alpha_1 | H_1 &= g_1 - g_1 A^2 (\beta/5) \left(41g_1^2 + 15g_0^2 + 75g_2^2\right) \end{aligned}$$

$$\alpha_2|H_3 = g_2 - g_2A^2(\beta/5)\left(41g_2^2 + 135g_0^2 + 75g_1^2\right)$$
$$\alpha_2|H_1 = g_2 - g_2A^2(\beta/5)\left(41g_2^2 + 15g_0^2 + 75g_1^2\right). \quad (5)$$

With nonlinearity, unique value of α_1 doesn't exist. It has different converged values depending on the error sampler threshold ($V_E = H_3$ or H_1), leading to inaccurate ISI cancellation. Since the difference arise due to nonlinearity, the normalized % difference serves as an estimate of nonlinearity

$$\widehat{NL}_1 = 100(\alpha_1|H_3 - \alpha_1|H_1)/(\alpha_1|H_1). \quad (6)$$

Since $\alpha_1|H_3$ and $\alpha_1|H_1$ are readily available in real time operation from the LMS engine, (6) can be evaluated to get an estimate of nonlinearity. For good circuit performance, $\widehat{NL}_1$ is small, generally $< 5\%$ for the receiver to be negligibly affected by nonlinearity.

Consider the $\alpha_1|H_3$ case. Back substituting, (5) in (3), the equalized data z_n (Fig. 2(a)) is obtained as

$$z_n = g_0a_n + g_1A^2(\beta/5)\left(41g_1^2 + 135g_0^2 + 75g_2^2\right)a_{n-1} + g_2A^2(\beta/5)\left(41g_2^2 + 135g_0^2 + 75g_1^2\right)a_{n-2} - \beta\{g_0a_n + g_1a_{n-1} + g_{-2}a_{n-2}\}^3. \quad (7)$$

When $a_n = 3A$, there are 16 possible z_n values, depending on 4×4 values of a_{n-1} and a_{n-2} ($\pm3A$, $\pm A$), showing that the ISI is not cancelled completely in the presence of nonlinearity. Simplifying (7) using $g_0 > g_1, g_2$ and keeping the dominant terms, we get

$$z_n \approx 3Ag_0 - 27\beta A^3g_0^3 - \Delta z_n \quad (8)$$
$$\Delta z_n = 9\beta Ag_0(a_{n-1}^2g_1^2 + a_{n-2}^2g_2^2 + 2a_{n-1}a_{n-2}g_1g_2) \quad (9)$$

The dependence of z_n on a_{n-1} and a_{n-2} in (8) is given by Δz_n. The peak-to-peak variation of z_n due to $a_{n-1}, a_{n-2} \in \pm3A, \pm A$ is obtained using (9) as

$$\Delta z_{n-pp} = 54\beta A^3g_0(6g_1g_2 + 3g_1^2 + 3g_2^2). \quad (10)$$

This is the residual nonlinear ISI which causes eye closure due to nonlinearity. Δz_n has cross product terms a_{n-1}^2, a_{n-2}^2 and $a_{n-1}a_{n-2}$. These terms give rise to nonlinear ISI and can be detected by correlating them with error sampler output e_n i.e., evaluate $E\left\{e_na_{n-1}^2\right\}$ etc. The time average of z_n in (8) will be tracked by the adaptation loop and the error sampler output e_n will have the residual nonlinear ISI terms which depend on the previous bits. Hence,

$$e_n = \Delta z_n \quad (11)$$

Correlating e_n with recovered bits a_{n-1}^2, a_{n-2}^2 and $a_{n-1}a_{n-2}$ and summing their magnitudes, we get

$$\left|E\{e_n\left(a_{n-1}^2 + a_{n-2}^2\right)\}\right| + |E\{e_na_{n-1}a_{n-2}\}| = 9\beta Ag_0\{\left|\left(66A^4g_1^2 + 66A^4g_2^2\right)\right| + |50A^4g_1g_2|\}. \quad (12)$$

Since this quantity is proportional to β, it serves as an estimate of nonlinearity. The first term is positive for all values of g_1, g_2 so the magnitude can be dropped. This gives the nonlinearity estimate as

$$\widehat{NL}_2 = 9\beta A^5g_0\{66\left(g_1^2 + g_2^2\right) + 50|g_1g_2|\}. \quad (13)$$

The terms $a_{n-1}^2g_1^2$, $a_{n-2}^2g_2^2$ and $2a_{n-1}a_{n-2}g_1g_2$ in (11) arise because of the nonlinearity of the analog circuits and is applicable to both DFE and FFE based receivers. From (13) we can see that if there is no linear ISI ($g_1, g_2 = 0$) then the nonlinear ISI is also zero ($\widehat{NL}_2 = 0$).

When the receiver uses a baud rate CDR with Mueller-Muller phase detector [11], g_2 should be replaced with g_{-1}. This is because g_{-1} will be bigger in magnitude as Mueller-Muller forces $g_{-1} \sim g_1$. During CDR locked state, (13) can be simplified to $\widehat{NL}_2 = 1638\beta A^5g_0g_1^2$.

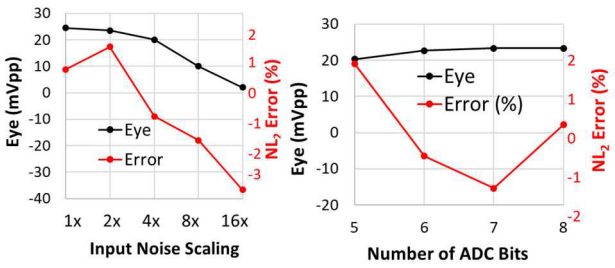

FIGURE 3. Eye opening and $\widehat{NL}_2$ variability error with (a) input noise and (b) ADC bits.

To test the robustness of the proposed estimate, white noise is added at the receiver's input and noise RMS is varied from 1x to 16x. Recovered data eye (corresponding to Q-Factor = 3) and $\widehat{NL}_2$ are plotted in Fig. 3. Noise of 8x causes eye to drop to a small value of 10 mVpp. Beyond 16x, the CDR fails to lock. The deviation of $\widehat{NL}_2$ from its value at 1x noise (called as $\widehat{NL}_2$ error, Fig. 3(a)) is $< 4\%$ for 16x noise, demonstrating that $\widehat{NL}_2$ remains reasonable stable. Similarly, $\widehat{NL}_2$ is estimated by varying the ADC (Fig. 1(b)) resolution bits from 5 to 8, keeping ADC full scale range as constant. As can be seen in Fig. 3(b), the estimate is reasonably stable, deviation with respect to average for all the bits is less than $< 2\%$. Eye opening improves slightly for higher bits due to lower quantization noise of the ADC.

IV. ADAPTATION

Nonlinearity has large dependence on the circuit biasing conditions (bias voltages/bias currents/swing). By using the nonlinearity estimates, tradeoff can be done with other performance parameters, by adapting circuit biasing conditions, leading to optimal overall performance. The use of the estimated nonlinearity is demonstrated using two methods A, B described next.

A. DECOMPRESSIVE ADAPTATION

The compressive characteristics of (2) given by $y_n = \acute{y}_n - \beta\acute{y}_n^3$ can be cancelled if the compressed output y_n is passed

through a decompressive filter. The output of decompressive filter s_{n+1} can be written as

$$s_{n+1} = y_n + \rho y_n^M; \rho \geq 0, \tag{14}$$

where ρ is the decompression parameter and M is the order of decompression. The resultant of compression by AFE and decompression using (14) will reduce the overall nonlinearity. The reduction of nonlinearity will be captured by nonlinearity estimation.

Combined transfer function of AFE circuits followed by decompression is shown in Fig. 4(a), for different values of ρ. As ρ is increased from 0 to 8x, the characteristics changes from compressive to decompressive. During decompression adaptation, the nonlinearity $\widehat{NL}_2$ is estimated and then ρ is adapted to minimize the estimated nonlinearity $\widehat{NL}_2$.

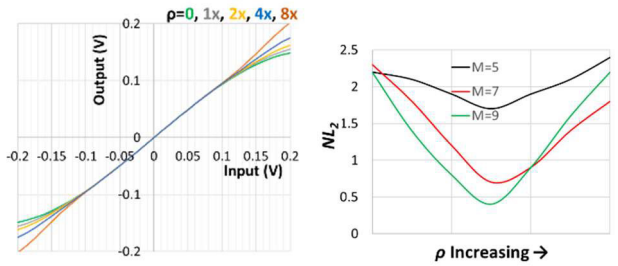

FIGURE 4. (a) Combined transfer function of AFE and decompression for different values of ρ, normalized to input (b) $\widehat{NL}_2$ as a function of ρ for $M = 5,7,9$.

The parameter M in (14) determines the order of decompression. If there are many cascaded stages contributing to nonlinearity, choosing a lower value of M leads to incomplete nonlinearity cancellation. Fig. 4(b) shows $\widehat{NL}_2$ obtained for different values of M. If $M = 5$, it is not sufficient to cancel the nonlinearity significantly for any value of ρ. Between 7 and 9, the difference of minimum $\widehat{NL}_2$ is not huge, so for the present design $M = 7$ is chosen.

B. VGA GAIN ADAPTATION

Fig. 5 shows the nonlinearity at AFE output with respect to AFE output swing for different corners and two channel losses, L2 = 18 dB and L3 = 39 dB. The CTLE boost settings are chosen to give similar boost across corners for a particular loss, resembling a real CTLE-Boost adapted case. The swing is varied by changing the VGA gain control. As seen, for some corners, THD is large, and the swing needs to be kept sufficiently low to limit the nonlinearity. While other corners can tolerate much higher swing for the same THD.

Choosing smaller output swing causes final eye opening (after FFE/DFE), to be dominated by noise (device noise, ADC quantization noise etc.) while larger swing causes eye to be degraded due to nonlinearity. Fig. 6 shows the eye opening (corresponding to Q-Factor = 3) by varying output swing using VGA gain control. Eye opening reaches maxima, beyond which it starts to degrade due to nonlinearity. Since

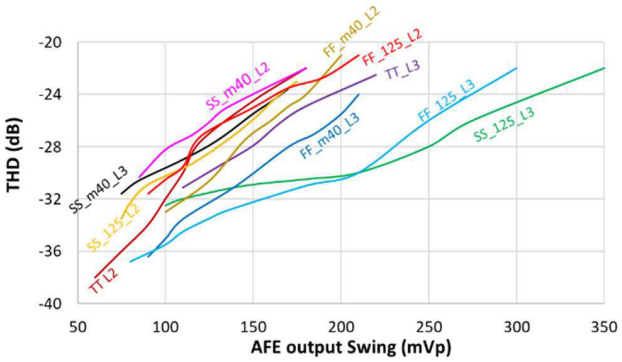

FIGURE 5. Nonlinearity (THD) for different corners and channel loss _L3 and _L2 with respect to AFE output swing.

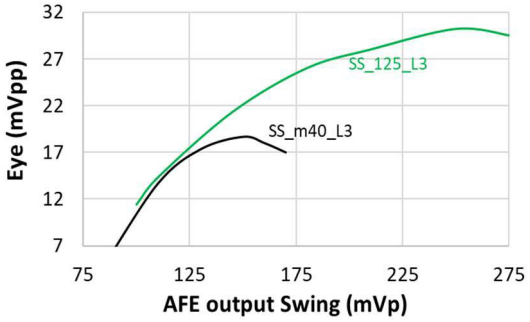

FIGURE 6. Eye opening vs. output swing for low and high nonlinearity corner.

the nonlinearity for SS_125_L3 is small, it can tolerate much higher output swing and reach a much bigger eye opening compared to SS_m40_L3.

During VGA Gain adaptation, the AFE output swing is adapted using VGA gain control, to reach a predefined nonlinearity target value. This results in much better eye opening across operating conditions.

V. RESULTS

The proposed circuits are implemented in 5nm FINFET technology. CTLE, VGA stage 1, 2, buffers (Buff), Track and Hold switches (SW) are real circuits, adopted from [1]. In ADC based receivers, the FFE & DFE are not analog but are implemented in digital domain. Hence in this work, FFE and the adaptation loops are implemented in Verilog/Verilog-A as shown in Fig. 7. ADC is a Verilog-A model with 7-bits resolution. FFE has 7 Taps. A Mueller-Muller based CDR is used to lock to the incoming data. Four non-overlapping [1] clock phases ($\phi_0 - \phi_3$) are used to control the Track and hold switch (SW) which does the sampling operation. Each switch is ON for slightly less than 1/4 of the cycle to guarantee nonoverlap with other three switches. Post layout simulations are done with two channel losses L3 = 39 dB and L2 = 18 dB and five analog corners for 200 Gbps PAM4 input data.

The decompression (14) is done after ADC, before the FFE. The estimated nonlinearity $\widehat{NL}_2$ is used to adapt

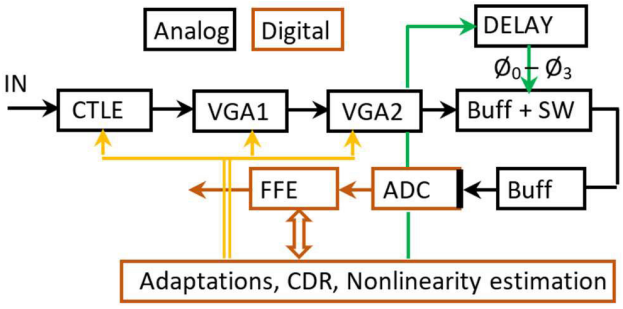

FIGURE 7. Receiver architecture with analog and digital domains.

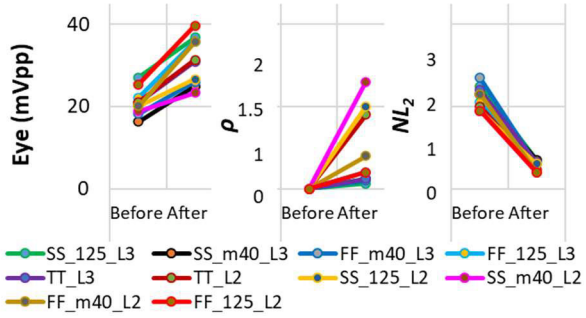

FIGURE 8. Eye opening, ρ and $\widehat{NL}_2$ before and after decompressive adaptation, demonstrating significant improvement in eye opening.

decompression parameter ρ. Adaptation loop starts with $\rho = 0$ and convergence is achieved when $\hat{NL}_2$ reaches minimum. Eye opening, ρ and $\widehat{NL}_2$ before and after the adaptation is shown in Fig. 8.

Maximum eye opening achieved for SS_m40_L3 corner is 19 mV, beyond which it cannot be improved further, as it gets nonlinearity limited (Fig. 6). By adapting the decompression ρ, $\widehat{NL}_2$ can be reduced from 2.6 to 0.7, and the eye can be further improved to 26 mV. Similarly, for all other corners, the eye opening 'Before' in Fig. 8 corresponds to the settings where nonlinearity starts to dominate. With $M = 7$ in (14) some residual nonlinearity remains when ρ reaches optimal and $\widehat{NL}_2$ doesn't reach zero. Good improvement in eye opening is seen for all corners 'After' adaptation in Fig. 8. The eye opening improvemnet is in the range of 29% to 77% across corners and loss.

During VGA gain adaptation mode, the VGA starts from the default gain setting which is same for all corners and loss. To estimate the nonlinearity during VGA gain adaptation, weighted sum of both the estimates $\widehat{NL}_1$, $\widehat{NL}_2$ is used, $\widehat{NL}_0 = (\widehat{NL}_1 + \mu\widehat{NL}_2)$. This improves the estimation accuracy. The parameter μ is predefined and fixed for all corners/channel loss, it is not adapted or estimated.

During receiver operation, $\widehat{NL}_0$ is estimated and compared with a nonlinearity target $\widehat{NL}_T$. If $\widehat{NL}_0 < \widehat{NL}_T$ then the VGA gain is increased, if $\widehat{NL}_0 > \widehat{NL}_T$, the VGA gain is reduced until $\widehat{NL}_0 = \widehat{NL}_T$. The target nonlinearity $\widehat{NL}_T$ is swept from 5 to 80 in steps of 5. For each step of $\widehat{NL}_T$, VGA gain is adapted, and eye opening is measured when

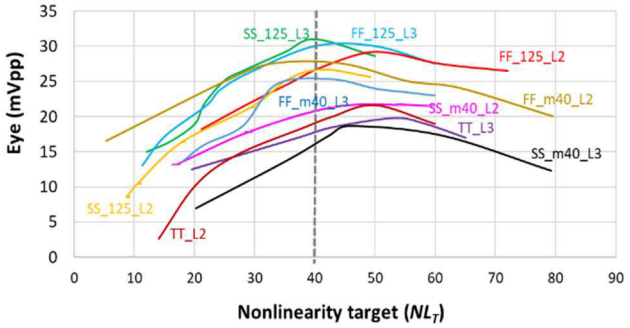

FIGURE 9. Eye opening with respect to $\widehat{NL}_T$ across corners and channel losses.

$\widehat{NL}_0 = \widehat{NL}_T$. Fig. 9 shows eye opening for different corners and two channel losses with respect to $\widehat{NL}_T$ sweep. Setting a target $\widehat{NL}_T$ around 40 gives close to optimum eye opening for corners and channel losses.

Without the proposed nonlinearity estimation, the VGA gain would be adapted to reach a target amplitude. This amplitude target would be chosen purely based on simulation results and amplitude target would be chosen 'small' enough such that nonlinearity does not dominate for all operating conditions. This will be optimal for highest nonlinearity conditions but will be overdesign for all other cases where nonlinearity doesn't dominate.

As seen in Fig. 5, SS_125_L3 and FF_125_L3 corners show much lower linearity compared to SS_m40_L3. They can tolerate almost 2x higher amplitudes for the same THD. This benefit is visible in the maximum eye opening for these corners in Fig. 9. SS_125_L3 and FF_125_L3 reach almost 31mV compared to SS_m40_L3 which is 19 mV.

Without the proposed adaptation, the nonlinearity will be unknown, and the AFE target amplitude will be set 'small' enough to suit SS_m40_L3, and the target will be same for all corners. This will cause almost 2x reduction of AFE output for SS_125_L3 and FF_125_L3 corners and hence their eye opening will also reduce by 2x, thus demonstrating the usefulness of the proposed estimation.

VI. CONCLUSION

A theory developed with simple approximation of two dominant ISI terms in (1) and third order nonlinearity in (2) works reasonably well for the circuits under consideration. This is because higher order ISI terms and nonlinearity terms are smaller in magnitude. Using the estimated nonlinearity circuit parameters can be optimally adapted leading to improvement in performance. Significant improvement in eye opening is demonstrated for both VGA gain adaptation and decompressive adaptation.

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ARCHIT JOSHI received the B.Tech. degree from the Indian Institute of Technology, Kanpur, India, in 2002, and the Ph.D. degree in electrical and electronic engineering from the Indian Institute of Technology, Delhi, India, in 2019.

From 2002 to 2010, he was with the Serdes Research and Development Group, STMicroelectronics, Greater Noida, India. He moved to Synopsys Inc., and then to Invecas Inc., where he was the Technical Director of Serdes Group, India. He is currently a Principal Engineer with the High-Speed Serial Link Group, Intel Corporation, India. His research interests include power and area efficient wireline transceiver design, and statistical signal processing and its applications to Serdes transceivers to achieve improvements in speed, performance, and power.