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RESEARCH ARTICLE

Vertical-Stack Nanowire Structure of MOS Inverter and TFET Inverter in Low-Temperature Application

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ABSTRACT Tunneling Field-Effect Transistors (TFET) have emerged as promising candidates for integrated circuits beyond conventional metal-oxide-semiconductor field-effect transistors (MOSFET) and could overcome the physical limit, which results in the Subthreshold Swing (SS) < 60mV/dec at room temperature. In this study, we compare the complementary TFET (CTFET) with complementary metal oxide semiconductor (CMOS) at low temperatures (70K) by using the Gate-All-Around (GAA) architecture. The experiment result clearly shows that the CTEFT inverter has better characteristics than the CMOS inverter in various temperatures. While operating at a fixed temperature, the CMOS inverter performs an excellent on/off ratio and SS, etc. However, when a CMOS inverter operates at varying temperatures, CMOS performs worse than CTFET. This is attributed to the influence of lattice scattering, leading to the instability of CMOS characteristics. Therefore, the CTFET inverter is suitable for operation in environments with varying temperatures, exhibiting high stability, which can be applied in space technology. The simulation tool TCAD has been used to investigate the characteristics of CMOS and CTFET at low temperatures.

INDEX TERMS Band-to-band tunneling (BTBT), CMOS, TFET, inverter, gate-all-around (GAA), low temperature, cryogenic, TCAD.

I. INTRODUCTION

In recent years, countries worldwide have increasingly emphasized space development. Therefore, semiconductor components that can withstand significant temperature variations and operate effectively at extremely low temperatures, such as in satellite systems, are gaining significant attention. A metal-oxide-semiconductor field-effect transistor (MOSFET) exhibits excellent device characteristics at room temperature (300K), with a minimum subthreshold swing (SS) as low as 60 mV/dec. MOSFETs play a crucial role in semiconductor devices. In 1965, Gordon E. Moore, co-founder of Intel, proposed Moore's Law, stating that the number of transistors on a semiconductor wafer would double approximately every 18 months with advancements in manufacturing technology.

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As transistor sizes continue to shrink, various defects emerge in short-channel MOSFETs, such as the Short Channel Effect (SCE). Influenced by the SCE, leakage current in MOSFETs becomes a significant challenge as devices shrink, making effective management of leakage current crucial. Otherwise, SCE can lead to reduced reliability and decreased device lifespan. For example, Drain-Induced Barrier Lowering (DIBL) occurs when a large electric field is applied to a MOSFET, causing a significant lowering of the energy band on the drain side, accelerating carrier velocities, and generating high currents. The continuous impact on the lattice at the drain end causes lattice damage, resulting in leakage current. Punch-through is a type of leakage current occurring in the sub-channel. As channel lengths decrease, the depletion region formed between the source and drain contacts the sub-channel, leading to current penetration and permanent device damage.

To overcome the defects caused by SCE in MOSFETs, we compare the characteristics of the Tunnel Field-Effect

Transistor (TFET) with traditional MOSFETs. TFET and MOSFET have similar structures, with the main difference lying in the high-concentration doping types in the source and drain regions, and the substrate being intrinsically doped. Taking NTFET as an example, the doping in the Source-Channel-Drain regions is P^+-I-N^+. Tunneling transistors exhibit excellent characteristics. TFET operates through Band-to-Band Tunneling (BTBT) [11], allowing TFET to function at lower gate voltages and achieve a good on/off ratio. Therefore, its SS can be below 60mV/dec. Due to its structural design, TFET can effectively suppress the SCE, enabling its operation in low-power consumption circuits. Due to the different doping types in the source and drain regions, when the gate is unbiased ($V_{gs} = 0V$), an effective energy barrier is formed between P^+ and I, preventing electrons from tunneling, and the transistor is in an OFF state. When a sufficient positive bias is applied to the gate ($V_{gs} > 0V$), it overcomes the energy barrier between P^+ and I, making electron tunneling easier, and the transistor enters the ON state (Tunneling Allowed) [1], [11]. This process is known as the band-to-band tunneling effect. The gate-all-around (GAA) structure involves a metal gate surrounding the channel, providing excellent gate and control capabilities even as the device dimensions continue to shrink. It effectively suppresses short-channel effects, ensuring the device maintains favorable characteristics.

In this paper, we will use the GAA nanowire structure to compare the characteristics of TFET and MOSFET under extreme temperature variations (325K-70K) and ultra-low temperatures (70K) [2], [9], [12], [13], [14], [15]. From the experimental results, it is evident that TFET, operating through band-to-band tunneling, exhibits minimal sensitivity to drastic temperature changes, making it well-suited for stable performance under varying temperature conditions [3]. Consequently, GAA CTFET demonstrates excellent stability and is highly suitable for applications in space technology.

II. MATERIAL AND METHODS

A. TECHNOLOGY COMPUTER-AIDED DESIGN (TCAD)

This study utilized the Synopsys Technology Computer-Aided Design (TCAD) simulation software, which is employed for semiconductor process and device simulations. Before actual production in semiconductor manufacturing, major corporations, to avoid the production of unreliable devices during the process and the resulting significant costs. In this study, we used two specific models to describe the transport mechanism of TFET transistors and the variety of temperatures. The model "Band2Band(E2)" is to describe the conduction of band-to-band tunneling of TFET transistor, and the model "Thermode {{name = "S" Temperature = @Temp@}}" is used to describe the ambient temperature conditions for transistor operation. Both of these models will be employed to describe the characteristics of the devices in the TCAD, within the SDEVICE program.

B. SIGMAPLOT

SigmaPlot is a graphing software designed for scientific charts and professional data analysis. It can directly read various file formats, including Microsoft Excel, and generate high-quality graphics. SigmaPlot provides users with various graph options, such as regression line charts, automated error bar charts, axis scaling, confidence intervals, worksheets, and nonlinear curves. In this paper, we used Sigmaplot to plot all the experimental data.

C. THE DEVICE PARAMETER

The GAA CMOS inverter is formed vertically by NMOS (N-P-N) and PMOS (P-N-P). The source (S), channel (C), and drain (D) of CMOS have dopant concentrations of 1×10^{19} cm^{-3}, 1×10^{15} cm^{-3}, and 1×10^{19} cm^{-3}, respectively. The gate length (L_g) is 20nm, and the S/D length is 30nm. The isolation layer has a length of 30nm, channel width (W) is 7nm, gate oxide thickness (G_{OX}) is 3nm, and metal layer thickness is 10nm [2]. The work function (WF) for NTFET and PTFET is 4.6eV and 4.7eV. The device structure is shown in Figure 1.

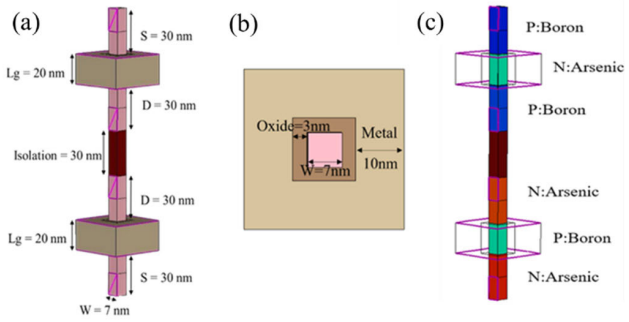

FIGURE 1. (a) The GAA CMOS 3D Structure. (b) The top view of the device. (c) The doping profile of the device.

The GAA CTFET inverter is formed vertically by NTFET (P^+-I-N^+) and PTFET (N^+-I-P^+). The S, C, and D of CTFET have dopant concentrations of 1×10^{19} cm^{-3}, 5×10^{17} cm^{-3}, and 1×10^{19} cm^{-3}, respectively. The L_g is 20nm, and the S/D length is 40nm. The isolation layer has a length of 20nm, W is 5nm, G_{OX} is 3nm, metal layer thickness is 10nm [1], [2]. The WF for NTFET and PTFET is 4.5eV and 4.8eV. The device structure is shown in Figure 2.

III. RESULT

A. I_d-V_g CHARACTERISTIC CURVE

1) GAA CMOS I_d-V_g

The I_d-V_g curve of NMOS and PMOS is shown in Figure 3, with an operating voltage of $V_g = \pm 2V$, $V_d = \pm 0.3V$, and a test temperature ranging from 70K to 325K. CMOS is sensitive to temperature, the graph illustrates that, with decreasing temperature, the ON current of CMOS remains within a certain range, while the SS decreases. This is influenced by lattice vibration, which is temperature-dependent [4].

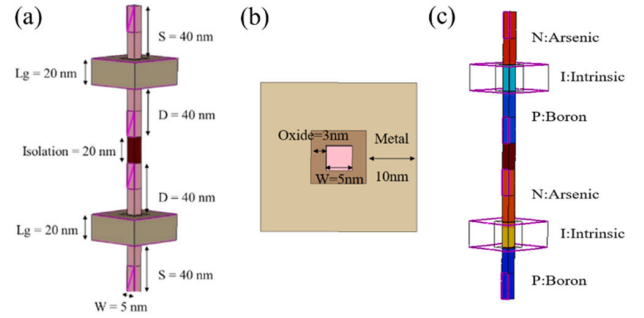

FIGURE 2. (a) The GAA CTFET 3D Structure. (b) The top view of the device. (c) The doping profile of the device.

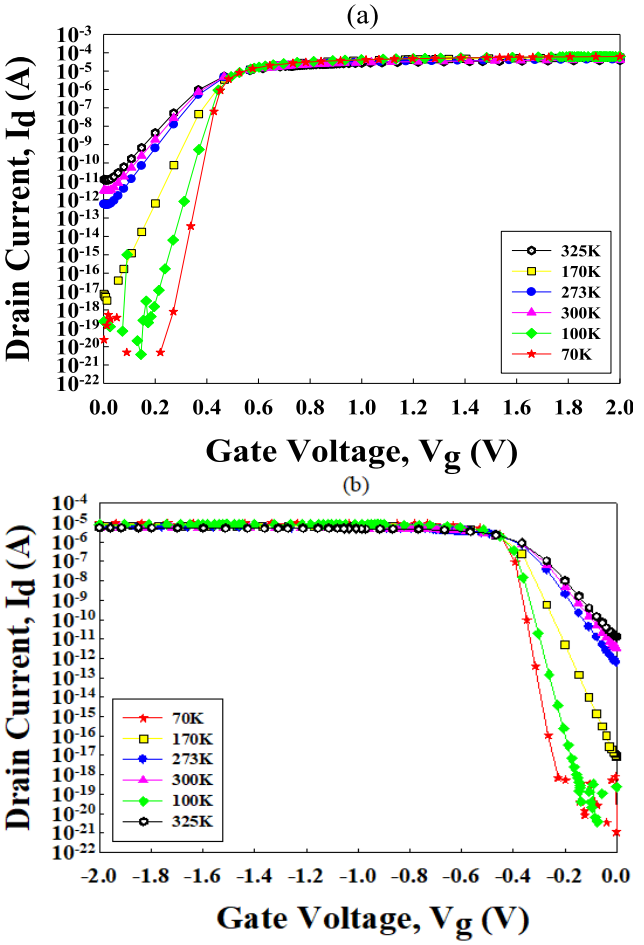

FIGURE 3. The Id-Vg characteristic of CMOS device. (a) The NMOS Id-Vg curve. (b) The PMOS Id-Vg curve. The result clearly shows the sensitivity of the temperature due to the impact of lattice scattering, the carrier mobility of the CMOS enhanced while decreasing the temperature.

According to $\mu_L = T^{-\frac{3}{2}}$, while operating at higher temperatures, the lattice absorbs more energy, resulting in increased vibration and more severe electron-phonon scattering, leading to a degradation in SS. Conversely, when operating at lower temperatures, the lattice absorbs less energy, resulting in decreased vibration and less electron-phonon scattering, leading to an improvement in SS and enhanced carrier mobility, decreased S/D resistance (R_{SD}), along with a slight increase in ON current [2], [4], [8], [9], [10], [13], [14]. Table 1 provides the detailed CMOS ON current and SS simulation values.

TABLE 1. The detailed values for GAA CMOS operate at various temps.

Temp(K)	NMOS I_d(A)	NMOS SS (mV/dec)	PMOS I_d(A)	PMOS SS (mV/dec)
70	6.86e-05	14.4	9.36e-06	14.2
100	6.22e-05	30.7	8.15e-06	20
170	5.48e-05	34.2	6.68e-06	34.3
273	4.34e-05	54.94	5.64e-06	55.7
300	4.09e-05	60.38	5.45e-06	61.2
325	3.88e-05	65.43	5.29e-06	66

While CMOS exhibits a good on/off ratio and high-quality ON current, its stability is limited to operation at a fixed voltage. If CMOS is intended to operate in environments with varying temperatures, its susceptibility to temperature variations may lead to instability, thereby reducing the reliability of the device.

Therefore, CMOS is inherently an unstable device, easily influenced by external factors, making it unsuitable for applications in space components [7], [12].

2) GAA CTFET I_d-V_g

Figure 4 illustrates the I_d-V_g curve of NTFET and PTFET, with an operating voltage of $V_g = \pm 2$V, $V_d = \pm 0.1$V, and a test temperature ranging from 70K to 325K. The conduction mechanism of a tunnel transistor is through band-to-band tunneling, making them minimally affected by temperature [3]. The low-temperature characteristics of CTFET remain nearly identical to those at room temperature, demonstrating stability across different environmental temperatures.

With decreasing temperature, TFET's ON current experiences a slight reduction due to the influence of thermal emission. When operating at low temperatures, the energy that carriers can obtain to overcome the binding energy is reduced, resulting in a slight decrease in ON current and OFF current. Another potential factor is the impact of interface traps, causing a decrease in SS at low temperatures, as shown in Table 2. However, given that TFET's SS is superior to that of traditional MOS at room temperature and is nearly unaffected by temperature, the overall change is minimal. This suggests that CTFET is well-suited for operation in environments with varying temperatures, providing high stability and significantly enhancing device reliability, making it suitable for application in space components.

B. I_d-V_d CHARACTERISTIC CURVE

1) GAA CMOS I_d-V_d

Figure 5 illustrates the I_d-V_d curve of the NMOS and PMOS with an operating voltage of $V_g = \pm 1$V, $V_d = \pm 1$V, and a test temperature ranging from 70K to 325K. As mentioned above, owing to the variation in the temperature will cause a dramatic change in the device's characteristics. We can observe that as the operating temperature decreases, the thermal impact on

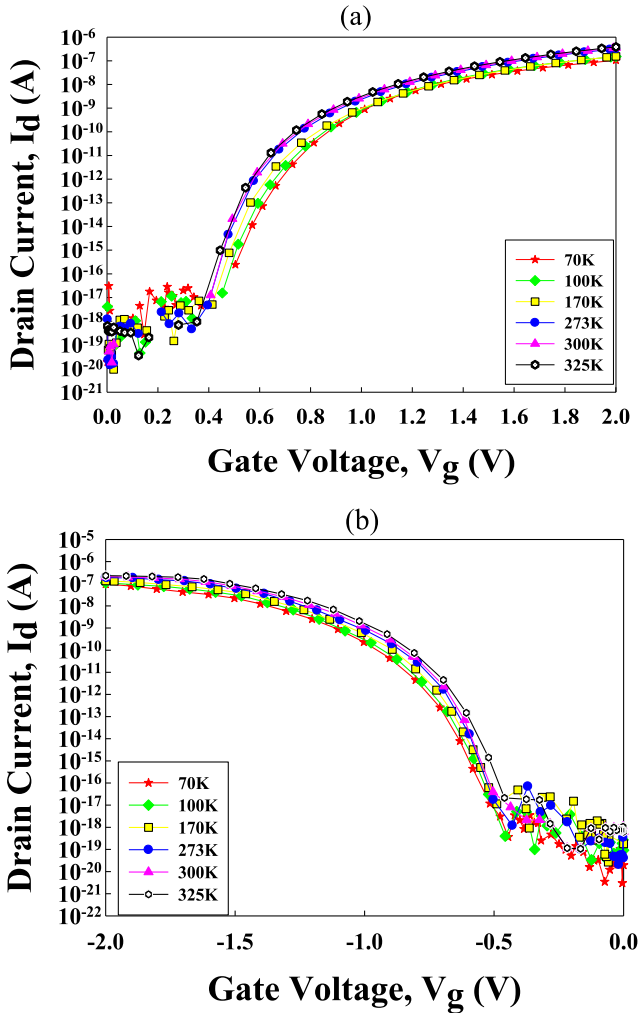

FIGURE 4. The Id-Vg characteristic of CTFET device. (a) The NTFET Id-Vg curve. (b) The PTFET Id-Vg curve. The experimental results demonstrate the stability of CTFET under high-temperature variations. Due to its conduction through tunneling, CTFET exhibits minimal sensitivity to temperature changes.

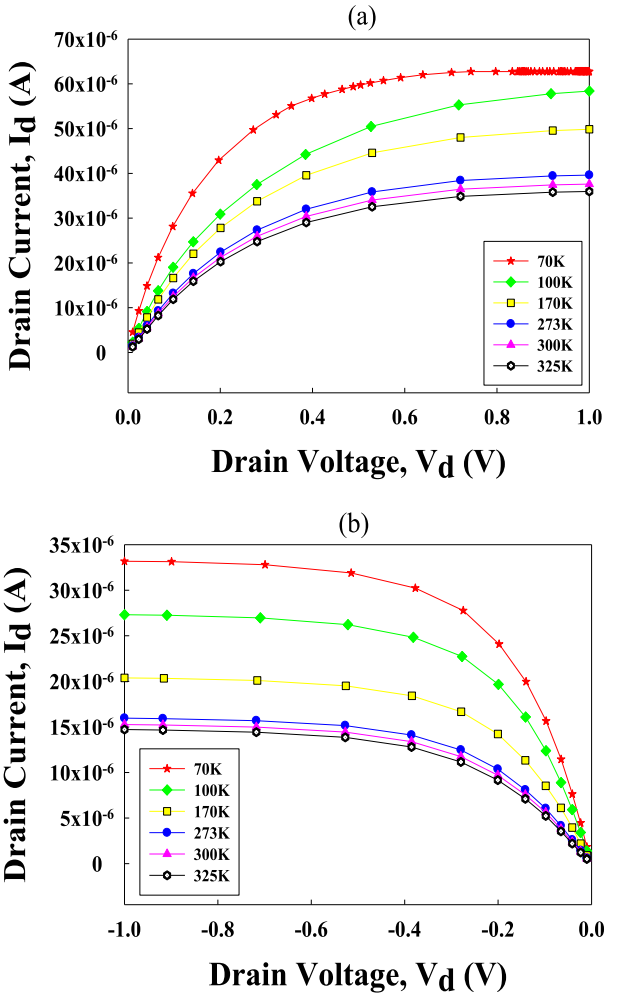

FIGURE 5. The Id-Vd characteristic of CMOS device. (a) The NMOS Id-Vd curve. (b) The PMOS Id-Vd curve. The result clearly shows the sensitivity of the CMOS structure due to the impact of lattice scattering, the R_{SD} resistance of the CMOS decreased while decreasing the temperature.

TABLE 2. The detailed values for GAA CTFET operate at various temps.

Temp(K)	NTFET I_d(A)	NTFET SS (mV/dec)	PTFET I_d(A)	PTFET SS (mV/dec)
70	1.06e-07	50	9.70e-08	49.8
100	1.51e-07	45.5	1.10e-07	49.3
170	1.53e-07	43.9	1.36e-07	45.3
273	3.22e-07	37.6	1.95e-07	39.9
300	3.53e-07	36.2	2.14e-07	38.3
325	3.84e-07	38.6	2.32e-07	42.9

the lattice diminishes, resulting in reduced lattice vibrations [4], [10], [12]. Therefore, it can be observed that compared to 325K, 70K owns a lower R_{SD} resistance which can provide better SS, ON current, and high-speed operation [3], [14].

2) GAA CTFET I_d-V_d

Figure 6 illustrates the I_d-V_d curve of the NTFET and PTFET with an operating voltage of $V_g = \pm 1V$, $V_d = \pm 1V$, and a test temperature range from 70K to 325K. As its conduction mechanism involves band-to-band tunneling, the CTFET is less affected by lattice scattering due to temperature variations than CMOS devices, avoiding alterations in device characteristics. The reason the ON current of the TFET is lower than that of the MOSFET is that the large tunneling resistance in the TFET significantly reduces the tunneling probability of the carriers [16], [17].

C. TRANSCONDUCTANCE (g_m)

1) GAA CMOS g_m

The g_m-V_g plot in Figure 7 illustrates the behavior of NMOS with a voltage of $V_g = 2V$, $V_d = 0.3V$, and testing temperatures ranging from 70K to 325K. As the temperature decreases, the reduction in lattice vibrations leads to a decrease in lattice scattering, resulting in a lower resistance value of R_{SD} resistance [4], [10], [14]. Since transconductance (g_m) is inversely proportional to R_{SD} resistance, the impact of low temperature on R_{SD} resistance can be observed through the g_m-V_g plot. Figure 8 presents the variation in R_{SD} resistance values for NMOS at different temperatures.

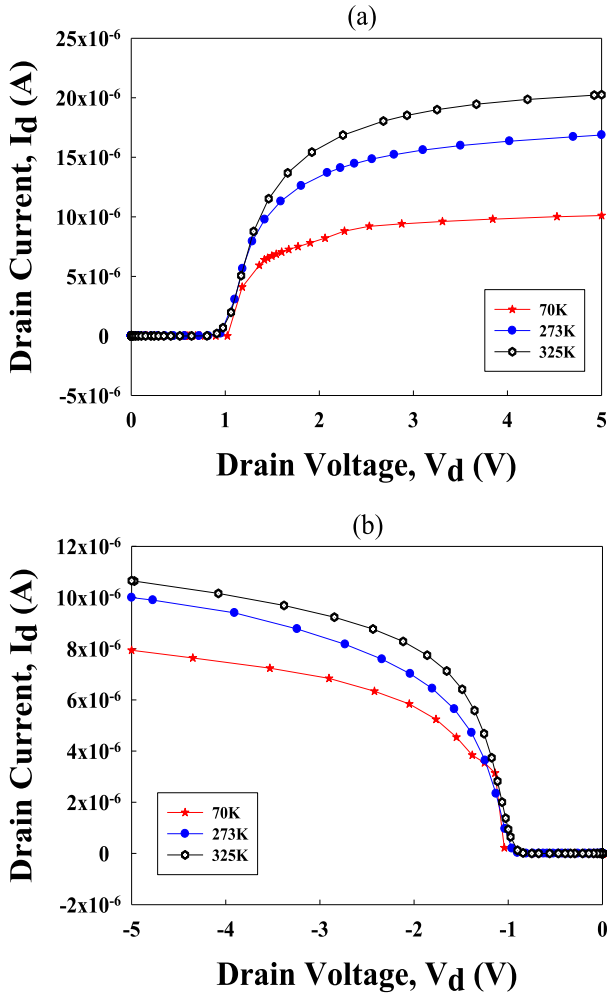

FIGURE 6. The Id-Vd characteristic of CTFET device. (a) The NTFET Id-Vd curve. (b) The PTFET Id-Vd curve. The result clearly shows the stability of the CTFET structure due to the band-to-band tunneling mechanism, CTFET is less affected by lattice scattering in temperature variations compared to CMOS devices, avoiding alterations in device characteristics. In contrast, CTFET demonstrates remarkable stability with minimal changes in ON current under high-temperature variations.

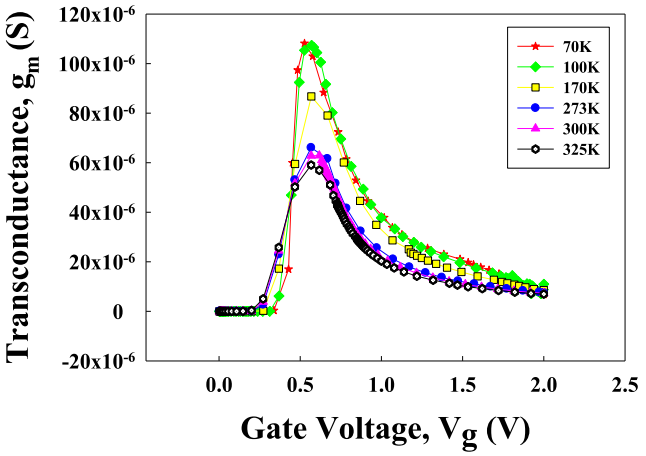

FIGURE 7. Variation of NMOS gm with different temperatures. The significant difference in gm between 70K and 325K is attributed to the inverse relationship between gm and R_{SD}. The observation indicates that as the temperature decreases, gm increases, thereby reducing the impact of lattice scattering on the mobility of the device.

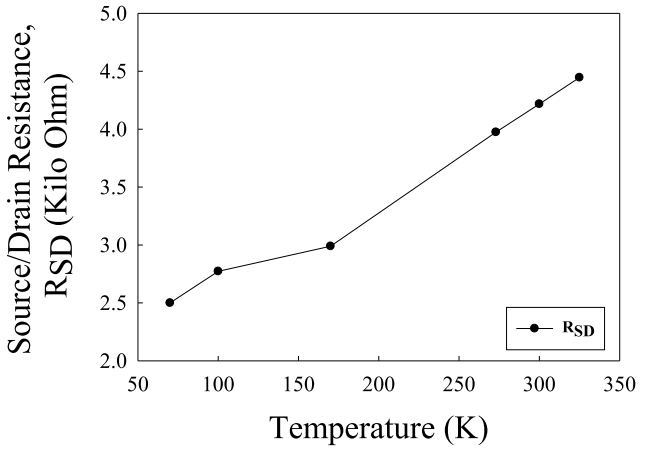

FIGURE 8. Variation of NMOS R_{SD} with different temperatures. As mentioned above, we can see the impact of temperature-induced lattice scattering on the R_{SD} of the device.

2) GAA CTFET g_m

The g_m-V_g plot for NTFET is shown in Figure 9, with an operating voltage of $V_g = 2V$, $V_d = 0.3V$, and a testing temperature ranging from 70K to 325K. Under the influence of thermal emission, at low temperatures, carriers acquire insufficient energy, leading to a slight increase in R_{SD} resistance. This increase in resistance slows down the tunneling speed of TFET, resulting in a slight decrease in ON current at low temperatures [8]. Therefore, it can be observed that g_m decreases with decreasing temperature. The variation in R_{SD} resistance values for different temperatures is illustrated in Figure 10.

D. THRESHOLD VOLTAGE (V_t)

1) GAA CMOS V_t

As shown in Figure 11, with decreasing temperature, the threshold voltage of NMOS increases, while the threshold voltage of PMOS decreases. Taking NMOS as an example, this phenomenon can be demonstrated through the following formulas (1) and (2):

$$n_0 = N_c e^{\frac{-(E_C - E_F)}{kT}} \tag{1}$$

$$E_C - E_F = kTln\left(\frac{N_C}{n_0}\right) = kTln(\frac{N_C}{N_D}) \tag{2}$$

As explained from the band diagram, when the temperature decreases, the position of the Fermi level (E_F) gradually moves closer to the conduction band (E_c), causing the distance between E_F and the intrinsic Fermi level (E_i) to increase. As a result, φ_{fp} increases, and the electric field strength increases. According to the formula (3) for V_t:

$$V_t = V_{FB} + 2\varphi_{fp} + \frac{\sqrt{4e\varepsilon N_A \varphi_{fp}}}{C_{OX}} \tag{3}$$

From the above formulas, it can be understood that when the temperature decreases, the changes in the Fermi level

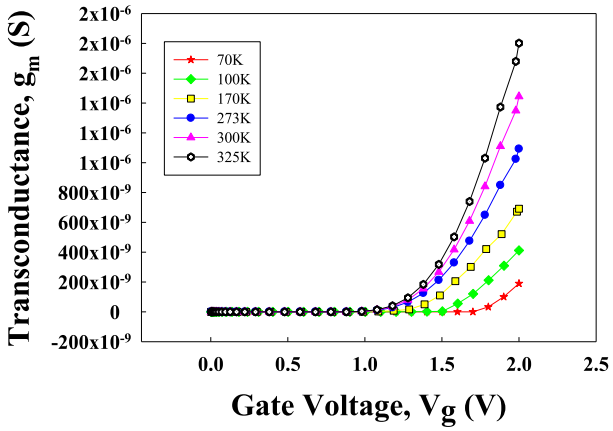

FIGURE 9. Variation of NTFET gm with different temperatures. Under the influence of low temperatures, the carrier acquires insufficient energy, leading to a decrease in the transconductance which will slightly influence the SS of CTFET.

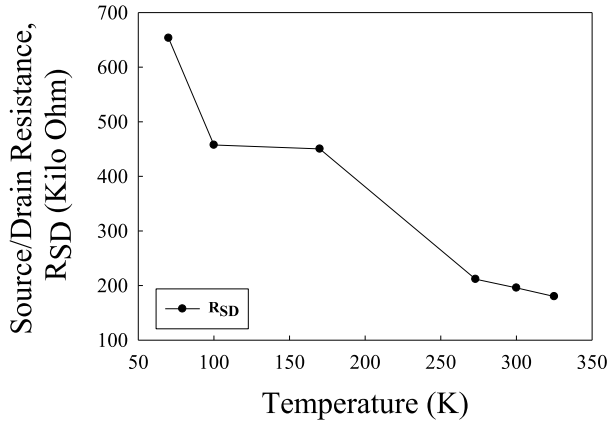

FIGURE 10. Variation of NTFET R_{SD} with different temperatures. As the temperature decreases, carriers acquire insufficient energy, leading to a slight increase in R_{SD} resistance.

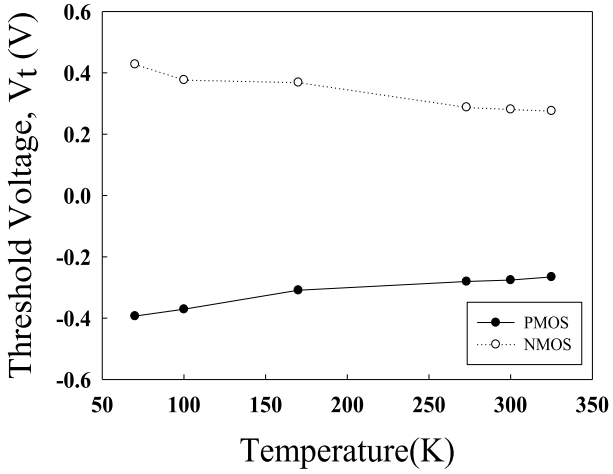

FIGURE 11. Variation of CMOS V_t with different temperatures. When the temperature decreases, the changes in the Fermi level concerning the threshold voltage lead to an increase in V_t as the temperature decreases.

concerning the threshold voltage lead to an increase in V_t as the temperature decreases [6]. The increase in electric field strength may cause the ionization of non-charged impurity ions in the oxide layer, increasing the charge, which may also contribute to the rise in V_t. This explains the trend of V_t variation for PMOS at different temperatures [4], [5], [6], [14].

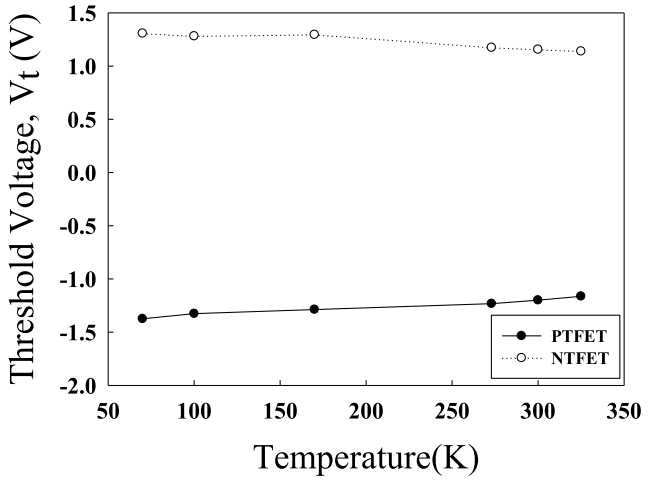

FIGURE 12. Variation of CTFET V_t with different temperatures. The impact of thermal emission results in reduced carrier transport capability at low temperatures, causing a slight increase in V_t.

2) GAA CTFET V_t

The TFET inverter operates through tunneling and is therefore not directly affected by temperature. However, due to the influence of thermal emission, there is a slight decrease in ON current when the temperature decreases, leading to a slight change in V_t.

As shown in Figure 12, the threshold voltage of the TFET inverter changes at different temperatures. The impact of thermal emission results in reduced carrier transport capability at low temperatures, causing a slight increase in V_t [8]. From the graph, it can be observed that the TFET inverter exhibits relatively small variations within an acceptable range. This indicates that the TFET inverter is suitable for operation in environments with varying temperatures.

E. SUBTHRESHOLD SWING (SS)

1) GAA CMOS SS

As shown in Figure 13, when considering a fixed temperature, especially at low temperatures, the characteristics of CMOS perform optimally when operated at a constant temperature (ex: T = 70K or 300K). However, for conditions requiring operation in environments with varying temperatures, CMOS exhibits relative instability. The wide range of SS variations leads to a reduction in device reliability [14], making it unsuitable for providing stable performance in space applications. Table 3 presents the values of SS for CMOS at different temperatures.

2) GAA CTFET SS

When considering a fixed temperature, CTFET's characteristics may not outperform CMOS, especially at lower temperatures (T < 300K). However, for conditions requiring

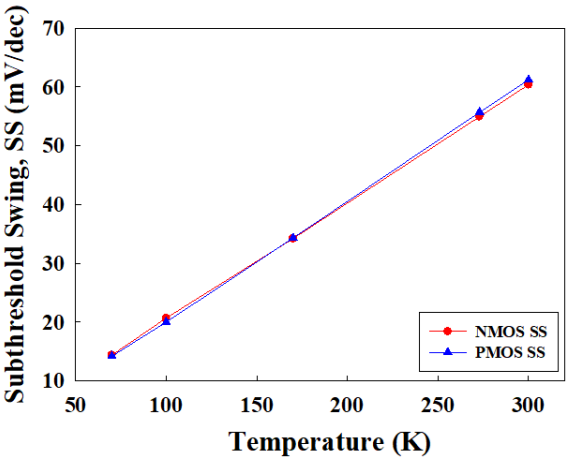

FIGURE 13. Variation of CMOS SS under different temperatures. The CMOS shows unstable characteristics in a wide range of temperatures, which is not suitable for space applications.

TABLE 3. Variation of CMOS SS under different temperatures.

	70K	100K	170K	273K	300K
NMOS SS (mV/dec)	14.4	20.7	34.2	54.9	60.4
PMOS SS (mV/dec)	14.2	20.0	34.3	55.7	61.2

TABLE 4. Variation of CTFET SS under different temperatures.

	70K	100K	170K	273K	300K
NTFET SS (mV/dec)	50	45.5	43.9	37.6	36.2
PTFET SS (mV/dec)	49.8	49.3	45.3	39.9	38.3

operation in environments with varying temperatures, CTFET exhibits excellent stability and remarkable device reliability. It is suitable for providing stable performance in space applications. Table 4 presents the values of SS for CTFET at different temperatures.

The reason for the decrease in CTFET's SS with decreasing temperature is attributed to the influence of thermal emission. At lower temperatures, the carrier transport capacity is insufficient, leading to a slight increase in carrier mobility. This, in turn, results in a minor increase in SS at low temperatures, as shown in Figure 14.

F. THE TRANSIENT ANALYSIS

Figure 15 and Figure 16 depict the transient response of CMOS and CTFET at 100K and 325K, respectively. While the CMOS inverter exhibits normal inversion functionality, the graphs illustrate that CMOS operates with different V_t and SS at varying temperatures due to lattice scattering effects, resulting in instability during device operation. On the other hand, the CTFET inverter demonstrates high stability

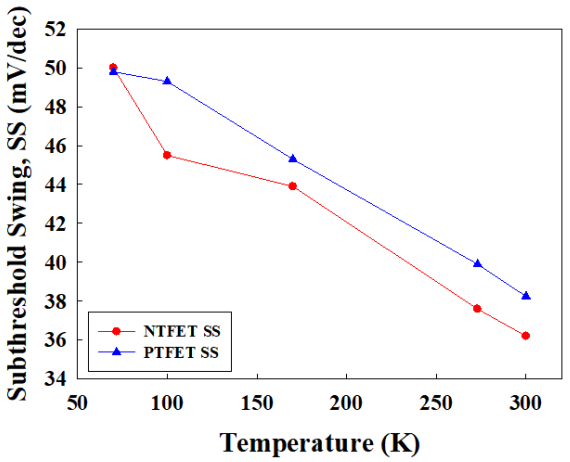

FIGURE 14. Variation of CTFET SS under different temperatures. Due to the influence of thermal emission. The carrier transport capacity is insufficient when operating at low temperatures, leading to a slight increase in carrier mobility, which will cause an increase in the SS.

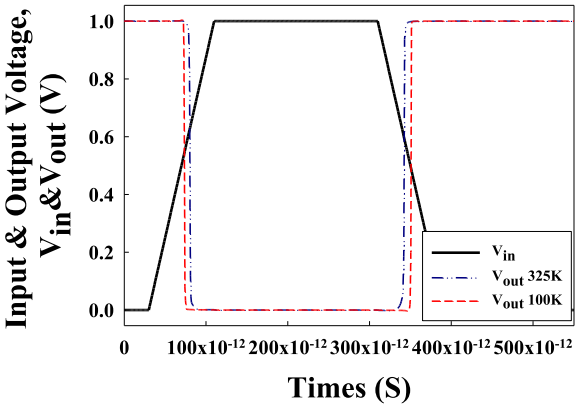

FIGURE 15. The transient analysis of CMOS in 100K & 325K. Due to lattice scattering effects, resulting in instability during device operation.

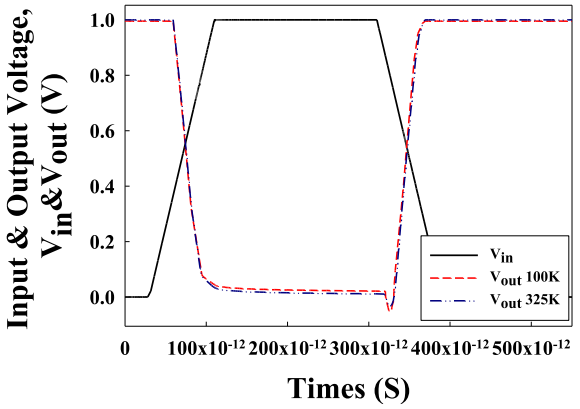

FIGURE 16. The transient analysis of CTFET in 100K & 325K. Due to the limited impact of temperature on CTFET, it is evident from the transient analysis that CTFET exhibits excellent stability under varying temperature conditions.

under different temperature conditions, with the voltage drop at low temperatures influenced by thermal emission.

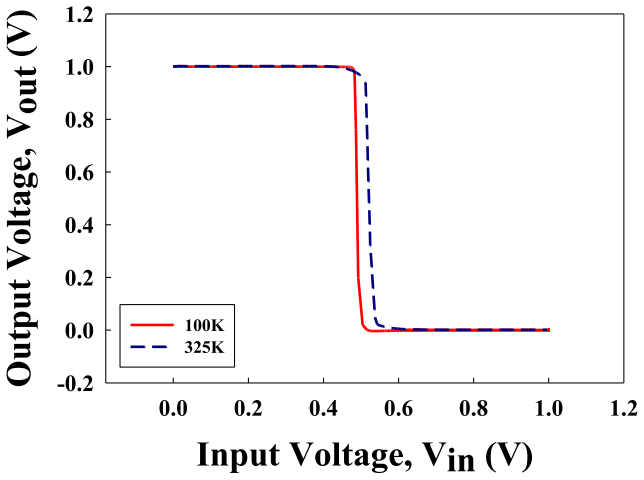

FIGURE 17. The voltage transfer characteristic of CMOS inverter. The CMOS inverter exhibits instability under different temperature conditions due to the influence of lattice scattering, resulting in non-overlapping VTC curves.

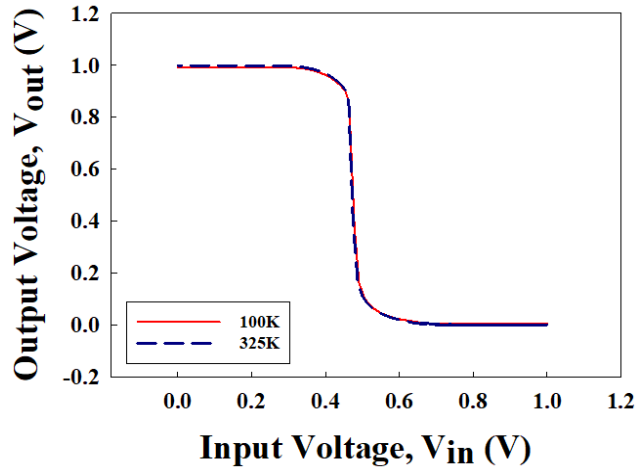

FIGURE 18. The voltage transfer characteristic of CTFET inverter. The CTFET demonstrates extremely high stability under varying temperatures.

G. VOLTAGE TRANSFER CHARACTERISTIC (VTC)

Figure 17 and Figure 18 illustrate the Voltage Transfer Characteristic (VTC) for CMOS and CTFET respectively at temperatures of 100K and 325K. As observed from the graphs, the CMOS inverter exhibits instability under different temperature conditions due to the influence of lattice scattering, resulting in non-overlapping VTC curves. In contrast, CTFET demonstrates extremely high stability under varying temperatures. The impact of thermal emission leads to a slight voltage drop, but it does not compromise the excellent performance of the CTFET inverter at low temperatures.

IV. CONCLUSION

We simulated the device characteristics of GAA-structured CMOS and CTFET under varying temperatures ranging from 325K to 70K. The simulation results reveal that CTFET is well-suited for operation in environments with high-temperature variations due to its unique operating mode. CTFET operates through band-to-band tunneling, and under drastic temperature changes, it does not experience direct effects on its characteristics. The only factor influencing changes in device properties is the insufficient carrier energy caused by low temperatures, leading to a decrease in carrier mobility and slight variations in CTFET's V_t and SS when the temperature reaches 70K. However, these changes do not significantly impact the overall device characteristics. CTFET still shows stability on ON current, SS, V_t, etc.

On the other hand, CMOS exhibits excellent device characteristics under fixed operating temperatures, but considering the need for operation in environments with high-temperature variations, CMOS proves to be highly unstable compared to CTFET. When CMOS operates at 70K, reduced lattice vibrations allow the device to operate in an ideal state. However, a rapid drop in temperature from 325K to 70K induces severe lattice scattering, causing dramatic changes in V_t and SS. If the operating temperature rapidly transitions from 325K to 70K, it may lead to significant damage to the device, with the sudden acceleration of carriers possibly causing lattice damage at the drain terminal, resulting in reduced device reliability.

Therefore, the results indicate that CTFET holds great potential as a transistor device for future space applications, offering stability and reliability in the face of varying temperature conditions.

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