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RESEARCH ARTICLE

Ultralow-Power Inverter-Based Delta-Sigma Modulator for Wearable Applications

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ABSTRACT This paper introduces and experimentally validates a switched-capacitor inverter-based second-order 3-tap FIR single-bit Delta-Sigma Modulator ($\Delta\Sigma$M) designed for nanowatt-level analog-to-digital conversion in wearable healthcare devices. The focus is on applications with energy harvesters, emphasizing continuous monitoring of chronic conditions and closed-loop drug-delivery systems. The design methodology addresses ultralow-power considerations at both architectural and transistor levels, tackling challenges like process variations without relying on complex digital calibration techniques. Experimental results from prototypes, implemented on a standard 180-nm CMOS process, reveal a peak SINAD of 77.8 dB and SNR of 79.4 dB, with a power consumption of 71.5 nW at a 900-mV supply. Measurements across nine chip samples are consistent, demonstrating low DC offset, with low temperature drift and live sensitivity. The outcomes confirm the modulator suitability for energy-harvested wearable systems.

INDEX TERMS Analog-to-digital converter, body-worn sensor, Delta-Sigma modulation, inverter-based circuits, low voltage, switched-capacitors, ultra-low power, wearable systems.

I. INTRODUCTION

Next-generation wearable systems are envisioned to seamlessly integrate multi-modal energy harvesters, sensor acquisition systems, and communication interfaces. Ubiquitous adoption of these innovative wearables hinges on their miniaturization and integration capabilities. Miniaturization relies on absence of traditional bulky batteries, small form factor and ultimately on ultra-low power operation of the whole system [1], [2], [3].

In order to reduce power, an intuitive solution might be to set the entire electronic acquisition interface to operate directly at the harvester voltage levels. These devices exhibit varied open-circuit voltages (OCVs) with values ranging between 200 mV and 700 mV [4], [5], [6], [7]. Realizing analog-to-digital converters (ADCs) at voltage level of 200 mV presents a formidable challenge. Only a handful of groundbreaking designs have been documented to function at these ultra-low supply voltages (ULVs) [8], [9], [10], [11]. Several issues affects such ULV implementations: offset, noise, non-linearity and process and temperature dependence. With reasonably low DC-DC step-up ratios, supply levels of around 1 V can be achieved with high-efficiency [12]. State-of-the-art ultra-low-power (ULP) ADCs contemplate both successive approximation register (SAR) architectures and Delta-Sigma Modulators ($\Delta\Sigma$Ms): designs of [13], [14], and [15] are based on SAR ADCs, featuring asynchronous, oversampling and Nyquist-rate solutions; works in [10], [16], [17], [18], and [19] propose switched-capacitors (SC) $\Delta\Sigma$Ms; works in [20] and [21] present asynchronous $\Delta\Sigma$Ms;

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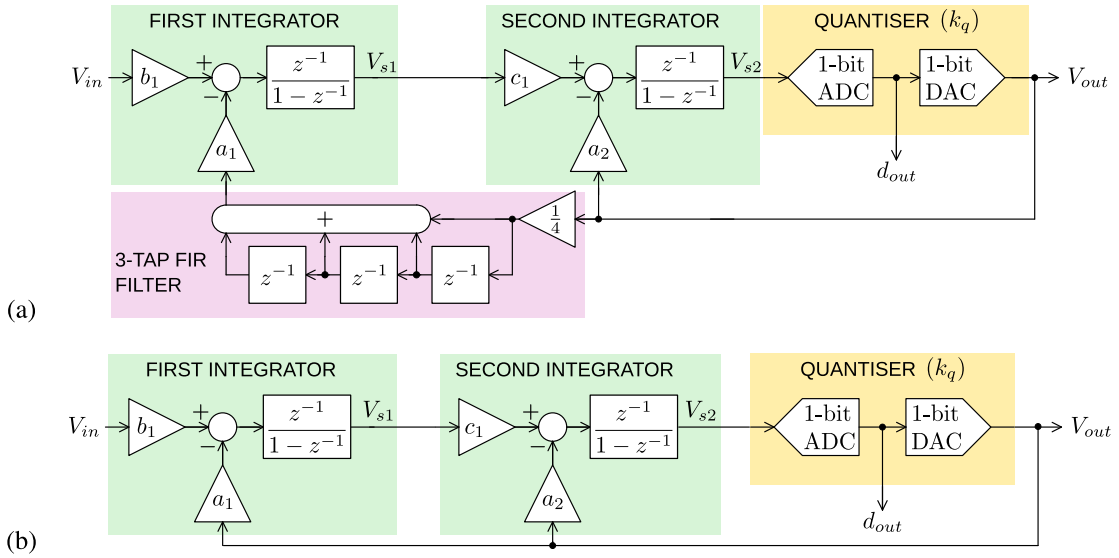

FIGURE 1. Inverter-based 3-tap FIR single-bit second-order ΔΣM: (a) block diagram; (b) block diagram of the reference modulator without FIR.

finally, [22] introduces an hybrid continuous/discrete-time ΔΣM with programmable digital autoranging.

In this work a ΔΣM is presented. The modulator achieves a baseline resolution of 12 ENOB, a minimum bandwidth of 15 Hz, while operating at a 900-mV supply. Section II delves into both architectural-level and transistor-level design choices. Inverter-based OTAs with extremely small aspect ratios (W/L in the order of 1/100) have been adopted. In order to increase the circuit resilience against process and temperature variations, a finite-impulse-response (FIR) feedback has been included in the modulator topology. All our design choices are devoted to obtain a power consumption levels below 100 nW while maintaining the design as minimalist as possible. Experimental results are showcased in Section III. To offer a comprehensive insight into the circuit resilience, performance ratings at 700 mV and at different temperatures are presented. Concluding the paper, Section IV benchmarks the proposed solution against state-of-the-art ULP ADCs.

II. DELTA-SIGMA MODULATOR FOR ULP APPLICATIONS

A. SECOND-ORDER SINGLE-BIT FIR-DAC MODULATOR

The block diagram of the proposed second-order ΔΣM with a SC single-bit 3-tap FIR DAC is shown in Fig. 1(a). The modulator is inspired by the minimalist design by Boser and Wooley [23] shown in Fig. 1(b). ΔΣMs with FIR DACs were introduced in [24]. While FIR DACs in ΔΣMs are common in continuous-time implementations in order to reduce clock-jitter sensitivity [25], [26], few examples have been presented regarding their use together with SC-based modulators [27], [28], [29]. The FIR DAC, incorporated only on feedback path to the first integrator stage, aims to ease settling requirements on the SC integrator amplifiers by reducing the amplitude of the output voltage steps, without incurring into the circuital complexity of multi-bit quantisation [30]. To our purpose, the same principle, is employed to mitigate the modulator sensitivity to process variability. In the following sections, the design choices related to the FIR filter are discussed in detail.

B. MODULATOR STABILITY

As mentioned earlier, a single FIR feedback branch has been employed, reducing the circuit complexity with respect to the full-FIR implementation of [24]. This choice, however, influences the modulator signal-transfer function (STF) and quantization-noise-transfer function (NTF), which are found to be, respectively:

$$\mathrm{STF}_3(z)=\frac{b_1c_1k_qz^{-2}}{1-(2-a_2k_q)z^{-1}+[1-a_2k_q+a_1c_1k_qF_3(z)]z^{-2}}, \tag{1}$$

$$\mathrm{NTF}_3(z)=\frac{(1-z^{-1})^2}{1-(2-a_2k_q)z^{-1}+[1-a_2k_q+a_1c_1k_qF_3(z)]z^{-2}}, \tag{2}$$

where the F_3 can be related to the generic N-tap FIR transfer function, $F_N(z)$, with equally weighted coefficients:

$$F_N(z)=\frac{1}{N+1}\sum_{i=0}^{N}z^{-i}. \tag{3}$$

The scaling factor $(N+1)^{-1}$ in Eq. (3) ensures the preservation of the full scale to that set by the feedback DAC. The effective quantizer gain, k_q, plays a fundamental role. k_q is defined as:

$$k_q=\frac{\mathcal{E}[|V_{s2}|]}{\mathcal{E}[V_{s2}^2]}, \tag{4}$$

where $\mathcal{E}$ denotes the expectation operator, and V_{s2} represents the input signal of the quantizer. Unfortunately, the value of k_q arises from the nonlinear behavior of the single-bit

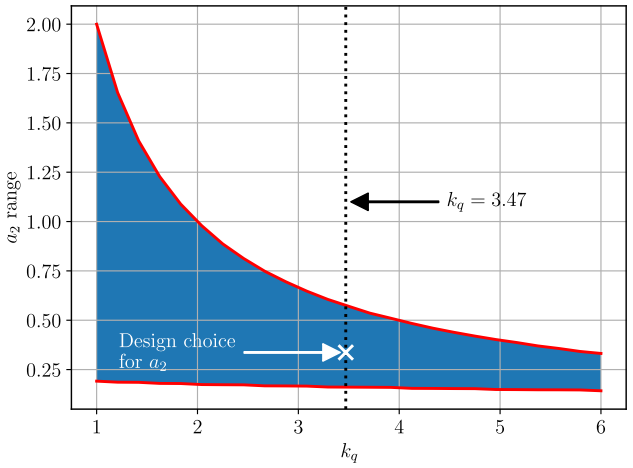

FIGURE 2. Stability region (shaded area) determined by the linearised model of the modulator of Fig. 1(a), in terms of a_2 *vs.* k_q. The rest of the coefficients are set as: $a_1 = b_1 = 0.1253$ and $c_1 = 0.4938$.

quantizer and can be determined only through simulation data. In determining the stability of the modulator, we also have to consider the influence of high-order polynomial terms in the denominator, $D(z)$, of STF_3 and NTF_3. With the inclusion of the FIR filter, the polynomial is expanded up to the fifth order, raising concerns about stability.

To obtain stable modulator operation, we proceed by first determining a suitable set of coefficients (a_1, a_2, b_1, c_1) for the reference (FIR-less) modulator of Fig. 1(b). Its STF and the NTF are, respectively:

$$\mathrm{STF}_0(z) = \frac{b_1 c_1 k_q z^{-2}}{1-(2-a_2 k_q)z^{-1}+[1-a_2 k_q+a_1 c_1 k_q]z^{-2}}, \quad (5)$$

$$\mathrm{NTF}_0(z) = \frac{(1-z^{-1})^2}{1-(2-a_2 k_q)z^{-1}+[1-a_2 k_q+a_1 c_1 k_q]z^{-2}}. \quad (6)$$

Using the widely adopted $\Delta\Sigma$ Toolbox [32], and setting the maximum output range of the integrators to 50% of the DAC full scale (V_{FS}), we obtained $a_1 = b_1 = 0.1621$, $a_2 = 0.1684$, $c_1 = 0.5195$. When translating this specification to actual voltage values, taking $V_{FS} = 900\,\mathrm{mV}$ into account and aligning the single-ended signal baseline to $V_{FS}/2$, it results in an integrator output, V_{s1}, occupying the range between 225 mV and 675 mV. This arrangement ensures a nominal $V_{DS,sat}$ headroom of $V_{FS}/4 = 225\,\mathrm{mV}$ for both the NMOS and PMOS devices. This choice is coherent with the use of non-cascdoded inverter-like amplifiers in order to reduce distortion components. Discussion on this aspect is provided at the end of Section II-D.

In the following we discuss the application of the previously found set of coefficients to the modulator of Fig. 1(a). To ensure stability, it is imperative that the roots of $D(z)$, denoted as r_i (with $i \in [1, 5]$), lie within the unit circle of the complex plane. To address this concern, the coefficient a_2 is adjusted to identify a stable region even in the presence of uncertainty in k_q. A roots-locus analysis of $D(z)$ as a function of a_2 and k_q has been conducted using a Python script employing the symbolic module SymPy [31]. The numerical evaluation yields the results depicted in Fig. 2. In the shaded region of the plot, $|r_i| < 1$, indicating stability. Conversely, outside the shaded region, the modulator is assuredly unstable.

To verify modulator stability a simple Python script implementing the difference equations describing the behaviour of the modulator of Fig. 1(a) has been implemented. With $a_2 = 0.3368$, doubling the value of the corresponding coefficient of modulator of Fig. 1(b), a stable modulator is found, providing also $k_q = 3.47$. Similar analyses have been performed with modulator prototypes implementing different order of FIR filters from $F_1(z)$ up to $F_4(z)$, as defined by Eq. (3). In all cases, a stable modulation has been achieved by setting $a_2 = 0.3368$. This design choice is also represented in Fig. 2, where large safety margins against possible variations of both a_2 and k_q are observed.

C. OCCUPATION RANGE OF THE STATE VARIABLES

In the subsequent design phase, we assessed the effects of the FIR technique to the statistical characteristics of the modulator states variables, focusing on V_{s1}. As demonstrated in Figs. 3(a) and (b), employing the FIR DAC induces two effects at the output of the first integrator stage, V_{s1}:

(i) An increase in range occupation, RO, defined as:

$$\mathrm{RO} = \frac{V_{s1,\max} - V_{i1,\min}}{V_{FS}}. \quad (7)$$

(ii) A decrease in the maximum step, defined as:

$$\Delta V_{s1,\max} = \max |V_{s1}[n] - V_{s1}[n-1]|, \quad (8)$$

where $V_{s1}[n]$ identifies the value of the integrator output at the clock-cycle number $n > 0$, while $V_{s1}[0]$ is the integrator initial condition.

The increase of RO is evidently a detrimental effect, whereas the reduction of $V_{s1,\max}$ is beneficial. In the context of system-level analysis we will refer to the normalized maximum step, $V_{s1,\max}/V_{FS}$.

The plots of Figs. 3(a) and (b) have been obtained through a simple numerical model of the modulator of Fig. 1(a). For these behavioural simulations implemented using the Python language, a sinusoidal stimulus $V_{in} = V_p \cdot \sin(2\pi f_{in})$ have been adopted, with $V_p = V_{FS}/3$ and $f_{in} = f_{ck}/3840$, being f_{ck} the modulator operating frequency. Quantitatively, with an increase in the number of taps of the FIR, the RO stabilizes slightly above 67% when the FIR is employed, irrespective of the number of taps. On the other hand, $\Delta V_{s1,\max}/V_{FS}$ monotonically decreases from a value of 14.4% when the FIR is not employed to slightly below 5% for the 3-tap FIR case. The same plot indicates that increasing the number of taps beyond 3 only yields marginal improvements. Therefore, a 3-tap FIR was chosen for this design, resulting in the architecture of Fig. 1(a). To guarantee an RO below 50%, additional uniform coefficient re-scaling has been implemented, resulting in: $a_1 = b_1 = 0.125$, $a_2 = 0.246$, $c_1 = 0.494$. With this final re-scaling step,

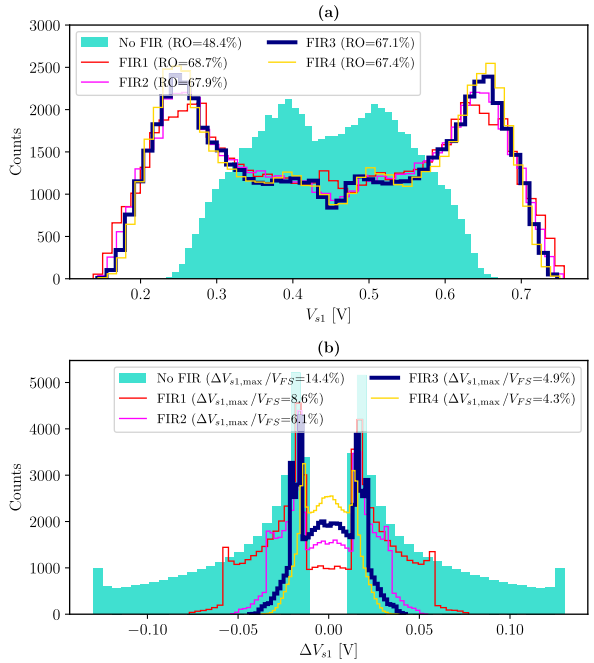

FIGURE 3. (a) Statistical distributions at first-integrator output V_{s1} for a single-tone input signal $V_{in} = V_P \sin(2\pi f_{in})$, ($V_P = 300$ mV, $f_{in} = f_{ck}/3840$); (b) ΔV_s accounting for integrator state variable variations at each clock cycle.

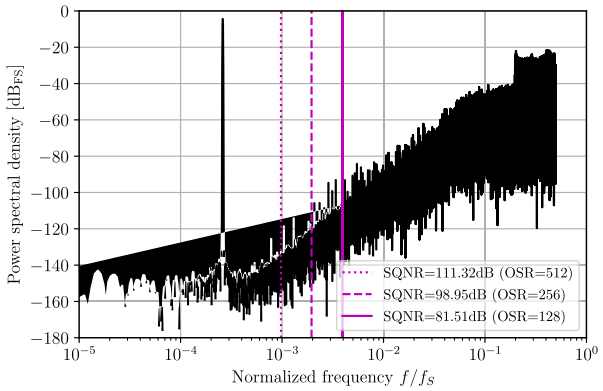

FIGURE 4. Output spectrum of the modulator for signal-to-quantization--noise ratio (SQNR) evaluation at different values of OSR.

there are no significant changes observed in the STF and NTF. From behavioural simulations, we observed also that a minimum OSR of 128, expressed as powers of 2, is needed to satisfy the ENOB≥12 requirement (see Fig. 4).

D. INVERTER-BASED DESIGN

The schematic diagram of the proposed modulator is shown in Fig. 5. This design is implemented using the 0.18-μm CMOS/N-well process by UMC. The functional parts of the circuit are: (i) the first integrator stage, embedding correlated double sampling (CDS) technique [33], formed by C_S (split capacitor), C_A, C_F and the inverter I1; (ii) a second integrator stage based on the standard parasitic insensitive structure around I2 and the capacitors C_{S1}, C_{S2}, C_{F2}; (iii) the minimalist inverter-based latched comparator, CMP, acting as a single-bit quantizer; (iv) the 3-tap FIR DAC formed by the array of inverter-based buffers (B1–B4) and D-edge triggered flip-flops (D1–D3), and finally, (v) the constant V_{inv} generator, constituted by I0 and the MOSFET labelled with MC in Fig. 5 used as bypass capacitor. The D-edge triggered flip-flops and the non-overlapping clock phase generator (not shown in the figure) are implemented using traditional NAND-based and NOR-based architectures, respectively.

The first integrator stage is the most critical block in our design, since its physical noise, offset and distortion possibly limit the achievable effective resolution and accuracy. Since the modulator is intended to convert very-low frequency signals, the deployment of the CDS technique is mandatory in order to suppress offset, offset thermal drift and to reduce flicker noise components. This is achieved by the configuration shown in Fig. 5, which has been adapted from [33]. The integrator employs an auxiliary capacitor C_A, updated every clock cycle in order to track both the offsets of I1 and I0. Straightforward analysis, reported in Appendix, reveals that the integrator output V_{s1}, at the end of phase 1, is:

$$V_{s1} = \frac{a_1 z^{-1/2}}{1-z^{-1}} \cdot \left(z^{-1/2} V_{in} - \frac{V_{f0}+V_{f1}+V_{f2}+V_{f3}}{4} \right) + \left(a_A + \frac{a_1 z^{-1/2}}{1+z^{-1/2}} \right) V_{os1} + (1-a_A) V_{os0}, \tag{9}$$

where V_{os0} and V_{os1} are the input-referred offset terms of I0 and I1, respectively, while the coefficients $a_1 (= b_1)$ and a_A are expressed as:

$$a_1 = \frac{C_S}{C_F}, \qquad a_A = \left(1 + \frac{C_A}{C_F}\right). \tag{10}$$

When these offset terms are referred to the modulator input, V_{in}, they undergo the discrete-time derivative $1 - z^{-1}$, hence their DC contribution is rejected.

Regarding kT/C noise, the critical in-band contribution is given by the split capacitor C_S. The signal-to-thermal-noise ratio (STNR) can be estimated by the simplified formula:

$$\mathrm{STNR} = \frac{V_p^2/2}{kT(2 + C_S/C_A)/(C_S \cdot \mathrm{OSR})}, \tag{11}$$

where kT is the thermal energy (4.11×10^{-21} J at 298 K). In this approximation, the on resistance of the switches is considered to be negligible with respect to $R_{th} = 1/(g_{mn} + g_{mp})$, being g_{mn} and g_{mp} the transcoductance parameters of the NMOS and PMOS, respectively [34]. While C_S is sampled twice per clock period, C_A is sampled only once. Letting OSR to be 256, an STNR of 89.15 dB is obtained assuming $C_S = 0.6$ pF and $C_A = 2.4$ pF (for $V_p = V_{FS}/3$). Since a_1 has been set from behavioural simulations to be 0.125, $C_F = 4.8$ pF is obtained from Eq. (10).

The second integrator stage, much less critical from the noise point of view, is implemented as a two-input parasitic insensitive structure, hence:

$$c_1 = \frac{C_{S1}}{C_{F2}}; \quad a_2 = \frac{C_{S2}}{C_{F2}}. \tag{12}$$

For this stage $C_{F2} = 0.8$ pF has been chosen. Consequently, $C_{S1} = 395$ fF and $C_{S2} = 197$ fF.

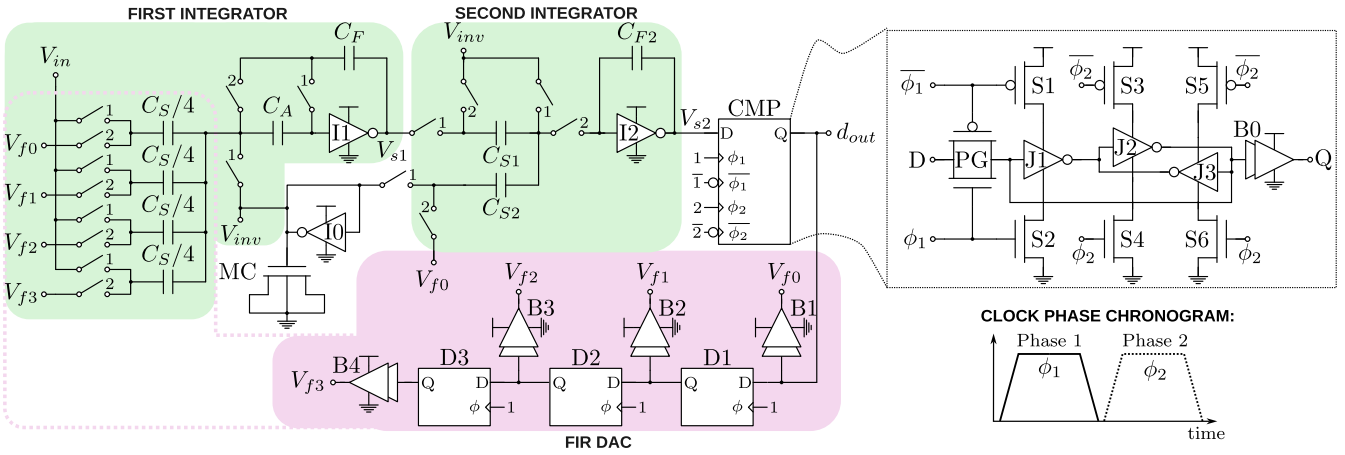

FIGURE 5. Inverter-based 3-tap FIR single-bit second-order Δ-ΣM: detailed schematic and clock phase chronogram.

The inverter-based latched comparator, also shown in Fig. 5, is built around three clocked inverters. The first clocked inverter formed by S1, S2 and J1 acts as preamplifier of the input D during ϕ_1. During the same phase, the J2-J3 latch is disabled (S3-S6 are off), hence the output Q is undefined. During ϕ_2 the latch is established and Q evolves to the logic level "0" or "1", depending on the output of J1. The pass-gates switches were implemented with the following dimensions for the NMOS and PMOS devices: $W_n = W_p = 1.2\ \mu$m, $L_n = L_p = 250$ nm, $m_n = 1$, and $m_p = 4$.

The use of inverters as OTAs within the integrator stages provides two important advantages: (i) wide input and output ranges, fundamental to enable low-voltage operation as in the present design, and (ii) higher g_m-power efficiency, due to bias current reuse between the PMOS and the NMOS, both contributing to the output current of the stage. On the other hand, performances of inverters are prone to PVT variations, and usually a worst-case scenario should be considered for robust design [35].

The worst PVT sensitivity is expected for weak-inversion operation of the devices, where the current-voltage relationships follow exponential laws involving both temperature and threshold voltage [36]. Strong inversion operation may offer reduced sensitivity to the aforementioned parameters, but it is still non optimal due to reduced transconductance efficiency and higher $V_{DS,sat}$-limits to the output range. To strike a balance between these two requirements, moderate inversion operation is set for the inverters in the current design. Inverters I0, I1, I2 are nominally identical, with $W_n = W_p = 0.5\ \mu$m, $L_n = L_p = 50\ \mu$m, $m_n = 1$, and $m_p = 4$. The larger multiplication factor, m, for p-type MOSFETs accounts for the intrinsic mobility difference between holes and electrons. The tiny aspect ratio of the devices allow obtaining nano-ampere level of current consumption. Simulation results of the electrical testbench are reported in Table 1 under the conditions of $V_{DD} = 900$ mV and $T = 27^{\circ}$C. For the three major corner cases, the inverter is set into class-AB operation (*i.e.* both the NMOS and the PMOS are biased in moderate inversion: $V_{DD} - 8kT/q < V_{Tn} + |V_{Tp}| < V_{DD}$)

TABLE 1. Simulated performace of the inverters I0-I2 against process corners. V_{Tn} and V_{Tp} are the p- and n-MOSFET threshold voltages, respectively; A_0 is the open-loop static gain of the inverter; $I_{DD,0}$ is the inverter static current at the inversion point ($V_{DD} = 900$ mV); GBP is the gain-bandwidth product with an effective capacitive load of 0.6 pF.

Corner	$V_{Tn} + \lvert V_{Tp}\rvert$ [mV]	A_0 [dB]	$I_{DD,0}$ [nA]	GBP [kHz]
Typical	785	64.3	8.8	77
Slow	872	65.0	3.5	37
Fast	701	62.6	18.6	135

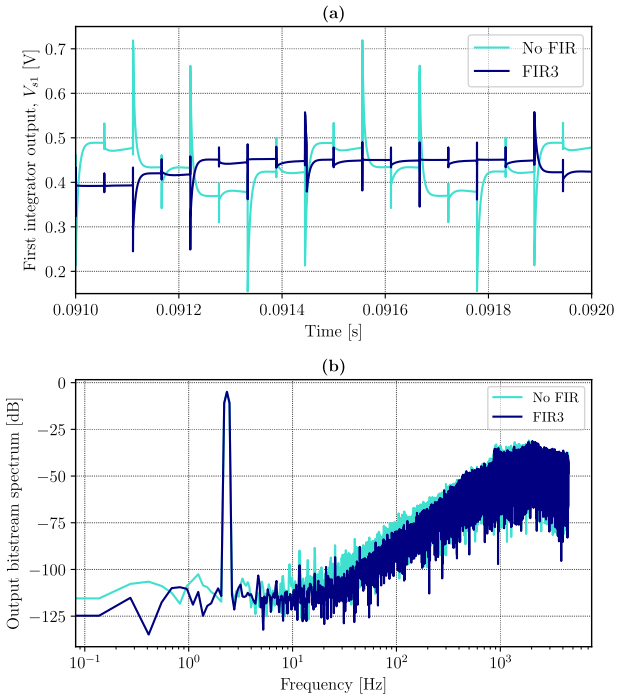

FIGURE 6. Comparison of $\Delta\Sigma$Ms of Fig. 1 (full-schematic electrical simulations, slow-process-corner case). A transient extract of $V_{s1}(t)$ is reported in (a), while output-bitstream (d_{out}) spectrum is reported in (b).

[16]. Hence, calibration techniques are not employed for this design, greatly reducing system complexity.

Significantly, in the slow corner, the inverters approach class-C (*i.e.* weak-inversion) operation ($V_{Tn} + |V_{Tp}| \geq$

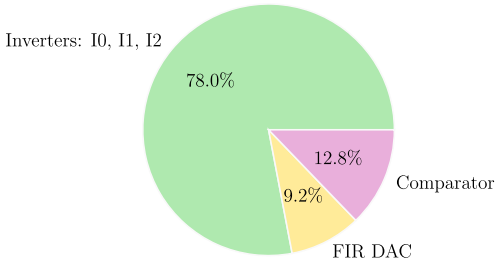

FIGURE 7. Power breakdown of the proposed ΔΣM.

V_{DD}). This is also the most limiting case in term of gain-bandwidth product (GBP). For this reason the FIR filter was introduced. By means of electrical simulations, we evaluated the modulator performance both with and without the FIR, ensuring consistent coefficient scaling for both scenarios. Figure 6(a) graphically illustrates the temporal response of the first integrator output both with and without the FIR filter. In both cases, voltage spikes are evident at the onset of the clock transitions. However, upon deploying the FIR filter, spikes result noticeably attenuated, translating to reduced GBP requirements to attain the same linearity [37]. Spectral behaviour, shown in Fig. 6(b), returns a SINAD enhancement of roughly 8 dB in the slow-process-corner case for the modulator embedding the FIR (OSR = 256).

It is worth noting that the transient spikes in Fig. 6(a), $\Delta V_{s1}[n, 0^+]$ (at the cycle n of the clock signal), are directly correlated to the ΔV_{s1} statistics analyzed in Section II-A:

$$\Delta V_{s1}[n, 0^+] = -\frac{C_F}{C_S}\Delta V_{s1}[n], \tag{13}$$

where $\Delta V_{s1}[n]$ indicates the settled value at the end of the same phase and corresponding to x-axis of Fig. 3(b). Hence, the statistic distribution of $\Delta V_{s1}[n, 0^+]$ correspond to that of $\Delta V_{s1}[n]$ magnified, in terms of horizontal spread, by a factor of 8. When considering the modulator without FIR, this translates into a non-negligible amount of samples affected by ground- and V_{DD}-clipping.

Figure 7 displays the power breakdown at V_{DD} = 0.9 V, derived from electrical simulations, revealing that the FIR accounts for a 9.2% increase (+0.38 dB) in power consumption. This slight increase in power consumption is well justified by the 8 dB reduction in SINAD observed when the slow-process case is considered.

III. EXPERIMENTAL RESULTS

The proposed ΔΣM was fabricated with the already mentioned 0.18-μm CMOS process by UMC. The ΔΣM was included in a test chip together with other experimental circuits. A microphotograph of the chip can be viewed in Fig. 8, with the layout superimposed to the optical photograph to show the area occupied by the various circuit components. The presented ΔΣM occupies a silicon area of 0.027 mm^2. In the following, we characterize the performances of the ΔΣM prototype by presenting results of extensive electrical measurements. In this respect, the following instrumentation

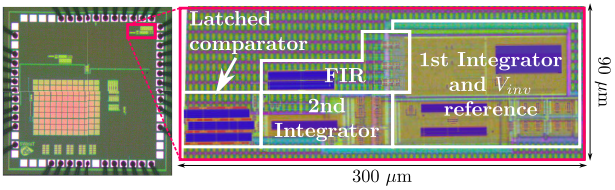

FIGURE 8. Chip microphotograph with zooming on the ΔΣM. The prototype size, implemented in standard 180-nm CMOS technology, is 300 μm × 90 μm.

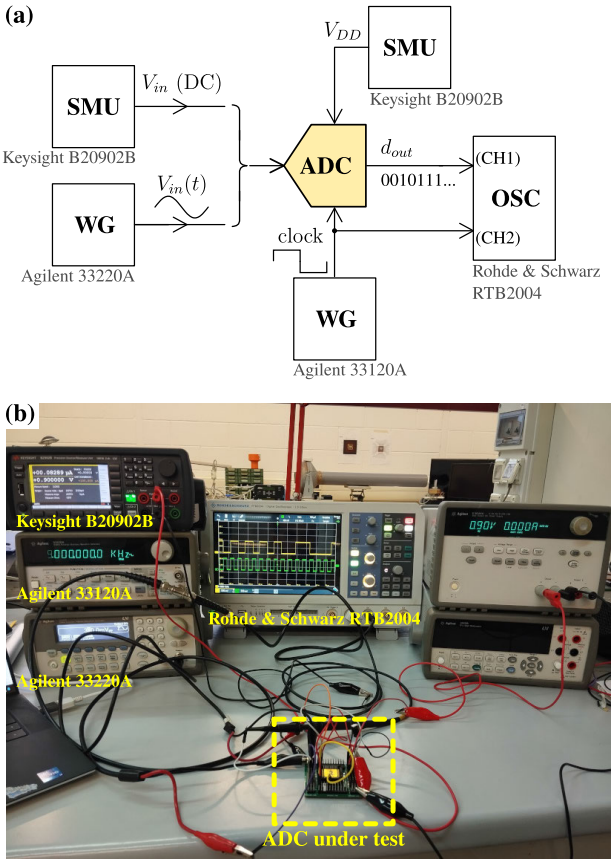

FIGURE 9. Experimental setup: (a) schematic diagram; (b) photograph.

was employed as depicted in Fig. 9: a Keysight B20902B two-channel Source-Measure Unit (SMU) for supplying and monitoring the prototype power, Agilent 33120A and 33220A waveform generators (WGs) for the clock signal and the input stimuli, respectively, a Rohde & Schwarz RTB2004 digital oscilloscope (OSC) for the output stream acquisition and, for temperature characterization, a Peltier-cell-based cryostat (not shown in Figure). The output signal of the ΔΣM (d_{out} in Fig. 5) and the clock signal were digitized by the oscilloscope. The resulting bitstream (d_{out}) was processed by means of a Python script running on a personal computer. For DC characterizations, the input V_{in} has been fed through the second channel of the SMU.

Figure 10 illustrates the spectrum of the modulator output stream, d_{out}. This measurement was carried out under specific testing conditions: V_{DD} = 900 mV, f_{ck} = 9 kHz, f_{in} = 2.335 Hz, and V_p = 0.3 V. The recorded metrics, calculated with OSR = 256, include a Signal-to-Noise Ratio (SNR) of

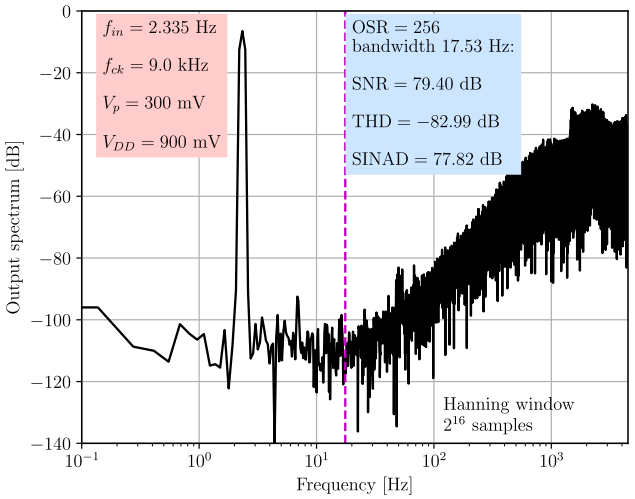

FIGURE 10. Measured output spectrum at peak SINAD.

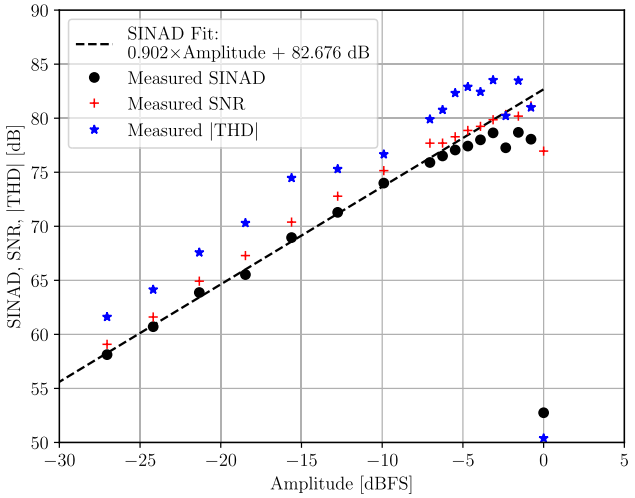

FIGURE 11. SINAD, SNR, THD *vs.* input-tone amplitude characteristics. Test conditions: V_{DD} = 900 mV (corresponding to full scale, FS), f_{ck} = 9 kHz, f_{in} = 2.335 Hz.

79.40 dB, a Total Harmonic Distortion (THD) of −82.99 dB, and a SINAD of 77.82 dB, corresponding to an ENOB of 12.6 (LSB = 145 μV). Over a 10-second window, the measured current consumption averages at 79.46 nA. This translates to the modulator power consumption being 71.51 nW (including the power contribution of the reference voltage, which corresponds to V_{DD}). Notably, measured performances match closely those of a fast-process-corner case, with a consequent penalization in power consumption with respect to the typical case. Nevertheless, we adopted the same bandwidth and supply specifications assumed initially.

Figure 11 illustrates the SINAD, SNR, and THD characteristics as the amplitude V_p of the input tone is swept from 20 mV (−27.04 dB of full scale) to 450 mV (full scale). A linear fit of SINAD data has been performed on the lower subset of the amplitude points (8 values). The linear fit returned a coefficient of 0.9023, and an intercept with the amplitude axis of −91.6 dB that virtually corresponds to the modulator Dynamic Range (DR).

TABLE 2. Statistical variation of measured performances over 9 samples: μ and σ indicated the mean and the standard deviation, respectively. Test conditions for SNR, THD and SINAD: V_{DD} = 900 mV, f_{ck} = 9 kHz, f_{in} = 2.335 Hz. Test conditions for OS and ϵ_G: V_{DD} = 900 mV, f_{ck} = 9 kHz.

max SNR [dB]		min THD [dB]		max SINAD [dB]		Power [nW]	
μ	σ	μ	σ	μ	σ	μ	σ
76.01	1.09	−81.12	2.93	74.70	1.33	71.10	2.73

OS [mV]		ϵ_G [%]	
μ	σ	μ	σ
−0.830	1.406	0.295	0.035

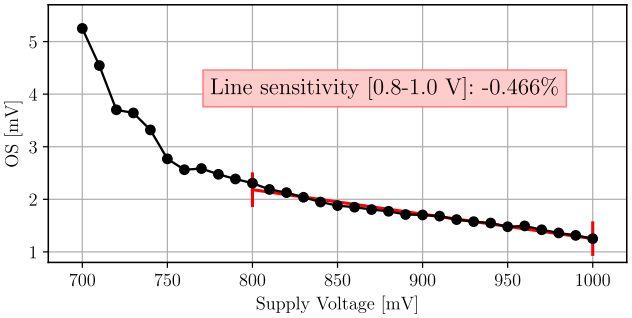

FIGURE 12. OS *vs.* supply voltage (V_{DD}) for chip sample #1.

Statistical variations from this analysis can be found in Table 2. For these results, nine chips were evaluated, all stemming from the same production batch and tested under the same conditions of our first experiment. Further characterization has been performed considering the offset, OS and the DC gain error, ϵ_G. OS has been estimated by adjusting the DC input provided by the SMU in order to have an average output stream (d_{out}) of 1/2. Each measured DC point has been acquired by averaging d_{out} for 10 seconds. On the other hand, ϵ_G is defined as:

$$\epsilon_G = G - 1, \tag{14}$$

where G is the measured gain extracted by simple linear regression fitted using the least squares approach, from 30 equally spaced points from zero to full scale in the DC transfer characteristics. The small values of the offset, compared to the typical variability of the inverter inversion voltage (V_{inv}), confirm the effectiveness of CDS application to the first integrator. We investigated also the offset sensitivity to V_{DD} variations: Fig. 12 shows a line sensitivity of less than 0.5% V/V tested on one of the chip samples.

Temperature effects have been characterised by means of an in-house Peltier-cell-based cryostat. A custom-made PCB with an access hole for thermal coupling was utilized, achieving thermal connection through a metal thermal bridge in contact with both the Peltier cell and the base of the chip packaging (JLCC type). Two PT100 probes were incorporated into the setup, coupled with thermal paste, to measure the temperature at both the base of the chip and on the top lid of the chip. The temperature displayed in the figure is the average of the two measured temperatures. To ensure a reliable reading of the measured value, a waited

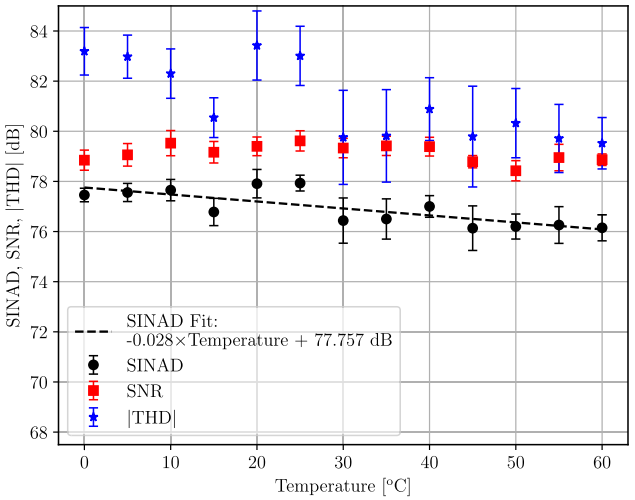

FIGURE 13. SINAD, SNR and THD *vs.* temperature (V_{DD} = 900 mV, f_{ck} = 9 kHz, f_{in} = 2.335 Hz, V_p = 0.3 V and OSR = 256).

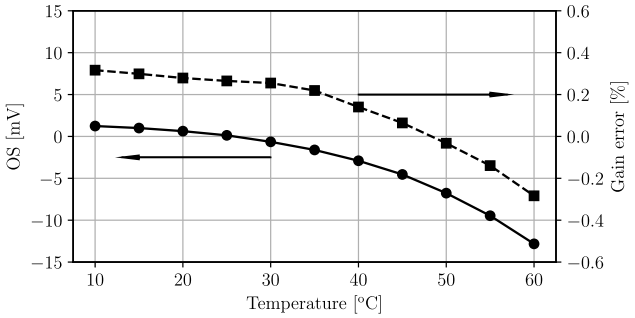

FIGURE 14. OS and gain error *vs.* temperature.

period of 20 minutes was observed after setting the set point on the cryostat. With this setup two experiments have been performed. In the first instance, the SINAD, the SNR and THD have been evaluated in the 0°C-60°C range taking temperature steps of 5°C and averaging the results measured at each temperature point between 10 samples. Results are shown in Fig. 13. The overall variation in the 0°C-60°C range of the SINAD is less than 1.8 dB. SINAD sensitivity to temperature is extracted from the linear fit, also shown in Fig. 13, and results in −0.0278 dB/°C.

A last experiment was devoted to characterize the OS and ϵ_G temperature drift. For OS-drift characterization, the modulator was fed with a 450 mV DC input, and the output stream was averaged for 10 seconds for each temperature point (after the waited period of 20 minutes for temperature stabilization). The gain error ϵ_G has been evaluated from 20 equally spaced points from zero to full scale in the DC transfer characteristics. Measurement results, reported in Fig. 14, show that in the 10°C-40°C range, the OS sensitivity to temperature is −0.11 mV/°C, and the ϵ_G variation is less than 0.6% with respect to the ideal gain in the whole explored range.

To gain a deeper understanding of the prototype's capabilities, we conducted tests under the following conditions: $V_{DD} = 700$ mV, $f_{ck} = 2$ kHz, $f_{in} = 0.520$ Hz, and $V_p = 0.3$ V. In this case, the supply provided to the circuit approximates the $V_{Tn} + |V_{Tp}|$ value for the fast corner (refer to Table 1). Under these conditions, the modulator consumes 10.4 nW. For fair comparison, we maintained the OSR and the f_{in}/f_{ck}-ratio as in the previous experiment. In this instance we obtained: SNR = 79.20 dB, THD = −74.99 dB, SINAD = 73.61 dB. The increased distortion is clearly the result of higher V_p/V_{DD} ratio for this particular case.

IV. DISCUSSION

Table 3 provides a performance summary of the proposed ΔΣM and juxtaposes it with state-of-the-art ADC designs that operate below 1 μW and are tailored for low-frequency acquisition systems (*i.e.*, bandwidth < 1.5 kHz). In assessing these designs, we employ the following figures of merit:

$$\text{FOMW} = \frac{\text{P}}{2^{\text{ENOB}} \times f_{\text{Nyq}}}; \tag{15}$$

$$\text{FOMS} = \text{DR} + 10\log_{10}\frac{f_{\text{Nyq}}/2}{\text{P}}. \tag{16}$$

Here, P, specified in nanowatts, represents power dissipation *at the input-signal amplitude corresponding to the peak* SINAD, f_{Nyq} is the Nyquist frequency ($f_{\text{Nyq}} = f_{ck}/\text{OSR}$). FOMW is the renowned Walden's figure of merit, typically employed for low-resolution designs, specifically when ENOB < 10, which are not limited by thermal noise. On the other hand, FOMS is the widely recognized Schreier's figure of merit, deemed more effective for ranking designs with higher resolution. The proposed ΔΣM scores well above the median when considering singularly the following three major parameters of interest: 12.6 ENOB (median: 9.6), 71.5 nW of power consumption (median: 180 nW) and 175.5 dB of FOMS (median: 151.6 dB).

In terms of absolute power consumption, the designs in [10], [13], [19], [20], and [21] surpass the performance of the proposed ΔΣM. However, it is noteworthy that none of these references achieve a 10-ENOB resolution. While [14], [16], [17], [22] do surpass the 10-ENOB benchmark, their FOMS metrics fall short when compared to the proposed ΔΣM, with [22] being the lone exception. The standout performance exhibited by [22] stems from the incorporation of advanced system-level techniques, including predictive digital autoranging and a hybrid analog/digital second-order oversampling ADC architecture that can achieve DC decoupling at exceptionally low cut-off frequencies. However, there exists a trade-off: it demands an instantaneous power consumption of 800 nW, which is over ten times greater than that of the proposed ΔΣM. This discrepancy is particularly significant for the design of an eventual power-management unit (PMU) to be integrated along with the modulator, as it translates also to stricter settling requirement for the PMU during power duty-cycled operations.

It is noteworthy to mention that despite employing the basic inverter-based topology, we observed no significant performance deviation across the 9 samples tested. Referencing the values in Table 2, SINAD shows a remarkably tight standard deviation of just 1.33 dB. In terms of absolute value,

TABLE 3. Performance summary and comparison with prior state-of-the-art low-frequency ($f_{Nyq} \leq 3$ kHz) ultralow-power (P < 1 μW) ADC designs.

Reference	[16]	[17]	[20]	[13]	[22]	[18]	[14]	[21]	[15]	[19]	[10]	This Work	
Year	2009	2014	2014	2017	2018	2018	2019	2019	2021	2020	2022	2024	
Process technology [nm]	350	65	130	180	65	65	55	180	180	180	180	180	
Silicon Area [mm^2]	0.350	0.125	0.141	-	0.024	0.020	-	0.141	0.050	0.026	0.088	0.027	
Supply voltage [V]	1.50	0.70	0.25	0.60	0.80	0.30	1.20	0.30	1.20	0.25	0.15	0.70	0.90
Signal bandwidth [Hz]	120	500	30	500	500	1500	150	62	500	42.9	0.3	3.9	17.6
Peak SINAD [dB]	65.0	65.0	58.0	48.3	66.2	60.0	78.8	53.3	57.7	37.2	59.3	73.6	77.8
Peak SNR [dB]	72.0	68.0	62.0	-	-	64.0	82.8	54.7	-	40.8	60.6	79.2	79.4
DR [dB]	75.0	53.0	58.0	48.3	92.0	65.0	78.8	53.3	57.7	37.2	59.3	-	91.6*
Power [nW]	730.0	430.0	28.0	2.7	800.0	180.0	900.0	37.0	204.0	2.1	0.6	10.4	71.5
ENOB	10.5	10.5	9.3	7.7	10.7	9.7	12.8	8.6	9.3	5.9	9.6	11.9	12.6
FOMW [fJ/conv-step]	2093.1	295.9	719.0	12.8	480.9	73.4	420.7	789.8	323.6	413.6	1326.5	339.9	319.8
FOMS [dB]	157.2	143.7	148.3	160.9	180.0	164.2	161.0	145.5	151.6	140.3	146.3	159.3**	175.5

* Extrapolated from linear fit of the measured set; ** Estimated using SINAD instead of DR.

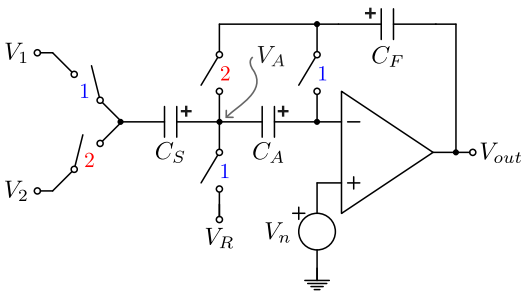

FIGURE 15. Schematich view of the generalised 3-capacitors Nagaraj integrator.

FOMS is in line with other state-of-the-art solutions targeting low-voltage and ultralow-power consumption required by wearable applications.

APPENDIX
ANALYSIS OF THE GENERALISED 3-CAPACITORS NAGARAJ INTEGRATOR

Let us consider the switched-capacitors integrator circuit of [33], generalised in order to accound also for a non-zero reference V_R, shown in Fig. 15. In the following analysis we denote V_{CS}, V_{CA} and V_{CF} as the voltage drops across the respective capacitors C_S, C_A and C_F, with the polarities indicated in Fig. 15.

We start to define the voltages across the capacitors at the end of phase 1 and of phase 2, indicated with the superscript "(1)" and "(2)", respectively.

$$V_{CS}^{(1)} = V_R^{(1)} - V_1^{(1)}; \tag{17}$$
$$V_{CA}^{(1)} = V_n^{(1)} - V_R^{(1)}; \tag{18}$$
$$V_{CF}^{(1)} = V_n^{(1)} - V_{out}^{(1)}. \tag{19}$$
$$V_{CS}^{(2)} = V_A^{(2)} - V_2^{(2)}; \tag{20}$$
$$V_{CA}^{(2)} = V_n^{(2)} - V_A^{(2)}; \tag{21}$$
$$V_{CF}^{(2)} = V_A^{(2)} - V_{out}^{(2)}. \tag{22}$$

The charge moved across C_A and C_S from phase 1 to phase 2 are, respectively:

$$\begin{aligned}\Delta Q_A^{(1\to2)} = 0 \implies V_{CA}^{(1)} = V_{CA}^{(2)} \implies \\ = V_A^{(2)} = V_R^{(1)} + V_n^{(2)} - V_n^{(1)};\end{aligned} \tag{23}$$

$$\begin{aligned}\Delta Q_S^{(1\to2)} &= C_S\left(V_{CS}^{(2)} - V_{CS}^{(1)}\right) = \\ &= C_S\left(V_A^{(2)} - V_R^{(1)} - V_2^{(2)} + V_1^{(1)}\right) \\ &= C_S\left(V_n^{(2)} - V_n^{(1)} - V_2^{(2)} + V_1^{(1)}\right).\end{aligned} \tag{24}$$

We observe a CDS action with respect to both V_n in both $\Delta Q_A^{(1\to2)}$ and $\Delta Q_S^{(1\to2)}$:

$$\Delta V_n = V_n^{(2)} - V_n^{(1)}. \tag{25}$$

Since $\Delta Q_F^{(1\to2)} = -\Delta Q_S^{(1\to2)}$, we can calculate the variation of $\Delta V_{CF}^{(1\to2)} = V_{CF}^{(2)} - V_{CF}^{(1)}$, as:

$$\Delta V_{CF}^{(1\to2)} = \frac{\Delta Q_F^{(1\to2)}}{C_F} = -\frac{C_S}{C_F}\left(\Delta V_n - V_2^{(2)} + V_1^{(1)}\right). \tag{26}$$

$V_{out}^{(2)}$ can now be calculated using (22), (23), (26) and (19):

$$\begin{aligned}V_{out}^{(2)} &= V_A^{(2)} - V_{CF}^{(2)} = V_A^{(2)} - V_{CF}^{(1)} - \Delta V_{CF}^{(1\to2)} \\ &= V_R^{(1)} + \Delta V_n - V_n^{(1)} + V_{out}^{(1)} \\ &\quad + \frac{C_S}{C_F}\left(\Delta V_n - V_2^{(2)} + V_1^{(1)}\right)\end{aligned} \tag{27}$$

At this point we need to express $V_{out}^{(1)}$ as function of the previous half-phase (2p):

$$V_{CA}^{(2p)} = V_n^{(2p)} - V_A^{(2p)}; \tag{28}$$
$$V_{CF}^{(2p)} = V_A^{(2p)} - V_{out}^{(2p)}, \tag{29}$$

At the same time, we can express (23), for the phase 2p:

$$V_A^{(2p)} = V_R^{(1p)} + V_n^{(2p)} - V_n^{(1p)} = V_R^{(1p)} - \Delta V_n^{(p)}, \tag{30}$$

were $\Delta V_n^{(p)} = V_n^{(2p)} - V_n^{(1p)}$, expresses the CDS action on the previous clock cycle.

The charge moved across C_A from phase 2p to phase 1 is:

$$\begin{aligned}\Delta Q_A^{(2p\to1)} &= C_A\left(V_{CA}^{(1)} - V_{CA}^{(2p)}\right) \\ &= C_A\left(\Delta V_n^{(1)} - \Delta V_R^{(1)}\right),\end{aligned} \tag{31}$$

where we elaborated (28) and (30) and we defined:

$$\Delta V_n^{(1)} = V_n^{(1)} - V_n^{(1p)} \tag{32}$$

$$\Delta V_R^{(1)} = V_R^{(1)} - V_R^{(1p)}. \tag{33}$$

Since $\Delta Q_F^{(2p\to1)} = -\Delta Q_A^{(2p\to1)}$, we can calculate the variation of $\Delta V_{CF}^{(2p\to1)} = V_{CF}^{(1)} - V_{CF}^{(2p)}$, as:

$$\Delta V_{CF}^{(2p\to1)} = \frac{\Delta Q_F^{(2p\to1)}}{C_F} = -\frac{C_A}{C_F}\left(\Delta V_n^{(1)} - \Delta V_R^{(1)}\right). \tag{34}$$

$V_{out}^{(1)}$ can be calculated using (19), (34) and (30) as:

$$\begin{aligned} V_{out}^{(1)} &= V_n^{(1)} - V_{CF}^{(1)} = V_n^{(1)} - V_{CF}^{(2p)} - \Delta V_{CF}^{(2p\to1)} \\ &= V_n^{(1)} - V_A^{(2p)} + V_{out}^{(2p)} \\ &\quad + \frac{C_A}{C_F}\left(\Delta V_n^{(1)} - \Delta V_R^{(1)}\right) \\ &= V_n^{(1)} - V_R^{(1p)} + \Delta V_n^{(p)} + V_{out}^{(2p)} \\ &\quad + \frac{C_A}{C_F}\left(\Delta V_n^{(1)} - \Delta V_R^{(1)}\right). \end{aligned} \tag{35}$$

This last equation can be used to elaborate (27), previously found:

$$\begin{aligned} V_{out}^{(2)} = V_{out}^{(2p)} + \frac{C_S}{C_F}\left(V_1^{(1)} - V_2^{(2)}\right) + \left(1 - \frac{C_A}{C_F}\right)\Delta V_R^{(1)} + \\ + \left(1 + \frac{C_S}{C_F}\right)\Delta V_n - \Delta V_n^{(p)} + \frac{C_A}{C_F}\Delta V_n^{(1)}. \end{aligned} \tag{36}$$

Since in modulator of Fig. 5 we are sampling V_{out} at the end of phase 1, we can use (35) expressed at the end of phase 1 of the next clock cycle, *i.e.* phase 1n:

$$\begin{aligned} V_{out}^{(1n)} = V_n^{(1n)} - V_R^{(1)} + \Delta V_n + V_{out}^{(2)} + \\ + \frac{C_A}{C_F}\left(\Delta V_n^{(1n)} - \Delta V_R^{(1n)}\right), \end{aligned} \tag{37}$$

where

$$\Delta V_n^{(1n)} = V_n^{(1n)} - V_n^{(1)}, \tag{38}$$

$$\Delta V_R^{(1n)} = V_R^{(1n)} - V_R^{(1)}. \tag{39}$$

Finally, using (27) in (37):

$$\begin{aligned} V_{out}^{(1n)} = V_{out}^{(1)} + \frac{C_S}{C_F}\left(V_1^{(1)} - V_2^{(2)}\right) - \frac{C_A}{C_F}\Delta V_R^{(1n)} + \\ + \frac{C_S}{C_F}\Delta V_n + \left(1 + \frac{C_A}{C_F}\right)\Delta V_n^{(1n)}. \end{aligned} \tag{40}$$

Now considering the coefficients defined in (10), we can calculate the Z-transform of (40) to find (9).

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