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RESEARCH ARTICLE

Performance Evaluation of a 17-Level Octuple Boost Inverter for a Grid-Connected PV System

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ABSTRACT This paper presents a novel single-phase, 17-level octuple boost switched-capacitor multilevel inverter (OBSC-MLI) for a grid-connected photovoltaic (PV) system. The proposed inverter can boost the low voltage obtained from a small PV source up to eight times at the output to reach the grid voltage level. Thus, the proposed inverter is most suitable for a PV system, as it can eliminate the need for any boost converter or step-up transformer for its grid integration application, resulting in an overall compact system. The inverter consists of a lower number of power electronic components and capacitors. The cost of each switch and diode is lower as the devices' standing voltages (SV) are only half of the output voltage. Due to its voltage-boosting capabilities, this inverter is a strong contender for transformer-less grid-connected PV systems. A closed-loop dq current control and DC-link voltage control are adopted to manage the active power supplied to the grid and balance the DC-link voltage. A near-sinusoidal output voltage with higher voltage levels is obtained owing to increased efficiency and lower harmonics. Furthermore, the filter size becomes smaller even at a much lower switching frequency. Experimental results for both RL-load and grid-connected modes are presented and analyzed.

INDEX TERMS Boost inverter, grid-connected inverter, multilevel inverter, seventeen-level inverter.

I. INTRODUCTION

Multilevel inverters (MLIs) have become popular in modern industrial applications for DC to AC conversion due to their special features, which include a near sinusoidal voltage-output waveform, a wide range of power processing abilities, improved efficiency, smaller filter size requirements, less DC sources, and so on. MLIs are commonly utilized in renewable energy systems, industrial applications, and transportation drives. The efficient converters are predominantly used in electric traction, electric vehicles (EVs), and power systems. Renewable energy sources such as wind farms and grid-connected solar power plants heavily depend on these MLIs [1], [2], [3].

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The MLI may convert a varying DC provided by renewable sources in changing environmental conditions to a fixed or variable AC voltage source as per the load requirements. Moreover, for a low-power PV system, the output voltage obtained from solar PV panels is usually lesser in magnitude than the required voltage levels for grid integration. To meet the grid voltage level, a boost converter, the step-up transformer, or their combinations are required, which makes the system bulky and lowers its overall efficiency.

Traditional multilevel inverters, such as cascaded H-bridge (CHB), require numerous DC sources, such as PV panels. For high-power, high-level applications, each source is linked to an individual H-bridge, and thus, many bridges are coupled in a cascade. However, during fluctuating solar irradiation in the multi-source MLI, the output power (current) of each PV panel may diverge from the required value, resulting in

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power mismatch issues. As a result, the total output may decrease, and the inverter output voltage may have a more significant ripple. A single DC source from a PV array and a step-up converter is mandatory to enhance the source voltage for the neutral point clamp (NPC) and flying capacitor (FC) MLI. This arrangement enables effective power conversion and control in the MLI system, which improves overall performance. Furthermore, the boost converter helps to maximize power output and reduce system losses. However, the two-stage power conversion increases the intricacy, cost, and size while reducing its overall efficiency [4], [5], [6]. On the other hand, the switched-capacitor MLIs (SC-MLIs) can obtain an output voltage of higher magnitude and a higher number of output voltage levels using a single DC supply of lower magnitude using its inherent boosting capabilities [7], [8]. Switched-capacitor multilevel inverters (SC-MLIs) utilize several capacitors to generate numerous voltage levels by charging and discharging them in combination of series and parallel with the DC source. It allows for flexibility in tailoring the output voltage to specific needs and distributes the load evenly, which helps to improve efficiency. However, SC-MLIs require more components than other topologies, which increases the total standing voltage (TSV), kVA rating, and cost. Furthermore, conduction and switching losses surge with the increase in the number of components, lowering efficiency. While some SC-MLIs like [9] and [10] achieve high voltage output with minimal components, their complexity outweighs the benefits. Alternatively, topologies like [12] offer improved efficiency by using fewer components and sacrificing some voltage gain, while those using multiple isolated DC sources like [11] achieve higher voltage without compromising performance but require an additional DC-DC converter. The topology presented in [14] has a comparatively lesser number of switches. However, there are more total semiconductor device counts due to diodes, which result in higher TSV. Moreover, this topology is not feasible for low power factor loads. The output voltage shows the voltage spikes due to the absence of a reactive current path. The topology presented in [15] has a comparatively smaller number of capacitors, but the TSV is very high due to higher voltages across the capacitors. The trade-off between component count, voltage gain, efficiency, and complexity becomes crucial when choosing an SC-MLI for specific applications. The MLI in [16] requires four unequal DC sources and ten switches to produce 17 voltage levels. However, its efficiency is comparatively higher due to lower conduction and switching losses. The key concern with this multi-source MLI structure is the power disparity caused by varying solar irradiation. The inverter in [17] requires twenty-six switches, seven capacitors, and a DC supply, lowering inverter efficiency, increasing costs, and complicating system design. It employs a selective harmonic elimination PWM (SHE-PWM) strategy to lessen the impact of dominant harmonics. This circuit consists of a single DC source, eight transistors, one bidirectional switch, four discrete diodes, and six capacitors. The topologies presented in [18] and [19] result in a 17-level output voltage with double the voltage gain. The topology [20] yields a 17-level output with four asymmetrical DC sources. The combination of components enables higher voltage gain and more accurate control over output levels. This design allows for versatility in power conversion applications while remaining efficient. This MLI architecture has a power mismatch problem, making it less viable. Another 17-level inverter topology is presented in [21] with low voltage stress across all components, along with a quasi-soft charging method to minimize the inrush current. However, the topology uses 14 switches, four diodes, and four capacitors to get a voltage gain of four. The article [22] proposed another 17-level modified inverter consisting of ten unidirectional switches, four bidirectional switches, four power diodes, and four capacitors. Moreover, it required a DC-DC flyback converter to produce two isolated DC sources of equal values for supplying the modified SC-based inverter that can produce a 17-level output voltage. In this modified inverter, the component-to-level ratio is very high, which affects the size, cost, and efficiency of the inverter. The idea is driven by the desire to develop a high-gain MLI with only one source, reduced TSV, fewer components, and more efficiency.

The key features of the proposed OBSC-MLI are as follows:

- The proposed 17-level inverter has an octuple voltage gain with a single DC source.
- For an output voltage (v_o), the inverter's TSV is $5.625v_o$, and the peak voltage rating of each semiconductor device is less than $v_o/2$, which is comparatively lower than the other similar MLIs; hence, this MLI appears economically viable.
- The total component count for the proposed inverter is lower than the other 17-level topologies.
- This inverter can work for a highly inductive load without spikes in the output voltage.
- The proposed inverter is implemented for a grid-connected system using dq current control, and its performance is analyzed.

The paper's content is organized as follows: Section II covers the operation of the proposed circuit. Section III presents its modulation technique and the theoretical calculations of the passive components. Section IV deals with the control of the proposed grid-connected inverter. Section V presents a comparative study of the proposed inverter with existing 17-level MLIs. Sections VI and VII provide simulation and experimental results for the closed-loop grid-connected applications. Finally, the key conclusions are discussed in Section VIII.

II. PROPOSED 17-LEVEL OBSC-MLI

A. CIRCUIT ANALYSIS

The suggested 17-level OBSC inverter is shown in Fig. 1. The circuit has 15 power switches denoted by T_i ($i = 1$ to 15), where thirteen switches have anti-parallel diodes and two

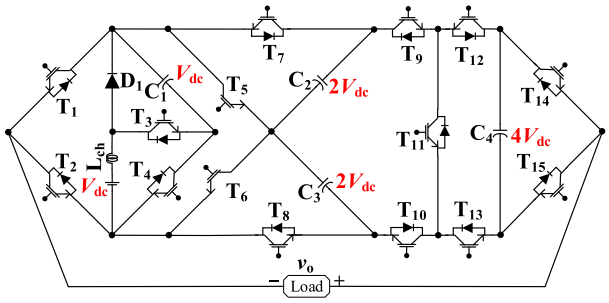

FIGURE 1. Power circuit of the 17-level OBSC-MLI.

switches with reverse blocking capabilities. The inverter also has four capacitors (C_1, C_2, C_3, and C_4), one diode (D_1), one DC source (V_{dc}), and one small charging inductor (L_{ch}). The symbol v_o indicates the output voltage across the load. The voltages of capacitors C_1, C_2, C_3, and C_4 are to be maintained at V_{dc}, $2V_{dc}$, $2V_{dc}$, and $4V_{dc}$, respectively.

B. OPERATION OF THE INVERTER AND CAPACITOR CHARGING/ DISCHARGING ANALYSIS

The proposed inverter is operated, and various voltage levels are obtained with the help of controlled switching. The current paths for the switching states for the positive cycle of the proposed inverter are shown in Fig. 2. The figure indicates the output current (i_o) with red lines, the charging current (i_{ch}) with green lines, and blue line indicates the second capacitor charging loop, respectively.

Table 1 demonstrates the complete switching states required to achieve 17 distinct output voltage levels. Additionally, it illustrates capacitor states using a green up arrow (↑) indicates charging, a red down arrow (↓) indicates discharging, and "↑↓" represents no change in the state of the capacitor.

1) STATE $\pm 8V_{dc}$

When switches T_2, T_3, T_5, T_9, T_{11}, T_{13}, and T_{14} are turned on, and the capacitors C_1, C_2, and C_4 are connected in a cascade with the supply voltage V_{dc}, the voltage across the load is $v_o = +8V_{dc}$. On the other hand, when switches T_1, T_3, T_6, T_{10}, T_{11}, T_{12}, and T_{15} are switched on, and the capacitors C_1, C_3, and C_4 are connected with V_{dc} in series, the output voltage appears across the load terminals is $v_o = -8\ V_{dc}$.

2) STATE $\pm 7V_{dc}$

The voltage across the load appears as $+7\ V_{dc}$ when the input source, V_{dc}, is connected in series with C_2 and C_4. Diode D_1 is in forward bias with the switches T_2, T_4, T_5, T_9, T_{11}, T_{13}, and T_{14} are turned on. Turning on the switch, T_4 charges the capacitor C_1, and when diode D_1 and switches T_1, T_4, T_6, T_{10}, T_{11}, T_{12}, and T_{15} are conducted, the voltage across the load is $-7\ V_{dc}$. To obtain $-7\ V_{dc}$, the source voltage V_{dc} is added to the voltage across the capacitors C_3 and C_4. In this instance, turning on T_4 causes the capacitor C_1 to become charged.

3) STATE $\pm 6V_{dc}$

T_2, T_3, T_7, T_9, T_{11}, T_{13}, and T_{14} are all conducting at the same time when C_1, C_4, and V_{dc} are linked in series to create $+6V_{dc}$. By turning on the T_6 switch, the newly formed loop charges the capacitor C_2 with the help of C_1 and V_{dc}, which are connected in series. To create an output voltage of $-6V_{dc}$ across the load, the switches T_1, T_3, T_8, T_{10}, T_{11}, T_{12}, and T_{15} are to be activated. Additionally, switch T_5 is switched on to charge the capacitor C_3 to $2V_{dc}$. C_1 and C_4 are connected in series with V_{dc}.

4) STATE $\pm 5V_{dc}$

Six switches, T_2, T_7, T_9, T_{11}, T_{13}, and T_{14}, are turned on at the same time. This creates a path for current to flow from the DC source (V_{dc}) and capacitor C_4 connected in series through the forward-biased diode D_1. This connection charges capacitor C_1 by placing it in parallel with V_{dc} through switch T_4.

In a similar way, turning on switches T_1, T_8, T_{10}, T_{11}, T_{12}, and T_{15} creates a negative voltage of $-5V_{dc}$ across the load. This happens because D_1 becomes forward-biased again, connecting capacitor C_4, V_{dc}, and the load in series. During this process, T_4 is also turned on to charge capacitor C_1.

5) STATE $\pm 4V_{dc}$

To generate $+4V_{dc}$, the capacitors C_1, C_2, and V_{dc} are connected in series while T_2, T_3, T_5, T_9, T_{12}, and T_{14} are conducting simultaneously. By connecting C_1 in series with V_{dc} and adding C_1 and C_2 by turning on the switches T_8, T_{10}, and T_{13}, another loop is also operating to charge the capacitors C_3 and C_4. The capacitors C_1 and C_3 are connected in series with V_{dc} to create $-4V_{dc}$ across the load, and the switches T_1, T_3, T_6, T_{10}, T_{13}, and T_{15} are conducting. Additionally, another loop is functioning to charge the capacitors C_2 and C_4 by turning on the switches T_7, T_9, and T_{12}.

6) STATE $\pm 3V_{dc}$

T_2, T_4, T_5, T_9, T_{12}, and T_{14} conduct simultaneously while the voltages between C_2 and V_{dc} are increased and reflected at the load to create $3V_{dc}$. D_1 provides the forward bias channel for this process. When switches T_1, T_4, T_6, T_{10}, T_{13}, and T_{15} are activated and connected to D_1 in forward bias, voltages across C_3 and V_{dc} are added and reflected at the load terminal, resulting in $-3V_{dc}$ voltage across the load. The activation of T_4 at this voltage level charges C_1.

7) STATE $\pm 2V_{dc}$

T_2, T_3, T_7, T_9, T_{12}, and T_{14} are all conducting simultaneously as the voltage between C_1 and V_{dc} is added to create $+2V_{dc}$, and the second loop charges C_2 by turning on T_6. In the negative voltage level, switching on T_5 connects C_1 in series with V_{dc} to charge the capacitor C_3. The switches T_1, T_3, T_8, T_{10}, T_{13}, and T_{15} are turned on. This results in $-2V_{dc}$ across the load terminal.

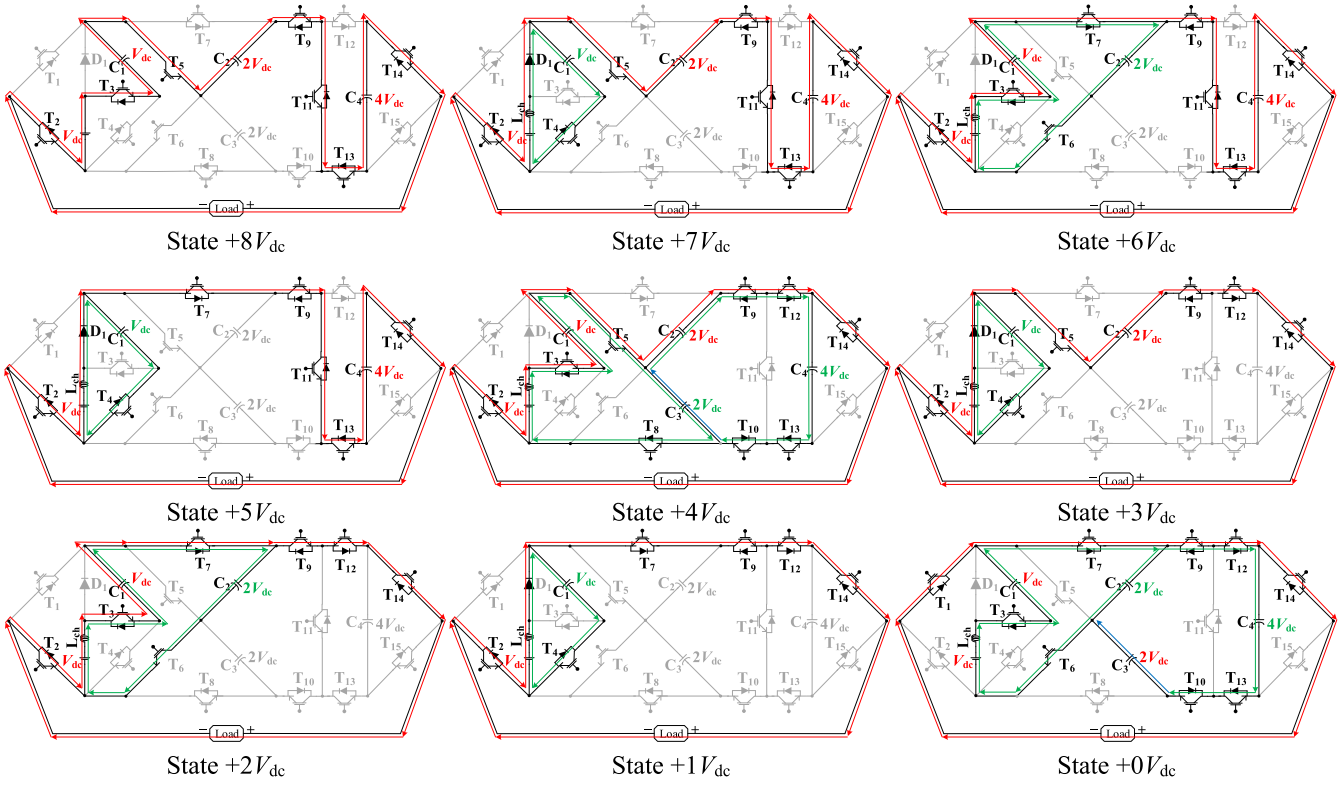

FIGURE 2. Current paths of the operating modes for the positive cycle of the proposed inverter.

TABLE 1. Switching states.

Level	ON state switch	Capacitor state			
		C_1	C_2	C_3	C_4
$+8V_{dc}$	$T_2, T_3, T_5, T_9, T_{11}, T_{13}, T_{14}$	↓	↓	↑↓	↓
$+7V_{dc}$	$T_2, T_4, T_5, T_9, T_{11}, T_{13}, T_{14}$	↑	↓	↑↓	↓
$+6V_{dc}$	$T_2, T_3, T_6, T_7, T_9, T_{11}, T_{13}, T_{14}$	↓	↑	↑↓	↓
$+5V_{dc}$	$T_2, T_4, T_7, T_9, T_{11}, T_{13}, T_{14}$	↑	↑↓	↑↓	↓
$+4V_{dc}$	$T_2, T_3, T_5, T_8, T_9, T_{10}, T_{12}, T_{13}, T_{14}$	↓	↓	↑	↑
$+3V_{dc}$	$T_2, T_4, T_5, T_9, T_{12}, T_{14}$	↑	↓	↑↓	↑↓
$+2V_{dc}$	$T_2, T_3, T_6, T_7, T_9, T_{12}, T_{14}$	↓	↑	↑↓	↑↓
$+1V_{dc}$	$T_2, T_4, T_7, T_9, T_{12}, T_{14}$	↑	↑↓	↑↓	↑↓
$+0V_{dc}$	$T_1, T_3, T_6, T_7, T_9, T_{10}, T_{12}, T_{13}, T_{14}$	↓	↑	↓	↑
$-0V_{dc}$	$T_2, T_3, T_5, T_8, T_9, T_{10}, T_{12}, T_{13}, T_{15}$	↓	↓	↑	↑
$-1V_{dc}$	$T_1, T_4, T_8, T_{10}, T_{13}, T_{15}$	↑	↑↓	↑↓	↑↓
$-2V_{dc}$	$T_1, T_3, T_5, T_8, T_{10}, T_{13}, T_{15}$	↓	↑↓	↑	↑↓
$-3V_{dc}$	$T_1, T_4, T_6, T_{10}, T_{13}, T_{15}$	↑	↑↓	↓	↑↓
$-4V_{dc}$	$T_1, T_3, T_6, T_7, T_9, T_{10}, T_{12}, T_{13}, T_{15}$	↓	↑	↓	↑
$-5V_{dc}$	$T_1, T_4, T_8, T_{10}, T_{11}, T_{12}, T_{15}$	↑	↑↓	↑↓	↓
$-6V_{dc}$	$T_1, T_3, T_5, T_8, T_{10}, T_{11}, T_{12}, T_{15}$	↓	↑↓	↑	↓
$-7V_{dc}$	$T_1, T_4, T_6, T_{10}, T_{11}, T_{12}, T_{15}$	↑	↑↓	↓	↓
$-8V_{dc}$	$T_1, T_3, T_6, T_{10}, T_{11}, T_{12}, T_{15}$	↓	↑↓	↓	↓

Charging of capacitors = ↑, Discharging of capacitors = ↓, and No state change = ↑↓

8) STATE $\pm 1V_{dc}$

T_2, T_7, T_9, T_{12}, and T_{14} are all conducting simultaneously, and they create a direct path for the DC source (V_{dc}) to generate V_{dc} at the load terminal. This path is completed by diode D_1. While switches control V_{dc} output, switch T_4 operates separately to charge the capacitor C_1. When T_4 is activated, C_1 becomes parallel with V_{dc}, allowing the capacitor to charge from the DC source. Similarly, when switches T_1, T_8, T_{10}, T_{13}, and T_{15} are switched on, a voltage level of $-1V_{dc}$ develops across the load.

9) STATE $\pm 0V_{dc}$

When switches T_1, T_7, T_9, T_{12}, and T_{14} conduct, there is no voltage at the load terminal. Meanwhile, two separate loops function to charge capacitors C_2 and C_4. The first loop is activated by T_6, while the second loop adds C_2 and C_3 in series through switches T_{10} and T_{13}. After turning on the switches T_2, T_8, T_{10}, T_{13}, and T_{15}, another path may be taken into consideration to achieve zero voltage at the load terminal. Additionally, another loop is in operation to charge the capacitors C_3 and C_4 by turning on the switches T_3, T_5, T_9, and T_{12}.

III. THEORETICAL DETERMINATION OF INVERTER PARAMETERS

A. PULSE-WIDTH MODULATION (PWM) TECHNIQUE

There are numerous modulation schemes for multilevel inverters to control their output voltage. The carrier-based PWM and space vector PWM (SVPWM) are used for higher switching frequency. The selective harmonic elimination (SHE) and nearest level control (NLC) are for reduced harmonic distortion and easier control. Carrier-based

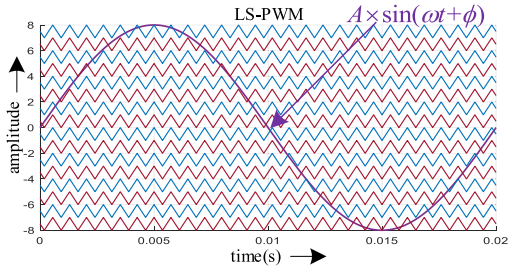

FIGURE 3. LS-PWM technique for the proposed 17-level inverter.

PWM is further classified into phase-shifted (PS-PWM) and level-shifted (LS-PWM). In this particular inverter design, Level-Shifted PWM (LS-PWM) is the chosen method for controlling the output.

The switching pulses for switches T_1 to T_{15} are obtained by comparing a reference sinusoidal signal ($A\times\sin(\omega t+\phi)$) with sixteen in-phase, high-frequency, triangular signals are shifted in level by equal increments of the amplitude of 1.0 each for the 17-level inverter. This level-shifted phase disposition PWM (PD-PWM) for a 17-level inverter, as shown in Fig. 3. It is a recognized technique for minimizing the line-to-line voltage harmonics [23]. The output of the PD-PWM is processed through logical operations that determine the specific switching sequence for each switch [24]. These tailored sequences activate different combinations of switches, resulting in 17 distinct voltage levels at the inverter's output, as shown in Fig. 4.

Fig. 5 illustrates the waveforms of inverter output voltage v_o, the reference grid voltage (v_α), and eight distinct voltage levels (P1-P8) for a positive half cycle. To better understand duty cycle concepts, the inverter output voltage waveform in Fig. 5 is intentionally depicted with a lower switching frequency. The duty cycle for each voltage level is determined using a fundamental principle known as the inductor volt-second balance (IVSB) law. This law is applied

across the filter inductor and considers the switching time period (T_S) [22].

The calculations of duty cycles for each level, P1 to P8, are shown in (1)-(15).

1) LEVEL P1

Consider Fig. 5 the inverter's output voltage ranges between $1V_{dc}$ and 0 at level 'P1'. The duty cycle of level P1 is d_{P1}. Therefore, by applying the IVSB principle for the voltage across the filter inductor during level P1 for the switching time period (T_s), the switching duty ratio of the inverter (d_{P1}) can be obtained as (1)-(5)

$$\int_0^{d_{P1}T_S}(1V_{dc}-v_\alpha)dt+\int_{d_{P1}T_S}^{T_S}(0-v_\alpha)dt=0;\ \text{for } t_1\le t<t_2 \tag{1}$$

Solving (1) the duty ratio for the level P1 is expressed in (2)

$$d_{P1}(t)=\frac{v_\alpha}{V_{dc}} \tag{2}$$

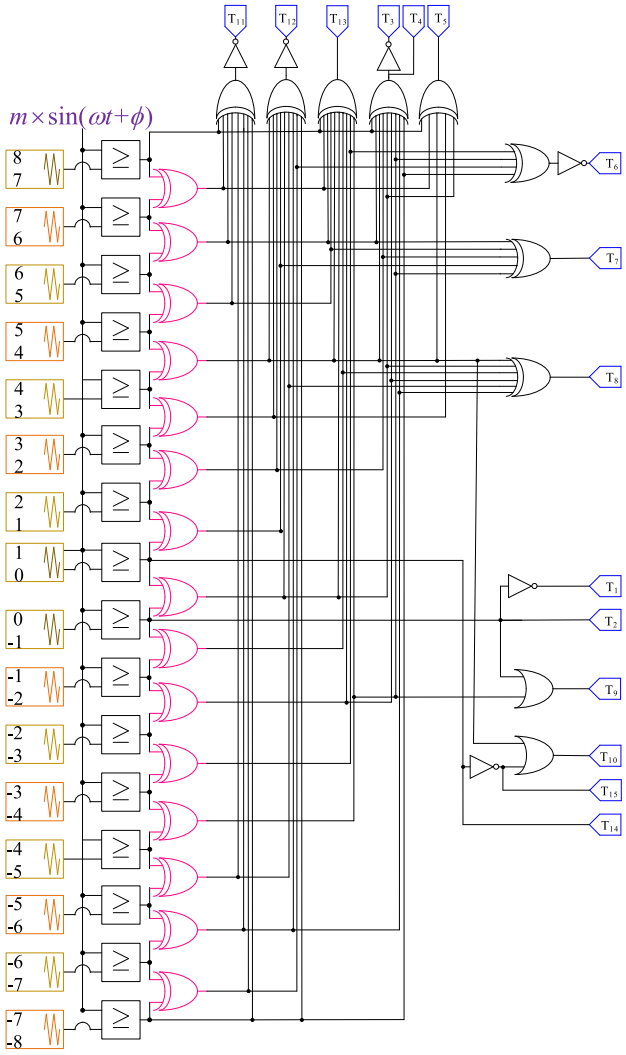

FIGURE 4. Logical implementation of the PWM for 17-level OBSC-MLI.

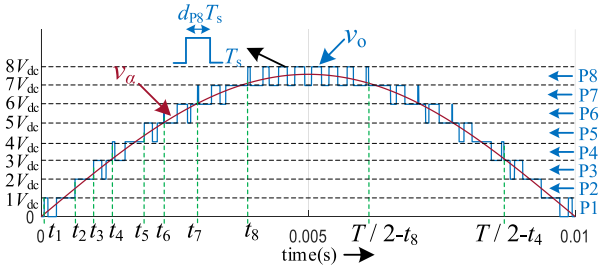

FIGURE 5. Duty ratio for charging and discharging of capacitors.

The reference signal (v_α) is the grid voltage with the peak value of v_{gm}, as shown in (3).

$$v_\alpha=v_g=v_{gm}\sin(\omega t) \tag{3}$$

By substituting (3) in (2), the duty cycle of level P1 is expressed as (4)

$$d_{P1}(t)=\frac{v_{gm}}{V_{dc}}\sin(\omega t);\quad \text{for } t_1\le t<t_2 \tag{4}$$

Solving (4) the value of t_1 is obtained as

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{0 \times V_{dc}}{v_{gm}}\right) = 0 \tag{5}$$

2) LEVEL P2

Based on Fig. 5, the inverter's output voltage is between $2V_{dc}$ and $1V_{dc}$ at level 'P2'. The duty cycle of level P2 is d_{P2}. Therefore, by applying the IVSB principle for the voltage across the filter inductor during level P2 for the switching period, the switching duty cycle of the inverter (d_{P2}) can be calculated as (6)-(9)

$$\int_0^{d_{P2}T_S}(2V_{dc} - v_\alpha)dt + \int_{d_{P2}T_S}^{T_S}(V_{dc} - v_\alpha)dt = 0;\ \text{for } t_2 \le t < t_3 \tag{6}$$

Solving (6) the duty ratio for the level P2 is expressed in (7)

$$d_{P2}(t) = \frac{v_\alpha}{V_{dc}} - 1 \tag{7}$$

By substituting (3) in (7), the duty cycle of level P2 is expressed as (8)

$$d_{P2}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 1; \quad \text{for } t_2 \le t < t_3 \tag{8}$$

Solving (8), the expression of t_2 is obtained as (9)

$$t_2 = \frac{1}{\omega}\sin^{-1}\left(\frac{1 \times V_{dc}}{v_{gm}}\right) \tag{9}$$

Similarly, the duty ratios of other levels (**Level P3-P8**) and expression of 't' are expressed in (10) - (15)

$$d_{P3}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 2;\ t_3 = \frac{1}{\omega}\sin^{-1}\left(\frac{2 \times V_{dc}}{v_{gm}}\right) \tag{10}$$

for $t_3 \le t < t_4$

$$d_{P4}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 3;\ t_4 = \frac{1}{\omega}\sin^{-1}\left(\frac{3 \times V_{dc}}{v_{gm}}\right) \tag{11}$$

for $t_4 \le t < t_5$

$$d_{P5}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 4;\ t_5 = \frac{1}{\omega}\sin^{-1}\left(\frac{4 \times V_{dc}}{v_{gm}}\right) \tag{12}$$

for $t_5 \le t < t_6$

$$d_{P6}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 5;\ t_6 = \frac{1}{\omega}\sin^{-1}\left(\frac{5 \times V_{dc}}{v_{gm}}\right) \tag{13}$$

for $t_6 \le t < t_7$

$$d_{P7}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 6;\ t_7 = \frac{1}{\omega}\sin^{-1}\left(\frac{6 \times V_{dc}}{v_{gm}}\right) \tag{14}$$

for $t_7 \le t < t_8$

$$d_{P8}(t) = \frac{v_{gm}}{V_{dc}}\sin(\omega t) - 7;\ t_8 = \frac{1}{\omega}\sin^{-1}\left(\frac{7 \times V_{dc}}{v_{gm}}\right) \tag{15}$$

for $t_8 \le t < \frac{T}{2} - t_8$

The sizing of the capacitor also depends on the switching duty cycle of each level and the value of time (t).

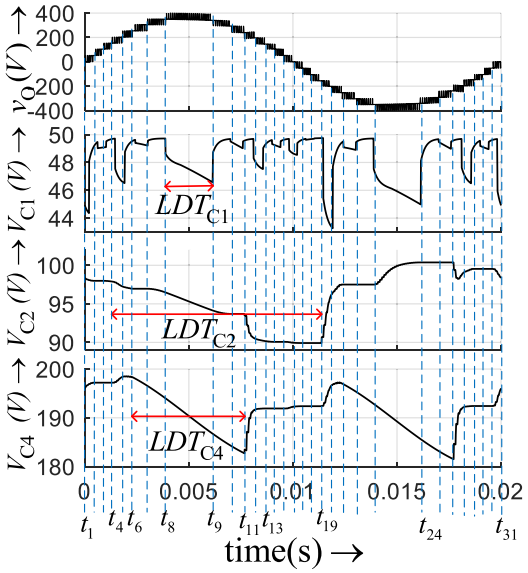

FIGURE 6. Waveforms of output voltage v_o and capacitor voltages V_C with *LDT*.

B. DESIGN OF SWITCHED CAPACITORS

The value of capacitances is determined by taking into consideration the capacitor's longest discharge time (*LDT*) during the course of the time period (T) [25], [26]. The waveforms of output voltage v_o, capacitor voltages V_{C1}, V_{C2}, and V_{C4} are displayed in Fig. 6. LDT_{C1} represents the *LDT* of capacitor C_1, LDT_{C2} represents the *LDT* of capacitor C_2, and LDT_{C4} represents the *LDT* of capacitor C_4. The amount of charge taken from the $C_1(Q_{C1})$, $C_2(Q_{C2})$, and $C_4(Q_{C4})$ for the maximum load current (i_{om}) for discharging the capacitors is provided in (16) - (18) in order to determine the value of capacitors which are given as:

$$Q_{C1} = \int_{t_8}^{t_9} i_{om}(t)dt = 2 \times \int_{t_8}^{T/4} i_{om}(t)dt \tag{16}$$

$$Q_{C2} = \int_{t_4}^{t_{19}} i_{om}(t)dt = \int_{t_4}^{T/2+t_4} i_{om}(t)dt = 2 \times \int_{0}^{T/4} i_{om}(t)dt \tag{17}$$

$$Q_{C4} = \int_{t_6}^{t_{11}} i_{om}(t)dt = 2 \times \int_{t_6}^{T/4} i_{om}(t)dt \tag{18}$$

The instantaneous load current (i_{om}(t)) at the fundamental frequency ($\omega = 2\pi f$), modulation index (m), power (S), and impedance angle (ϕ) are calculated in (19).

$$i_{om}(t) = I_{gm}\sin(\omega t - \phi) \tag{19}$$

The capacitor discharging time instants t_6 and t_8 are given by (13) and (15). Additionally, t_x represents one-quarter of

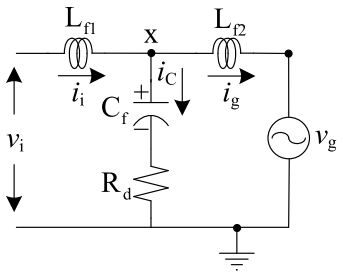

FIGURE 7. LCL filter with damping resistor for grid interfacing.

the overall time period (T) of the v_o.

$$t_x = \frac{T}{4} \tag{20}$$

The optimal value of capacitances, C_1, C_3, and C_4 (i.e., $C_{1\min}$, $C_{3\min}$, $C_{4\min}$) are obtained [25] as (21) – (23) using (16) – (20).

$$C_{1\,\min} = \frac{Q_{C1}}{\Delta V \times V_{C1}} = \frac{2I_{gm}}{\omega \times \Delta V \times V_{C1}} \times \cos(\omega t_8 - \phi) - \cos(\omega t_x - \phi) \tag{21}$$

$$C_{2\min} = \frac{Q_{C2}}{\Delta V \times V_{C2}} = \frac{2I_{gm}}{\omega \times \Delta V \times V_{C2}} \times \cos(\omega \times 0 - \phi) - \cos(\omega t_x - \phi) \tag{22}$$

$$C_{4\min} = \frac{Q_{C4}}{\Delta V \times V_{C4}} = \frac{2I_{gm}}{\omega \times \Delta V \times V_{C4}} \times \cos(\omega t_6 - \phi) - \cos(\omega t_x - \phi) \tag{23}$$

Since the operation of capacitors C_2 and C_3 are identical but are phase-shifted by half of the time period ($T/2$), the minimum capacitance required for capacitor C_3 is the same as that for capacitor C_2.

C. SIZING OF LCL FILTER ELEMENTS

As illustrated in Fig. 7, an LCL filter is employed to ensure the power quality standards set by IEEE Std 1547^{TM}-2018. It stands out for its exceptional ability to suppress high-frequency disturbances, surpassing the performance of both L and LC filters.

The LCL filter is designed with an inverter-side filter inductor (L_{f1}) to filter out high-frequency harmonics generated by the inverter, a grid-side filter inductor (L_{f2}) prevents high-frequency harmonics from entering the grid, maintaining grid quality, a filter capacitor (C_f) to attenuate high-frequency noise, and a damping resistor (R_d) to dampens resonances within the filter, ensuring stability as explained in [27]. The values are tabulated in Table 3.

D. DESIGN OF CHARGING INDUCTOR

A self-balanced switched-capacitor inverter faces the challenge of a high-capacitor charging current. During state $4V_{dc}$, capacitor C_4 is charged by connecting capacitors C_1, C_2, and the DC voltage source V_{dc} in series, generating an output voltage of $4V_{dc}$. However, this process involves a direct connection of C_4 to $4V_{dc}$ formed by C_1, C_2, and the input source V_{dc} in series. This connection is established through seven switches and a charging inductor, leading to a high charging current. In the charging loop, only the on-state internal resistance (r_{on}) of the switches, the equivalent internal series resistance (r_{Lch}) of the inductor, and the equivalent series resistance ($r_{c1}, r_{c2}, r_{c3}, r_{c4}$) of the capacitors are considered when analyzing the circuit. The corresponding equivalent circuit, including the charging inductor (L_{ch}), is shown in Fig. 8.

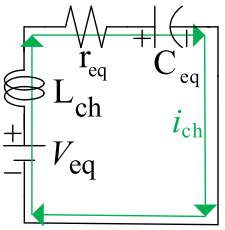

FIGURE 8. Equivalent circuit with charging inductor (L_{ch}).

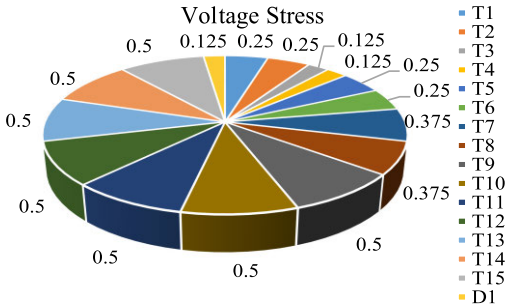

FIGURE 9. The voltage stress of switching components.

An appropriate charging inductor (L_{ch}) value is chosen to limit the inrush current passing through the semiconductor devices and capacitors of the proposed inverter from the input source. The L_{ch} must be connected in series with the input voltage source V_{dc} [14]. The value of the charging inductor (L_{ch}) is calculated as follows:

$$R_{eq} < \sqrt{\frac{4 \times L_{ch}}{C_{eq}}} \tag{24}$$

$$R_{eq} = r_{C1} + r_{C2} + 7 \times r_{on} + r_{C4} \tag{25}$$

$$C_{eq} = \frac{C_1(C_2 + C_3)C_4}{C_1C_4 + C_1(C_2 + C_3) + (C_2 + C_3)C_4} \tag{26}$$

where r_{C_1}, r_{C_2}, and r_{C_4} are the ESR of the capacitors C_1, C_2, and C_4; r_{on} refers to the internal resistance of the IGBT.

E. VOLTAGE STRESS OF COMPONENTS

The voltage stress experienced by each component is summarized in Fig. 9. This parameter is essential for selecting the components in the proposed inverter. The voltage stress of each component shown in Fig. 9 is expressed relative to the output voltage v_o. According to the voltage stress depicted

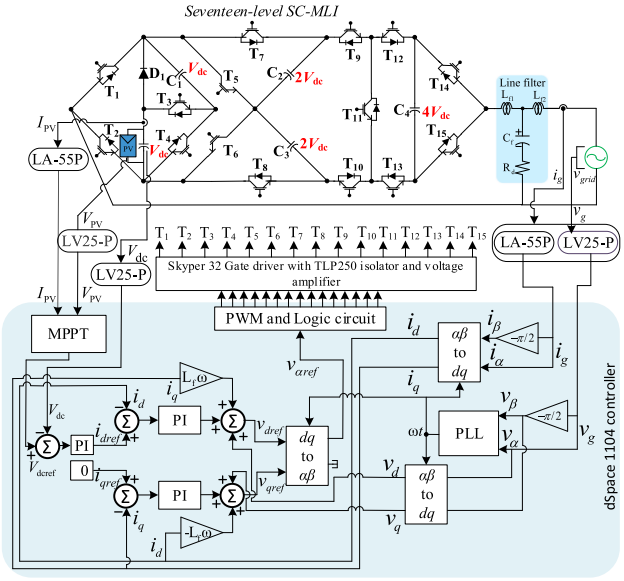

FIGURE 10. Proposed Grid-connected 17-level SC-MLI system.

in Fig. 9, the total standing voltage (TSV) is calculated by summing the individual voltage stresses of all components. Thus, the TSV of the switches and diode in the proposed inverter is equal to $5.625v_o$.

IV. DESIGN OF DQ CURRENT CONTROL FOR GRID-CONNECTED PV SYSTEM

In this section, a grid-connected 17-level SC-MLI with an LCL filter, featuring an outer DC-link voltage controller and an inner dq current controller in a cascaded manner, is shown in Fig. 10. The MPPT controller continuously senses the PV voltage and current (V_{PV}, I_{PV}) obtained from dedicated current and voltage sensors and generates a V_{dcref} signal, that guides the outer DC-link voltage controller to achieve optimal DC voltage for maximum power extraction from the PV array. In this design Perturb and Observe (P&O) MPPT technique is used to achieve the maximum power point (MPP). The P&O method evaluates the power obtained in the current cycle with the power of the previous cycle and periodically increases or decreases the PV's output terminal voltage. The control system modifies the operating point in the direction that the voltage and power vary, and in the opposite direction if they don't. Current is altered at a steady rate when the direction of the change in current is established.

The voltage controller compares the voltage reference signal (V_{dcref}) generated by the MPPT to the actual DC-link voltage V_{dc}, and the resultant error signal is routed through the PI controller to generate a d-axis reference current (i_{dref}), which is fed into the current controller. The q-axis reference current (i_{qref}) is purposefully set to zero in order to deliver only active power to the grid.

The inner current controller controls the current to be injected into the grid by tracking the grid parameters (v_{g}, i_{g}).

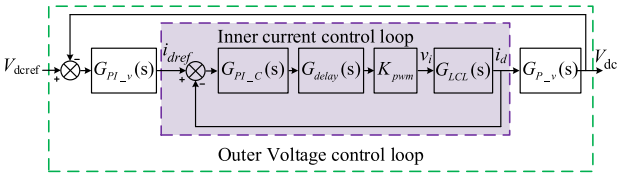

FIGURE 11. Block diagram of closed loop dq current controller.

The grid parameters obtained from grid-side current and voltage sensors are assumed to align with the α-axis. The β-axis quantities are obtained by phase shifting the α-axis quantities by (T/4). The α and β quantities are converted to DC (time-invariant) quantities (d-q axis grid currents (i_d, i_q), and d-q axis grid voltages (v_d, v_q)). This conversion is done using a phase-locked loop (PLL) that generates the angle ωt and dq transformations.

Separate PI controllers are employed for both the d and q-axis currents [28], [29]. The control signals are calculated based on the difference between the reference and measured currents. The current signal from the PI controller is summed with filter parameters and grid voltage parameters to generate v_{dref} and v_{qref}, which are then transformed into $v_{\alpha ref}$ and $v_{\beta ref}$. The $v_{\beta ref}$ signal is terminated; however, $v_{\alpha ref}$ is crucial in controlling the inverter's output voltage. The signal $v_{\alpha ref}$ is the reference signal for generating the switching pulses that directly control the inverter's power switches with the help of PD-PWM and the logic circuits.

The design of the current control loop for the d and q-axis has the same dynamics. Thus, the design procedure for the d-axis grid current (i_{d}) is detailed. The DC-link voltage is strategically set 1.2 times higher than the peak grid voltage to prevent over-modulation, ensuring grid stability and optimal inverter performance.

Fig. 11 illustrates the entire control structure of the grid-connected system, incorporating the LCL filter. The inner loop includes the transfer function of the PI current controller (G_{PI_C}(s)), the system sampling delay (G_{delay}(s)), the LCL filter (G_{LCL}(s)), and the modulation gain (K_{PWM}).

The transfer function of the respective blocks used in the current control loop can be obtained by (27) - (29)

$$G_{PI\_C}(\mathrm{s}) = K_{P\_C} + \frac{K_{I\_C}}{\mathrm{s}} \tag{27}$$

$$G_{delay}(\mathrm{s}) = \frac{1}{1 + 1.5T_{\mathrm{S}}(\mathrm{s})} \tag{28}$$

$$G_{LCL}(\mathrm{s}) = \frac{\mathrm{s}C_{\mathrm{f}}R_{\mathrm{d}} + 1}{\mathrm{s}^3 L_{\mathrm{f1}}L_{\mathrm{f2}}C_{\mathrm{f}} + \mathrm{s}^2\left(L_{\mathrm{f1}} + L_{\mathrm{f2}}\right)R_{\mathrm{d}}C_{\mathrm{f}} + \mathrm{s}\left(L_{\mathrm{f1}} + L_{\mathrm{f2}}\right)} \tag{29}$$

where K_{P_C} and K_{I_C} are the proportional and integral gains of the PI current controller, and T_{s} is the sampling time, which is assumed to be equal to the switching time and derived from the switching frequency (f_s) [30], [31]. The filter parameters, L_{f1}, L_{f2}, C_{f}, and R_{d}, are calculated from Section III-C, and L_{f} is considered as $L_{\mathrm{f1}} + L_{\mathrm{f2}}$.

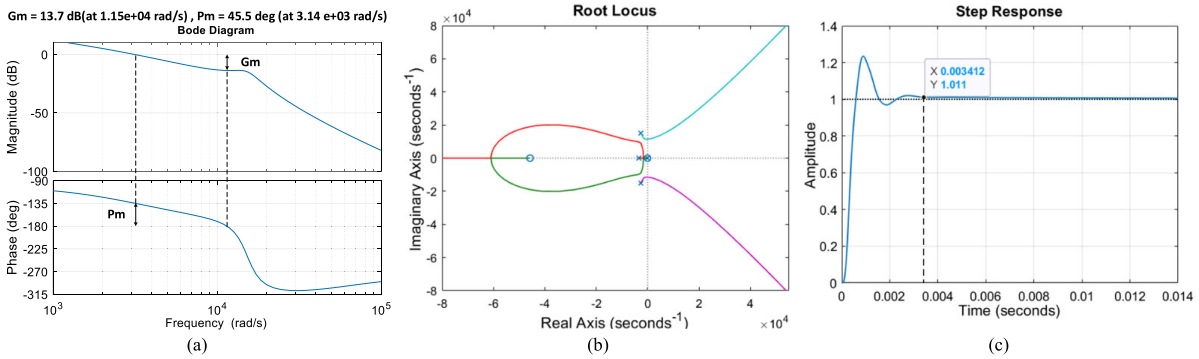

FIGURE 12. (a) Bode plots, (b) Root locus of open-loop current controller ($GOL_C(s)$), and (c) Step response of closed-loop current controller ($GCL_C(s)$).

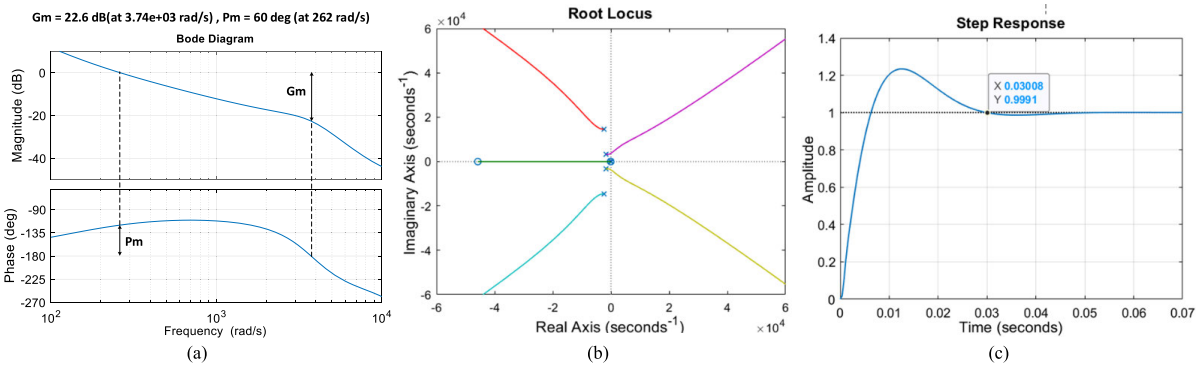

FIGURE 13. (a) Bode plots, (b) Root locus plot of open-loop voltage controller ($GOLv(s)$), and (c) Step response of closed-loop voltage controller ($GCLv(s)$).

The open-loop transfer function of the current controller ($GOL_C(s)$) can be expressed as:

$$GOL_C(s) = \frac{0.0003973s^2 + 18.21s + 1000}{5.663e^{-15}s^5 + 4.77e^{-11}s^4 + 1.416e^{-6}s^3 + 0.0044s^2} \tag{30}$$

The gain of modulation is considered as $K_{PWM} = v_{ref}/v_{tri}$ [32]. The corresponding Bode and Root locus plots of $GOL_C(s)$ are obtained for the stability of the system, as shown in Fig. 12(a) and 12(b). It is observed from the frequency responses of the $GOL_C(s)$ that a phase margin (Pm) of 45.5° and gain margin (Gm) of 13.7dB make the system stable. Further, it is observed that all the Roots of the system lie on the left side of the s-plane, ensuring the system's stability. The transfer function of the closed-loop current controller is obtained by

$$GCL_C(s) = \frac{7.016e^{10}(s + 4.58e^4)(s + 54.98)}{(s + 55.72)(s^2 + 3497s + 1.45e^7)(s^2 + 4875s + 2.18e^8)} \tag{31}$$

The step response of (31) is shown in Fig. 12(c).

The transfer function of the PI-type outer voltage controller ($G_{PI\_v}(s)$) and the transfer function for the dc-link voltage model ($G_{P\_v}(s)$) can be expressed as follows:

$$G_{PI\_v}(s) = K_{P\_v} + \frac{K_{I\_v}}{s} \tag{32}$$

$$G_{P\_v}(s) = \frac{3}{2} \times \frac{v_{om}}{V_{dc}C_{eq}(s)} \tag{33}$$

The DC-link voltage is considered 1.2 times greater than the peak voltage of the grid to avoid over-modulation. Thus, the overall transfer function of open-loop voltage control is computed as:

$$GOL_v(s) = \frac{1.6176e^{13}(s + 4.6e^4)(s + 130.7)(s|! + 54.98)}{s^2(s + 55.7)(s^2 + 3497s + 1.45e^7)(s^2 + 4872s + 2.18e^8)} \tag{34}$$

The transfer function of the closed-loop voltage controller $GCL_v(s)$ with a simplified current control loop shown in Fig. 13 is given by

$$GCL_v(s) = \frac{1.6e^{13}(s + 4.6e^4)}{(s + 55)(s^2 + 240s + 3.2e^4)} \times \frac{(s + 130.7)(s + 55)}{(s^2 + 3240s + 1.37e^7)(s^2 + 4889s + 2.2e^8)} \tag{35}$$

As presented in Figs. 13(a)-13(b), the Bode and Root locus plot of $GOL_v(s)$ is obtained for closed-loop stability. It is

TABLE 2. Comparison of the proposed 17-level OBSC-MLI with recently published 17-level MLIs.

Topology	N_S	N_{sw}	N_D	N_C	k_b	k_b/N_c	Simulated η (%)
[9]	1	29	6	8	8	0.18	89.2 @ 523.4 W
[10]	2	18	2	6	4	0.14	91.06 @ 200 W
[11]	4	16	0	4	1	0.042	90.87 @ 998.4 W
[12]	1	10	6	6	8	0.35	92.75 @ 1 kW
[13]	1	26	0	7	8	0.24	91.94 @506.2 W
[14]	1	12	5	4	8	0.36	95.48 @ 1 kW
[15]	1	14	2	3	8	0.4	94.07 @ 500 W
[16]	4	10	0	0	1	0.07	98.6 @ 100 W
[17]	1	26	0	7	8	0.24	97.7 @ 400 W
[18]	1	10	4	6	2	0.095	95.45 @ 1 kW
[19]	1	13	6	4	2	0.33	96.86 at 512 W
[20]	4	10	0	0	1	0.07	97.35 @ 562 W
[21]	1	14	4	4	4	0.17	94.5 @ 522 W
[22]	1	16	8	4	2	0.068	95.5 @ 400 W
Proposed	**1**	**15**	**1**	**4**	**8**	**0.38**	**96.03 @ 419 W**

observed from Figs. 13(a) and 13(b) that the (Pm = 60°) and (Gm = 22.6 dB) are positive. Further, it is observed that all the roots of the system lie on the left side of the s-plane, ensuring the system's stability. Moreover, from Figs. 12(c) and 13(c), it is observed that the speed of the current controller is faster than that of the voltage controller.

V. PERFORMANCE COMPARISON

Table 2 in this section compares the suggested 17-level OBSC-MLI with the existing 17-level SC-MLI topologies. The sources (N_S), needed switches (N_{SW}), diodes (N_D), capacitors (N_C), boosting gain (k_b), boosting gain per number of components (k_b/N_c), and simulated efficiency ($\eta(\%)$) are the comparative criteria.

Table 2 shows that, compared to the inverters proposed in [9], [12], [13], and [17], the suggested 17-level OBSC-MLI needs fewer semiconductor devices (switches and Diodes) and capacitors for 8-times boosting gain (k_b). Furthermore, all topologies except those given in [18], [21], and [22] have lesser boosting gain than the proposed 17-level. Moreover, the topologies described in [10], [11], [16], and [20] have multiple DC sources. Further, the proposed 17-level OBSC-MLI performs better when compared to boosting gain per number of components (k_b/N_c).

VI. SIMULATION RESULTS

In order to show the performance of the proposed MLI, the inverter is simulated in MATLAB/Simulink using PLECS Blocksets for R-load ($R = 80\ \Omega$). The inverter parameters for a specimen output power of 1 kW are considered, with peak inverter output voltage, $v_{om} = 400$ V, at a fundamental frequency, $f = 50$ Hz, and the input DC-link voltage $V_{dc} = 50.0$ V. The parameters of the inverter for MATLAB/Simulink are given in Table 3.

In Fig. 14(a) and 14(b), the conduction and switching losses of components are illustrated at a rated input power of 1037 W, resulting in an overall power loss

TABLE 3. Simulation and experimental parameters.

Parameters		Values
Inverter parameters		
DC source (V_{dc})		50 V
Switching frequency (f_{sw})		5 kHz
Peak Inverter output voltage (v_{om})		400 V
Load resistance (R)		80 Ω
Load inductance (L)		150 mH, 300 mH, 500 mH
Switches (IGBTs)		v_f = 1.0 V, r_{on} = 6.7 mΩ, v_d = 1.2 V, r_d = 6.0 mΩ
Discrete diodes D_1, D_2		v_{dd} = 0.75 V, r_{dd} = 9.1 mΩ
Grid parameters		
Grid voltage (v_g)		240 V
Grid frequency (f)		50 Hz
Current controller (K_{P_C}, K_{I_C})		20.2, 1110
Voltage controller (K_{P_v}, K_{I_v})		0.012, 1.56
Components	**Part No.**	**Specifications**
Programmable DC laboratory power supply	ET System 3 kW LAB/SMS 3150	0-150 V/0-20 A
Switches (IGBTs)	Semikron SKM100GB12T4	V_{CE} = 1200 V, I_C = 100 A
Discrete diode	Infineon D75E60	V_R = 600 V, $I_{F(AV)}$ = 75 A
Gate Driver	-	Skyper 32
Capacitor C_1	Alcon PG-8K	100 V, 2200 µF
Capacitors C_2, C_3	Alcon PG-8K	150 V, 3300 µF
Capacitor C_4	Alcon PG-8K	250 V, 1000 µF
Filter inductors (L_{f1}, L_{f2})	Rishab Industries	2.2 mH
Capacitor (C_f)	Tecate	400 V, 3.9 µF
Resistor (R_d)	MEGA	5.6 Ω
Charging inductor (L_{ch})	Rishab Industries	15 µH

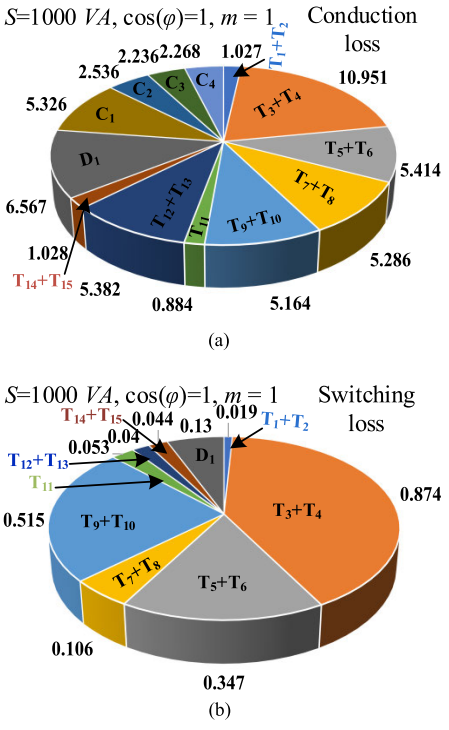

FIGURE 14. Power loss of the components, (a) Conduction loss, (b) Switching loss.

of 56.20 W. Fig. 15(a) displays the simulated and measured efficiencies (η) across a wide range of output power (P_o). It is observed that the maximum experimental efficiency is 96.27% at $P_o = 119.62$ W, slightly lower than the

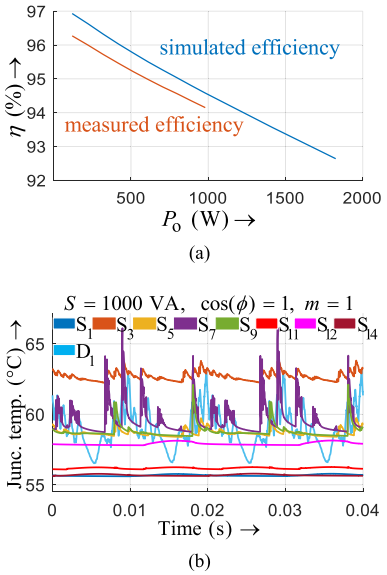

FIGURE 15. (a) Measured and simulated efficiency with respect to output power P_o, (b) Junction temperature of the switches and diode of the proposed inverter.

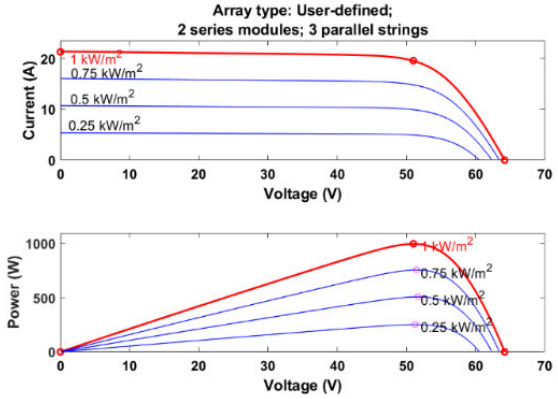

FIGURE 16. I-V and P-V characteristics of the PV array.

simulated value (96.93%). However, efficiencies decrease with increased P_o, reaching 94.15% at $P_o = 980.79$ W compared to the simulated value of 94.58%. The heat sink temperature variation of the semiconductor devices is presented in Fig. 15(b), with an average temperature of 58.23° C recorded at rated power.

Further, to check the performance of the closed-loop control of the grid-connected PV system, a user-defined PV array consisting of three parallel strings, each containing two PV modules connected in series (2 × 3), is considered as the input source of the inverter. Each module has a capacity of 167 Wp ($V_{oc} = 30.76$ V, $I_{sc} = 6.926$ A, $V_{mp} = 25.5$ V, $I_{mp} = 6.53$ A). The entire PV array generates an output power of approximately 1000 W with a PV array voltage of 51 V. The simulation results of the current-voltage (I-V) and power-voltage (P-V) characteristics of the entire PV array are shown in Fig. 16.

For a grid-connected application, the value of the LCL filter, as given in Table 3, is derived based on [27], which is

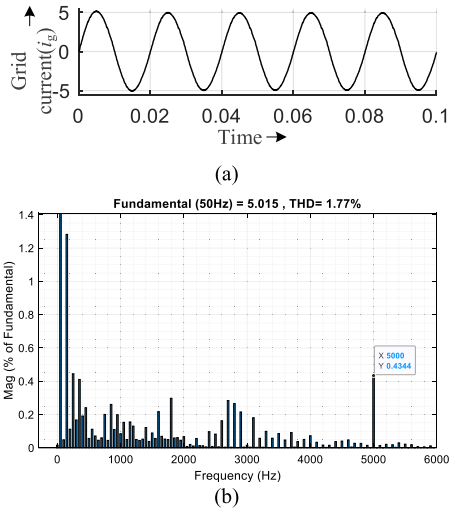

FIGURE 17. (a) The waveform of grid current (i_g) and (b) Harmonic spectrum of grid current i_g.

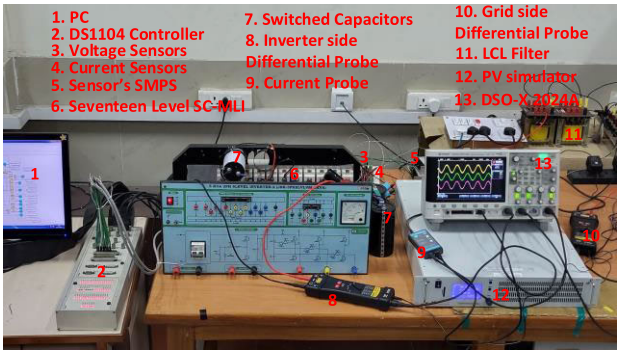

FIGURE 18. Experimental Setup of the proposed grid-connected 17-level SC-MLI.

outlined in Section III-C. The filter parameters ($L_{f1} = L_{f2} = 2.2$ mH, $C_f = 3.9$ μ F, and $R_d = 5.6$ Ω) are appropriate for the proposed grid-connected system in terms of negligible grid-current harmonics. The waveform of the grid current and the corresponding harmonic spectrum is depicted in Fig. 17. It is observed that the grid current is sinusoidal and contains much fewer harmonic components. The grid current's total harmonic distortion (THD) is measured at 1.77% and a switching frequency harmonic of 0.43%, ensuring the power quality standards established by the IEEE Std 1547™-2018.

VII. EXPERIMENTAL RESULTS

To validate the performance of the proposed 17-level inverter with a single PV source, experiments are conducted for different loads, such as resistive, inductive, and grid-connected loads. The parameters of the resistive loads (R), inductive load (L), grid, and PV source are given in Table 3.

A laboratory prototype of the proposed grid-connected inverter designed to handle 1 kW power is shown in Fig. 18. The major components of the proposed systems, as tabulated in Table 3, are shown in the figure. A programmable DC

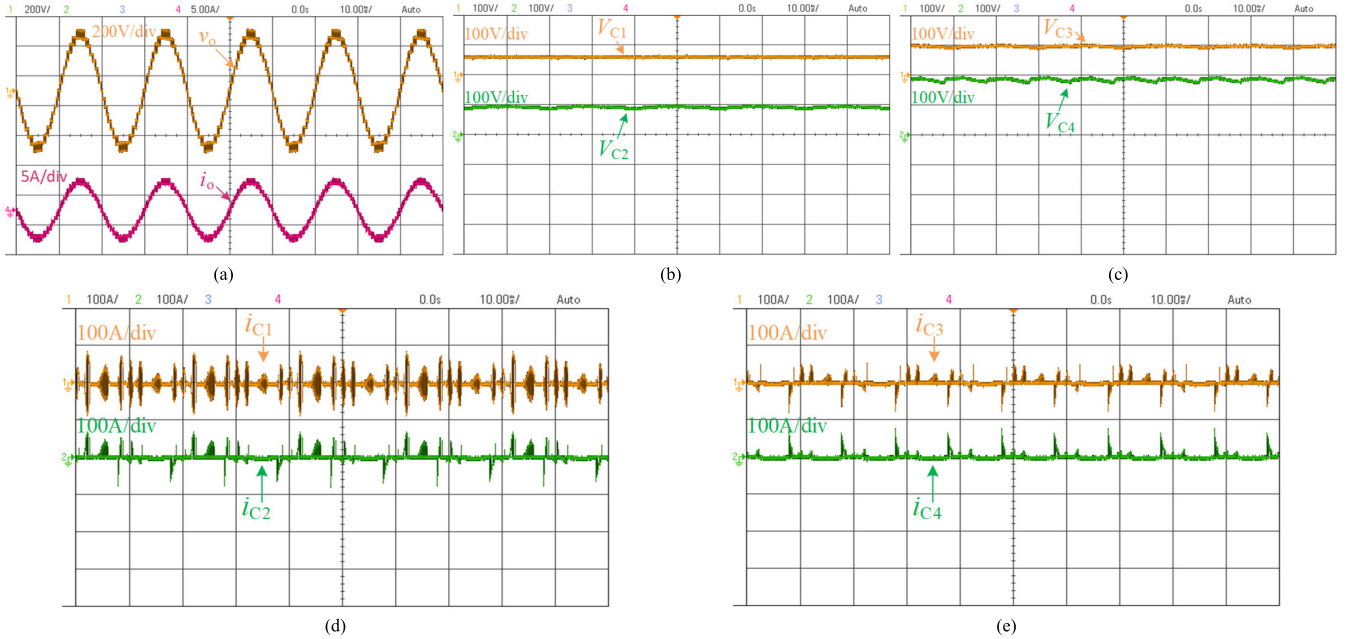

FIGURE 19. Experimental results showing (a) inverter output voltage, v_o and current, i_o for the resistive load ($R = 80\ \Omega$), (b) capacitors voltage V_{C1} and V_{C2} (c) capacitors voltage V_{C3} and V_{C4} (d) capacitors current i_{C1} and i_{C2}, and (e) capacitors current i_{C3} and i_{C4}.

source with a solar array simulator (ET System LAB/SMS 3150) is used as a PV source for testing the system's dynamic performance. For a single-phase grid of voltage 240 V, the corresponding DC-link voltage $V_{dc} = 51$ V is chosen for the proposed 17-level MLI, as it is boosted eight times by the inverter. LEM (LV25-P) and LEM (LA 55-P) are used as voltage and current sensors to sense the voltage and current and feed it to the controller (DS1104) to implement closed-loop control of the grid-connected system. The inverter's performance is initially tested with R-load, considering the voltage $v_{om} = 400$ V for an input voltage V_{dc} of 50 V. Fig. 19(a) shows the experimental results of the proposed inverter for a $R = 80\ \Omega$ at modulation index, $m = 1$ with a fixed DC voltage $V_{dc} = 50$ V. It is observed that the output voltage v_o of the inverter has 17 voltage levels with a maximum value v_{om} of 400 V and current i_o of a maximum value of 5 A. The corresponding peak-to-peak voltage ripple voltages of capacitors C_1 and C_2 are 4.98 V and 9.93 V, with a mean value of 50.6 V and 99.34 V, as observed in Fig. 19(b). In Fig. 19(c), the peak-to-peak voltage ripple value and mean value of capacitor C_4 are 19.06 V and 198.3 V, respectively. These voltage ripple values are within the specified capacitor ripple voltage ΔV of 10%, and the mean values remain constant in the steady state. Furthermore, the mean values of capacitor currents in Fig. 19(d) - Fig. 19(e) are consistently 0 A, ascertaining that the energy extracted from and delivered to the capacitors averaged over a fundamental cycle is zero. The blocking voltage waveforms of each switching device are shown in Figs. 20(a)-20(d).

Subsequently, the feasibility of the inverter with a low power factor load is also tested with a resistive and inductive ($R = 80\ \Omega$ and $L = 150$ mH) load at power factor ($\cos(\phi) = 0.86$). The experimental waveforms in Fig. 21(a) show the 17-level output voltage v_o of 400 V and sinusoidal output current i_o of peak value 4.06 A. Fig. 21(b) shows the experimental result under a dynamic change in modulation index (m) from 1.0 to 0.4 with RL-load ($R = 80\ \Omega$, $L = 150$ mH). The output voltage and current waveform are observed to change from 17-level (400 V) to 9-level (200 V) and 4.06 A to 1.71 A, respectively.

To further validate the performance of the inverter under lower power factor, the inverter is loaded with highly inductive load, and their output voltage, v_o, and current, i_o for the resistive-inductive load ($R = 80\ \Omega$, $L = 300$ mH ($\cos(\phi) = 0.64$)) are 400 V, 3 A and for ($R = 80\ \Omega$, $L = 500$ mH ($\cos(\phi) = 0.45$)) are 404 V, 2.12 A, respectively, as shown in Fig. 21(c) and 21(d).

For grid-connected operations, the parameters of the closed-loop inner-current and outer voltage controllers (K_P and K_I) are calculated and tuned to obtain a sinusoidal current that synchronizes with the grid voltage to ensure maximum active power injections to the grid. The experimental results of inverter output voltage v_o, grid voltage (v_g), and the injected grid current (i_g) are presented in Fig. 22(a).

It is observed from Fig. 22(a) that the peak magnitude of inverter output voltage v_o is 404 V with 17 stepped voltage levels, which is near sinusoidal. the grid voltage v_g is sinusoidal with a peak voltage magnitude of 340 V, and the injected grid current i_g is 5.0 A, respectively. All three waveforms are in phase, which ensures zero reactive power is injected into the grid.

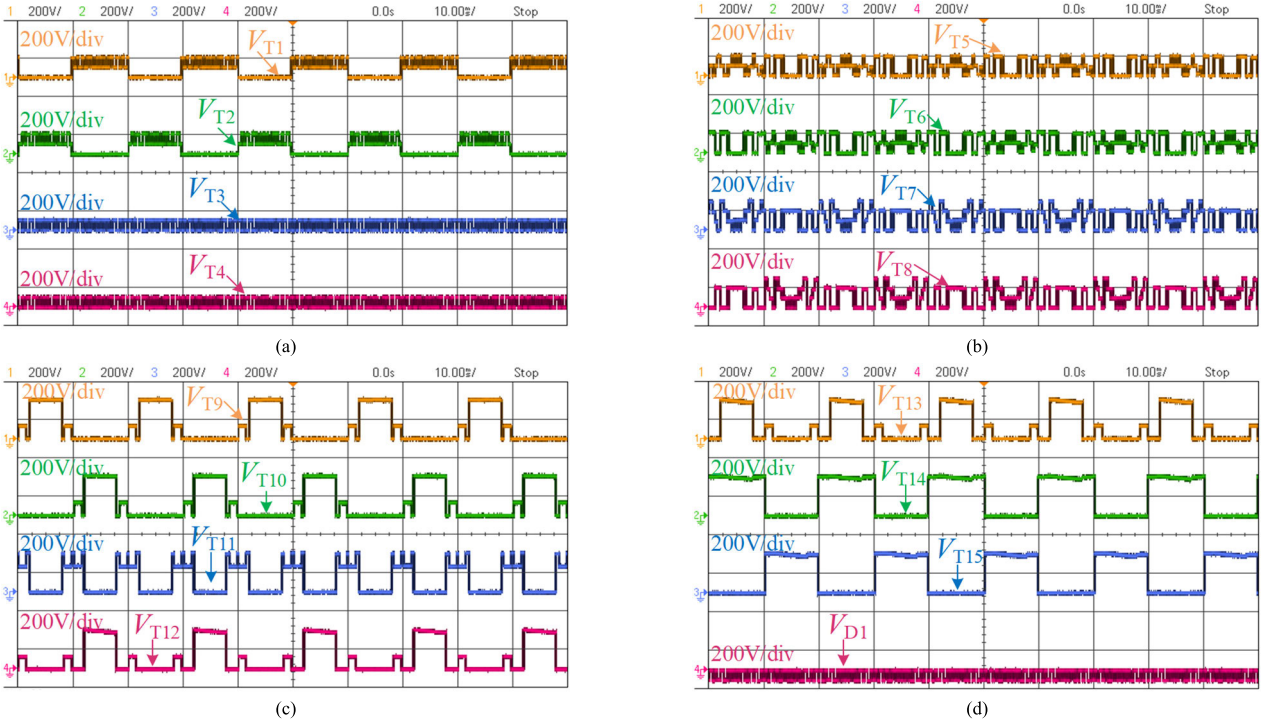

FIGURE 20. Experimental waveforms of blocking voltage of switches (T_1-T_{15}) and diode (D_1).

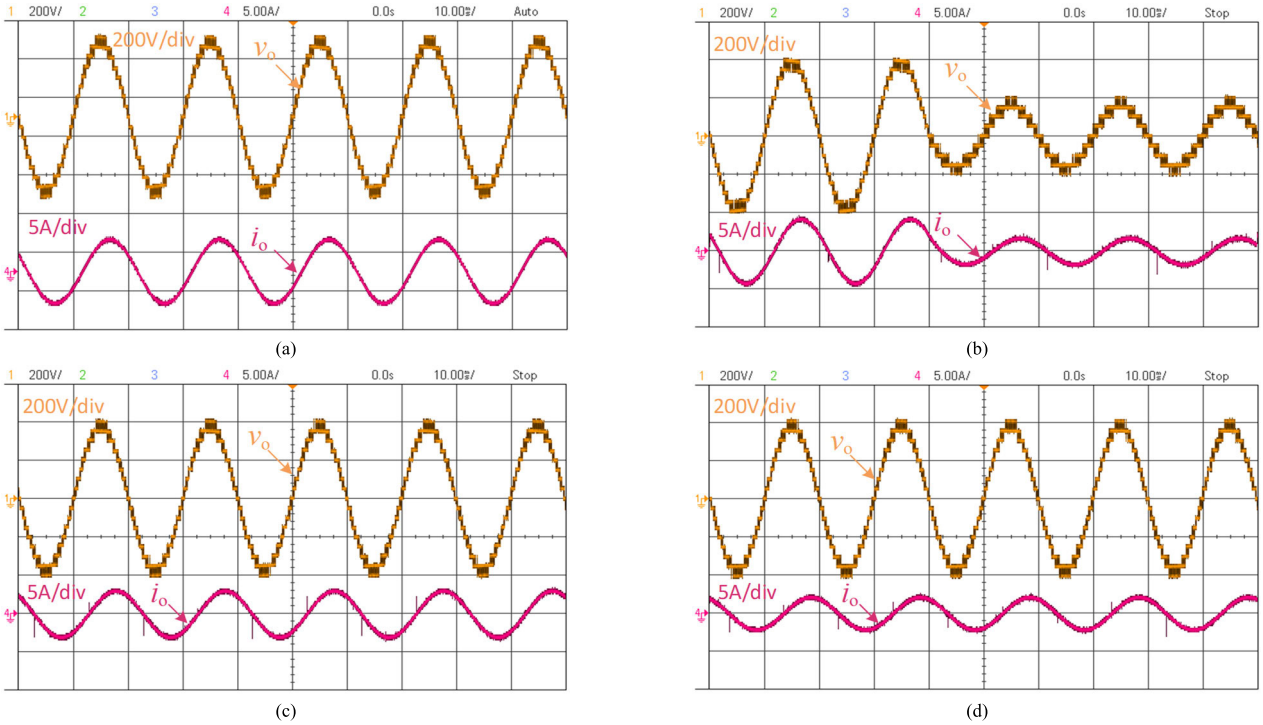

FIGURE 21. Experimental results showing inverter output voltage, v_o, and its current, i_o for (a) resistive-inductive load ($R = 80\ \Omega$, $L = 150$ mH), (b) $R = 80\ \Omega$, $L = 150$ mH with change in modulation index (m) from 1.0 to 0.4 (c) $R = 80\ \Omega$, $L = 300$ mH, and (d) $R = 80\ \Omega$, $L = 500$ mH.

The system's performance is also tested under dynamic irradiance, changing from 1000 W/m^2 to 500 W/m^2 and vice versa, which is obtained from a programmable power source with a solar array emulator (LAB/SMS 3150). Fig. 22(b) shows the corresponding dynamic behavior of the injected grid current (i_g), which changes according to the change

TABLE 4. Measured lower-order voltage harmonic components in percent of the fundamental voltage.

h%	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
IEEE Std 1547-2018	1.0	4.0	2.0	4.0	3.0	4.0	4.0	4.0	4.0	2.0	2.0	2.0	2.0	2.0	2.0	1.5	1.5	1.5	1.5	1.5	1.5
Without line filter	0.02	1.23	0.09	0.50	0.09	0.33	0.14	0.31	0.08	0.06	0.09	0.11	0.02	0.04	0.06	0.17	0.06	0.16	0.04	0.12	0.06
With line filter	0.02	1.24	0.09	0.51	0.09	0.33	0.14	0.32	0.09	0.06	0.10	0.12	0.02	0.05	0.08	0.21	0.08	0.21	0.06	0.17	0.09

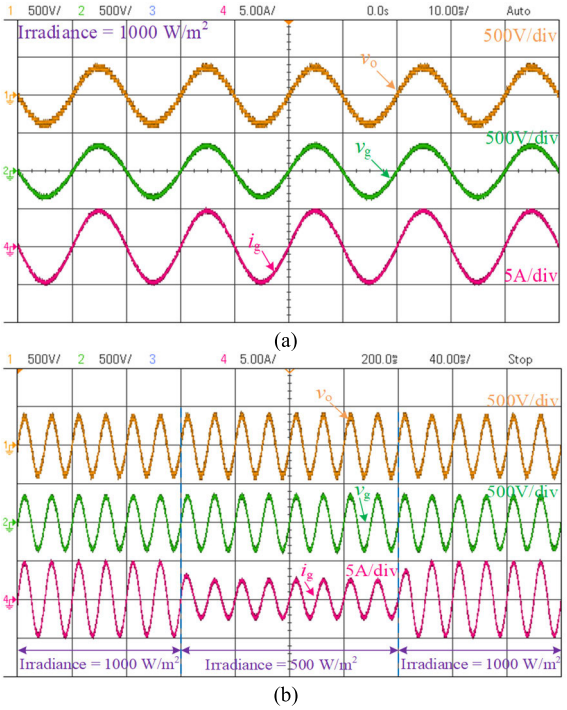

FIGURE 22. Experimental results showing the inverter output voltage v_o, the grid voltage v_g, and the injected grid current i_g (a) at 1 kW power injected to the grid, (b) under a dynamic change in irradiance and q-axis reference current (I_{qref}) = 0.

in irradiance. Considering these figures, it can be concluded that the dq control for 17-level MLI performed well under different transient conditions.

The total harmonic distortion of inverter output voltage v_o(%THDv_o) is 7.23%, and the filtered output voltage is 1.87%. As presented in Table 4, the individual harmonic components of the output voltage with and without line filter meet the power quality standards specified by IEEE Std 1547™-2018 [33].

VIII. CONCLUSION

A newly developed 17-level grid-connected SC-MLI with an octuple gain is developed, requiring few semiconductor components, and the capacitor voltages are balanced in the steady state at the appropriate value. In comparison to other multilevel inverters, the proposed topology improves efficiency and reduces power losses. Furthermore, the control technique enables consistent performance under a variety of operational situations. The 17-level OBSC-MLI has the advantage of a maximum voltage stress upon the switches $\leq 0.5\ v_o$ and an aggregate standing voltage (TSV) of $5.625v_o$. The switched capacitor voltages are self-balanced because they are charged/discharged equally without any sensor-based balancing techniques. Moreover, the inverter can handle reactive power even at a very low power factor. The proposed grid-connected system with a PV voltage of 51 V is implemented without a DC-DC converter and transformer, making the overall design compact and efficient. A detailed circuit analysis is carried out, including its operation, parameter determination, experimental verification, and comparative analysis. Experimental results of the proposed grid-connected system are tested and verified under dynamic conditions.

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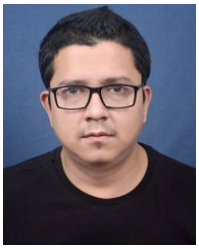

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