RESEARCH ARTICLE

Equivalent Circuit Modelling of Hybrid Supercapacitors Through Experimental Spectroscopic Measurements

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ABSTRACT In this paper, a strategy for the identification of models based on supercapacitors equivalent circuits is proposed. The approach is based on an innovative and efficient encoding procedure, suitable for a generic impedance network. The latter, in combination with an optimization algorithm, is used to investigate the components and topology of the best-fitting network for a given dataset. To demonstrate the generality of the proposed approach, equivalent circuits involving both integer and fractional order elements have been derived. The identification of each model is performed using a cascade optimization algorithm for maximum robustness against local minimum entrapment. The approach is applied to the identification of a 4000 F hybrid supercapacitor, for which data is acquired from an extensive experimental spectroscopy campaign at different states of charge and temperatures. Two models are selected, one for each set, both in excellent agreement with the experimental measurements.

INDEX TERMS Hybrid supercapacitor, electrochemical impedance spectroscopy, equivalent circuit, modeling.

I. INTRODUCTION

Supercapacitors (SCs) represent an emerging energy storage technology able to bring several advancements to different sectors, such as transportation [1], power grids [2] and energy generation [3]. SCs allow for a significant increase in the number of charge/discharge cycles compared to traditional batteries, maintaining high performance over the long term [4]. In addition, their high power density makes them well-suited for applications that require quick bursts of power, such as in regenerative braking systems in electric vehicles, or for smoothing out fluctuations in power delivery [5].

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Despite these notable advantages, this technology currently has also some relevant limitations. The main drawback of SCs is their lower energy density compared to Li-Ion batteries: for applications that demand long-term energy storage, batteries still represent a more practical choice [6]. In addition, SCs have a higher self-discharge rate, losing the stored energy more quickly when not in use respect to Li-Ion batteries [7]. To overcome these limitations, Hybrid Supercapacitors (HSCs) have been recently developed [8]. Unlike the classic Electric Double-Layer Capacitor (EDLC) supercapacitors, HSCs combine elements of SCs and traditional batteries to harness the benefits of both technologies [9], [10], [11]. Many studies have recently focused on the analysis and electrical characterization of this emerging technology. For example, in [12], spectroscopy

measurements have been carried out by varying the State of Charge (SOC) and the operating temperature, in order to investigate the HSCs in different conditions. What emerges from this study is that the equivalent impedance of HSCs has a strongly nonlinear behavior and is significantly sensitive to changing SoC and temperature.

The large sensibility of the impedance from these variations makes the derivation of equivalent electrical models more challenging. However, the development of equivalent electrical models, capable of accurately describing the behavior of a HSC under different operating conditions, is extremely useful for implementing these devices in time domain simulations and control design procedures.

In Fig. 1, three main different classifications of an equivalent model under different points of view are shown.

- Math: Numerical models rely on mathematical equations to simulate the behavior of SCs. Numerical methods, such as finite element analysis (FEA) or finite difference methods, are commonly used to solve these equations numerically. Physical models attempt to describe the behavior of SCs based on fundamental physical principles, such as electrochemistry and thermodynamics. These models often involve detailed descriptions of the structure and composition of the SCs electrodes, electrolyte, and separator materials, as well as the mechanisms governing charge storage and transport. Physical models can provide deep insights into the underlying physics of SCs but may be more complex and computationally intensive compared to equivalent circuit models. Finally, Equivalent circuit models represent SCs using electrical components, such as resistors, capacitors, and inductors, that mimic their electrical behavior. These models simplify the complex physical processes occurring within the SCs into a circuit topology that can be easily analyzed using circuit theory.
- Dataset: each model is based on experimental measurements. These measurements can be expressed in the time domain, such as the response of the cell to some charging profiles, or the frequency domain, such as Electrochemical Impedance Spectroscopy (EIS).
- Parameter: Models are derived to predict a particular parameter of SCs. Most of the models take into account the effect of ageing, SoC and temperature on the system's response.

The pressing need for accurate SCs models is confirmed by the numerous studies already available in the literature. In Table 1, a literature overview of the equivalent SC models is shown.

The main equivalent circuit topologies used in the literature are summarized in Fig. 2. For each paper, the main technical aspects are summarized. Some considerations as follows derive from the state of the art as summarized in Table 1:

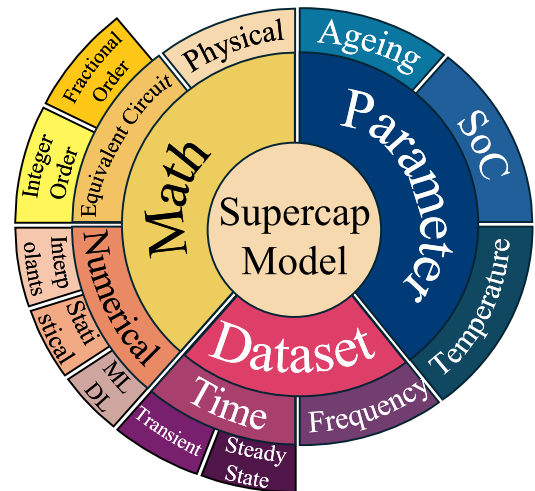1) Although most papers are very accurate in modelling the SC behavior under different SOCs, only a few

FIGURE 1. Classifications of equivalent supercapacitor models.

take into account the effects of the temperature on the SC impedance. This aspect is extremely critical for HSCs, because the impedance strongly depends on temperature variations. The models investigated in this paper allow temperature effects to be considered.

2) Most of the models are derived from voltage/current measurements under particular charge/discharge profiles. This solution greatly simplifies the dataset collection phase but leads to less general models. Using a time-domain response produces very accurate models only for certain charging profiles, but the accuracy significantly decreases under different scenarios. For this reason, in this paper, frequency domain measurements obtained through EIS are used as a dataset. Although this choice increases the time required to create the dataset because of numerous tests and it necessity of particular instrumentation, this choice allows for extending the validity of the model and makes it accurate independently of the charging profile.

3) All the models available in the literature have been identified for traditional EDLC supercapacitors. Therefore, the literature is currently lacking an evaluation of electrical models for HSCs. For this reason, attention has been placed on HSC technology.

4) Most of the models in Table 1 are nonlinear. This assumption is necessary if good accuracy is desired over a wide range of SoC variations and temperatures. Linear models are computationally advantageous but quickly degrade their accuracy when the device is not operated close to the nominal conditions. Although the circuits in Fig. 2 may all appear to be linear, in reality, the components vary with nonlinear laws as functions of the parameter under study, such as SoC. The use of nonlinear parameters is necessary if accurate models are to be obtained over wide ranges of variation. Since in this paper models that are valid in wide ranges of SoC and temperatures are presented, the focus is placed on nonlinear models.

TABLE 1. Equivalent Electrical Circuit: Literature Overview.

| Ref.	Tech.	Model	Temperature Variation	Electrical Model	Dataset
[13]	EDLC	Maxwell BCAP3000	Yes	(c)	Time Domain
[14]	EDLC	Maxwell BCAP0350	No	(f)	Time Domain
[15]	EDLC	ACN TEABF4	No	(b)	Frequency Domain
[16]	EDLC	22F Cooper Bussmann PowerStor	No	(f)	Time Domain
[17]	EDLC	Maxwell 10 F	No	(f)	Time Domain
[18]	EDLC	Maxwell 310 F	No	(d)	Time Domain
[19]	EDLC	Maxwell BCAP0140, BCAP0150	No	(f)	Time Domain
[20]	EDLC	Maxwell BCAP0650	Yes	(f)	Time Domain
[21]	EDLC	Maxwell 3000 F	No	(a)	Time Domain
[22]	EDLC	Maxwell BCAP0350	No	(b)	Time Domain
[23]	EDLC	Eaton XL60, LSUC EA ST01, MAXWELL BCAP, SPSCAP 2R7STA	No	(f)	Time Domain
[24]	EDLC	Maxwell BCAP0025	No	(b)	Frequency Domain
[25]	EDLC	Maxwell BCAP3000	No	(f)	Time Domain
[26]	EDLC	-	No	(b)	Frequency Domain
[27]	EDLC	SAMWHA 350F	No	(f)	Time Domain
[28]	EDLC	Maxwell BCAP1200	No	(f)	Time Domain
[29]	EDLC	Maxwell BCAP2000	No	(d)	Frequency and Time Domain
[30]	EDLC	Vinatech 100F	No	(a)	Time Domain
[31]	EDLC	Panasonic S5R5155 1.5 F	No	(a)	Fractional Order
[32]	EDLC	FGR0H105ZF 1F	No	(a)	Fractional Order
[33]	EDLC	Nippon Chemicon 2300F	No	(b)	Time Domain
[34]	EDLC	325 F	No	(d)	Time Domain
[35]	EDLC	Eaton 400 F	No	(f)	Time Domain
[37]	EDLC	Maxwell BMOD0083	Yes	(e)	Time domain
[38]	EDLC	AVX, Eaton, Kemet	No	(e)	Fractional Order, Time domain
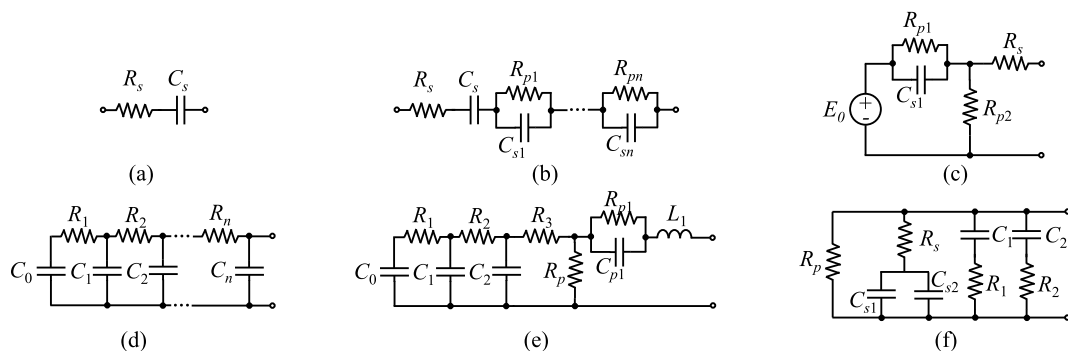
FIGURE 2. Supercapacitor equivalent circuits adopted in the literature reviewed in Table 1.

Given the many choices which characterize the definition of an equivalent electrical model, this article aims to propose a general procedure for the automatic identification of the model parameters once the equivalent circuit has been chosen. In particular, two strongly different equivalent circuits are selected to highlight the generality of the procedure.

The first equivalent circuit consists of an integer order model, made up of resistances, inductances, and capacitors. These models are suitable for replicating the response of the supercapacitor in the time domain, for example, in simulators such as Matlab, Simulink or LTspice.

The second equivalent circuit includes fractional order elements, i.e., Constant Phase Elements (CPEs) and can better capture the frequency-dependent behaviour of supercapacitors. Unlike classical models, which typically rely on fixed values of resistance and capacitance, CPEs allow for a more flexible representation of impedance that can vary with frequency. Supercapacitors exhibit nonideal characteristics such as frequency dispersion, leakage, and double-layer capacitance. CPEs offer a more accurate representation of these nonideal behaviors compared to classical models, which may oversimplify the impedance characteristics. On the other hand, the parameters of CPEs, such as the

magnitude and exponent, may not have intuitive physical meanings. This makes it difficult to interpret their values in the context of supercapacitor behavior without extensive calibration and experimentation. In addition, while CPEs excel at capturing frequency-dependent behavior due to their impedance being proportional to a power-law function of frequency, extrapolating this information to the time domain can be complex and less straightforward compared to classical models. CPE impedance does not directly translate to an exponential time response, which is often seen in classical circuit elements like resistors and capacitors. Instead, CPE impedance varies with frequency according to a power-law relationship, leading to a non-exponential time response. Anyway, the CPE models are widely used mainly for the estimation of the remaining useful life [39], [40], [41].

Therefore, the main contributions of this paper are as follows:

- To introduce a novel equivalent electrical model for HSCs, evaluating the performance that can be achieved despite their strong nonlinear behavior.
- To propose a model based on extensive EIS campaign measurements under various temperature and SoC conditions instead of time domain measurements.
- To provide a systematic procedure for the identification of equivalent electrical models. To demonstrate the generality of the proposed approach, it has been used to derive both integer order and fractional order models.

This manuscript is organized as follows. In Section II, the proposed codification strategy is shown, describing in detail how to obtain a matrix representation of a generic network. In Section III, the considered equivalent circuits and the optimization procedure adopted to identify the component values are presented. In Section IV, the EIS measurement setup and the collected experimental dataset are described. Section V presents the results of the equivalent circuit identification procedure, both for the integer and fractional order models, comparing the performance of the two solutions in modelling the HSC impedance. Finally, section VI concludes, providing some hints for future studies.

II. PROPOSED ENCODING FOR A GENERIC IMPEDANCE NETWORK

In this section, the methodology used to encode a generic impedance network, both of fractional and integer order, is described in detail.

Three levels of information are required to describe any equivalent electrical circuit: the topology, the components, and the parameters, as shown in Fig. 3.

The topology defines the structure of the network, i.e. the sequence of series and/or parallels connections of the model components., which define the type of impedances that are used. These can be of integer order, such as resistors, inductances and capacitances, or of fractional order such as CPE or Warburg elements. Finally, parameters define the numerical values of each component.
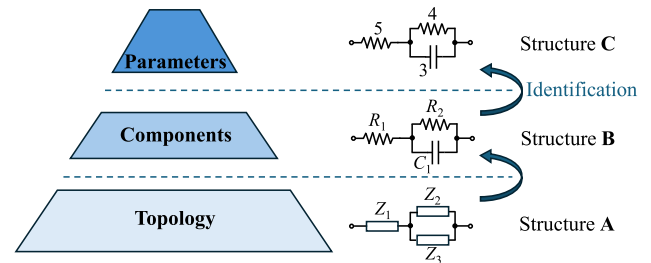

FIGURE 3. Levels of information required to describe an equivalent circuit.

Topology, components, and parameters must be accessible in the form of a codified structure if an optimization approach must be used for identification. Several approaches can be found in the literature to describe a circuit, however, only a few of them use a numerical structure that can be accessed directly from an optimization algorithm.

The approach proposed in this work defines the equivalent circuit topology, components and parameters using a tree diagram, described by three structures plus a fourth structure used to store the actual values of impedance for each frequency.

The principle of operation is shown in Fig. 4.

Given a generic circuit accessible from two terminals, as shown in Fig. 4(a), a tree representation can be associated to it, as in Fig. 4(b). The tree diagram consists of main *branches* (in black) that end on elements called *leaves*. This tree representation is particularly advantageous because it allows for an easy and automatic representation through three structures called **A**, **B** and **C**, as shown in Fig. 4(c), easily managed by an optimization algorithm.

Firstly, the structure **A** is derived. This structure describes the topology of the equivalent circuit and contains the order and the number of operands involved in the series and parallel operations. The procedure required for its derivation is extensively described in Fig. 5.

The second structure, addressed as **B**, contains the operands, which can be either series, parallel, or leaf elements. The procedure for its definition is described in Fig. 6.

Finally, the third structure, addressed as **C**, contains the lumped parameters of the leaf elements. If some elements are defined by more than one parameter, e.g. the constant phase elements, the parameters will be grouped in a vector. The number of elements for each row depends on the number of operations and leaf elements. The procedure for its definition is described in Fig. 7.

All three structure have the same number of rows and the same number of elements per row. Non-null elements in **A** correspond to series or parallel operations, and must correspond, in the same position, to a "+" (series) or "‖" (parallel) element in **B**. On the other hand, null elements in **A** correspond to leaf elements and must correspond to a type of circuit element in **B**. The possible circuit elements considered are summarized in Fig. 8.
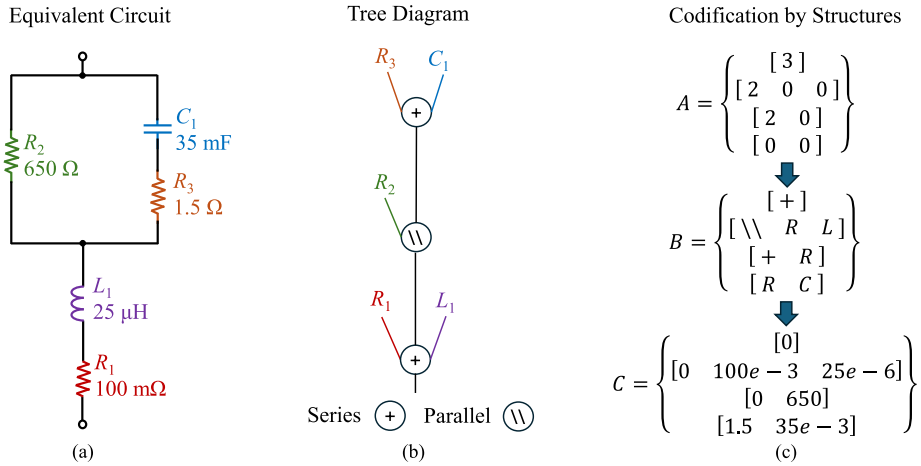
Equivalent Circuit

Tree Diagram

Codification by Structures

$$A = \left\{ \begin{array}{c} [\ 3\ ] \\ [\ 2\ \ 0\ \ 0\ ] \\ [\ 2\ \ 0\ ] \\ [\ 0\ \ 0\ ] \end{array} \right\}$$

$$B = \left\{ \begin{array}{c} [\ +\ ] \\ [\ \backslash\backslash\ \ R\ \ L\ ] \\ [\ +\ \ R\ ] \\ [\ R\ \ C\ ] \end{array} \right\}$$

$$C = \left\{ \begin{array}{c} [0] \\ [0\ \ 100e-3\ \ 25e-6] \\ [0\ \ 650] \\ [1.5\ \ 35e-3] \end{array} \right\}$$

Series (+)   Parallel (\\)

(a)   (b)   (c)

FIGURE 4. Representation of the equivalent circuit. (a) Circuit schematic. (b) Tree diagram representation. (c) Structures representation.

[0 0]: Bifurcations of the Second branch
↳ R_3 has no additional bifurcation, it is a leaf element
↳ C_1 has no additional bifurcation, it is a leaf element

[2 0]: Bifurcations of the Second branch
↳ R_2 has no additional bifurcation, it is a leaf element
↳ The central branch has two further branches (★)

[0 2 0]: Bifurcations of the main branch
↳ R_1 has no additional bifurcation, it is a leaf element
↳ The central branch has two further branches (✕)
↳ L_1 has no additional bifurcation, it is a leaf element

[3]: Number of main branches (•)

$$A = \left\{ \begin{array}{c} [\ 3\ ] \\ [\ 2\ \ 0\ \ 0\ ] \\ [\ 2\ \ 0\ ] \\ [\ 0\ \ 0\ ] \end{array} \right\}$$

FIGURE 5. Procedure for the derivation of structure A.

$$A = \left\{ \begin{array}{c} [\ 3\ ] \\ [\ 2\ \ 0\ \ 0\ ] \\ [\ 2\ \ 0\ ] \\ [\ 0\ \ 0\ ] \end{array} \right\} \Rightarrow B = \left\{ \begin{array}{c} [\ +\ ] \\ [\ \backslash\backslash\ \ R\ \ L\ ] \\ [\ +\ \ R\ ] \\ [\ R\ \ C\ ] \end{array} \right\}$$

The three main branches are in series (+)

First branch is two branches in parallel (\\)
Second branch is a resistance R
Third branch is an inductance L

First branch is two branches in series (+)
Second branch is a resistance R

First branch is a resistance R
Second branch is a capacitance C
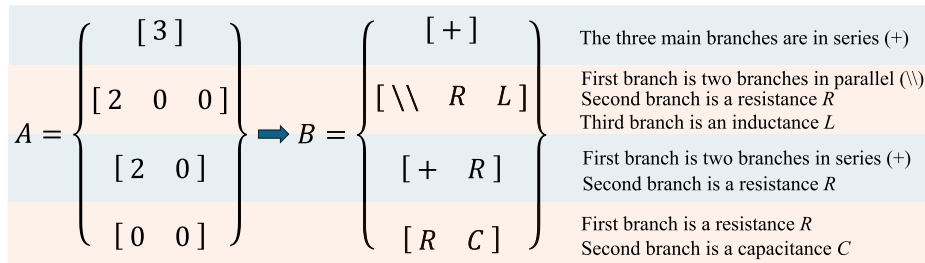
FIGURE 6. Procedure for the derivation of structure B.

$$B = \left\{ \begin{array}{c} [\ +\ ] \\ [\ \backslash\backslash\ \ R\ \ L\ ] \\ [\ +\ \ R\ ] \\ [\ R\ \ C\ ] \end{array} \right\} \Rightarrow C = \left\{ \begin{array}{c} [0] \\ [0\ \ 100e-3\ \ 25e-6] \\ [0\ \ 650] \\ [1.5\ \ 35e-3] \end{array} \right\}$$

$R_1 = 100\ \text{m}\Omega$
$L_1 = 25\ \mu\text{H}$

$R_2 = 650\ \Omega$

$R_3 = 1.5\ \Omega$
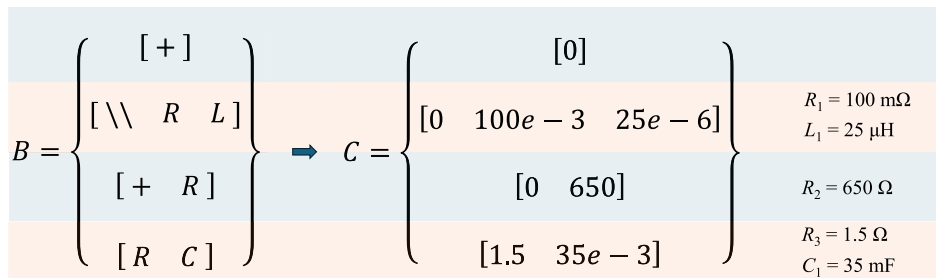$C_1 = 35\ \text{mF}$

FIGURE 7. Procedure for the derivation of structure C.

For the Z_R, Z_C, Z_L elements a single lumped parameter (R, C, L) is present. For the Z_{CPE} element two lumped parameters (Q, n) are present. The Z_W element is a particular case of Z_{CPE} where $n = 0.5$. The Z structure is computed starting

Element	Symbol	Parameters	Equation
Resistance	—⋀⋀⋀—	R	$Z_R(f) = R$
Inductance	—⌒⌒⌒—	L	$Z_L(f) = j2\pi f L$
Capacitance	—||—	C	$Z_C(f) = \dfrac{1}{j2\pi f C}$
Constant Phase Element	—≫—	Q, n	$Z_{CPE}(f) = \dfrac{1}{Q(2\pi f)^n} e^{-jn\frac{\pi}{2}}$
Warburg Element	—⋁⋁—	Q	$Z_W(f) = \dfrac{1}{Q(2\pi f)^{1/2}} e^{-j\frac{\pi}{4}}$

FIGURE 8. Elements for equivalent circuits.
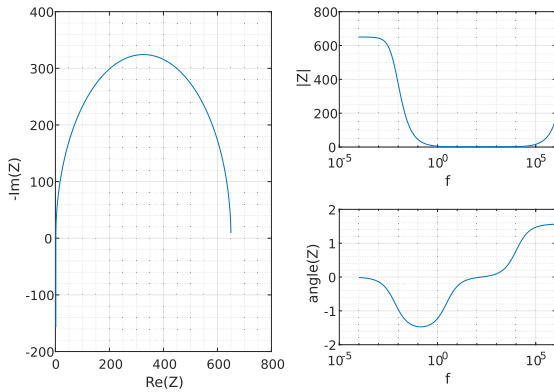
FIGURE 9. Nyquist and Bode plots of an impedance.

from the bottom of the structure (i.e., the one containing only leaf elements) and moving upward. The final impedance value can be found in the upper and leftmost element of Z. The impedance response of the network can be seen in both Nyquist and Bode plots shown in Fig. 9.

To let the circuit have topological meaning, in $\mathbf{A}$, the number of non-zero elements on the k-th row must be equal to the sum of elements in the (k-1)-th row. The last row of $\mathbf{A}$ is composed only of zeroes, since corresponds to the bottom layer of the tree where only leaf elements exist. Through the three structures, the impedance can be calculated starting from the bottom rows toward the top, constructing the impedance of the network progressively. The $\mathbf{Z}$ structure, shown in Fig. 10, has the same shape as $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$, but each element corresponds to a complex vector, containing impedance values at different frequencies. The vector containing the frequencies must be known before impedance analysis.

The representation adopting the $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ structures is extremely useful as it allows for automating the calculation of the impedance of a generic network. In fact, an algorithm able to decode the three structures and to compute the total impedance can be easily developed. In this way, circuit topologies can be tested more quickly by just specifying the associated structure. Using this method, as detailed in the following, five different topologies are investigated as possible equivalent circuits of the HSCs.
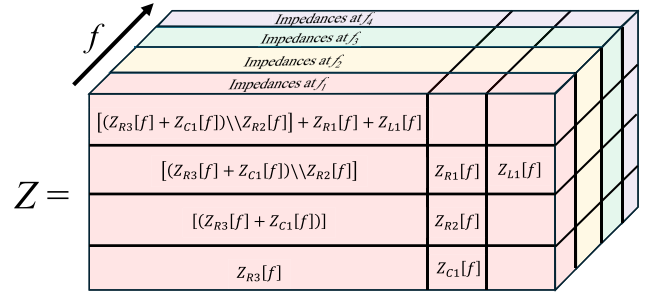
FIGURE 10. Impedance graphical representation.

III. IDENTIFICATION OF THE NETWORK

In this section, a procedure for the identification of the equivalent circuit model for different conditions of SoC and temperature starting from EIS measurements is presented. Two sets of circuit networks are considered, one that includes constant phase elements, and one that contains integer order elements.

1) COST FUNCTION FOR EQUIVALENT NETWORK IDENTIFICATION

The approach just described to compute the impedance Z of a generic network can be used in conjunction with an optimization algorithm to identify the equivalent circuit from a set of experimentally measured impedance values. The problem can be formulated as a least squares (LSQ) problem. Assuming no prior knowledge of topology and circuit values, the problem can be formulated as shown in Eqs. (1-3):

$$\{\mathbf{A}, \mathbf{B}, \mathbf{C}\} = argmin \left\{ \sum_{f=f_1}^{f_{Nf}} r_{Re}[f]^2 + r_{Im}[f]^2 \right\} \quad (1)$$

$$r_{Re}[f] = \frac{Re\{Z_{EXP}[f]\} - Re\{Z_{SIM}[f, \mathbf{A}, \mathbf{B}, \mathbf{C}]\}}{|Z_{EXP}[f]|} \quad (2)$$

$$r_{Im}[f] = \frac{Im\{Z_{EXP}[f]\} - Im\{Z_{SIM}[f, \mathbf{A}, \mathbf{B}, \mathbf{C}]\}}{|Z_{EXP}[f]|} \quad (3)$$

where the cost function to minimize is shown in (1), f is the frequency used to sample the experimental data, belonging to a vector $f = f_1 \ldots f_{Nf}$, $Z_{EXP}[f]$ is the complex experimentally measured impedance at frequency f, $Z_{SIM}[f, \mathbf{A}, \mathbf{B}, \mathbf{C}]$ is the impedance of a network defined by $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$ at frequency f, and $r_{Re}[f]$ and $r_{Im}[f]$ are respectively the real residual and the imaginary residual, normalized to the magnitude of the experimental impedance at that frequency. Such normalization is in general desired to facilitate convergence and steer the fitting process towards achieving better results for more relevant frequencies. Indeed, if the topology of the network is defined, and only the circuit lumped parameters are unknown, the issue can be reduced to the identification of the $\mathbf{C}$ structure solely. On the other hand, if the topology is unknown, all the tree structures can be optimized, as long as $\mathbf{A}$ and $\mathbf{B}$ follow the topological rules described in Section II.
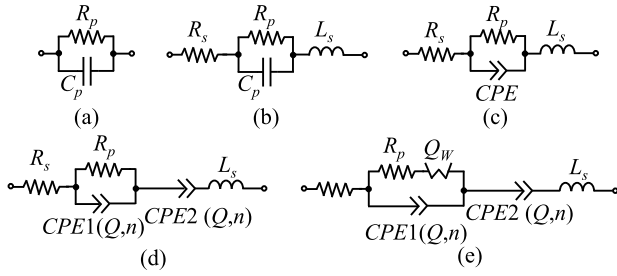
FIGURE 11. Investigated network topologies as possible equivalent circuits for the SCs.

2) OPTIMIZATION ALGORITHM

The identification problem proposed is solved, for this work, through a three-step process. In the first step, the **A** and **B** structures are selected from a predefined set of structures created through observation of the dataset. The networks investigated are shown in Fig. 11.

After selecting the **A** and **B** networks, the **C** structure featuring the lumped parameters is identified using a hybrid optimization strategy. The strategy is composed of the cascade of a Genetic Algorithm (GA) and a deterministic local search algorithm solving the LSQ problem. The GA is initialized with a random population of 40 individuals uniformly distributed in the solution space. The boundaries of the solution space are shown in Table 2.

The stopping criteria of the GA are a tolerance on fitness improvement of 10^{-3} and a maximum number of function evaluations of 2000. The three best individuals of the GA are then selected from the population.

For each individual, a least-squares algorithm based on gradient descent is applied, refining the solutions of the three individuals. The stopping criteria are again fitness improvement of 10^{-4} and a maximum number of function evaluations of 500. Among the three refined solutions, the best one is considered as a solution to the identification problem. With the resulting **C** structure, together with **A** and **B**, the network is completely defined. The strategy flowchart is shown in Fig. 12. The procedure is repeated 50 times to account for bad initialization for the GA, and the best result among the 50 identifications is selected.

3) INTEGER ORDER MODEL

The full model obtained from the identification procedure described above can be useful for several applications, e.g., monitoring device degradation. However, the nonlinear fractional order nature of such a model prevents its inclusion in time-domain circuit simulations (unless a fractional integration approach such as the one shown in [38] is used) and its use for the design of control systems. For this reason, starting from the full network, an integer order network is also derived. Indeed, identification of an integer order model opens several options with different tradeoffs between accuracy, robustness, complexity and synthesizability, including approaches that prioritize the network function identification and then synthesize a suitable network (a notable example
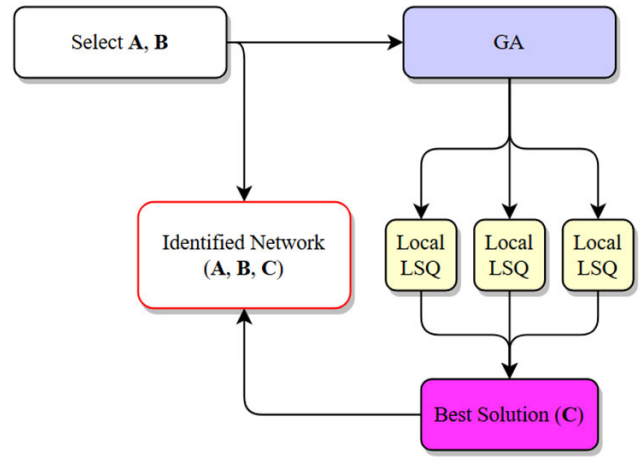

FIGURE 12. Identification procedure flow-chart.

using simple curve-fitting and operational transconductance amplifiers can be found in [42]. In this case, the network is composed of several RC parallel cells in series and a single resistor R_{HF} accounting for high-frequency resistance and is derived from fitting optimally the circuit in a central frequency region where the design of the control loops for typical conversion circuits are designed. This representation is generally referred to as a finite Voigt circuit and is shown in Fig. 13 for M cells.

The process of identifying the R_k and C_k parameters is performed through the distribution of relaxation times (DRT). The process involves the initial definition of a finely spaced vector of time constants $\boldsymbol{\tau} = [\tau_1, \tau_2 \ldots \tau_M]$, each relative to one of the cells of the Voigt circuit. The impedance of each cell then is given by:

$$Z_S[f] = R_{HF} + \sum_{k=1}^{M} \frac{R_k}{1 + j2\pi f R_k C_k}$$
$$= R_{HF} + \sum_{k=1}^{M} \frac{R_k}{1 + j2\pi f \tau_k} \tag{4}$$

Since the τ_k elements are imposed, the R_k terms must be found. For an impedance $Z[f]$ defined on N_f frequencies, and defining $reZ[f]$ and $imZ[f]$ respectively as column vectors containing the real and imaginary part of $Z[f]$, the two concatenated vectors can be indicated as:

$$\mathbf{b} = \begin{bmatrix} Re\{Z(f_1) - R_{HF}\} \\ Re\{Z(f_2) - R_{HF}\} \\ \ldots \\ Re\{Z(f_{Nf}) - R_{HF}\} \\ Im\{Z(f_1)\} \\ Im\{Z(f_2)\} \\ \ldots \\ Im\{Z(f_{Nf})\} \end{bmatrix} \tag{5}$$

Which constitutes the known terms vector of the linear problem to define the R_k terms. The coefficients matrix is

TABLE 2. Boundaries of the solution space for the investigated networks introduced in Fig. 11.

Circuit	$R_P(\Omega)$		$C(F)$		$R_s(\Omega)$		$L_s(\mu H)$		$Q_1(F/s^{n_1})$		n_1		$Q_2(F/s^{n_2})$		n_2		$Q_w(F/\sqrt{s})$	
	lb	ub	lb	ub	lb	ub	lb	ub	lb	ub	lb	ub	lb	ub	lb	ub	lb	ub
(a)	0.001	10	0.001	5000	—	—	—	—	—	—	—	—	—	—	—	—	—	—
(b)	0.001	10	0.001	5000	0.001	10	—	—	—	—	—	—	—	—	—	—	—	—
(c)	0.001	10	0.001	5000	0.001	10	0.001	100	—	—	—	—	—	—	—	—	—	—
(d)	0.001	10	—	—	0.001	10	0.001	100	0	10000	0	1	—	—	—	—	—	—
(e)	0.001	10	—	—	0.001	10	0.001	100	0	10000	0	1	0	10000	0	1	—	—
(f)	0.001	10	—	—	0.001	10	0.001	100	0	10000	0	1	0	10000	0	1	0	10000
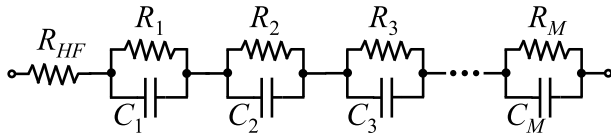
FIGURE 13. Voigt circuit with M parallel RC cells and a single high frequency R_{HF} resistor.

defined by using the following functions:

$$reA(f,\tau) = Re\left\{\frac{1}{1+j2\pi f\tau}\right\}$$

$$imA(f,\tau) = Im\left\{\frac{1}{1+j2\pi f\tau}\right\} \quad (6)$$

And is a $(2*N_f) \times M$ matrix for which each element is given by:

$$\mathbf{A} = \begin{bmatrix} reA(f_1,\tau_1) & .. & reA(f_1,\tau_M) \\ reA(f_2,\tau_1) & .. & reA(f_2,\tau_M) \\ .. & .. & .. \\ reA(f_{Nf},\tau_1) & .. & reA(f_{Nf},\tau_M) \\ imA(f_1,\tau_1) & .. & imA(f_1,\tau_M) \\ imA(f_2,\tau_1) & .. & imA(f_2,\tau_M) \\ .. & .. & .. \\ imA(f_{Nf},\tau_1) & .. & imA(f_{Nf},\tau_M) \end{bmatrix} \quad (7)$$

The problem of determination for the unknowns vector $\mathbf{x} = [R_1, R_2 \ldots R_M]'$ can be formulated as:

$$\mathbf{x} = \mathbf{A}^{-1}\mathbf{b} \quad (8)$$

The obtained $\mathbf{x}$ vector exhibits peaks at time constants corresponding to RC cells that represent the dynamics of the original impedance $Z[f]$. An example of the resulting $\mathbf{x}$ distribution for different time constants is given in Fig. 14 for experimental data.

A number N_{cells} of those time constants can be considered for further identification of the reduced order linearized model, for which the individual C_k and R_k must be identified. Since the solution of (8) is not exact, it is not possible to consider the τ_k as constant and identify solely the resistance or the capacitance. Instead, both the τ_k and the resistance R_k are determined via identification and the C_k capacitance is found by inversion of $\tau_k = R_k C_k$. This approach has two advantages. First, the two variables to be determined (τ_k, R_k) are more similar in scale than a shunt resistance and a capacitance. Second, it is possible to assume sensible guess
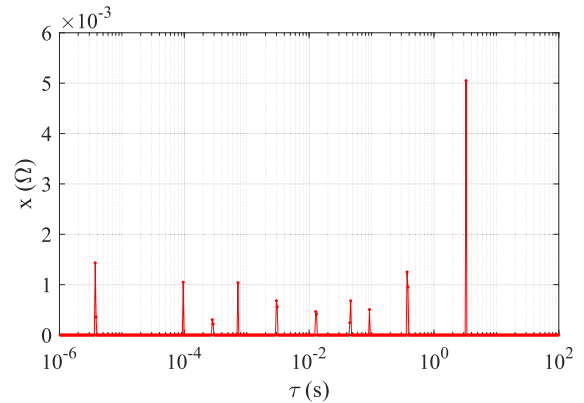

FIGURE 14. Distribution of relaxation times for experimental EIS data, showing peaks at different time constants.

values for the resistance from the pseudo-DC value:

$$R_{DC} = \left(\sum_{k=1}^{N_{cells}} R_k\right) - R_{HF} \quad (9)$$

where the term R_{HF} can be extracted from the high frequency zero-crossing of Nyquist plot for the original Z_{EXP}. Starting from these guess values, the N_{cells} parameters are found through the same cost functions used for the full network identification shown in (2) and (3).

From the identification, the impedance for the integer order model can be expressed as:

$$Z = R_{HF} + \sum_{k=1}^{N_{cells}} \frac{1}{1+sR_kC_k}$$

IV. EXPERIMENTAL MEASUREMENTS FOR DATASET

The HSC considered in this paper is manufactured by Gonghe Electronics. The main characteristics are summarized in Table 3.

The tests carried out on the HSC take into account multiple operating conditions, in terms of different SoC, different operating temperatures and multiple frequencies of investigation. All the operating testing conditions are reported in Table 4.

EIS measurements were conducted starting from a fully charged state (i.e., SoC = 100%), followed by discharging the cell through all SoC conditions. For each SoC condition, EIS measurements were repeated at all eight temperatures, ranging from the coldest to the hottest. Adequate resting periods

TABLE 3. Hybrid Supercapacitor Characteristics according to manufacturer's datasheet [43].

Parameter	Value
Nominal Capacitance C_{nom}	4000 F
Nominal Capacity C_{dis}	4Ah
Maximum Voltage V_{max}	4.2 V
Minimum Voltage V_{min}	3V
Continuous Maximum Current I_{max}^{con}	5 A
Peak Maximum Current I_{max}^{peak}	10 A
Operating Temperature Range T	-20°C, +55°C

TABLE 4. Summary of the multiple operating conditions considered in the dataset.

Operating Temperature	
Range	$-20°C \div 50°C$
Steps	$10°C$
State of Charge	
Range	$0\% \div 100\%$
Steps	10%
Frequency Range	
Range	$1mHz \div 100kHz$
Steps	Logarithmically distributed 10 data points for each decade

after charging/discharging the cell have been guaranteed to ensure standard and consistent conditions of all the tests.

The experimental measurement campaign has been implemented using the customized experimental platform shown in Fig. 15, composed of five major equipment:

- A climatic chamber, to regulate the operating temperature using a PT100 temperature transducer installed in direct contact with the HSC.
- A bi-directional power supply is used to charge and discharge the cell to set the specific SoC condition.
- The Gamry Interface 5000E system is used to carry out the EIS measurements.
- An external and independent data logger equipped with T-type thermocouples used to set safety thresholds.
- A computer with adequate software is used to set the instruments and store the acquired data.

An interesting finding, emerging from such studies, is that the impedance of HSCs is extremely variable depending on these two parameters, as shown in Fig. 16. A more detailed and exhaustive discussion of the experimental campaign, test plan and measurement results is reported in [12], where the DOI resource to download the dataset used in this work is also present.

V. RESULTS
In this section, the identification results for both the fractional order full circuit and the integer order circuit are presented.

A. FRACTIONAL ORDER MODEL
This section presents the results achieved when modelling the behavior of the supercapacitor with the equivalent circuits in Fig. 11. For each equivalent circuit topology, the optimization procedure described in section III-2 is adopted to obtain a
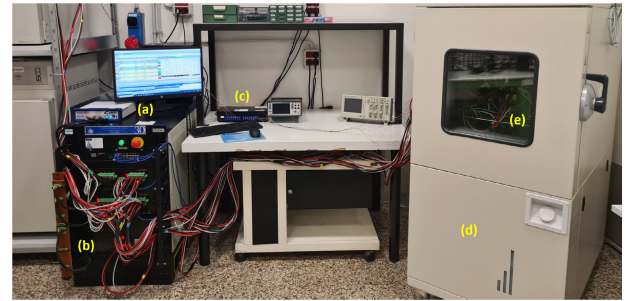
FIGURE 15. Experimental setup for electrochemical spectroscopy measurements, featuring: (a) Gamry interface 5000E, (b) bi-directional power supply, (c) datalogger and thermocouples, (d) climatic chamber, (e) device under test.

different set of component values for each SOC-temperature pair. Fig. 17 displays the squared errors on the real part r_{Re}^2, defined in (2), and on the imaginary part r_{Im}^2, defined in (3), averaged on all the tested SOCs, temperatures and frequencies, as detailed in Table 4. As expected, more complex equivalent circuits achieve better accuracy, with the circuits *(d)* and *(e)* being the most accurate models of the actual supercapacitor. However, it should be noted that introducing the Warburg element in circuit *(e)* does not lead to a relevant improvement of the equivalent circuit model. Therefore, in the following the equivalent circuit *(d)* is taken as the best solution.

Furthermore, for circuit *(d)*, we investigated the sensitivity of the model accuracy to variations of the circuit parameters using a Monte Carlo approach. Such variations may occur mainly due to measurement uncertainty, and, to a lesser extent, due to numerical inaccuracy. Each circuit component was varied following a normal distribution centered on the value identified by the optimization procedure, with gradually increasing levels of perturbation (standard deviation of 1%, 5%, 10% and 20% of the nominal values). For each standard deviation value, 1000 "perturbed" circuits were generated. The result of this analysis is plotted in Fig. 18. It is interesting to notice that the performance of circuit *(d)* becomes comparable to the results achieved by circuit *(c)* only when the uncertainty increases beyond 10% of the optimal component values.

B. INTEGER ORDER MODEL
As explained in section III-3, an integer order model of the HSC can be useful in various power electronics applications, such as time domain simulations and the design of control systems. Therefore, in this section, the strategy presented in III-3 for identifying the time constants of a Voigt circuit is used to establish the minimum number of RC cells capable of approximating the HSC behavior. This is done in a narrowed frequency interval Δf_{Voigt} ranging from 0.1 Hz to 250 kHz, where the supercapacitor impedance exhibits a more regular behavior. This frequency range is selected as it is more interesting for DC-DC conversion applications. As before, the algorithm individuates a different set of time constants
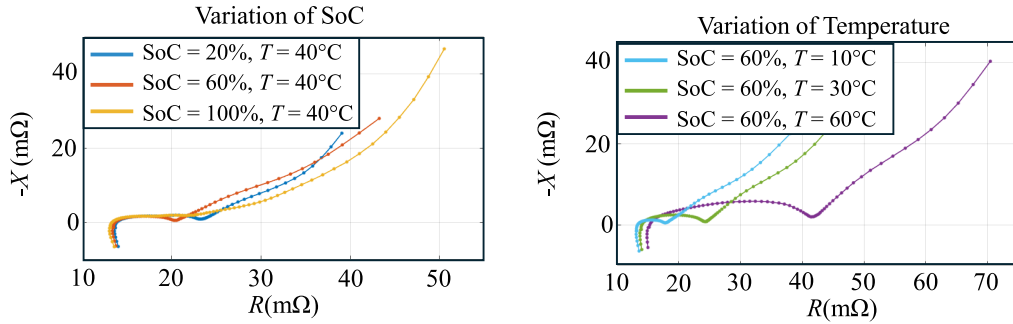
FIGURE 16. Hybrid Supercapacitor impedance variation. (a) Effects of SoC. (b) Effects of temperature.
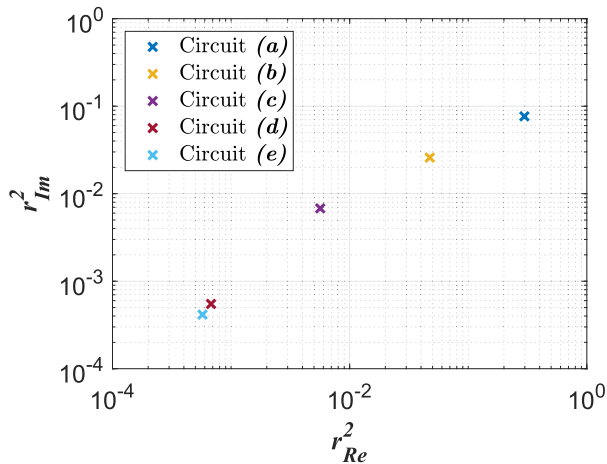

FIGURE 17. Error on real and imaginary parts of the supercapacitor impedance for the five equivalent circuits considered, averaged on all the tested SOCs, temperatures and frequencies.
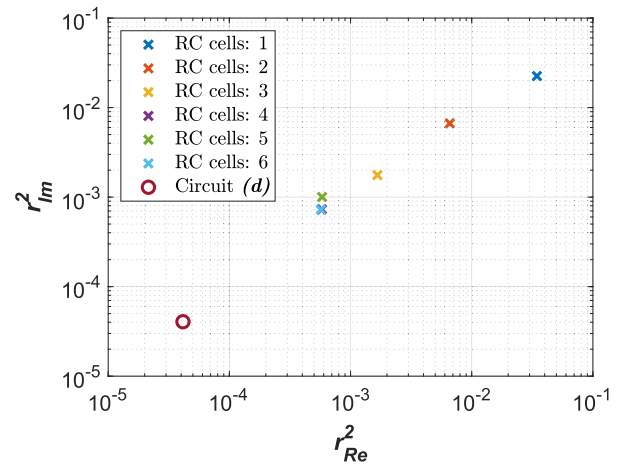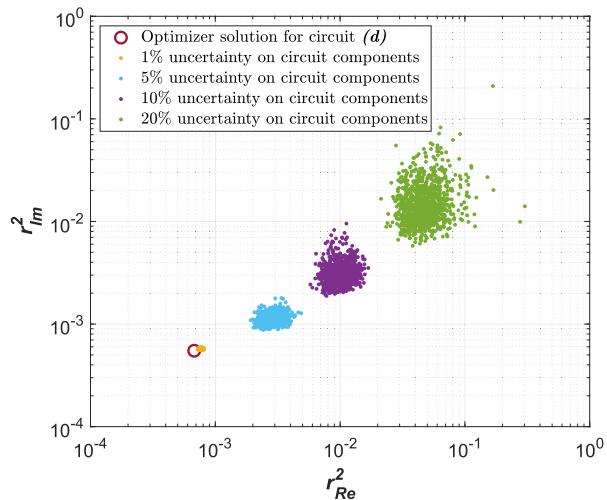

FIGURE 19. Errors on real and imaginary parts of the supercapacitor impedance when approximating the HSC impedance with Voigt circuits, averaged on all the tested SOCs and temperatures, in the reduced frequency range Δf_{Voigt}.

FIGURE 18. Error on real and imaginary parts of the supercapacitor impedance for the equivalent circuit *(d)*, averaged on all the tested SOCs, temperatures and frequencies, with increasing levels of perturbation on the circuit parameters.

Similarly to Fig. 17, Fig. 19 shows the errors r_{Re}^2 and r_{Im}^2, obtained when approximating the HSC as a Voigt circuit with an increasing number of RC elements, from $N_{cells} = 1$ to $N_{cells} = 6$, averaged on all the tested SOCs and temperatures, and in the reduced frequency range Δf_{Voigt}. It is worth noting that increasing the number of RC cells beyond four does not lead to any better approximations. Thus, we conclude that a Voigt circuit with $N_{cells} = 4$ is the best choice. To compare these results with those presented in section V-A, Fig 19 reports also the errors committed by the equivalent circuit *(d)* in the frequency range Δf_{Voigt}.

To visualize how the proposed equivalent circuits approximate the HSC impedance, Figs. 20-23 show the behavior of the equivalent circuit *(d)* and of the Voigt circuit with 4 cells, compared to the experimental data from the actual HSC, in four operating conditions ($T = 30\,°C$, $SOC = 40\%$; $T = 30\,°C$, $SOC = 60\%$; $T = 40\,°C$, $SOC = 40\%$; $T = 40\,°C$, $SOC = 60\%$). We selected these cases as they are representative of the typical working conditions of a medium-charged supercapacitor for photovoltaic applications. In Figs. 20-23, the left plot is the impedance Nyquist plot, the upper right plot is the impedance magnitude, the lower right plot is

for each SOC-temperature pair. The procedure is repeated 50 times and the best result is kept.

TABLE 5. Component values obtained for equivalent circuit *(e)* and for Voigt circuit with $N_{cells} = 4$ in the four operating conditions T = 30 °C, SOC = 40%; T = 30 °C, SOC = 60%; T = 40 °C, SOC = 40%; T = 40 °C, SOC = 60%.

Operating conditions	SOC = 40%, T = 30 °C	SOC = 40%, T = 40 °C	SOC = 60%, T = 30 °C	SOC = 60%, T = 40 °C
Fractional order model - Circuit *(d)*	—	—	—	—
$R_s(\Omega)$	0.013	0.013	0.013	0.013
$R_p(\Omega)$	0.012	0.008	0.011	0.007
$Q_1(F/s^{n_1})$	2.072	1.922	1.339	1.231
n_1	0.508	0.543	0.555	0.589
$Q_2(F/s^{n_2})$	539.31	516.711	386.187	370.699
n_2	0.521	0.504	0.539	0.517
$L_s(nH)$	10.855	10.929	10.214	10.381
Integer order model - $N_{cells} = 4$	—	—	—	—
$R_{HF}(\Omega)$	0.014	0.014	0.014	0.013
$R_1(\Omega)$	0.003	0.003	0.004	0.005
$C_1(F)$	0.024	446.29	0.172	337.91
$R_2(\Omega)$	0.004	0.003	0.003	0.003
$C_2(F)$	0.2	0.302	0.022	0.029
$R_3(\Omega)$	0.004	0.003	0.005	0.001
$C_3(F)$	2.735	0.032	349.931	6.942
$R_4(\Omega)$	0.003	0.002	0.003	0.003
$C_4(F)$	456.44	4.058	2.279	0.289
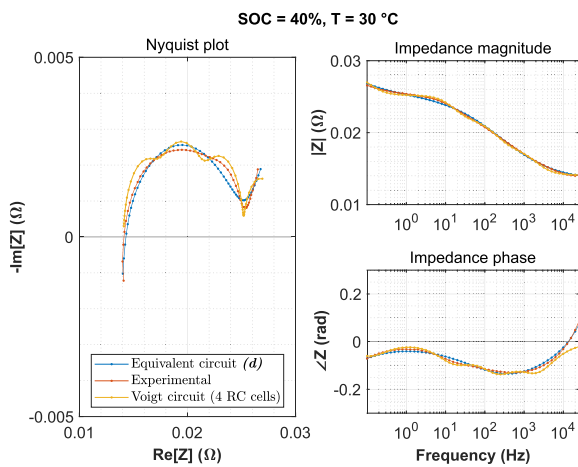
FIGURE 20. Nyquist and Bode plots of the impedance at SoC = 40%, T = 30 °C, . Comparison between experimental measurement (red), integer order Voight model (yellow) and fractional order *(d)* (blue).
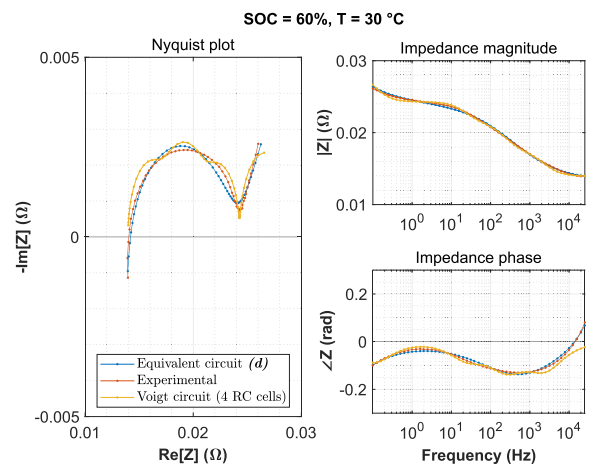

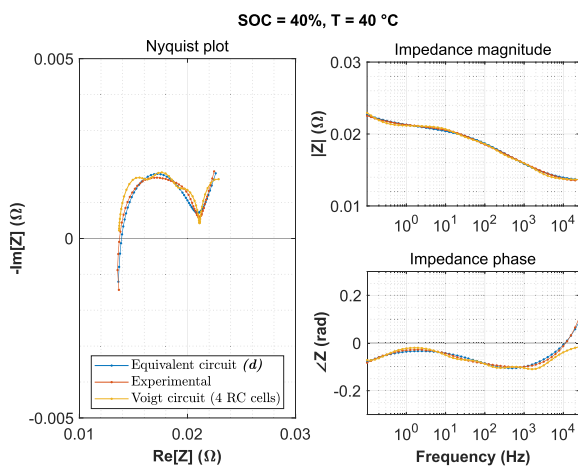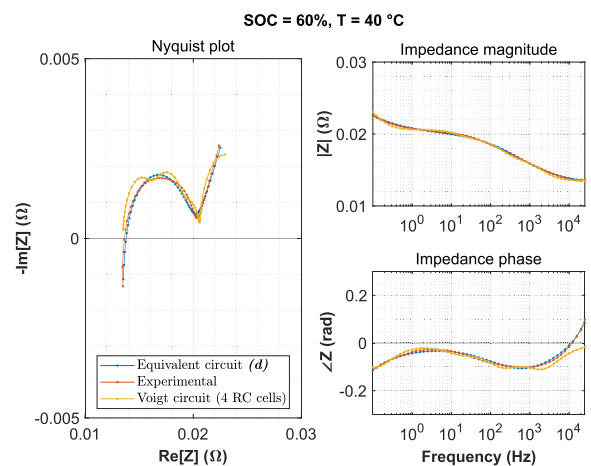**FIGURE 22.** Nyquist and Bode plots of the impedance at SoC = 60%, T = 30 °C. Comparison between experimental measurement (red), integer order Voight model (yellow) and fractional order *(d)* (blue).

FIGURE 21. Nyquist and Bode plots of the impedance at SoC = 40%, T = 40 °C. Comparison between experimental measurement (red), integer order Voight model (yellow) and fractional order *(d)* (blue).

FIGURE 23. Nyquist and Bode plots of the impedance at SoC = 60%, T = 40 °C. Comparison between experimental measurement (red), integer order Voight model (yellow) and fractional order *(d)* (blue).

the impedance phase; the blue, yellow and red curves refer respectively to the equivalent model *(d)*, to the Voigt circuit

with $N_{cells} = 4$, and the experimental data. The equivalent circuit *(d)* impedance accurately follows the one obtained

from the measurements, while the Voigt circuit, according to the results in Fig. 19, is a worse approximation, especially in the phase at the higher frequencies in the considered range.

Table 5 reports the component values obtained for the fractional order circuit (d) and for the Voigt circuit with $N_{cells} = 4$, in the four aforementioned operating conditions. It is worth noticing that, for the fractional order model, the main change happens in the CPE2 component when passing from 40% to 60% SOC, while varying the temperature from 30 °C to 40 °C appears to have a negligible impact on the component values. For the fourth-order Voigt circuit, the algorithm always individuates one capacitance in the range (0.01÷0.1) F, one in the range (0.1÷1) F, one in the range (1÷10) F, and one in the range (10÷1000) F.

VI. CONCLUSION

This paper investigated equivalent circuit modeling of HSCs based on spectroscopy data. An extensive spectroscopy dataset was collected on a supercapacitor manufactured by Gonghe Electronics, varying the operating temperature and the state of charge in a wide frequency range (from 1 mHz to 100 kHz). This dataset was used to individuate an equivalent circuit of the HSC in each operating condition. To validate the potentiality of the proposed approach, both fractional order circuits (i.e., circuits including at least one CPE), and integer order linear circuits (Voigt circuits) have been identified. A two-step optimization algorithm, composed of the cascade of a GA and a least squares optimization, was implemented to individuate the optimal values of the equivalent circuit components best fitting the experimental data. To ease the investigation of a large number of circuits, a matrix representation of a generic impedance network was devised, allowing for the automatic calculation of the equivalent impedance.

The study led to the identification of one fractional order topology and one Voigt circuit capable of modeling the HSC impedance with excellent accuracy. The first equivalent circuit, which includes two CPEs, exhibits the best performance; on the other hand, the integer order model (with four RC cells) achieves slightly worse results but presents the crucial advantage of being easily applicable in time domain simulations.

We foresee three main possible future developments of this work. First, since the creation of EIS dataset can be time-consuming, the investigation of particular charging/ discharging profiles able to extract the same frequency impedance information of EIS for different SoC and temperatures will be investigated. Secondly, more experimental data can be acquired, by testing different HSCs from other manufacturers. In this way, the validity of the individuated equivalent models can be further proved. Finally, the optimization algorithm can be improved for determining not only the component values but the equivalent circuit topology itself (i.e., the structures **A** and **B**). This can lead to a generic workflow, valid not only for the investigation of HSCs, but for individuating automatically the optimal circuit representation of any impedance based on spectroscopy measurements.

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