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RESEARCH ARTICLE

New Interleaved-Input Double Float-Output DC/DC Converter Topology for Battery-Based EVs: Design, Modeling, Analysis and Experimental Implementation

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ABSTRACT Matching between low-voltage high-current capacity battery/fuel cell with high-voltage low-current motors in electric vehicles (EVs) requires paralleling-connection multi-stage power electronic converter with accurate modeling and control system. For high-voltage low-current drives of EVs with high-boosting/bucking gain, single-stage single-arm DC/DC converters suffer from unstable output voltage and the impractical choice of charging/discharging elements. Therefore, a multi-stage multi-arm DC/DC converter is researched to solve the problems of high boosting/bucking gain and minimized the voltage and current ripples. This paper presents parametric sizing, dynamic modeling, and analysis of all logical operational modes for a new high-gain DC/DC converter suitable for deployment in EV applications. The proposed topology composes of three-stage interleaved-input composed of cascaded two stages and double float-output as a third stage with bidirectional current capability. In this study, parametric design, and sizing for the three stages are performed according to the prerequisite ratings. Then, an analysis is conducted on rules of operating the DC/DC converter along with a discussion on considerations taken into account for such a critical design. An investigation of the dynamic behavior of the suggested DC/DC converter is carried out through a state-space model with switches' states. Furthermore, a simulation and measurement-based validation of the derived mathematical models are conducted. The theoretical based analysis, design, and boosting gains are confirmed through a constructed and tested prototype given data on power supply and load utilization. A discussion on the choice of semiconductor equipment and reactive elements is provided for the proposed DC/DC converter. The experimental results show that the three stages can be used in a separate mode or in a cascaded booster.

INDEX TERMS DC-DC converters, double float-output converter, battery pack, voltage regulation, electric vehicles, interleaved boost converter.

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NOMENCLATURE

DC/DC	Direct current/direct current.
D	Duty ratio.
EV	Electric vehicles.

HVM	High voltage AC or DC motors.
IIDFOC	Interleaved-input double-float output converter.
FDBDSB	Floating double-boost double-stage boost converter.
FDIDB	Floating double-interleaved dual boost converter.
FPGA	Field-programmable gate array board.
PWM	Pulse width modulation signals.
n	Number DC/DC boost converters connected in parallel.
T_{sw}	Switching period of the converter.

I. INTRODUCTION

A. MOTIVATION

Usually, electric vehicles (EVs) are driven by high voltage AC or DC motors (HVMs). A high voltage amplification is mandated as batteries and fuel cells are of comparatively high current level output and low voltage level output. Hence, the HVM needs a step-up DC/DC converter for transforming the source voltage to a desired DC-bus voltage and reduced source ripple current [1]. Figure 1 describes a chart for an EV driven by a low voltage battery and high gain boosting converter to feed HVMs. It shows the position of the proposed DC-DC converter for boosting the low battery voltage to a high voltage to feed the DC or AC motors.

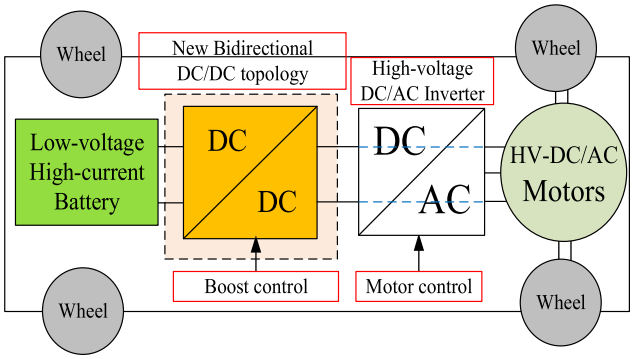


FIGURE 1. Overview of the studied system.

When the power level of the load rises, the consideration of a single-stage power converter is insufficient. Thus, deploying a parallel DC/DC power circuits considering an interleaved method can offer enhanced functionality [2]. The simple boost chopper topology would not have made it possible to respond to the issues identified by the specification drawings in the context of fuel cell and battery applications. Indeed, it has many drawbacks such as: (i) low compactness due to the weight and volumes of the passive elements, (ii) high current ripple, and (iii) sensitivity to faults.

B. LITERATURE SURVEY

Like the proposed converter, the authors in [3], [4], and [5] developed a boost-based high step-up DC/DC converter topology but without the advantages of the cascaded gain and interleaved phases. Also, reference [6] presented how to design, model, and control an isolated DC/DC three-port converter considering an interleaved-boost full-bridge converter. The authors in [7] treated the topology of one stage interleaved DC/DC boost converter of three legs, with H infinity control technique to insure the stability of the system. The paper of [8] has studied a non-isolated interleaved boost topology allowing to boost the voltage from 24V to 480V. However, here with the proposed topology, the voltage can be boosted with a high gain from 20V to 600V and the current could be managed as bidirectional flow. The study of [9] has addressed the converter topology based on isolated buck-boost with single stage power convergence. In this structure, a high-frequency bridgeless-interleaved boost rectifier is suggested for a voltage output of 380V. In [10], a topology of interleaved converter based on a zero-voltage switching-zero-current switching is studied. In this topology, only one stage interleaved DC/DC boost converter with two legs was adopted. The suggested structure was validated on prototype for output voltage of 1.2kW. Authors in [11] have presented an interleaved converter based on three-input DC/DC boost converter (two sources and battery within them as storage device). The suggested topology has a single stage with two legs to able to step up the output voltage until 350V.

Numerous converter configurations are introduced in the literature. The switched capacitor based multistage step-down converter was introduced in [12]. Such a converter does not serve as a sufficient remedy for the power train when targeting fuel cell applications. Nevertheless, the converter is useful in driving the low voltage deluxe vehicles' loads. In [13], a triple-switch-triple-mode high step-up converter was presented with an extended range of duty cycle through the incorporation of an extra switch in the circuit of the converter. In this reference, a high voltage conversion ratio was attained excluding the use of a transformer, coupled inductor, and multiple stages of switched capacitors. However, this topology was experimentally tested at small power ratings of 100W and 500W. Moreover, no interleaved phases produce high ripples in the input currents. In [14], a four-phase interleaved buck-boost converter was analyzed and designed with modified load connection to activate the fuel cell. Although this converter was implemented for high current applications, the prototype was only tested in buck mode with low voltage gain. Also, a three-phase interleaved DC/DC boost converter was shown in [15]. However, this work focused only on designing an online integral reinforcement learning based data-driven control method for a single-stage low-gain DC/DC converter. The authors in [16] proposed an interleaved high step-up DC/DC converter with coupled inductor and built-in transformer when renewable energy is used. In this reference, two double-winding and one triple-winding are combined with a switched-capacitor voltage multiplier cells to attain a high-voltage gains in the absence of extreme duty cycles. However, existing two more degrees of freedom -in addition to duty cycle- leads to big challenge in control stage. Moreover, in that reference, the one stage DC/DC

converter is implemented in very low power rating (40W-200W) with a voltage deviation from the ideally calculated values that is a result of the circuit's parasitic elements. Another effort was made in [17] to introduce a three-phase interleaved buck-boost converter with a reduction in power electronics. However, the converter was implemented with maximum voltage gain of 3 in a low power rating of 375W.

To overcome the above-mentioned drawbacks, a series of multi-cellular topologies with paralleling of phases and cascaded stages of interleaved boost converters has been suggested and researched. Regarding this topic, several converter topologies have been investigated for different applications. Reference [18] presents a simple multiphase interleaved boost fuel cell (FC) converter for relevant applications of DC microgrids. Cascaded stages interleaved and/or floating-output DC/DC converter topologies were investigated for increasing the voltage gain and improving the current/voltage shapes. Two DC/DC stages (interleaved boost converter with reduced input current ripple and a series resonant converter) were presented in [19]. In which, by analytic investigation, a pre-estimation of the converter's efficiency was shown and a method for calculating the current ripple of multi-phase interleaved converters was presented. Other topologies of two floating type high-gain transformer-less boost converter topologies, including floating double-interleaved dual boost (FDIDB) converter and floating double boost double stage boost (FDBDSB) converter, have been presented in [20]. Also, reference [21] has analyzed, designed, and presented key converter waveforms operating in the continuous conduction mode of an interleaved boost-derived converter topology. A two-phase interleaved DC/DC converter of [22] was used to control the DC-bus voltage in a permanent magnet synchronous motor (PMSM) drive system.

The operation has incorporated three modes, i.e., buck, boost, and regenerative buck modes of operation. Two-leg interleaved bidirectional front-end DC/DC buck–boost converter was controlled with a three-phase inverter for driving PMSM in [23]. In depth analysis on the rating, designing the components of the circuit and appropriately controlling the interleaved converter were conducted. Moreover, a robust voltage tracking error cancelation controller was set. The control of the four phases interleaved boost converter was made through an artificial neural network controller in [24] to assure the output voltage level at the targeted reference value when inputs parameters of the FC (e.g., fuel flow rate, the pressure, the air supply pressure, and the temperature of the working environment) are strongly fluctuating.

Various configurations of the converter have been studied given the multiple boosting stages with no transformer and coupled inductors. The efforts of the researchers continued to survey several topologies of DC/DC non-isolated in [25] for unidirectional power flow in fuel cell-based vehicles. The design of DC/DC multistage power converter topologies with many boosting stages together with conventional DC/DC converter for satisfying the high voltage load demand and enhancing the reliability, efficiency and attaining small size of the system has been shown in [25].

Multi-stage interleaved DC/DC converters could be efficiently used for connecting the EVs to the grid with the availability of charge and discharge operations. In the literature, the authors in [26] proposed a robust game-theoretic approach to optimize the BESS capacity and energy consumption for multi-microgrid considering the uncertainty of PV-WT generation. The main contribution was to predict the charging and discharging power of the battery and, therefore, a Markov Decision Process model of random variables was established and then, a robust game-theoretic optimization model was established for MMG's economical operation by considering the renewable based DGs uncertainty. In [27], managed charging and vehicle-to-grid (V2G) scenarios are proposed to evaluate the system reliability concerning the stochastic modeling of PHEVs, renewable resources, availability of devices, etc. with bidirectional-power-conversion technologies.

C. CONTRIBUTION OF THE PAPER

This paper presented a suggested DC/DC converter applicable for FC/battery hybrid EVs, considering an interleaved and cascaded structure. The paper presented the following contributions:

- Design the proposed converter with analyzing its characteristics, operating modes and analyzed them in detail along with modelling the system under study.
- All the published research efforts assumed a fluctuation-free input voltage wave even from a battery or fuel cell modules. On the contrary, the suggested converter topology has considered the variation of input voltage.
- The suggested converter has the below merits for EVs applications fed by battery/FC:
  - ✓ Sharing of high input currents produced by input interleaved stage.
  - ✓ Sharing of high output voltage produced by output double float stage.
  - ✓ Redundancy of current paths and voltage terminals.
  - ✓ Minimizing of the input current and output voltage fluctuations.

The content structure of this paper is as follows: a functional study as well as a very detailed description of the proposed topology content are presented in section II. Then, in section III, the different theoretical parts (modes of operation) will be studied. Finally, in section IV, simulations and implementation based on experiment are presented for validating the dynamic and steady state behavior of the proposed DC/DC converter.

II. DESIGN OF INTERLEAVED-INPUT DOUBLE FLOAT-OUTPUT DC/DC CONVERTER TOPOLOGY

A. CONCEPT OF INTERLEAVED CONVERTERS

The interleaving concept for this converter is made of a connection of a number n of DC/DC boost converters connected in parallel and in share of the same common output DC bus

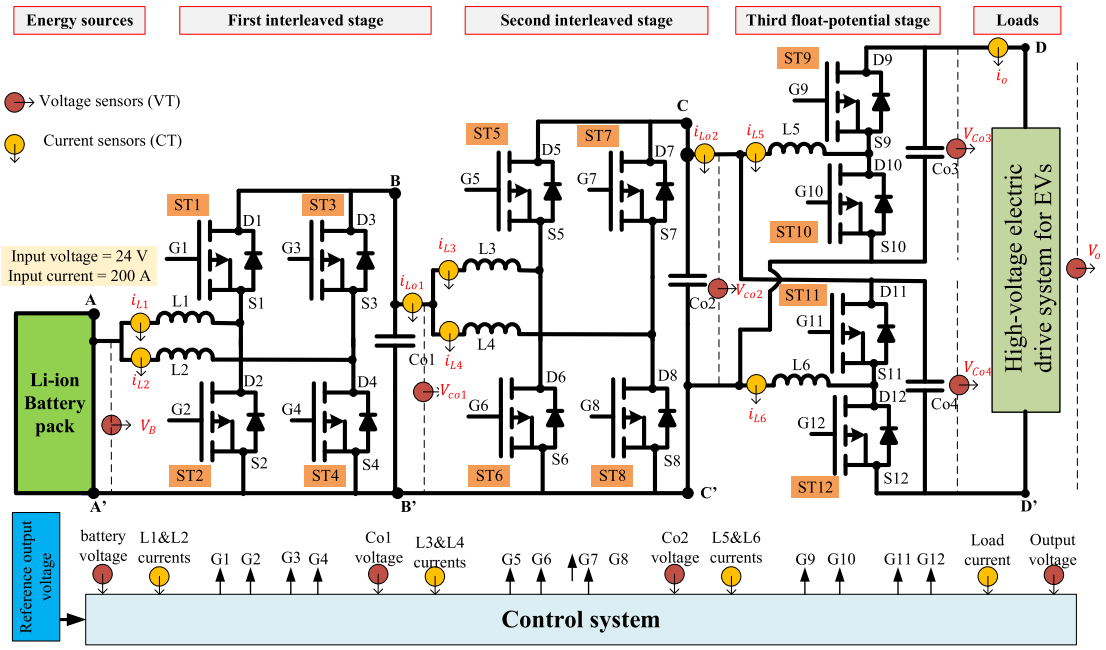


FIGURE 2. Topology of the suggested three-stage DC/DC converter.

TABLE 1. Given values of the proposed 4.8 kW DC/DC converter.

Li-ion battery pack	1st Interleaved converter	2nd Interleaved converter	3rd Float converter
Open-circuit voltage, $\bar{V}_B = 24V$	Output voltage, $\bar{V}_{co1} = 90\ V$	Output voltage $\bar{V}_{co2} = 250\ V$	Output voltage $\bar{V}_o = 600\ V$
Input current $\bar{I}_B = 200A$	Output current $\bar{I}_{o1} = 44.44A$.	Output current $\bar{I}_{o2} = 16A$	Load current $\bar{I}_L = \bar{I}_o = 6.78A$
Energy = (7*3.2V) (2*40Ah) =1792Wh.	Efficiency $\eta_1 = 91\%$.	Efficiency $\eta_2 = 95\%$	Efficiency $\eta_3 = 97\%$
$P_B = 4.8$ kW	P_{o1}= 4370 W	P_{o2}= 4150 W	P_o= 4000 W

to distribute the current on n arms. This interleaving allows splitting the high input current in parallel and consequently reducing the costly and volumetric inductances and wires. In one concern, to respect the rules of interconnection of sources, it is imperative to shift the orders of control of the power switches according to the number of converter arms. The offset is equal at T_{sw}/n where T_{sw} represents the switching period of the converter and n represents the number of arms in the DC/DC converter.

This interleaved boost topology has many advantages over a simple boost chopper topology: (1) the size and volume of the passive elements are reduced, (2) the input current ripple is largely attenuated, and it can even be cancelled for a certain value of duty cycle, (3) the frequency of the input current ripple is raised, (4) the converter is modular and thus, enhancing the system reliability as a matter of the availability of a degree of freedom and increasing the power of converter thanks to phases' parallel connection, (5) thermal management is easy i.e., a better thermal distribution, (6) phase paralleling allows to reduce the fluctuation of the source current, and (7) finally, this topology offers the possibility of achieving high power with standard components of lower caliber. This therefore also makes it possible to reduce design costs.

B. STRUCTURE OF A NEW CONVERTER TOPOLOGY WITH HIGH TRANSFORMATION RATIO

The structure of the new interleaved-input double-float output DC/DC converter (IIDFOC) is demonstrated in Fig. 2. It shows the circuit topology of the three-stage DC/DC converter with interleaved input-parallel at the first and second stages and float output-double connection at the third stage. This topology allows a bidirectional current flow in regenerative mode to recharge the battery or supercapacitor. It is designed for a very high transformation ratio DC/DC boost converter for fuel cell/battery or supercapacitor applications.

Static converters used in battery systems are subject to many constraints. This converter, therefore, meets stringent specifications in terms of compactness, current ripple, transformation ratio, and energy performance. Indeed, to optimize the life and performance of the battery, it is essential to ensure a current with as little ripple as possible. For this, the inductors of the converter have been judiciously dimensioned to respond to this problem. The current constraints on the power components of the assembly are enormous due to the low 24V input voltage for an active power of 4.8kW. This corresponds to a current of 200A passing through the input of the first interleaved boost converter. For the sake of reducing the size

of the components and the space between them, a multi-stage topology of interconnected converters was retained.

The interleaving notion is assured through connecting in parallel the two modules at the input side and phase shifted control of (S_{T2} and S_{T4}) switches and (S_{T6} and S_{T8}) switches for 1st and 2nd stages, respectively. High voltage gain is attained through connecting in-series the two modules at the output side. The input source of the third stage (voltage across capacitor C_{o2}) is as well always in in-series connection with (Co_3 and Co_4). Considering the in-series connection at the output side leads to a reduction in the whole output voltage ripple. This last merit promotes this topology to be the last stage of the presented converter.

The first stage includes an input voltage source V_B, two inductors L_1, L_2, four switches $S_{T1}, S_{T2}, S_{T3}, S_{T4}$ four diodes D1, D2, D3, D4 and DC link capacitors C_1. Second stage includes an input voltage source Vco1, two inductors L_3, L_4, four switches S_{T5}, S_{T6}, S_{T7}, S_{T8} four diodes D_5, D_6, D_7, D_8 and DC link capacitor C_2. Third stage includes an input voltage source V_{co2}, two inductors L_5, L_6, four switches S_{T9}, S_{T10}, S_{T11}, S_{T12} four diodes D_9, D_{10}, D_{11}, D_{12} and two DC link capacitors C_3 and C_4 and an equivalent load resistor R_L.

The new topology has the following benefits: (1) two arms: to decrease the ratings, decrease the ripples, duplicates the switching frequency for the same modulator, and provides redundant paths; (2) three-stage: to provide a very high voltage gain, lower ratings, and low relatively overall price; (3) bidirectional: for achieving regenerative braking, buck and boost operations; (4) multi devices: causes lower rating of power switches and redundant at high current side; and (5) float potential: gives benefits containing interleaving besides larger gain value for the whole converter; and furthermore, reduces voltage constraints at the level of power switches.

C. DESIGN, RATINGS, AND SYSTEM VARIABLES

Table 1 lists the input rating as well as the output rating of the proposed DC/DC converter. The design is based on the given power rating in the table i.e., overall efficiency is considered as 84 %.

1) INTERLEAVED (STAGE 1)

According to the given data in Table 1, the set values of $\bar{V}_B = 24V$, $\bar{V}_{co1} = 90V$, current fluctuation in each inductor is set at $\Delta\bar{I}_{L12} = 20A$, $\eta_1 = 91\%$, $\bar{P}_{o1} = 4.37kW$, $\bar{I}_B = 200A$, $\bar{I}_{L1} = \bar{I}_{L2} = 100A$, and switching frequency of $F_{sw} = 10kHz$ are used to determine the minimum value of inductances and capacitances. To allow both boost and buck converters all operating under continuous current mode (CCM) with common energy storage inductor, the minimum value of the duty should be set as

$$\bar{D}_1 = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{\bar{V}_B}{\bar{V}_{co1}} = 1 - \frac{24}{90} = 0.73. \quad (1)$$

According to the selected duty, the inductances of the coils of

$$L_1 = L_2 = \frac{\bar{V}_B\bar{D}_1}{\Delta\bar{I}_{L12}F_{sw}} = \frac{24 \times 0.73}{20x10^4} \cong 80\mu H \quad (2)$$

are chosen and it is installed in the setup system. For the same given set values, the equivalent load resistance of $R_{Lo1} = \frac{\bar{V}_{co1}^2}{\bar{P}_{o1}} = \frac{90^2}{4370} = 1.85\Omega$ could be applied at the terminals B1B2 of first stage. Then, the equivalent capacitor is selected with a deviation 5% of output voltage i.e., $\Delta\bar{V}_{co1} = 4.6V$ as

$$C_{o1} = \frac{\bar{V}_{co1}\bar{D}_1}{\Delta\bar{V}_{co1}R_{dc}F_{sw}} = \frac{90 \times 0.73}{4.6 \times 1.85 \times 10^4} = 770\mu F. \quad (3)$$

In the setup system, three capacitors with $C_{11} = C_{12} = C_{13} = \frac{C_{o1}}{3} \cong 260\mu F$ are installed in parallel.

2) INTERLEAVED (STAGE 2)

By the same way, according to the given data in Table 1, the specified and considered values of input voltage $\bar{V}_{co1} = 90V$, output voltage $\bar{V}_{co2} = 250V$, current fluctuation $\Delta\bar{i}_{L34} = 26$ of input current, $\eta_2 = 95\%$, output power $\bar{P}_{o2} = 4.15k$, $\bar{I}_{L3} = \bar{I}_{L4} = 22.22A$, and switching frequency $F_{sw} = 10kHz$ are used to determine the inductances for the second stage. To allow the boost converter as well as the buck converter operate under the CCM with common storage inductor, the minimum value of the duty should be set as

$$\bar{D}_2 = 1 - \frac{\bar{V}_{co1}}{\bar{V}_{co2}} = 1 - \frac{90}{250} = 0.64 \quad (4)$$

According to the selected duty, the inductance of the coil of

$$L_3 = L_4 = \frac{\bar{V}_{co1}\bar{D}_2}{\Delta\bar{I}_{L34}F_{sw}} = \frac{90 \times 0.64}{26 \times 10^4} \cong 220\mu H \quad (5)$$

is chosen. From simulations, $\Delta i_{L3} = \Delta i_{L4} \cong 50\%$ of the inductor current is observed. For the same given ratings, the second stage equivalent load resistance of $R_{Lo2} = \frac{\bar{V}_{co2}^2}{\bar{P}_{o2}} = \frac{250^2}{4150} = 15.06\Omega$. Then, the equivalent capacitor is determined in this design, $\Delta\bar{V}_{co2} = 2$ V is considered.

$$C_{o2} = \frac{\bar{V}_{co2}\bar{D}_2}{\Delta\bar{V}_{co2}R_{Lo2}F_{sw}} = \frac{250 \times 0.64}{2 \times 15.06 \times 10^4} = 512\mu F. \quad (6)$$

In the setup, two capacitors with $C_{21} = C_{22} = \frac{C_{o2}}{2} \cong 260\mu$ are installed in parallel.

3) FLOAT (STAGE 3)

In float potential double boosting stage, the current and voltage ripples are chosen by same way in [28]. In this structure, the input voltage $\bar{V}_{co2}$ equals to 250 V and the output voltage $\bar{V}_o$ equals to 600 V and $\eta_3 = 97\%$. Therefore, for the given input and output voltages, the duty is estimated as (7). In all modes of operation, both capacitors are placed in series connection with the voltage source. The voltage across capacitors is expressed as in terms of input and output voltages as $\bar{V}_{co3} + \bar{V}_{co4} = \bar{V}_o + \bar{V}_{co2} = 600 + 250 = 850V$. So, the voltage across each capacitor is set as $\bar{V}_{co3} = \bar{V}_{co4} = 425V$.

$$\bar{D}_3 = 1 - \frac{\bar{V}_{co2}}{\bar{V}_{Co3}} = 1 - \frac{250}{425} = 0.41.$$

$$\bar{D}_4 = 1 - \frac{\bar{V}_{co2}}{\bar{V}_{Co4}} = 1 - \frac{250}{425} = 0.41. \quad (7)$$

By referring to Fig. 1 and considering the Kirchhoff's current law at the input side and, one has $\bar{I}_{L6} = \bar{I}_0 + \bar{I}_1$ and $\bar{I}_{Lo1} = \bar{I}_{L5} + \bar{I}_1$. Then the input current is $\bar{I}_{Lo1} = \bar{I}_{L5} + \bar{I}_{L5} - \bar{I}_0$. Therefore, the current of each inductor is $\bar{I}_{L5} = \bar{I}_{L5} = \frac{1}{2}\left(\bar{I}_{Lo1} + \bar{I}_0\right) = \frac{1}{2}(16 + 6.667) = 11.33A$. Current fluctuation in these inductors is taken as $\Delta\bar{I}_{L5} = \Delta\bar{I}_{L6} = 10\text{A}$. The equivalent capacitor is selected with a deviation 1% of output voltage i.e., $\Delta\bar{V}_o = 6V$ When the duty ratio $\bar{D}_3 = \bar{D}_4 (= 0.41) < 0.5$, the inductors and capacitor are calculated as (8) and (9) respectively.

$$L_5 = L_6 = \frac{2(\bar{V}_o - \bar{V}_{co2})(0.5 - \bar{D}_3)}{\Delta\bar{I}_{L5}F_{sw}} = \frac{2 \times (600 - 250)(0.5 - 0.41)}{10{\times}10^4} \cong 700\mu H \tag{8}$$

$$C_{o3} = \frac{2\bar{I}_o\bar{D}_3(0.5 - \bar{D}_3)}{\Delta\bar{V}_{co3}F_{sw}} = \frac{2 \times 6.667 \times 0.41(0.5 - 0.41)}{6{\times}10^4} \cong 8\mu F.$$

$$C_{o4} = \frac{2I_o\bar{D}_4(0.5 - \bar{D}_4)}{\Delta\bar{V}_{co4}F_{sw}} = \frac{2 \times 6.667 \times 0.41(0.5 - 0.41)}{6{\times}10^4} \cong 8\mu F. \tag{9}$$

Four capacitors with minimum capacitances of $C_{31} = C_{32} = \frac{C_{o3}}{2} = 4\mu F$, and $C_{41} = C_{42} = \frac{C_{o4}}{2} = 4\mu F$ are connected in the floated output such that each two capacitors are in parallel. Load equivalent resistance is $R_L = \frac{V_o^2}{P_o} = \frac{600^2}{4000} = 90\Omega$. However, in experimental installation and in simulations, four capacitors with $260\mu F$ are fixed (each two in parallel) and four inductors are fixed (each two in series) to give $L_5 = L_6 = 724\mu H$, as demonstrated in Table 2.

TABLE 2. Specifications of the suggested DC/DC converter.

Element	Stage 1	Stage 2	Stage 3	Unit
Inductors	$L_1 = L_2 = 80$	$L_3 = L_4 = 220$	$L_5 = L_6 = 724$	μH
	$r_{L1} = r_{L2} = 0.01$	$r_{L3} = r_{L4} = 0.01$	$r_{L5} = r_{L6} = 1.2$	Ω
Capacitors	$C_{11} = C_{12} = C_{13} = 260$	$C_{21} = C_{22} = 260$	$C_{31} = C_{32} = C_{41} = C_{42} = 260$	μF

D. INPUT CURRENT RIPPLE

1) BOOST INTERLEAVED STAGES 1 AND 2

In a single-phase DC/DC converter, inductor current ripples match and can be observed with the boost converter mode and duty ratio D as (10) [23].

$$\Delta i_{L_{in-1}} = \frac{V_{in}D}{L_{in}F_{sw}} = \frac{V_oD(1 - D)}{L_{in}F_{sw}} \tag{10}$$

The maximum value of the result in (10) takes place at $D = 0.5$ as

$$\Delta i_{L_{in-1-max}} = \frac{V_o}{4L_{in}F_{sw}}. \tag{11}$$

Per unit trend of inductor current ripples as a function of D can be defined by

$$\Delta i_{L_{in-1-pu}} = \frac{\Delta i_{L_{in-1}}}{\Delta i_{L_{in-1-max}}}, \tag{12}$$

and it is provided in Fig. 3 by a solid line. Through the deployment of the interleaving method, another current ripple ratio should be defined. Equation (13) provides a description of the ratio of the current ripple in a converter with N phases $\Delta i_{L_{in-N}}$ and a single-phase converter's current ripple $\Delta i_{L_{in-1}}$, [19]:

$$F_{L_{in-N}} = \frac{\Delta i_{L_{in-N}}}{\Delta i_{L_{in-1}}} = \frac{(ND - (x - 1))\,(x - ND)}{ND\,(1\text{-}D)}, \tag{13}$$

where $\frac{x-1}{N} < D < \frac{x}{N}, x = 1, 2, \ldots, N$. For $N = 2$ to $N = 4$, the behavior of $F_{L_{in-N}}$ is given in Fig. 4.

The resulting current ripple in multiple phases interleaved boost converter $\Delta i_{L_{in-N}}$ is

$$\Delta i_{L_{in-N}} = \Delta i_{L_{in-1}} \frac{F_{L_{in-N}}}{N}. \tag{14}$$

Per unit trend of inductor current ripples as a function of D as a percentage of the ripple via an inductance is defined by

$$\Delta i_{L_{in-N-pu}} = \frac{\Delta i_{L_{in-N}}}{\Delta i_{L_{in-1-max}}}. \tag{15}$$

It is observed on the graph, shown in Fig. 3, that for a DC/DC converter with two arms, there is one point for canceling current ripple i.e., when duty cycle $D = 0.5$. It is observed, by comparing with simple chopper, that the current ripple for multi-arm converters is attenuated regardless of the duty cycle except for extreme values (<0.1 or >0.9).

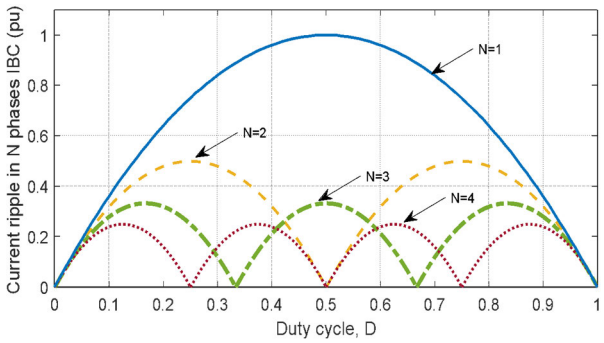


FIGURE 3. Input current ripple versus duty cycle for *N* arms.

2) BOOST FLOAT-POTENTIAL STAGE 3

There are interesting observations about operating points relevant to the duty cycles (D = 0.25, 0.50 and 0.75) for four arms with float output, whereas there are other interesting duty values of 0.33 and 0.67 in case of three arms. In our case, i.e., two arms, the input current ripple of the converter does not exist as per the theory and as demonstrated in Fig. 3 at D = 0.5. When the duty ratio is less than 50% (D< 0.5),

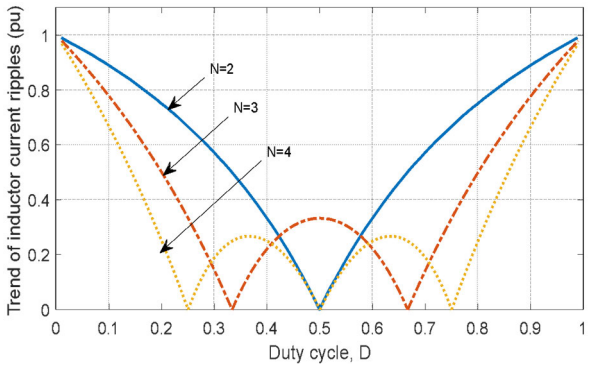


FIGURE 4. Input current ripple versus duty cycle as a percentage of ripple via an inductance.

ripples of input current and output voltage are calculated by (16) and (17) respectively.

$$\Delta i_{in} = \frac{2(V_c - V_{in})(0.5 - D)}{L_{in} F_{sw}} \tag{16}$$

$$\Delta V_o = \frac{2 I_o D(0.5 - D)}{C_o F_{sw}} \tag{17}$$

whereas the moment D >0.5, ripples of both the input current and output voltage would be calculated as shown in Eq. (18) and Eq. (19), respectively.

$$\Delta i_{in} = \frac{2 V_{in}(D - 0.5)}{L_{in} F_{sw}} \tag{18}$$

$$\Delta V_o = \frac{2 I_o (D - 0.5)}{C_o F_{sw}} \tag{19}$$

III. OPERATIONAL MODES OF AN INTERCONNECTED THREE-STAGE DC/DC CONVERTER TOPOLOGY

This section presents the dynamic model of a suggested three-stage DC/DC converter with detailed description of its operation at all logical switching modes. This converter is made in three stages: a) two stages of interleaved converters and 2) a double boost converter with float potential.

A. TOPOLOGY AND OPERATION PRINCIPLE

Figures 5 through 8 show modes of operation of the topology of IIDFO boost DC/DC converter (shown in Fig. 2). During the time that the DC/DC converter is operating in boost mode, it will serve energy to the DC bus to assure maintaining the stability of DC bus voltage. During this time, the power transistors (S_{T1}, S_{T3},S_{T5}, S_{T7}, S_{T9}, and S_{T12}) are turned OFF; whereas the power transistors (S_{T2}, S_{T4},S_{T6}, S_{T8}, S_{T10}, and S_{T11}) and diodes (D_1, D_3, D_5, D_7, D_9, andD_{12}) are turned ON/OFF in alternation. In Table 3, 0/1 means MOSFETs are ON/OFF, and F/R means diodes are forward/reverse bias.

Table 3 lists the switching states of the three stages of the IIDFO converter in boosting operation. In Table 3, 0/1 means MOSFETs are ON/OFF, and F/R means diodes are forward/reverse bias. In modes 1 through 4, the switches of two interleaved stages are turned OFF, whereas the 3rd float converter works in four different logic states. In modes 5 through 8, the 1st stage is still OFF while 2nd stage is turned ON. In modes 9 through 12, the 1st stage is ON, and the 2nd is OFF. Finally, in modes 13 through 16, both 1st and 2nd stages are turned ON.

In boost mode, $S_{T1}, S_{T3,}S_{T5}, S_{T7}, S_{T9}$, *and* S_{T12} are turned OFF. In the first and second interleaved stages, the power switches of $S_{T1}, S_{T3,}S_{T5}$, and S_{T7} are driven OFF while $S_{T2}, S_{T4,}S_{T6}$, *and* S_{T8} are controlled ON/OFF according to the required voltage level. For accurate representation, inductors' resistances are considered. The inductors currents $\bar{I}_{L1}$, $\bar{I}_{L2}$ and output voltage V_{co1} are considered as state variables.

1) MODE 1: $S_{T2\&4}, S_{T6\&8}, S_{T10}, S_{T11}$ ARE OFF

In this mode, the switches S_{T2}, $S_{T4}S_{T6}$, S_{T8}, S_{T10}, and S_{T11} are turned OFF as shown in Fig. 5(a). Diodes D1, D3, D5, D7, D9 and D12 are in the ON state. The energy that has been stored in the inductors L_1 and L_2 are supplied to the capacitor Co_1 and to inductors L_3 and L_4; and in turn, the energy that has been stored in the inductors L_3 and L_4 are supplied to the capacitor Co_2 and to inductors L_5 and L_6.

TABLE 3. Switching states of the boost DC/DC topology.

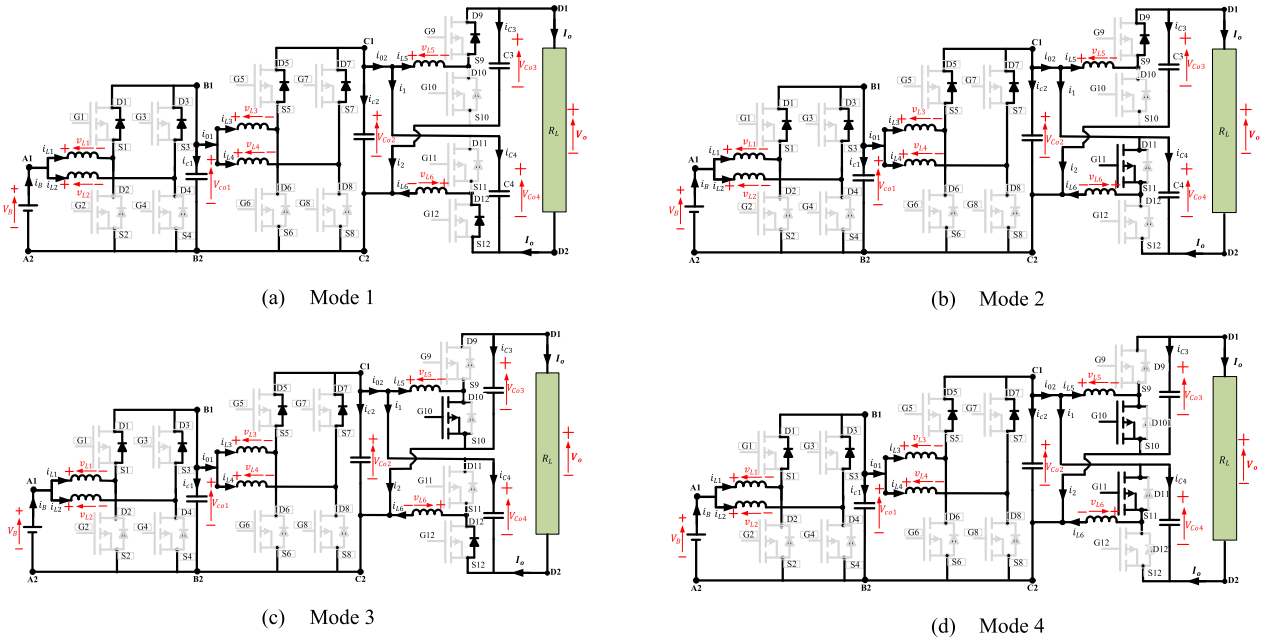
Mode	$S_{T2\&4}$	$S_{T6\&8}$	S_{T10}	S_{T11}	$D_{1\&3}$	$D_{5\&7}$	D_9	D_{12}
1	0	0	0	0	F	F	F	F
2	0	0	0	1	F	F	F	R
3	0	0	1	0	F	F	R	F
4	0	0	1	1	F	F	R	R
5	0	1	0	0	F	R	F	F
6	0	1	0	1	F	R	F	R
7	0	1	1	0	F	R	R	F
8	0	1	1	1	F	R	R	R
9	1	0	0	0	R	F	F	F
10	1	0	0	1	R	F	F	R
11	1	0	1	0	R	F	R	F
12	1	0	1	1	R	F	R	R
13	1	1	0	0	R	R	F	F
14	1	1	0	1	R	R	F	R
15	1	1	1	0	R	R	R	F
16	1	1	1	1	R	R	R	R

The inductors currents i_{L1}, i_{L2}, i_{L3}, i_{L4}, i_{L5} and i_{L6} decrease. In addition, energies stored in the inductors L_5 and L_6 are supplied to the output capacitors Co_3 and Co_4, and the load resistor R_L. Applying Kirchhoff Current Law (KCL) at node D11 in Fig. 2 gives $i_1 = i_{Co4} = i_{L6} - \frac{V_0}{R_L}$. Then, applying Kirchhoff Voltage law (KVL) in stage 3 gives

$$V_0 - V_{Co3} + V_{Co2} - V_{Co4} = 0$$

$$\xrightarrow{yields} V_0 = -V_{Co2} + V_{Co3} + V_{Co4} \tag{20}$$

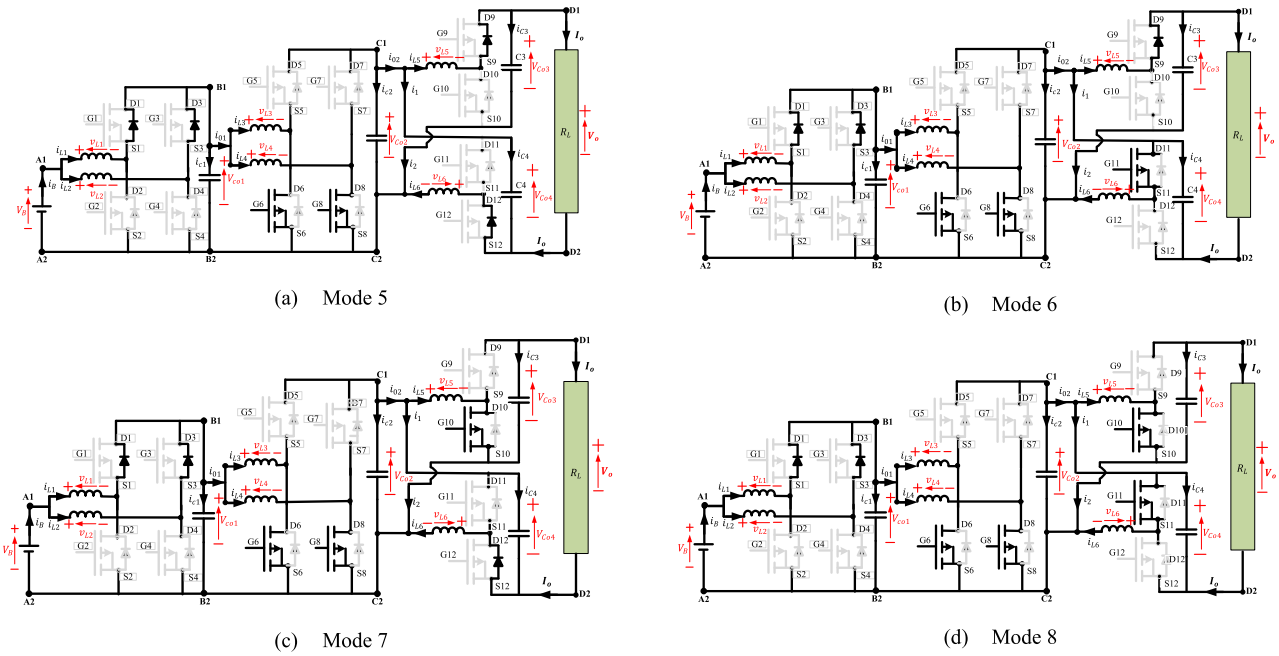
When KVL is applied in the closed loops for the interleaved stages, state equations of inductors currents and capacitors voltage are described as in (21) and (22) for stage 1 and 2, respectively. As depicted from the equations, the inductors L_1 and L_2 would be discharging and the capacitor Co_1 would be charging, whereas the inductors L_3 and L_4 are discharged and the capacitor Co_2 would be charging. By the same way, when KVL is applied in the closed loops for the float stage, state equations of inductors currents and



(a) Mode 1 (b) Mode 2

(c) Mode 3 (d) Mode 4

FIGURE 5. Operation modes of the DC/DC converter topology from mode 1 to mode 8.



(a) Mode 5 (b) Mode 6

(c) Mode 7 (d) Mode 8

FIGURE 6. Operation modes of the DC/DC converter topology from mode 5 to mode 8.

capacitors voltages are described as in (23). It means that the inductors L_5 and L_6 are discharged and the capacitors Co_3 and Co_4 are charged.

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{1}{L1}\left(V_B - V_{Co1}\right) \\ \dfrac{di_{L2}}{dt} = \dfrac{1}{L_2}\left(V_B - V_{Co1}\right) \\ \dfrac{dV_{Co1}}{dt} = \dfrac{1}{Co1}\left(i_{L1} + i_{L2} - i_{L3} - i_{L4}\right) \end{cases} \tag{21}$$

$$\begin{cases} \dfrac{di_{L3}}{dt} = \dfrac{1}{L3}\left(V_{co1} - V_{Co2}\right) \\ \dfrac{di_{L4}}{dt} = \dfrac{1}{L_4}\left(V_{co1} - V_{Co2}\right) \\ \dfrac{dV_{Co2}}{dt} = \dfrac{1}{Co2}\left(i_{L3} + i_{L4} - i_{L5} - i_{L6}\right) \\ + \dfrac{1}{Co2R_L}\left(-V_{Co2} + V_{Co3} + V_{Co4}\right) \end{cases} \tag{22}$$

$$\begin{cases} \frac{di_{L5}}{dt} = \frac{1}{L_5}(V_{Co2} - V_{Co3}) \\ \frac{di_{L6}}{dt} = \frac{1}{L_6}(V_{Co2} - V_{Co4}) \\ \frac{dV_{C3}}{dt} = \frac{1}{C_{o3}}\left(i_{L5} - \frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \\ \frac{dV_{C4}}{dt} = \frac{1}{C_{o4}}\left(i_{L6} - \frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \end{cases} \tag{23}$$

2) MODE 2: $S_{T2\&4}, S_{T6\&8}, S_{T10}$ ARE OFF AND S_{T11} IS ON

In mode 2, switches and diodes of both stages (1 and 2) remain in the same state to mode1. Then, state equations of inductors current and capacitors voltage are described by the same (21) and (22) for stage 1 and 2, respectively. In stage 3, the switch S_{T10} remains OFF and S_{T11} is turned ON, as shown in Fig. 5(b). Energy stored in the inductor L_5 is supplied to the output capacitors Co_3 and to the load resistor R_L; whereas the capacitor Co_4 discharges its energy to the inductor L_6. The inductor L_6 would also be charging through the input voltage of V_{Co2} in shoot through mode via S_{T11}. By the same way, when KVL is applied in the closed loops for the float stage, state equations of inductors' currents as well as capacitors' voltages are described as in (24).

$$\begin{cases} \frac{di_{L5}}{dt} = \frac{1}{L_5}(V_{Co2} - V_{Co3}) \\ \frac{di_{L6}}{dt} = \frac{1}{L_6}V_{Co2} \\ \frac{dV_{Co3}}{dt} = \frac{1}{C_{o3}}\left(i_{L5} - \frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \\ \frac{dV_{Co4}}{dt} = \frac{-1}{Co_4}\left(\frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \end{cases} \tag{24}$$

3) MODE 3: $S_{T2\&4}, S_{T6\&8}, S_{T11}$ ARE OFF AND S_{T10} IS ON

In mode 3, both switches and diodes of stage 1 and stage 2 remain in the same state as the model. Then, state equations of inductors currents and capacitors voltages are described by equations (21) and (22) for stages 1 and 2, respectively. In stage 3, switch S_{T10} would be turning ON and S_{T11} would be turning OFF, as given in Fig. 5(c). The inductor L_5 is charging by the input voltage of V_{Co2} in shoot through mode via S_{T10}. The capacitor Co_4 is charged from the capacitor V_{Co2}; whereas the capacitor Co_3 discharges its energy into the load resistor R_L. By the same way, when KVL is applied in the closed loops for the float stage, state equations of inductors currents and capacitors voltages are described as in (25).

$$\begin{cases} \frac{di_{L5}}{dt} = \frac{1}{L_5}V_{Co2} \\ \frac{di_{L6}}{dt} = \frac{1}{L_6}(V_{Co2} - V_{Co4}) \\ \frac{dV_{Co3}}{dt} = \frac{1}{Co_3}\left(\frac{-1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \\ \frac{dV_{Co4}}{dt} = \frac{1}{C_{o4}}\left(i_{L6} - \frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \end{cases} \tag{25}$$

4) MODE 4: $S_{T2\&4}, S_{T6\&8}$ ARE OFF AND S_{T10}, S_{T11} ARE ON

In mode 4, both switches and diodes of stages (1 and 2) remain in the same state to the model. Then, state equations of inductors current and capacitor voltage can be described using equations (21) and (22) for stage 1 and 2, respectively. In stage 3, both switches S_{T10} and S_{T11} are turned ON, as shown in Fig. 5(d). The inductors L_5 and L_6 are charging by the input voltage of V_{Co2} in shoot through mode via S_{T10} and S_{T11}, respectively. It means that the inductors L_5 and L_6 store energy and its voltages are raised up and the capacitors C_3 and C_4 are discharged. By the same way, when KVL is applied in the closed loops for the float stage, state equations of inductors currents and capacitors voltages are described as in (26).

$$\begin{cases} \frac{di_{L5}}{dt} = \frac{1}{L_5}V_{Co2} \\ \frac{di_{L6}}{dt} = \frac{1}{L_6}V_{Co2} \\ \frac{dV_{Co3}}{dt} = \frac{-1}{C_{o3}}\left(\frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \\ \frac{dV_{Co4}}{dt} = \frac{-1}{Co_4}\left(\frac{1}{R_L}(-V_{Co2} + V_{Co3} + V_{Co4})\right) \end{cases} \tag{26}$$

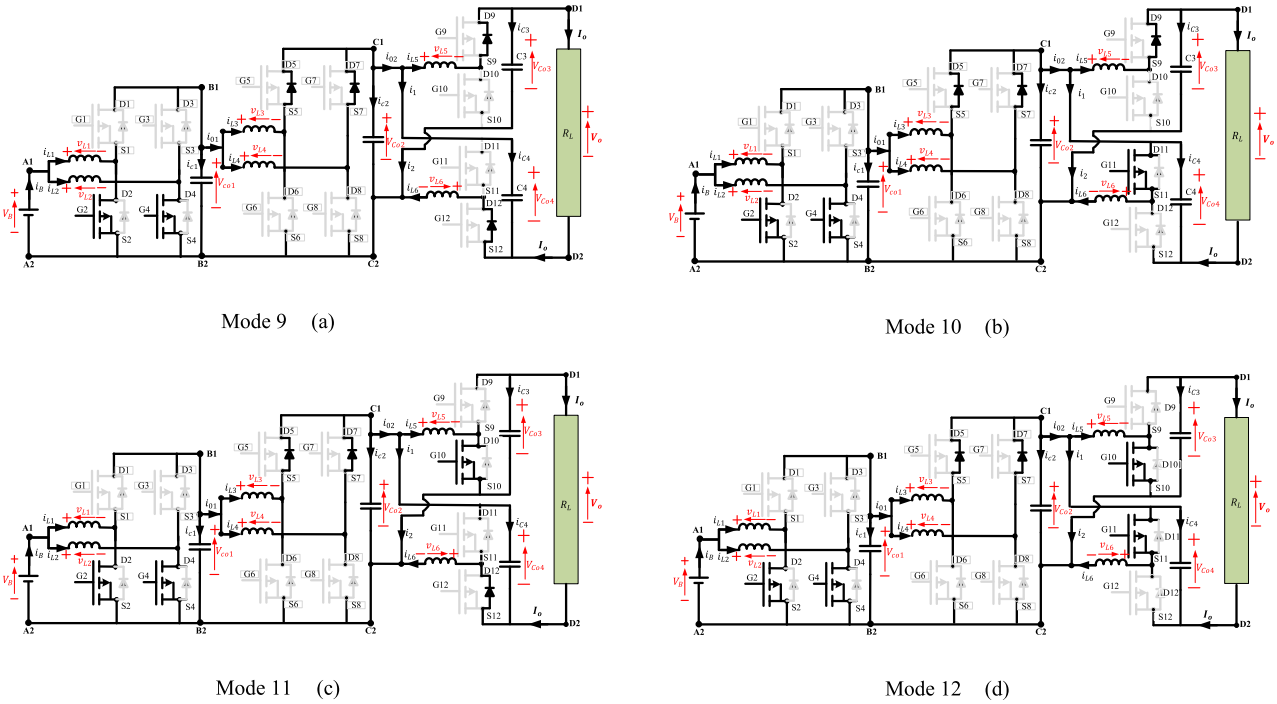
5) MODE 5: $S_{T2\&4}, = 0, S_{T6\&8} = 1, S_{T10} = 0, S_{T11} = 0$

In this mode, switches S_{T2} are S_{T4} remain OFF, switches S_{T6} and S_{T8} are in the ON mode and the switches S_{T10} and S_{T11} are in the OFF mode, as shown in Fig. 6(a). Hence, for the 1st interleaved stage, state equations of inductors current and capacitor voltage are described as in (21). Diodes D1, D3, D9 and D12 are in ON state whereas D5, D7 become OFF. The energy being stored in the inductors L_1 and L_2 would be supplied to capacitor C_1 and to inductors L_3 and L_4. The inductors L_3 and L_4 are charged by the capacitor C_1 during the shoot-through state via the switches S_{T6} and S_{T8}. The inductors currents i_{L1}, i_{L2}, i_{L5} and i_{L6} decrease while the currents i_{L3}, i_{L4} increase. In addition, energies in the inductors L_5 and L_6 are supplied to the output capacitors C_3 and C_4, and the load resistor R_L. When KVL is applied in the closed loops for the 2nd interleaved stage, state equations of inductors currents and capacitors voltage are described as in (23) and (27). In this mode, the inductors L_3 and L_4 are charged from battery and from inductors L_1 and L_2 and the capacitor C_2 will discharge into the third stage. By the same way in mode 1, when KVL is applied in the closed loops for the float stage, state equations of inductors currents and capacitors voltages are described as in (23).

$$\begin{cases} \frac{di_{L3}}{dt} = \frac{1}{L3}(V_{c1}) \\ \frac{di_{L4}}{dt} = \frac{1}{L_4}(V_{c1}) \\ \frac{dV_{C2}}{dt} = \frac{1}{C2}(-i_{L5} - i_{L6}) + \frac{1}{C2R_L}(-V_{C2} + V_{C3} + V_{C4}) \end{cases} \tag{27}$$

6) MODE 6: $S_{T2\&4}, = 0, S_{T6\&8} = 1, S_{T10} = 0, S_{T11} = 1$

In mode 6, both switches and diodes of stages (1 and 2) remain in the same state as mode 5, as shown in Fig. 6(b). Therefore, state variables of 1st stage can be described by (21), and the 2nd stage can be described by (27). Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (24).



Mode 9 (a) Mode 10 (b)

Mode 11 (c) Mode 12 (d)

FIGURE 7. Operation modes of the converter topology from mode 9 to mode 12.

Mode 13 (a) Mode 14 (b)

Mode 15 (c) Mode 16 (d)

FIGURE 8. Operation modes of the converter topology from mode 13 to mode 16.

7) MODE 7: $S_{T2\&4}, = 0, S_{T6\&8} = 1, S_{T10} = 1, S_{T11} = 0$

In mode 7, both switches and diodes of stages (1 and 2) remain in the same state as mode 5, as shown in Fig. 6(c). Therefore, state variables of 1st stage can be described by (21), and the 2nd stage can be described by (27). Finally, state equations of inductors current and capacitors voltages of the 3rd stage are described as in (25).

8) MODE 8: $S_{T2\&4,}=0, S_{T6\&8}=1, S_{T10}=1, S_{T11}=1$

In this mode, the switches and diodes of stage 1 and stage 2 remain in the same state as mode 5, as shown in Fig. 6(d). Therefore, state variables of 1st stage can be described by (21), and the 2nd stage can be described by (27). Finally, state equations of inductors current and capacitors voltages of the 3rd stage are described as in (26).

9) MODE 9: $S_{T2\&4,}=1, S_{T6\&8}=0, S_{T10}=0, S_{T11}=0$

In this mode, the switches S_{T2} are S_{T4} are switched ON, and switches S_{T6} and S_{T8} are in the OFF mode and switches S_{T10} and S_{T11} are in the OFF mode, as shown in Fig. 7(a). In this case, state variables of 1st stage are described by (28). Diodes D1 and D3 are in the OFF state, and diodes D5, D7, D9 and D12 are in ON state. Inductors (L_1 and L_2) would be charging by the battery V_B during the shoot-through state via the switches S_{T2} and S_{T4}. The energy in storage in inductors L_3 and L_4 are supplied to capacitor C_2 and to inductors L_5 and L_6. The inductors currents i_{L1}, i_{L2}, i_{L5} and i_{L6} increase while the currents i_{L3}, i_{L4} decrease. In addition, energies in the inductors L_5 and L_6 are supplied to the output capacitors Co_3 and Co_4, and the load resistor R_L.

When KVL is applied in the closed loops for the interleaved 2nd stage and 3rd stage, it was found that the state equations of inductors currents and capacitors voltage are described as in (22) and (23), respectively.

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{1}{L1}(V_B) \\ \dfrac{di_{L2}}{dt} = \dfrac{1}{L_2}(V_B) \\ \dfrac{dV_{Co1}}{dt} = \dfrac{1}{Co1}(-i_{L3} - i_{L4}) \end{cases} \tag{28}$$

10) MODE 10: $S_{T2\&4,}=1, S_{T6\&8}=0, S_{T10}=0, S_{T11}=1$

In mode 10, switches and diodes of stages (1 and 2) remain in the same state as mode 6, as shown in Fig. 7(b). Therefore, state variables of 1st stage can be described by (28), and the 2nd stage can be described by (22). Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (24).

11) MODE 11: $S_{T2\&4,}=1, S_{T6\&8}=0, S_{T10}=1, S_{T11}=0$

In mode 11, switches and diodes of stages (1 and 2) remain in the same state as mode 7, as shown in Fig. 7(c). Therefore, state variables of 1st stage can be described by (28), and the 2nd stage can be described by (22). Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (25).

12) MODE 12: $S_{T2\&4,}=1, S_{T6\&8}=0, S_{T10}=1, S_{T11}=1$

In this mode, the switches and diodes of stage 1 and stage 2 remain in the same state as mode 8, as shown in Fig. 7(d). Therefore, state variables of 1st stage can be described by (28), and the 2nd stage can be described by (22). Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (26).

13) MODE 13: $S_{T2\&4,}=1, S_{T6\&8}=1, S_{T10}=0, S_{T11}=0$

In mode 13, switches S_{T2}, S_{T4}, S_{T6} and S_{T8} are switched ON, and switches S_{T10} and S_{T11} are turned OFF, as shown in Fig. 8(a). Diodes D1, D3, D5 and D7 are in the OFF mode, and diodes, D9 and D12 are in ON mode. Inductors L_1 and L_2 are charging by battery V_B during the shoot-through state via the switches S_{T2} and S_{T4}, and the inductors L_3 and L_4 are charged by the capacitor Co_1 during the shoot-through state via the switches S_{T6} and S_{T8}. The inductors currents i_{L1}, i_{L2}, i_{L3} and i_{L4} increase while the currents i_{L5}, i_{L6} decrease. In addition, energies in the inductors L_5 and L_6 are supplied to the output capacitors Co_3 and Co_4, and the load resistor R_L. In this mode, the state variables of 1st stage can be described by (28) as in mode 9, and the 2nd stage can be described by (27) in mode 5. Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (23) in mode 1.

14) MODE 14: $S_{T2\&4,}=1, S_{T6\&8}=1, S_{T10}=0, S_{T11}=1$

In mode 14, as demonstrated in Fig. 8(b), state variables of 1st stage can be described by (28) as in mode 9, and the 2nd stage can be described by (27) in mode 5. Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (24) in mode 2.

15) MODE 15: $S_{T2\&4,}=1, S_{T6\&8}=1, S_{T10}=1, S_{T11}=0$

In mode 15, as demonstrated in Fig. 8(c), state variables of 1st stage can be described by (28) as in mode 9, and the 2nd stage can be described by (27) in mode 5. Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (25) in mode 3.

16) MODE 16: $S_{T2\&4,}=1, S_{T6\&8}=1, S_{T10}=1, S_{T11}=1$

In mode 16, as demonstrated in Fig. 8(d), state variables of 1st stage can be described by (28) as in mode 9, and the 2nd stage can be described by (27) in mode 5. Finally, state equations of inductors currents and capacitors voltages of the 3rd stage are described as in (26) in mode 4.

B. SWITCHING AND AVERAGE MODELS OF THE PROPOSED CONVERTER

Dependency of state variables of the three stages are derived in detail. For each stage, the switching and average models have been obtained as a function of modulation indices.

1) 1ST STAGE INTERLEAVED DC/DC BOOST CONVERTER

State variables of 1st stage are described by (21) for modes 1-4 and modes 5-8, and by (28), for modes 9-12 and modes 13-16. As a general form, the state variables are written as a switching model in matrix form as in (29), shown at the bottom of the next page. S_{Ti} (i = 2, 4) denotes the switch position of S_{T2} and S_{T4}, $S_{Ti}=1$ means Ti is ON, and $S_{Ti}=0$ means Ti is OFF.

In 1st stage, S_{T1} and S_{T3} are the complement of S_{T2} and S_{T4}, respectively. In the model, S_{T4} is considered a shift of S_{T2} by 360/2 i.e., $S_{T4}=S_{T2}+180^{\circ}$. Hence, the matrix (29) can be formed as in (30), shown at the bottom of the next page.

When the goal is the control design, it is appropriate to take into consideration the averaged model [29], determined by considering the average of the model in Eq. (30) over one switching period. Then, (30) can be written in average form as in (31), shown at the bottom of the page. I_{L1}, I_{L2},I_{L3} and I_{L4} correspond to the average values of the inductors currents i_{L1}, i_{L2}, i_{L3} and i_{L4}, respectively; V_{Co1} represents the average value of the output voltage v_{Co1}, and $D1$ represents the duty cycle, i.e. average value of a binary control input $S_{T4} = (S_{T2} + 180^{\circ}) = D1$, which takes values in [1, 0].

2) 2ND STAGE INTERLEAVED DC/DC BOOST CONVERTER

State variables of 2nd stage are described by (22) for modes 1-4 and modes 9-12, and by (27), for modes 5-8 and modes 13-16. As a general form, the state variables are written as a switching model in matrix form as in (32), shown at the bottom of the next page.

In the 2nd stage, S_{T5} and S_{T7} are the complement of S_{T6} and S_{T8}, respectively. In the model, it is considered that S_{T8} is a shift of S_{T6} by 360/2 i.e., $S_{T8} = S_{T6} + 180^{\circ}$. Hence, the matrix (32) can be formed as (33) considering switch S_{T6} only.

In an average model of stage, determined by considering the average of the model as in Eq. (33), shown at the bottom of the next page, over one switching period, the modulation indices could be considered as $S_{T6} = S_{T6} + 180^{\circ} = D2$, $S_{T10} = D3$, and $S_{T10} + 180^{\circ} = D4$. Then, (33) can be written in average form as in (34), shown at the bottom of the next page. Being I_{L3}, I_{L4},I_{L5} and I_{L6} are the average values of inductors' currents i_{L3}, i_{L4}, i_{L5} and i_{L6}, respectively; V_{Co2}, V_{Co3} and V_{Co4} are the average values of the output voltages v_{Co2}, v_{Co3}, and v_{Co4}, and $\mu 2$,$\mu 3$ and $\mu 4$ are the duty cycles, i.e. average values of the binary control input $S_{T6} = (S_{T6} + 180^{\circ})$,$S_{T10}$, and S_{T11}, which take values in [0,1].

3) 3RD STAGE FLOAT DOUBLE DC/DC BOOST CONVERTER

State variables of 3rd stage are described by (23) for modes 1, 5, 9, and 13, and by (24) for modes 2, 6, 10, and 114, and by (25) for modes 3, 7, 11, and 14, and by (26) for modes 4, 8, 12, and 16. As a general form, the state variables are written as a switching model in matrix form as in (35), shown at the bottom of the next page.

The average model of float converter is stated as in (36), shown at the bottom of the next page.

For the third float double stage, the input voltage is V_{C2} and output voltage is related to the state variables and control indices. In general, different modes of operations of this converter can be described as (37).

$$V_0 = -V_{Co2} - (2D3 - 1)\, V_{Co3} - (2D4 - 1)V_{Co4} \tag{37}$$

Then (37) could be rewritten as in (38), shown at the bottom of the next page.

For control system design, the matrices of (31), (34), and (38) will be discretized to be used to get the optimal modulation indices for each stage to achieve the reference output voltage.

IV. SIMULATIONS

All figures from Fig. 9 through Fig. 13 will follow the calculated duty from equations (1), (4), and (7) and the specifications of the suggested DC/DC converter of Table 2. Many efforts in high step-up DC/DC converters have been made to directly boost the low-supply voltage to the high-load voltage [31], [32], [33]. To prove the superiority of the

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{Co1}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & \frac{-1}{L_1}(1 - S_{T2}) & 0 & 0 & \frac{1}{L1} \\ 0 & \frac{-r_{L2}}{L_2} & \frac{-1}{L_2}(1 - S_{T4}) & 0 & 0 & \frac{1}{L2} \\ \frac{1}{Co_1}(1 - S_{T2}) & \frac{1}{Co_1}(1 - S_{T4}) & 0 & \frac{-1}{Co_1} & \frac{-1}{Co_1} & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{Co1} \\ i_{L3} \\ i_{L4} \\ V_B \end{bmatrix} \tag{29}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{Co1}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & \frac{-1}{L_1}(1 - S_{T2}) & 0 & 0 & \frac{1}{L1} \\ 0 & \frac{-r_{L2}}{L_2} & \frac{-1}{L_2}\left(1 - (S_{T2} + 180^{\circ})\right) & 0 & 0 & \frac{1}{L2} \\ \frac{1}{Co_1}(1 - S_{T2}) & \frac{1}{Co_1}\left(1 - (S_{T2} + 180^{\circ})\right) & 0 & \frac{1}{Co_1} & \frac{1}{Co_1} & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{Co1} \\ i_{L3} \\ i_{L4} \\ V_B \end{bmatrix} \tag{30}$$

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{I}_{L2} \\ \dot{V}_{Co1} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & \frac{-1}{L_1}(1 - D1) & 0 & 0 & \frac{1}{L1} \\ 0 & \frac{-r_{L2}}{L_2} & \frac{-1}{L_2}(1 - D1) & 0 & 0 & \frac{1}{L2} \\ \frac{1}{Co_1}(1 - D1) & \frac{1}{Co_1}(1 - D1) & 0 & \frac{1}{Co_1} & \frac{1}{Co_1} & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{Co1} \\ I_{L3} \\ I_{L4} \\ V_B \end{bmatrix} \tag{31}$$

proposed topology, a comparison is made to the results of a one-step high step-up DC-DC Converter in [32].

A. STEADY-STATE PERFORMANCE WITH FIXED MODULATION DUTIES

Figure 9 shows the terminal voltages of the three stages of the converter. Designed set voltages i.e., 90V, 250V, and 600V are obtained when a 24V battery is supplied and the modulation indices are set at 0.77, 0.64, and 0.41 for 1st, 2nd, and 3rd stages, respectively. Fast response without any overshoot in terminal voltage can be observed. With zero initial voltage of capacitors, high overshoot currents are drawn from battery (See Fig.10). To suppress this inrush current, two methods could be used: initialization with high capacitor voltages and control of the duty of each stage. Same surge currents can be seen in inductors currents, as shown in Fig. 11.

$$\begin{bmatrix} \frac{di_{L3}}{dt} \\ \frac{di_{L4}}{dt} \\ \frac{dv_{Co2}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L3}}{L_3} & 0 & \frac{-1}{L_3}(1-S_{T6}) & 0 & 0 & 0 & 0 & \frac{1}{L3} \\ 0 & \frac{-r_{L4}}{L_4} & \frac{-1}{L_4}(1-S_{T8}) & 0 & 0 & 0 & 0 & \frac{1}{L4} \\ \frac{1}{Co_2}(1-S_{T6}) & \frac{1}{Co_2}(1-S_{T8}) & \frac{-1}{Co_2R_L} & \frac{1}{Co_2} & \frac{1}{Co_2} & \frac{1}{Co_2R_L}(2S_{T10}-1) & \frac{1}{Co_2R_L}(2S_{T11}-1) & 0 \end{bmatrix} \begin{bmatrix} i_{L3} \\ i_{L4} \\ v_{Co2} \\ i_{L5} \\ i_{L6} \\ v_{Co3} \\ v_{Co4} \\ v_{co1} \end{bmatrix} \tag{32}$$

$$\begin{bmatrix} \frac{di_{L3}}{dt} \\ \frac{di_{L4}}{dt} \\ \frac{dv_{Co2}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L3}}{L_3} & 0 & \frac{-1}{L_3}(1-S_{T6}) & 0 & 0 & 0 & 0 & \frac{1}{L3} \\ 0 & \frac{-r_{L4}}{L_4} & \frac{-1}{L_4}\left(1-(S_{T6}+180^\circ)\right) & 0 & 0 & 0 & 0 & \frac{1}{L4} \\ \frac{1}{C_{o2}}(1-S_{T6}) & \frac{1}{Co_2}\left(1-(S_{T6}+180^\circ)\right) & \frac{-1}{Co_2R_L} & \frac{1}{Co_2} & \frac{1}{Co_2} & \frac{1}{Co_2R_L}(2S_{T10}-1) & \frac{1}{Co2R_L}\left(2(S_{T10}+180^\circ)-1\right) & 0 \end{bmatrix} \times \begin{bmatrix} i_{L3} \\ i_{L4} \\ v_{Co2} \\ i_{L5} \\ i_{L6} \\ v_{Co3} \\ v_{Co4} \\ v_{co1} \end{bmatrix} \tag{33}$$

$$\begin{bmatrix} \dot{I}_{L3} \\ \dot{I}_{L4} \\ \dot{V}_{Co2} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L3}}{L_3} & 0 & \frac{-1}{L_3}(1-D2) & 0 & 0 & 0 & 0 & \frac{1}{L3} \\ 0 & \frac{-r_{L4}}{L_4} & \frac{-1}{L_4}(1-D2) & 0 & 0 & 0 & 0 & \frac{1}{L4} \\ \frac{1}{Co_2}(1-D2) & \frac{1}{Co_2}(1-D2) & \frac{-1}{Co_2R_L} & \frac{1}{Co_2} & \frac{1}{Co_2} & \frac{1}{Co_2R_L}(2D3-1) & \frac{1}{Co2R_L}(2D4-1) & 0 \end{bmatrix} \begin{bmatrix} I_{L3} \\ I_{L4} \\ V_{Co2} \\ I_{L5} \\ I_{L6} \\ V_{Co3} \\ V_{Co4} \\ V_{co1} \end{bmatrix} \tag{34}$$

$$\begin{bmatrix} \frac{di_{L5}}{dt} \\ \frac{di_{L6}}{dt} \\ \frac{dv_{co3}}{dt} \\ \frac{dv_{co4}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L5}}{L_5} & 0 & \frac{-1}{L_5}(1-S_{T10}) & 0 & \frac{1}{L5} & 0 \\ 0 & \frac{-r_{L6}}{L_6} & 0 & \frac{-1}{L_6}(1-S_{T11}) & \frac{1}{L6} & 0 \\ \frac{1}{Co_3}(1-S_{T10}) & 0 & 0 & 0 & 0 & \frac{1}{Co_3R_L}(2S_{T10}-1) \\ 0 & \frac{1}{Co_4}(1-S_{T11}) & 0 & 0 & 0 & \frac{1}{Co_3R_L}(2S_{T11}-1) \end{bmatrix} \begin{bmatrix} i_{L5} \\ i_{L6} \\ v_{co3} \\ v_{co4} \\ v_{co2} \\ v_0 \end{bmatrix} \tag{35}$$

$$\begin{bmatrix} \dot{I}_{L5} \\ \dot{I}_{L6} \\ \dot{V}_{Co3} \\ \dot{V}_{Co4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_5}(1-D3) & 0 & \frac{1}{L5} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_6}(1-D4) & \frac{1}{L6} & 0 \\ \frac{1}{Co_3}(1-D3) & 0 & 0 & 0 & 0 & \frac{1}{Co_3R_L}(2D3-1) \\ 0 & \frac{1}{Co_4}(1-D4) & 0 & 0 & 0 & \frac{1}{Co_3R_L}(2D4-1) \end{bmatrix} \begin{bmatrix} I_{L5} \\ I_{L6} \\ V_{Co3} \\ V_{Co4} \\ V_{Co2} \\ V_0 \end{bmatrix} \tag{36}$$

$$\begin{bmatrix} \dot{I}_{L5} \\ \dot{I}_{L6} \\ \dot{V}_{Co3} \\ \dot{V}_{Co4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_5}(1-D3) & 0 & \frac{1}{L5} \\ 0 & 0 & 0 & \frac{-1}{L_6}(1-D4) & \frac{1}{L6} \\ \frac{1}{Co_3}(1-D3) & 0 & \frac{-1}{Co_3R_L}(2D3-1)^2 & \frac{-1}{Co_3R_L}(2D3-1)(2D4-1) & \frac{-1}{Co_3R_L}(2D3-1) \\ 0 & \frac{1}{Co_4}(1-D4) & \frac{-1}{Co_4R_L}(2D3-1)(2D4-1) & \frac{-1}{Co_4R_L}(2D4-1)^2 & \frac{-1}{Co_4R_L}(2D4-1) \end{bmatrix} \begin{bmatrix} i_{L5} \\ i_{L6} \\ V_{Co3} \\ V_{Co4} \\ V_{Co2} \end{bmatrix} \tag{38}$$

To validate the designed set values for the inductors and capacitors, the steady-state behavior of inductors' currents and capacitors' voltages are presented in Fig. 12 and Fig. 13, respectively. Figure 12 depicts the inductors' current set values, current fluctuations, and current over leaving between the inductors. In simulations, the inductors' currents are fluctuating in a range of 18 A, 24A, and 12A for the 1st, 2nd, and 3rd stages, respectively. Also, in Fig. 12, 180° phase shift among the two phases is observed. Figure 13 demonstrates charging and discharging of the capacitors. Double switching frequency is validated by the interleaving stages. Minimum voltage fluctuations can be observed because of using higher capacitances values than the calculated ones.

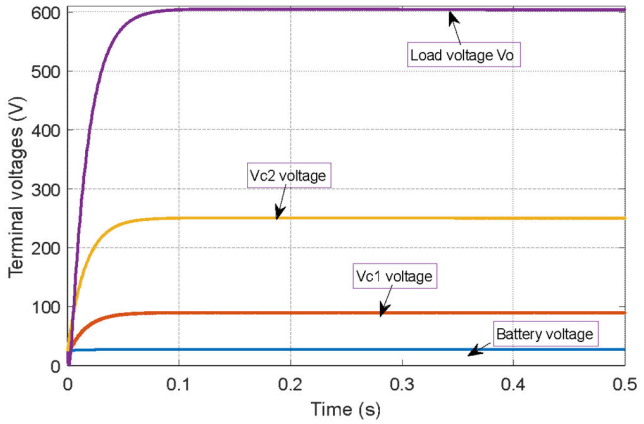


FIGURE 9. Terminal voltages of three stages (Simulation results).

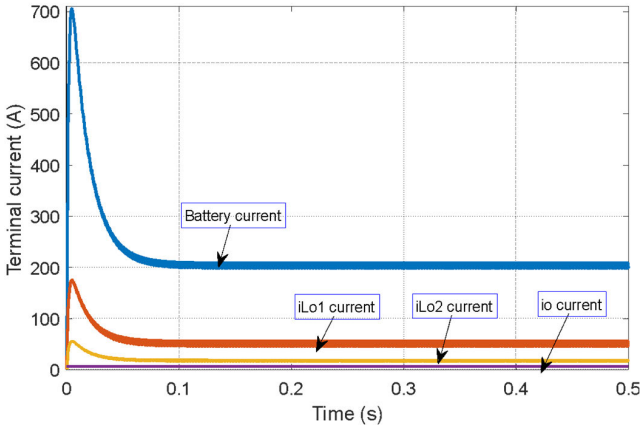


FIGURE 10. Terminal currents of three stages (Simulation results).

Figures 14 through 16 show the performance of the presented DC/DC interleaved boost converter with mutual inductance in [32]. These results are used to salient the performance of our proposal compared to the topology of [32] with same ratings. Fast boosting is happened to the battery from 24V to 600V at load terminal, seen in Fig. 14. In Fig. 15 a current around 225A is drawn from the battery to reach as 6.665A at the load. Compared to Fig. 10 for the proposed topology here, it could be noticed that the current drawn from

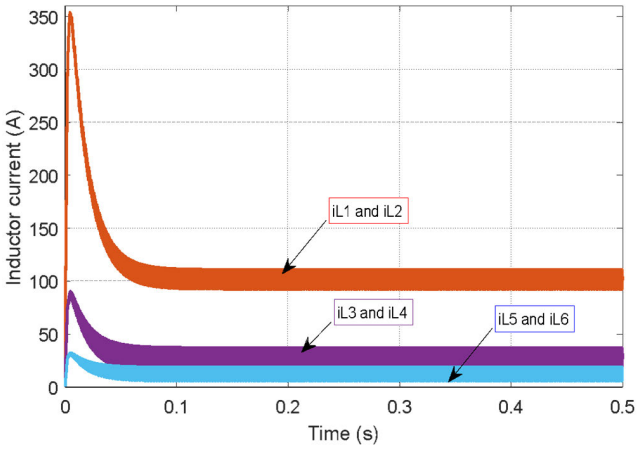


FIGURE 11. Inductors currents of three stages (Simulation results).

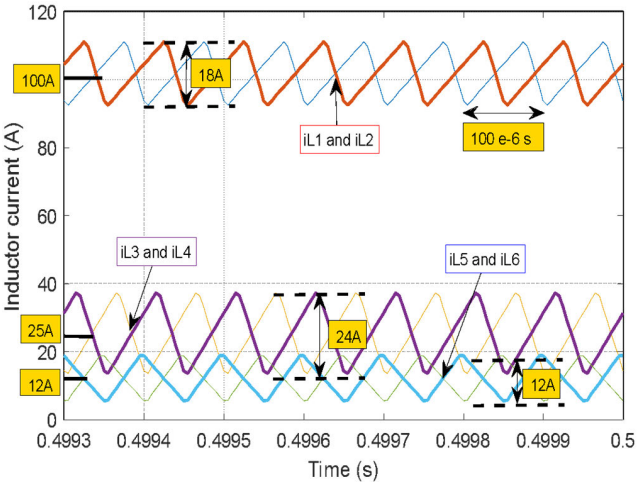


FIGURE 12. Inductors currents at steady state (Simulation results).

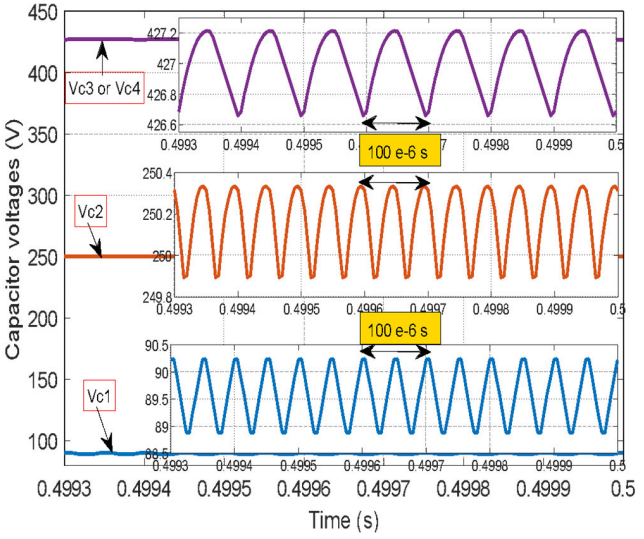


FIGURE 13. Capacitors' voltages at steady state (Simulation results).

the battery in [32] is larger with a higher starting current of 1800 A rather than of 700A in our proposal. The inductor

currents in Fig. 16 fluctuate between 50A and 170A whereas in Fig. 12 it is in range of 91A to 109A. it could be concluded that the proposed topology, compared to the presented topology in [32] presents better performance with low current behavior and hence better efficiency.

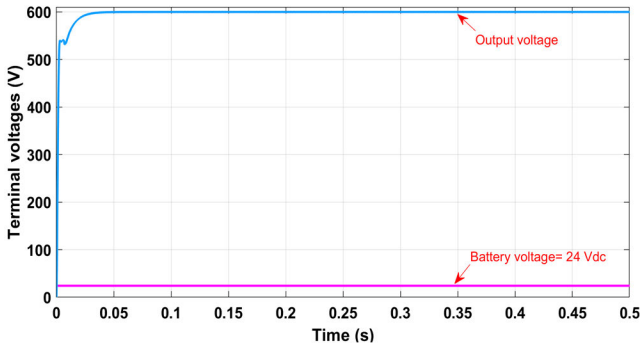


FIGURE 14. Terminal voltages (Simulation results).

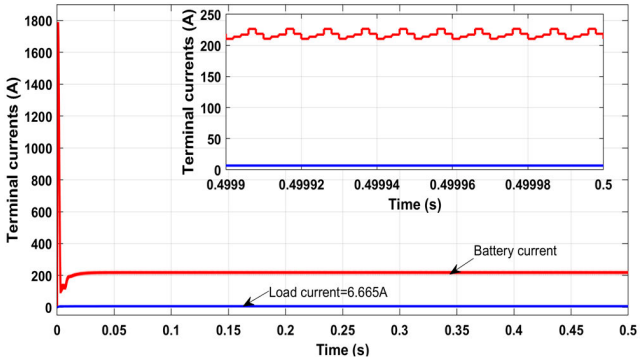


FIGURE 15. Terminal currents (Simulation results).

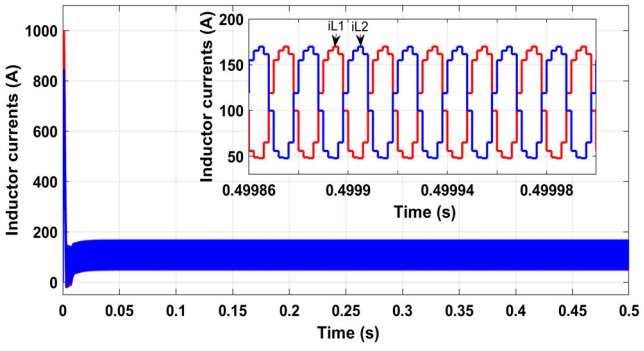


FIGURE 16. Inductor currents (Simulation results).

B. DYNAMIC PERFORMANCE WITH STEP CHANGE IN MODULATION DUTIES

The dynamic behavior of the suggested DC/DC topology is tested and analyzed in this section at different values of modulation duties, as shown in Figs. 17 through 20. Figure 17 presents the modulation duties of the three stages. Figures 18, 19, and 20 show the terminal voltages, terminal currents, and inductors currents of the three stages. First, when the duties are fixed at D1 = 0.66, D2 = 0.54, and D3 = D4 = 0.31, the terminal voltages are boosted to 70V, 255V, and 290V, respectively. At t = 0.2s, D1 is stepped to 0.76 and then the terminal voltages are boosted to 100V, 220V, and 420V, respectively. At t = 0.4s, D2 is stepped to 0.64 and then the terminal voltages are boosted to 95V, 266V, and 520V, respectively. Finally, when D3 = D4 are stepped to 0.41 at t = 0.6s, the terminal voltages are adjusted at the designed values of 90V, 250V, and 600V, respectively. It could be noticed that when the duties are set at the designed values, the terminal voltages are boosted to the designed values. Moreover, the terminal voltages and currents of each stage depend on the terminal voltages and currents of other stages. Therefore, the state variables are dependent for each stage and are related to each other.

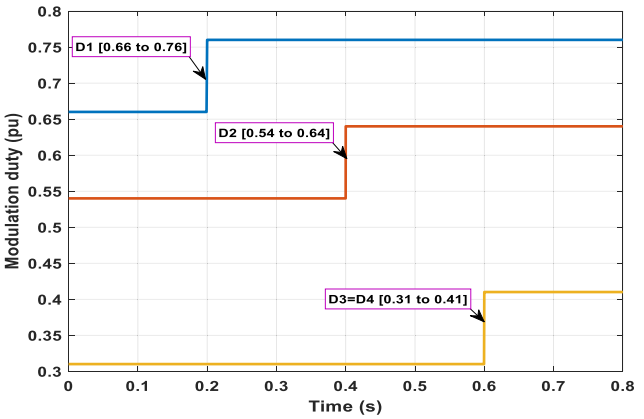


FIGURE 17. Modulation duties of three stages (Simulation results).

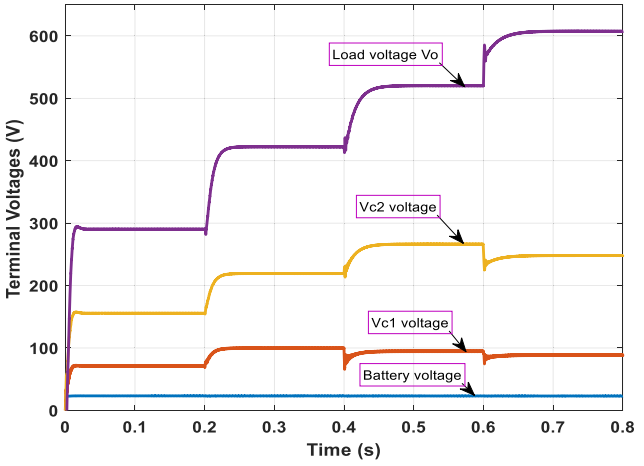


FIGURE 18. Terminal voltages of three stages (Simulation results).

V. EXPERIMENTAL IMPLEMENTATIONS

A. EXPERIMENTAL SETUP

A laboratory prototype is implemented in FC Lab (Fuel Cell Lab) UTBM university in France to test and validate the

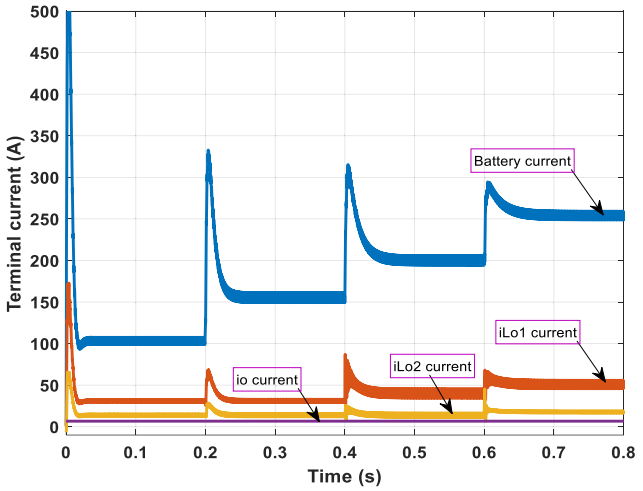


FIGURE 19. Terminal currents of three stages (Simulation results).

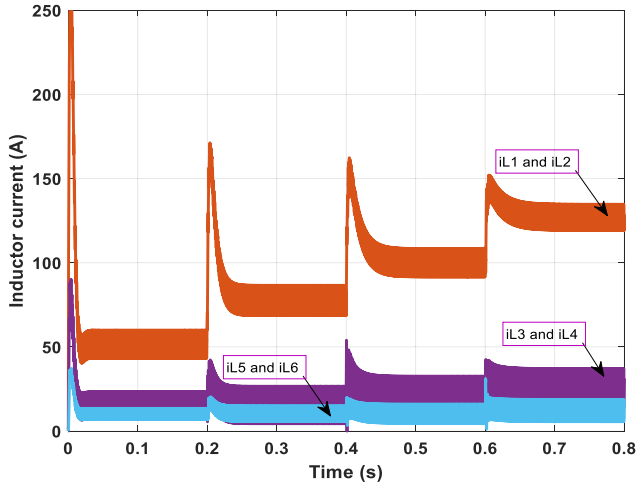


FIGURE 20. Inductors currents of three stages (Simulation results).

suggested converter's design and theoretical analysis. Photos of the built test bench, proposed three stages DC/DC converter, and a Field-Programmable Gate Array (FPGA) board, are presented in Fig. 21 (a)-(c). The design of the suggested IIDFOC converter is accomplished as per the aforementioned design steps given a load power of 4 kW, an input voltage of 24 V, and an output voltage of 600 V.

As demonstrated in Fig. 21 (a), the experimental setup is established with an emulated battery by an electronic programmable power source, and the load is emulated by a DC electronic load. The applied duties established in this study are based on the Matlab-Simulink and Control Desk software of dSPACE 1103. Those control pulses are applied to the power switches via interface boards. The advantages of interleaving the input current ripple are seen when shifting the main switches' control signals of the main switches by 180° from each other. In the experimental assessment developed for two-phase DC/DC converter, the control signals are shifted by 180° from each other using a FPGA control card.

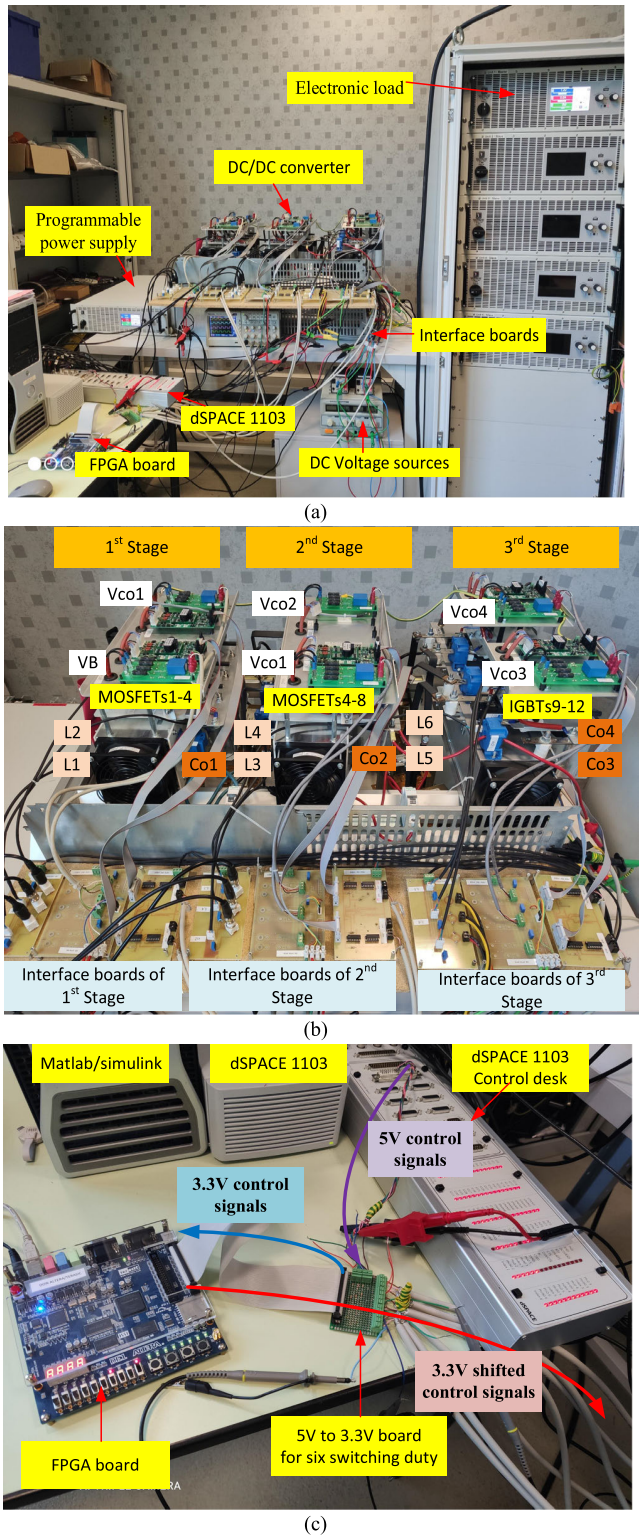


FIGURE 21. Experimental setup of the proposed topology: (a) overall Lab setup, (b) proposed DC/DC converter, (c) FPGA board.

As shown in Fig. 21 (b), twelve power switches are used for the three stages. Each of the two switches are driven by a dual driver. Every inductor current is linked to a Hall effect current

sensor for achieving both monitoring and feedback control, and each capacitor has a Hall effect voltage sensor for attaining monitoring and feedback control as well. specifications of the power switches, gate drivers, and sensors that make up DC/DC converter are provided in Table 4. For designing the prototype, two typical ferrite core type inductors (L_1 and L_2) are chosen in the first stage, two typical ferrite core type inductors (L_3 and L_4) are chosen for the second stage, and two typical ferrite core type inductors (L_5 and L_6) are chosen for the third stage.

As shown in Fig. 21(b), thee identical capacitors $C_{11} = C_{12} = C_{13}$ are used in middle between the first and second stage to represent Co_1, two identical capacitors $C_{21} = C_{22}$ are used in middle between the second and third stage to represent Co_2, and four identical capacitors $C_{31} = C_{32} = C_{41} = C_{42}$ are used at the output of the float stage to represent Co_3 and Co_4. The values of inductances and their internal resistances, and capacitances of the three stages are chosen according to the designed quantities in Table 2. The prototype includes six gate drivers ARCAL2108 with their interface boards [30], as shown in lower part of Fig. 21(b). The ARCAL2108 board is an intelligent double IGBTs and MOSFETs driver. All functions necessary to develop the power converters are implanted on a small size and adaptable single board. The SPWM pulses have been generated for power electronic DC/DC converter through Simulink blocks in RTI library as given in Fig 21 (a). The pulses are connected to the base pins of the MOSFETs and IGBTs via interface boards shown in lower part of Fig. 21(b). This board treats the signals within two stages i.e., inverting stage by 7400 chip and buffering stage by 7417 chips for fixing and powering the gate pulses.

TABLE 4. Ratings of all elements of the DC/DC converter.

Device	Specification
Power MOSFET: S_{T1} to S_{T4}	8x IXFN82N60P
Power MOSFET: S_{T5} to S_{T8}	4x IXFN82N60P
Power IGBT : S_{T9} to S_{T12}	2x CM100DU-24NFH
Dual IGBTs and MOSFETs Driver	6x ARCAL2106 board
Inductors	As in Table 2
Capacitors	As in Table 2
Programmable power supply	Sorensen SGA40x250D-0AAA
Programmable DC Electronic load	Chroma CHR 63202A-600-140

B. INTERLEAVE PHASE-SHIFT IMPLEMENTATION

The control of interleaved converters needs N (N >2) synchronized Pulse Width Modulation (PWM) signals phase shifting. Some control boards have this possibility such as DSP from TI and Microchip, all FPGA, dSPACE DS1105/DS1106 associated with a DS5203 FPGA or Micro-LabBox, etc. Nevertheless, some rapid prototyping boards such as dSpace DS1103 and DS1104 don't allow designing N synchronized phases shifting PWM signals. To resolve this issue, one solution consists of generating one PWM signal with a DS1103/DS1104 and an external FPGA analyzes the signal to retrieve the duty cycle and generate N synchronized phase shifting PWM signal synchronized with the main PWM signal. A photo of the FPGA and its peripherals are demonstrated in Fig. 21(c).

Figure 22 presents the principle that is based on a 16-bits up-counter that computes the duty cycle of dSPACE PWM signal. At the falling edge of dSPACE PWM signal, the duty cycle is updated and used at the next period to generate the N synchronized phase shifting PWM signal. In this example, N has been fixed at two. The proposed solution is simple but introduces a delay of one PWM period that can be compensated for in the design of the controller.

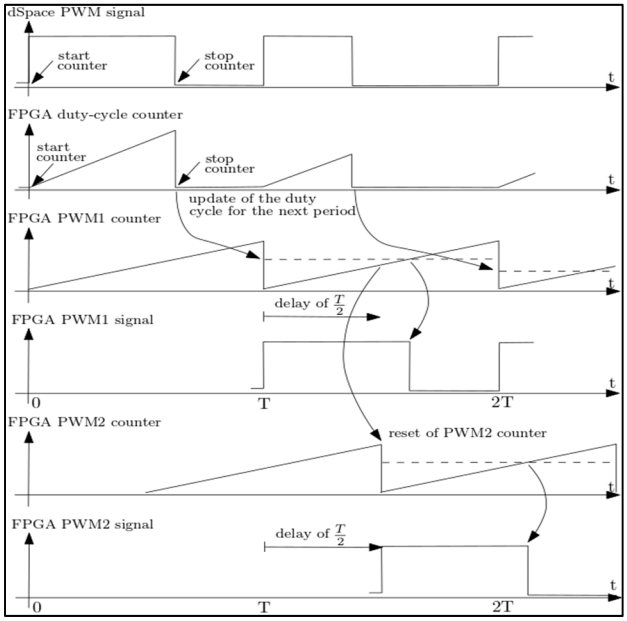


FIGURE 22. Implementation algorithm of phase shifting between N interleaved phases.

C. STEADY-STATE EXPERIMENTAL TESTS

This section presents the measured waveforms for the three stages of the converter to examine the boosting ratio and phase shift. The inductor currents, capacitor voltages, and output voltages are illustrated for each stage. The common measured condition is $F_{sw} = 10kHz$. Figures 23 and 24 show the control signals and measured waveforms for the first stage. Figure 23 shows a photograph of the generated 5V PWM control pulse from the dSPACE with duty D = 0.5 and the two driver control signals that are generated in the FPGA board. Then, a trigger pulse depicts the rising edge detection of a 3.3V signal. This last signal is used to generate another control signal for the second interleaved phase. For the two parallel phases of the interleaved converter, a shift of 180° is programmed in the FPGA. Figure 24 shows the measured waveforms for inductors currents and capacitors voltages. At load of $i_{o1} = 22A$, inductors currents i_{L1} and i_{L2} fluctuate between 19A and 27A at $D_1 = 0.5$. A phase shift of 180° is observed between i_{L1} and i_{L2}, as demonstrated in Fig. 24(a) and (b). Input and output voltages are sensed and recorded in Fig. 24(c) and (d) with voltage boosting

G = 43/24 = 1.8 times with efficiency of 87.5%. When the load current is increased, some notches in the inductor currents could be observed. This phenomenon has been deeply studied and it is decreased by using an earthed shield to mitigate the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems between power circuits and control boards. This improvement is observed in the measurements of stages 2 and 3.

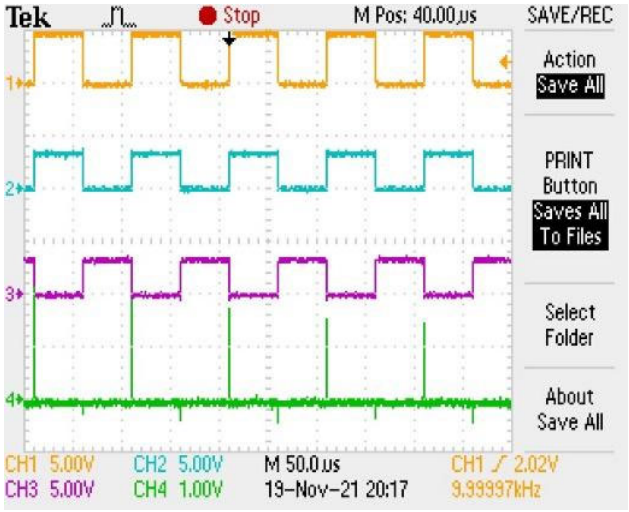


FIGURE 23. Generated PWM control pulse (dSPACE) and the driver control signals (FPGA) for 1st stage.

Figures 25 and 26 show the control signals and measured waveforms for the second stage. Figure 25 shows a photography of the generated 5V PWM control pulse from the dSPACE with duty $D_2 = 0.5413$ and the two driver control signals that are built in the FPGA. Then, a trigger pulse depicts the rising edge detection of a 3.3V signal. This last signal is also used to generate another control signal for the second interleaved phase. For the two parallel phases of the interleaved converter, a shift of 180° is programmed in the FPGA. Figure 26 shows the measured waveforms for inductors currents and capacitors voltages.

At load of $i_{o2} = 10A$, inductors currents i_{L3} and i_{L4} fluctuate between 0A and 30A at D = 0.5413. A phase shift of 180° is observed between i_{L3} and i_{L4}, as demonstrated in Fig. 26 (a) and (b). Input and output voltages are sensed and recorded in Fig. 26 (c) and (d) with a value of voltage boosting G = 202/90 = 2.24 times with efficiency of 81.4%. It is observed that the notches in the inductor currents are mitigated due to the earthed shield.

Figures 27 and 28 show the control signals and measured waveforms for the third stage. Figure 27 shows a photograph of the generated 5V PWM control pulse from the dSPACE with duty $D_3 = D_4 = 0.44$ and the two driver control signals that are generated in the FPGA, then a trigger pulse depicts the rising edge detection of a 3.3V signal. This last signal is also used to generate another control signal for the second interleaved phase. For the two floated phases of the converter, a shift of 180° is also programmed in the

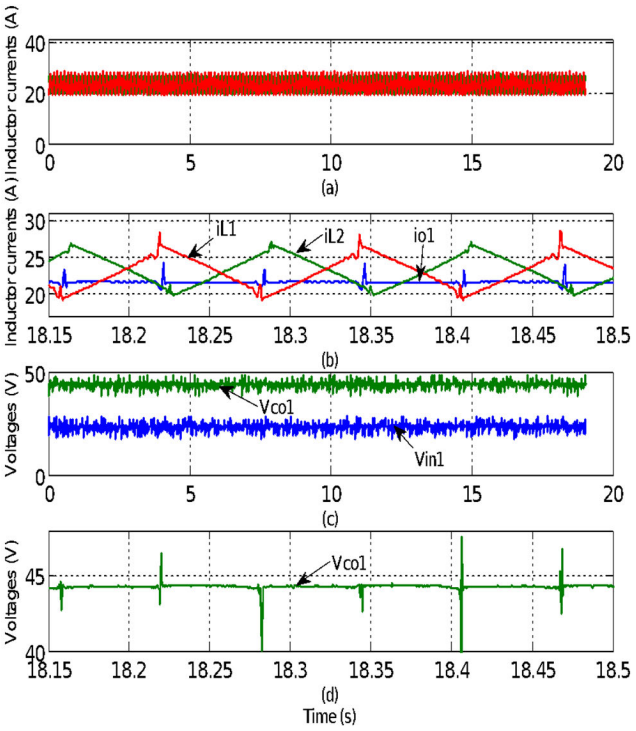


FIGURE 24. Currents and voltages of 1st stage (Experimental results) at $T_s = 20\mu s$, $F_{sw} = 10kHz$: (a) inductors and terminal currents, (b) zoom of (a), (c) input and output voltages, and (d) zoom of (c). $V_B = 24V$, $I_B = 45.7A$, $P_B = 1096W$, $P_{o1} = 960W$, $D_1 = 0.5$.

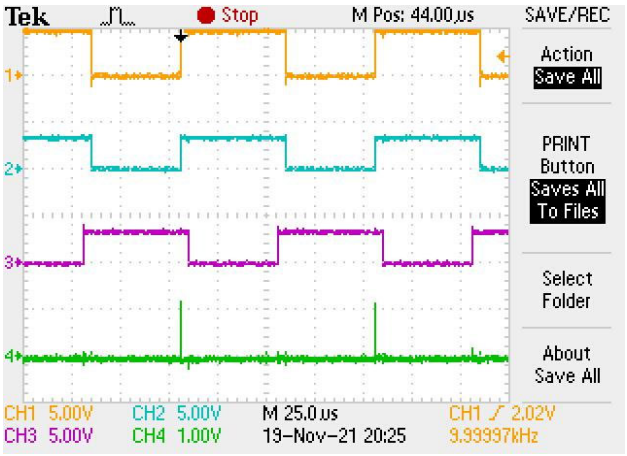


FIGURE 25. Generated PWM control pulse (dSPACE) and the driver control signals (FPGA) for 2nd stage.

FPGA. Figure 28 shows the measured waveforms for inductors currents and capacitors voltages. At load of $i_o = 6.2A$, inductors currents i_{L5} and i_{L6} fluctuate between 8A and 18A at D = 0.44. A phase shift of 180° is observed between i_{L5} and i_{L6}, as demonstrated in Fig. 28 (a) and (b). Input and output voltages are sensed and recorded in Fig. 28 (c) and (d). In this stage, Vco3 = Vco4 = 228.5V with voltage boosting G = 327/130 = 2.5 times with efficiency of 87.3%. It could be observed that the notches in the inductor currents are also decreased due to the earthed shield.

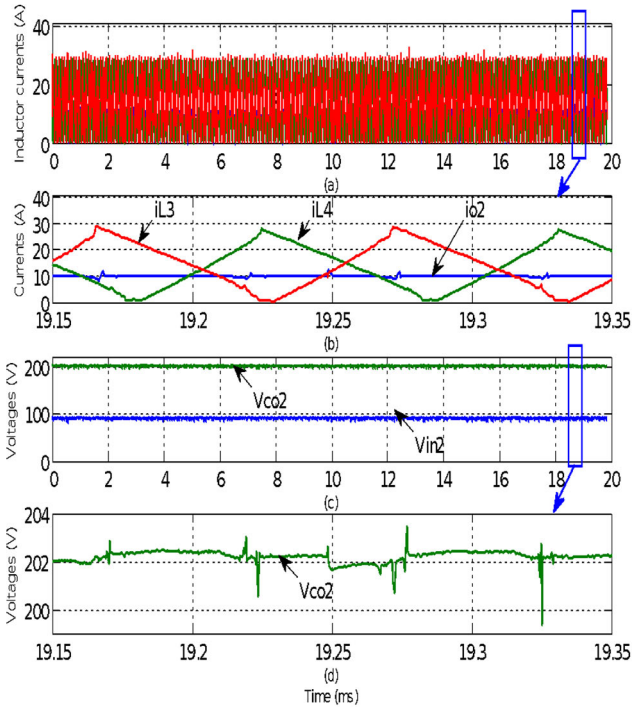


FIGURE 26. Currents and voltages of 2nd stage (Experimental results) at $T_s = 20\mu s$, $F_{sw} = 10kHz$,: (a) inductors and terminal currents, (b) zoom of (a), (c) input and output voltages, and (d) zoom of (c). $V_{o1} = 90V$, $I_{o1} = 27.3A$, $P_{o1} = 2457W$, $P_{o2} = 2000W$, $D_2 = 0.5413$.

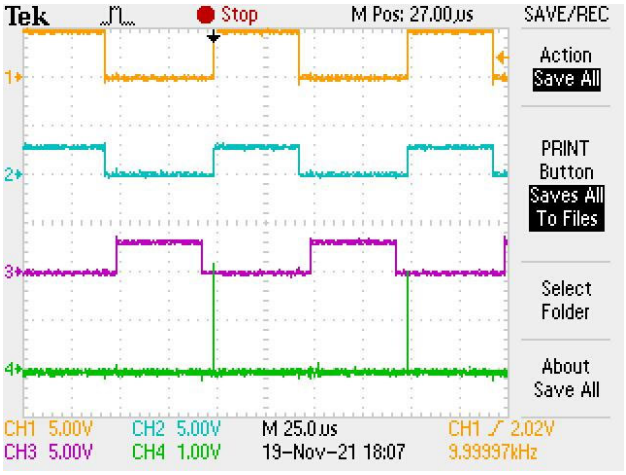


FIGURE 27. Generated PWM control pulse (dSPACE) and the driver control signals (FPGA) for 3rd stage.

D. MEASURED EFFICIENCY

IILFOC loss is classified into 1) switching losses, 2) inductor losses, and 3) conductive losses. It is important to highlight that the inductor's loss is a main loss source whose estimation precisely is a difficult task. In brief, as a matter of hardware constraints, the IILFOC's efficiency will not be very high. Many experimental tests are performed in the proposed converter. Different input voltages have been applied at different duties and the output voltages and currents have been recorded. From experimental readings, the measured

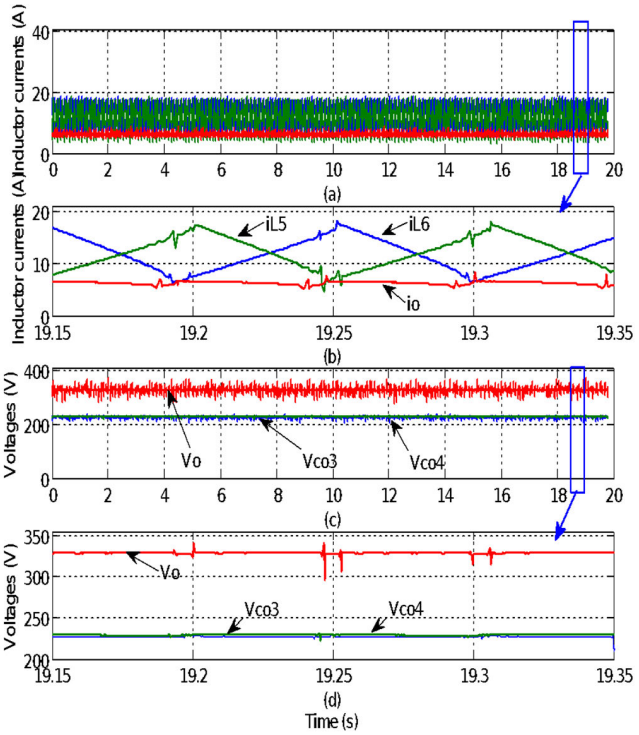


FIGURE 28. Currents and voltages of 3rd stage (Experimental results) at $T_s = 20\mu s$, $F_{sw} = 10kHz$: (a) inductors and terminal currents, (b) zoom of (a), (c) input and output voltages, and (d) zoom of (c). $V_{o2} = 130V$, $I_{o2} = 17.6A$, $P_{o2} = 2290W$, $V_o = 327V$, $I_o = 6.2A$, $P_{o2} = 2029W$, $D_3 = D_4 = 0.44$.

efficiency is related to the output power as demonstrated in Fig. 29. It is possible to optimize efficiency by considering soft-switching technology as well as considering components of low losses. Moreover, optimization of modulation duties for the three stages can be considered.

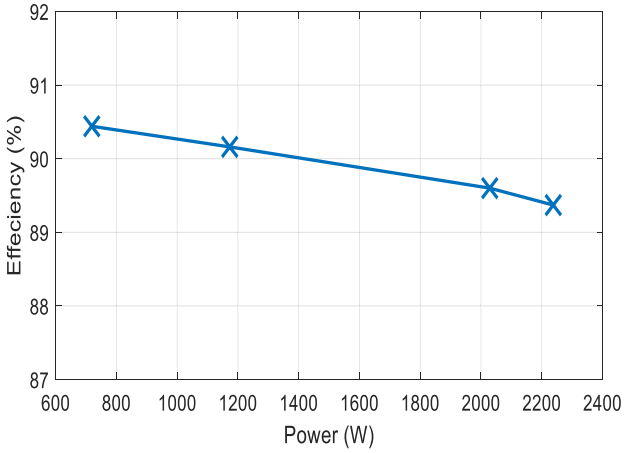


FIGURE 29. Measured efficiency versus the output power.

From the assessed simulation and experimental results, it could be noticed that this topology suffers from some limitations such as the EMI problem, and too many modes of operation making controlling the topology a hard task.

Moreover, the large number of topology components and narrow duty range are serving as disadvantages to this topology. Therefore, intensive work is in progress to enhance the simulated results. Hence, a new and innovative nonlinear control system is in the implementation phase to optimize the performance, especially at different load conditions and different voltage levels.

VI. CONCLUSION AND FUTURE PERSPECTIVES

A high-gain DC/DC converter topology is obtained through double interleaved-input cascaded stages and double float-output stage with bidirectional current capability for battery-based EVs. The paper first presented the design procedures and its characteristics, operating modes and analyzed them in detail along with modelling the system under study. Simulation and experimental results of a prototype converter then validate the predicted low-ripple I/O currents due to application of interleaved technique.

The quantitative amount of the contribution is concluded in the following table:

TABLE 5. Quantitative amount of the contribution.

	Duty	Boosting times	Current ripples in inductors	Efficiency
In simulation				
Stage 1	0.77	3.75	18 %	------
Stage 2	0.64	2.78	96 %	------
Stage 3	0.41	2.40	100 %	------
In experiments				
Stage 1	0.5	1.80	------	87.5 %
Stage 2	0.54	2.24	------	81.4 %
Stage 3	0.44	2.50	------	87.3 %

Lower average ripples in inductors (71.3%) are obtained compared to that of [32] (114.2%). For the stated duties, the proposed converter can generate a voltage with 25 and 10 times greater than the input side voltage theoretically and in implementation, respectively.

Simulation results demonstrated that the suggested converter has the below merits for EVs applications fed by battery or even FC: (i) Sharing of high input currents produced by input interleaved stage, (ii) Sharing of high output voltage produced by output double float stage, (iii) Redundancy of current paths and voltage terminals, and (iv) Minimizing of the input current and output voltage fluctuations.

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