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RESEARCH ARTICLE

# Digital Linear Slope Control for Boost Converter to Improve Load Transient

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**ABSTRACT** Digital linear slope control (DLSC) method is proposed to attenuate the undershoot and overshoot of the output voltage of a boost converter during the load transient without sensing current. The proposed DLSC method adjusts the slope of the control signal to improve the load transient response. DLSC requires the information of output voltage only and is realized by adding only a few lines of extra program code to the conventional VMC. A mathematical analysis is performed to demonstrate the viability of the DLSC method, and the corresponding algorithms are introduced. A 10 V-15 V, 100-W boost converter operating at 100-kHz switching frequency was built and experimented to validate the effectiveness of the DLSC technique.

**INDEX TERMS** Digital control, boost converter, load transient, voltage deviation, linear slope control, transient response, voltage mode control, overshoot and undershoot.

## I. INTRODUCTION

DC-DC boost converters are widely implemented in various applications such as portable devices, electrified vehicles, and renewable energy systems due to its simple structure, low cost, and high-power efficiency [1], [2], [3], [4]. However, unlike buck converters, the presence of the right-half-plane zero (RHPZ) of duty-to-output-voltage transfer function in continuous conduction mode poses a challenge in designing high-performance controllers [5], [6], [7], [8], [9], [10], [11], [12].

Voltage mode control (VMC) is one of the simplest control methods for DC-DC converters. The VMC utilizes a compensator to adjust the unity gain bandwidth (UGB) and phase margin of the loop gain for desired transient response and stability of a converter. Yet, the RHPZ of a boost converter limits the maximum UGB, which causes poor transient performance such as high undershoot and overshoot in the output voltage and long settling time.

Extensive research has been carried out to enhance the transient performance. One of the representative methods is current-mode control such as peak, average, valley current control [2], [13], [14]. The current-mode control attenuates the effect of the RHPZ by using two loops–inner loop for inductor current and outer loop for output voltage control. The two-loop control simplifies the design of a compensator by changing a quadratic pole of the power stage into a single pole [2].

Although the current-mode control increases UGB, its use may be limited in high power application because of the bulky and costly circuitry for current sensing. To overcome the disadvantage of the current-mode control, $V^2$ control method was introduced in [15], [16], [17], [18], and [19]. The current sensor is not required for $V^2$ control because the output voltage ripple provides the information of the inductor current. However, the conventional $V^2$ control, originally intended for

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buck converters, cannot be applied to boost converters due to the discontinuous current flow in their output capacitors [15]. Therefore, valley $V^2$ control method is especially utilized for boost converters [15], [16]. While these $V^2$ control methods are attractive for improving the transient response without inductor current sensing, high equivalent series resistance (ESR) of the output capacitor degrades the performance of a converter [16].

With the advancement and decreasing price of digital control processors, digital control in DC-DC converters has become widespread. Real-time tuning improves the transient response by enhancing the digital controllers during load changes [20], [21], [22], [23], [24], [25], [26]. Converting complex and expensive analog circuits into digital codes facilitates the implementation of various control methods [27], [28], [29], [30], [31]. Nevertheless, many digital control techniques require more sensors or complicated algorithms than the VMC.

In this paper, A digital linear slope control (DLSC) method is proposed for the boost converter to mitigate the overshoot and undershoot of the output voltage during a load transient. The DLSC modulates the slope of the control signal $v_c$ during the load transient to attenuate the output voltage deviation. The proposed method is realized by detecting the output voltage $v_o$ only without requiring any additional hardware such as current sensors. Algorithm for the DLSC is constructed using addition and subtraction operations to reduce the workload on a microcontroller unit (MCU).

This paper is structured as follows: Section II provides an explanation of the proposed DLSC method. In Section III, the algorithms to implement the DLSC method are presented. Experimental results are discussed in Section IV, followed by conclusions in Section V.

## II. DIGITAL LINEAR SLOPE CONTROL METHODS

The schematic of the boost converter with the proposed DLSC method is depicted in Fig. 1. The circuit elements $Q_1$, $Q_2$, $L$, $C$, and $R$ are the low-side switch, high-side switch, input inductor, output capacitor, and load resistance, respectively. Currents through $L$, $C$, and $R$ are denoted as $i_L$, $i_c$, and $i_o$. The input and output voltages are expressed as $V_g$ and $v_o$, respectively.

The DLSC controller block (yellow shaded area in Fig. 1), which consists of load transient detector (LTD), step-up transient mode, and step-down transient mode, is added to the voltage-mode control loop of the conventional VMC. The analog output of the voltage sensor is transformed into the digital signal $v_{o.sen}$ through an analog-to-digital converter (ADC) in MCU. The LTD receives $v_{o.sen}$ and generates the signal *flag*. The output of the step-up transient mode, step-down transient mode, and conventional VMC mode are defined as $v_{cu}$, $v_{cd}$, and $v_{cc}$, respectively. If *flag* is 1, $v_c$ becomes $v_{cc}$ based on the error signal $v_e$, which is equal to $v_{o.sen} - v_{ref}$. When *flag* is set 2, $v_c$ switches to $v_{cd}$ that decreases linearly with the slope -$m_d$. If *flag* is 3, $v_c$ becomes $v_{cu}$ which increases linearly with the slope $m_u$. The gate

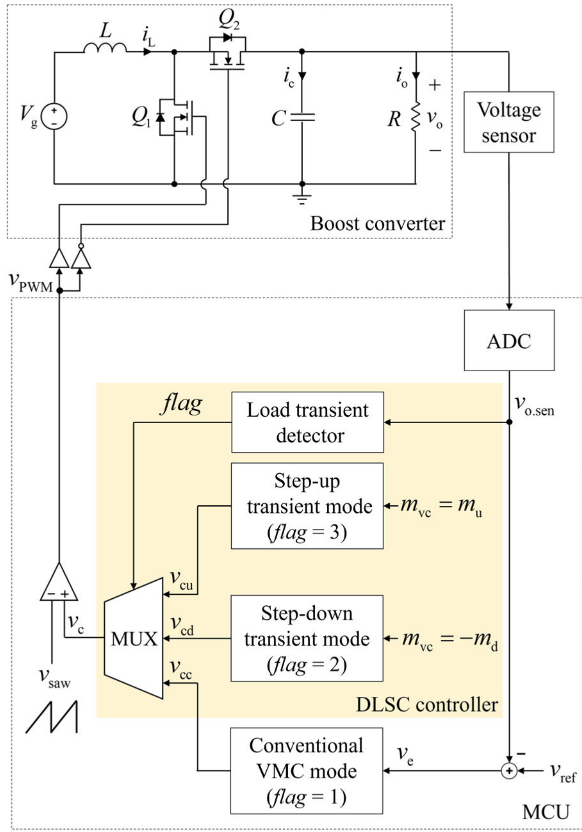


**FIGURE 1. The schematic of a boost converter with the proposed DLSC method.**

signal $v_{PWM}$ is finally generated by comparing the saw-tooth waveform $v_{saw}$ and $v_c$.

### A. OPERATION OF DIGITAL LONEAR SLOPE CONTROL

Fig. 2 illustrates the operation of the proposed DLSC. Four threshold voltages such as $V_{thd1}$, $V_{thd2}$, $V_{thu1}$, and $V_{thu2}$ are set by the LTD to detect load transients. When $v_o$ reaches each threshold voltage, *flag* changes to determine the operation mode of DLSC. The blanking windows A, B, C, and D are also configured by the LTD. The lengths of the blanking windows are defined as $T_A$, $T_B$, $T_C$, and $T_D$, respectively. During each blanking window, the LTD stops working to prevent inappropriate operation due to noise signals.

When the load current steps down, $v_o$ exhibits an overshoot. Once $v_o$ reaches $V_{thd1}$ at $t_{d1}$, *flag* changes from 1 to 2. The blanking window A is triggered during $T_A$, pausing the LTD until $t_{d2}$. When $v_o$ hits $V_{thd2}$, *flag* is reset to 1 to recover the operation of the conventional VMC. The LTD remains idle during $T_B$ to allow $v_o$ to stabilize in a steady state.

Conversely, $v_o$ experiences an undershoot during the step-up load transient. Upon $v_o$ reaching $V_{thu1}$ at $t_{u1}$, *flag* switches from 1 to 3. The blanking window C is activated during $T_C$, causing the LTD to halt until $t_{u2}$. Once $v_o$ reaches $V_{thu2}$, *flag* reverts to 1, resuming the operation by conventional VMC. The blanking window D continues during $T_D$ before $v_o$ reaches the steady state. The aforementioned

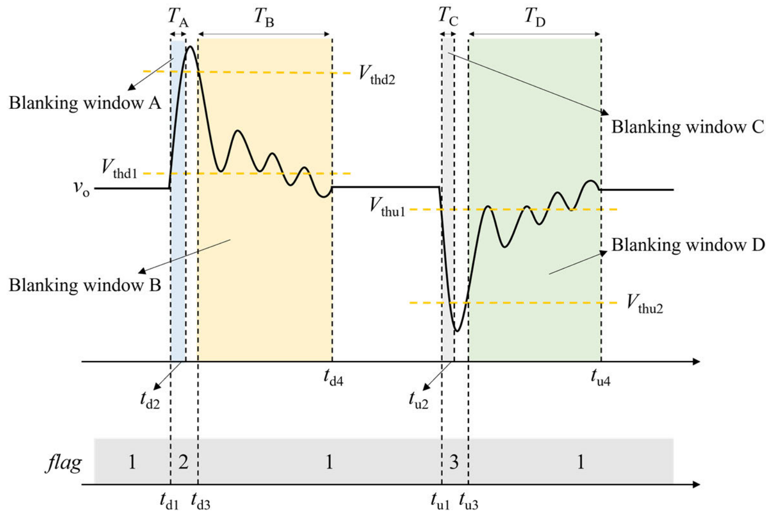


**FIGURE 2.** **The operation of the proposed DLSC method.**

sequences repeat throughout the operation of the boost converter to reduce the overshoot and undershoot of $v_o$ during the load transient.

## B. OVERSHOOT DURING THE STEP-DOWN LOAD TRANSIENT

The key waveforms of the boost converter with DLSC during the step-down load transient are illustrated in Fig. 3. The averaged $i_L$ and $i_c$ are expressed as $i_{L.avg}$ and $i_{c.avg}$, respectively. The peak-to-peak voltage of $v_{saw}$ is defined as $V_M$. When $i_o$ decreases from $I_{o1}$ to $I_{o2}$, $v_o$ starts to increase. The controller operates by the conventional VMC mode until $v_o$ reaches the $V_{thd1}$. If $v_o$ reaches $V_{thd1}$ at $t_1$, the first interval of the step-down transient mode begins. Until the end of $i$-th interval or $t_{i+1}$, $i_o(t)$ decreases to $I_{o2}$ with the slope of $m_o$ as (1) and then keeps $I_{o2}$ after $t_{i+1}$.

$$i_o(t) = m_o(t - t_0) + I_{o1} \tag{1}$$

Accessing $v_c(t_1)$ from the memory of MCU enables straightforward calculation of $v_{cd}$ as (2).

$$v_{cd}(t) = v_c(t_1) - m_d(t - t_1) \tag{2}$$

Because $v_c(t)$ should have discrete values in MCU, its calculation is derived as (3) after $t_1$.

$$v_c(t) = \lfloor v_{cd}(t) \rfloor \tag{3}$$

The symbol $\lfloor x \rfloor$ in (3) indicates rounding down $x$. When $T_i$ in Fig. 3 is defined by (4), $i_L(t_{i+1})$ is derived as (5) with $m_{Li}$ calculated as (6).

$$T_i = \left(1 - \frac{v_c(t_i)}{V_M}\right) T_s \tag{4}$$

$$i_L(t_{i+1}) = i_L(t_i) + m_{Li} T_s \tag{5}$$

$$m_{Li} = \frac{V_g T_s - v_o(t_i) T_i}{L T_s} \tag{6}$$

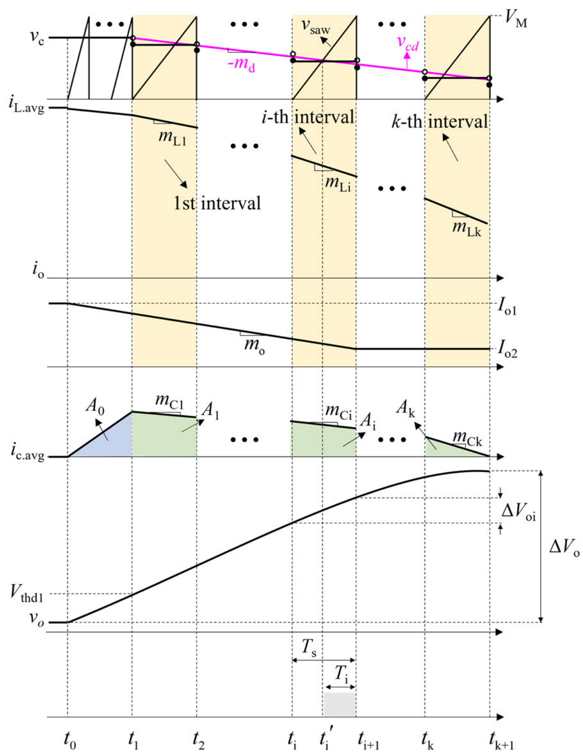


**FIGURE 3.** **The key waveforms during the step-down load transient with the DLSC method.**

In Fig. 4, $i_c$ tracks -$i_o$ from $t_i$ to $t_i$' and follows $i_L(t)$-$i_o(t)$ from $t_i$' to $t_{i+1}$. As a result, $i_{c.avg}(t)$ is determined as (7) using (8).

$$\begin{aligned} i_{c.avg}(t_{i+1}) &= \frac{1}{T_s}\left(\int_{t_i}^{t_i+T_s-T_i} -i_o(t)\,dt + \int_{t_i+T_s-T_i}^{t_{i+1}} i_L(t) - i_o(t)\,dt\right) \\ &= i_{c.avg}(t_i) + m_{ci} T_s \end{aligned} \tag{7}$$

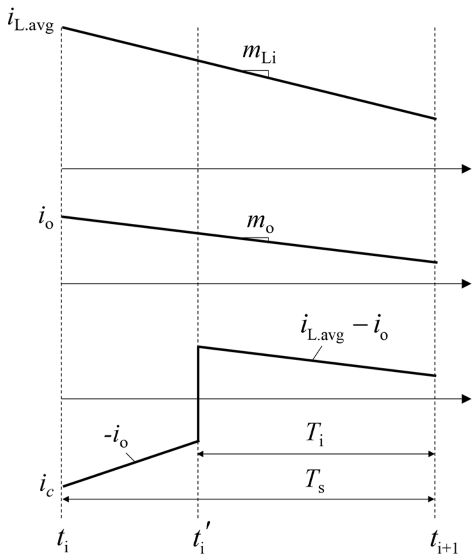


**FIGURE 4.** The waveforms of $i_{L.avg}$, $i_o$, and $i_c$ during $i$-th interval.

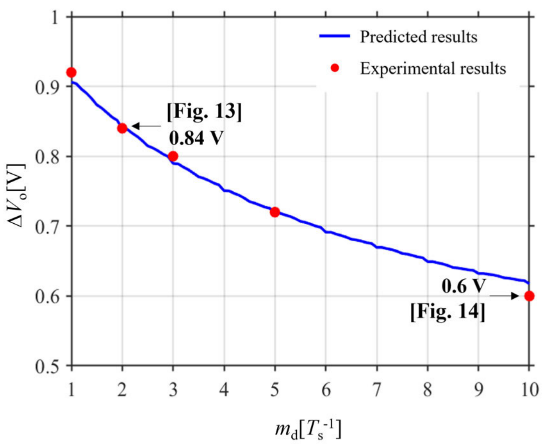


**FIGURE 5.** The variation of $\Delta V_o$ according to $m_d$.

$$m_{ci} = \left(-m_o + m_{Li}\left(1 - \frac{v_c(t_{1i})}{V_M}\right)\left(1 + \frac{v_c(t_{1i})}{V_M}\right)\right) \tag{8}$$

The blue shaded area $A_0$ in Fig. 3 is calculated using $v_o(t_0)$, $V_{thd1}$, and $C$ as (9) and $i_c(t_1)$ is calculated as (10).

$$A_0 = C\left(V_{thd1} - v\left(t_0\right)\right) \tag{9}$$

$$i_{c.avg}\left(t_1\right) = \sqrt{-2A_0 m_o} \tag{10}$$

Equation (11) calculates $A_i$, and (12) determines the output voltage deviation in the $i$-th interval $\Delta V_{oi}$.

$$A_i = \frac{\left(i_c\left(t_i\right) + i_c\left(t_{i+1}\right)\right) T_s}{2} \tag{11}$$

$$\Delta V_{oi} = \frac{A_i}{C} \tag{12}$$

The calculation of $v_o(i+1)$ is computed by (13) and the total voltage deviation $\Delta V_o$ is derived as (14) through $k$ iterations of (1)-(13) until $\Delta V_{oi}$ falls below zero.

$$v_o\left(t_{i+1}\right) = v_o\left(t_i\right) + \Delta V_{oi} \tag{13}$$

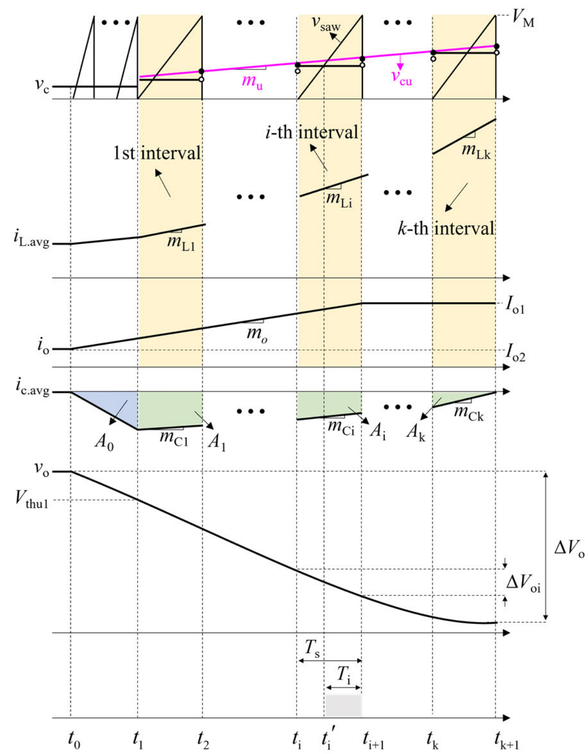


**FIGURE 6.** The key waveforms during the step-up load transient with the DLSC method.

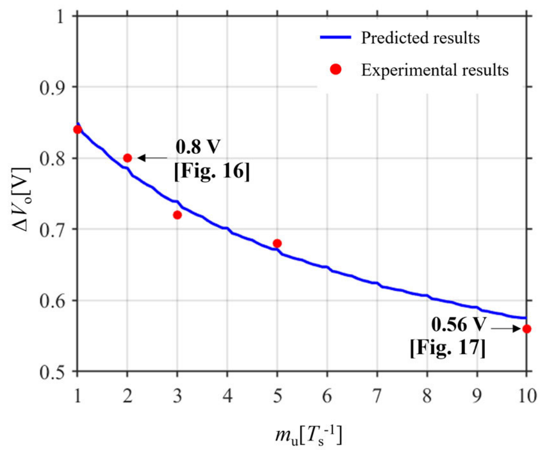


**FIGURE 7.** The variation of $\Delta V_o$ according to $m_u$.

$$\Delta V_o = \sum_{i=0}^{k} \Delta V_{oi} \tag{14}$$

The blue curve in Fig. 5 is derived from (1)-(14) and shows that increasing $m_d$ enables the decrease of $\Delta V_o$.

### C. UNDERSHOOT DURING THE STEP-UP LOAD TRANSIENT

The key waveforms of the boost converter with DLSC during the step-up load transient are illustrated in Fig. 6. When $i_o$ increases from $I_{o2}$ to $I_{o1}$, $v_o$ begins to decrease. The conventional VMC regulates $v_o$ until it hits $V_{thu1}$. If $v_o$ reaches $V_{thu1}$ at $t_1$, the step-up transient mode begins. Until the end of $i$-th

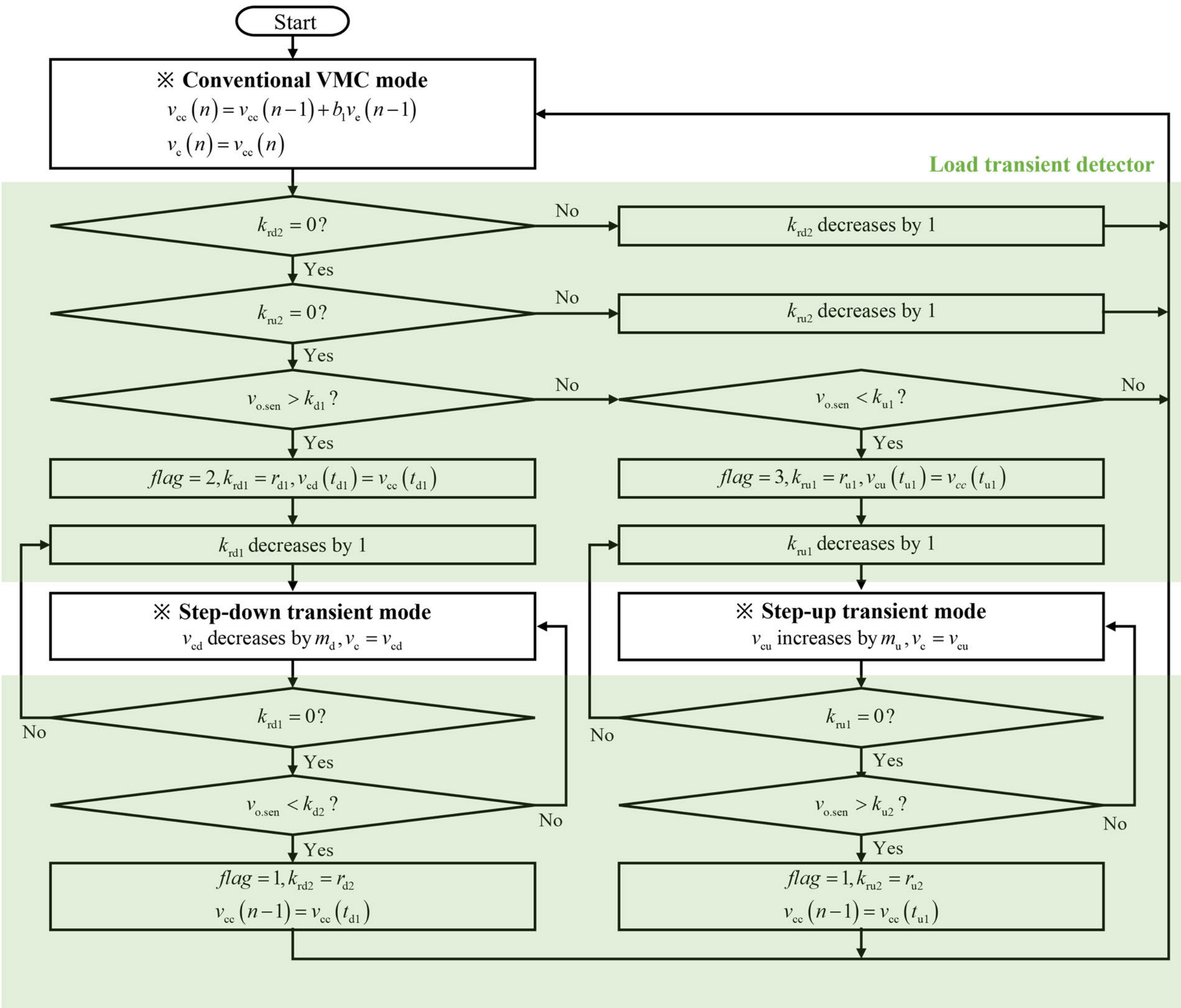


**FIGURE 8.** The flowchart of the proposed DLSC method.

interval or $t_{i+1}$, $i_o(t)$ increases to $I_{o1}$ with the slope of $m_o$ as (15) and then keeps $I_{o1}$ after $t_{i+1}$.

$$i_o(t)=m_o(t-t_0)+I_{o2} \tag{15}$$

Accessing $v_c(t_1)$ from the memory of MCU enables straightforward calculation of $v_{cu}$ as (16).

$$v_{cu}(t)=v_c(t_1)+m_u(t-t_1) \tag{16}$$

Because $v_c(t)$ should have discrete values in MCU, its calculation is derived as (17) after $t_1$.

$$v_c(t)=\lfloor v_{cu}(t)\rfloor \tag{17}$$

The blue shaded area $A_0$ in Fig. 6 is calculated with $v_o(t_0)$, $V_{thu1}$, and $C$ as (18) and $i_{c.avg}(t_1)$ is calculated as (19).

$$A_0=C\left(V_{thu1}-v(t_0)\right) \tag{18}$$

$$i_{c.avg}(t_1)=\sqrt{2A_0m_o} \tag{19}$$

Eqs. (4)-(8) and (11)-(14) are again used to compute $\Delta V_o$ during the step-up load transient. The blue line in Fig. 7 is obtained from (4)-(8) and (11)-(19) and illustrates that increasing $m_u$ achieves the decrease in $\Delta V_o$.

## III. ALGORITHM FOR THE PROPOSED METHOD

The flow chart in Fig. 8 illustrates how the proposed DLSC works. The LTD is realized by the simple blocks in green shaded area. The other blocks are for the three operation modes shown in Fig. 1: step-up transient mode, step-down transient mode, and conventional VMC mode.

The LTD has eight parameters: $k_{d1}$, $k_{d2}$, $k_{u1}$, $k_{u2}$, $k_{rd1}$, $k_{rd2}$, $k_{ru1}$, and $k_{ru2}$. The parameters $k_{d1}$, $k_{d2}$, $k_{u1}$, and $k_{u2}$ determine the threshold voltages in Fig. 2 as (20)-(23) where $k_{ADC}$ and $k_v$ represent the gains of the ADC and the voltage sensor, respectively.

$$V_{thd1}=\frac{k_{d1}}{k_{ADC}k_v} \tag{20}$$

$$V_{thd2}=\frac{k_{d2}}{k_{ADC}k_v} \tag{21}$$

$$V_{thu1}=\frac{k_{u1}}{k_{ADC}k_v} \tag{22}$$

**Conventional VMC mode**

```
v_e[1] = v_e[0];
v_e[0] = V_ref - v_o.sen;
v_cc[0] = v_cc[1] + b_1*v_e[1]
v_c = v_cc[0];
```

(a)

**Step-down transient mode**

```
if (flag == 2)
 {
  k_rd1--;
  v_cd -= m_d;
  v_c = v_cd;
  V_ccR = v_cc[0]
}
```

(b)

**Step-up transient mode**

```
if (flag == 3)
 {
  k_ru1--;
  v_cu += m_u;
  v_c = v_cu;
  V_ccR = v_cc[0]
}
```

(c)

**Load transient detector**

```
if (v_o.sen > k_d1 && flag == 1 && k_rd2 == 0)
{
 flag = 2;
 k_rd1 = r_d1;
 v_cd = v_c;
}
if (v_o.sen < k_u1  && flag == 1 && k_ru2 == 0)
 {
  flag = 3;
  k_ru1 = r_u1;
  v_cu = v_c;
 }
if (flag == 1 && k_rd2 > 0)
{
 k_rd2--;
 }
if (flag == 1 && k_ru2 > 0)
{
 k_ru2--;
}
```

```
if (v_o.sen < k_d2 && k_rd1 == 0)
 {
  flag = 1;
  v_cc[0] = V_ccR;
  v_cc[1] = V_ccR;
  k_rd2 = r_d2;
 }
if (v_o.sen > k_u2 && k_ru1 == 0)
 {
  flag = 1;
  v_cc[0] = V_ccR;
  v_cc[1] = V_ccR;;
  k_ru2 = r_u2;
  }
```

(d)

**FIGURE 9.** The pseudo code for the proposed DLSC: (a) conventional VMC mode, (b) step-down transient mode, (c) step-up transient mode, and (d) load transient detector.

**TABLE 1.** Specification for the Prototype Boost Converter.

| Name | Value | Description |
|---|---|---|
| $T_s$ | 10 µs | Switching period |
| $f_s$ | 100 kHz | Switching frequency |
| $V_g$ | 10 V | Input voltage |
| $v_o$ | 15 V | Output voltage |
| $C$ | 600 µF | RFS-50V470MH4 (Elna) |
| $L$ | 20 µF | B82559A023A024 (EPCOS) |
| $Q_1$, $Q_2$ | - | STP140N6F7(STMicroelectronics) |
| Gate driver | - | IR2184 (Infineon Technologies) |

$$V_{\text{thu2}} = \frac{k_{\text{u2}}}{k_{\text{ADC}} k_{\text{v}}} \tag{23}$$

The periods of the blanking windows in Fig. 2 are configured by setting $k_{\text{rd1}}$, $k_{\text{rd2}}$, $k_{\text{ru1}}$, and $k_{\text{ru2}}$ as (24)-(27).

$$T_{\text{A}} = k_{\text{rd1}} T_{\text{s}} \tag{24}$$

$$T_{\text{B}} = k_{\text{rd2}} T_{\text{s}} \tag{25}$$

$$T_{\text{C}} = k_{\text{ru1}} T_{\text{s}} \tag{26}$$

$$T_{\text{D}} = k_{\text{ru2}} T_{\text{s}} \tag{27}$$

The LTD is activated when $k_{\text{rd2}} = k_{\text{ru2}} = 0$. The DLSC operates in the conventional VMC mode with an integrator where the coefficient of $v_{\text{e}}(n\text{-}1)$ is set to $b_1$ during the steady state, $T_{\text{B}}$ and $T_{\text{D}}$ in Fig. 2. When the LTD is activated and

**TABLE 2.** Parameters for the Proposed DLSC Method.

| Name | Value | Description |
|---|---|---|
| $b_1$ | 0.0003 | Coefficient for the conventional VMC |
| $k_{\text{d1}}$ | 2360 | $V_{\text{thd1}} = 15.22$ V |
| $k_{\text{d2}}$ | 2430 | $V_{\text{thd2}} = 15.68$ V |
| $k_{\text{u1}}$ | 2290 | $V_{\text{thu1}} = 14.8$ V |
| $k_{\text{u2}}$ | 2220 | $V_{\text{thu1}} = 14.3$ V |
| $k_{\text{rd1}}$ | 9 | $T_{\text{A}} = 90$ µs |
| $k_{\text{rd2}}$ | 100 | $T_{\text{B}} = 1$ ms |
| $k_{\text{ru1}}$ | 9 | $T_{\text{C}} = 90$ µs |
| $k_{\text{ru2}}$ | 100 | $T_{\text{D}} = 1$ ms |

$v_{\text{o.sen}}$ exceeds $k_{\text{d1}}$, the step-down transient mode is initiated with *flag* being 2. Once the step-down transient mode is activated, $k_{\text{rd1}}$ and $v_{\text{cd}}(t_{\text{d1}})$ are set to $r_{\text{d1}}$ and $v_{\text{cc}}(t_{\text{d1}})$, respectively. At the same time, $v_{\text{cc}}(t_{\text{d1}})$ remains in the memory of MCU. In every switching period $T_{\text{s}}$, $k_{\text{rd1}}$ decreases by 1 and $v_{\text{c}}$ decreases by $m_{\text{d}}$ until $k_{\text{rd1}}$ reaches zero. If $k_{\text{rd1}}$ becomes zero, the LTD waits for $v_{\text{o.sen}}$ to drop below $k_{\text{d2}}$ and then changes *flag* to 1. Upon transitioning the step-down load transient mode into the conventional VMC mode, $k_{\text{rd2}}$ is set to $r_{\text{d2}}$ and $v_{\text{cc}}(n\text{-}1)$ is set to $v_{\text{cc}}(t_{\text{d1}})$.

If $v_{\text{o.sen}}$ is equal to or smaller than $k_{\text{d1}}$ and smaller than $k_{\text{u1}}$, the proposed controller operates in the step-up load transient mode, changing *flag* to 3. At the beginning of the step-up load transient mode, $k_{\text{ru1}}$ and $v_{\text{cu}}(t_{\text{u1}})$ are assigned to $r_{\text{u1}}$ and $v_{\text{cc}}(t_{\text{u1}})$, respectively. Simultaneously, $v_{\text{cc}}(t_{\text{u1}})$ is saved in the memory of MCU. In every $T_{\text{s}}$, $k_{\text{ru1}}$ decreases by 1 and $v_{\text{c}}$ increases by $m_{\text{u}}$ until $k_{\text{ru1}}$ reaches zero. If $k_{\text{ru1}}$ becomes zero, the LTD waits until $v_{\text{o.sen}}$ exceeds $k_{\text{u2}}$ and then changes *flag* to 1. When the operation mode returns into the conventional VMC mode, $k_{\text{ru2}}$ is set to $r_{\text{u2}}$ and $v_{\text{cc}}(n\text{-}1)$ is set to $v_{\text{cc}}(t_{\text{u1}})$.

Fig. 9 shows pseudo code for the proposed DLSC. The array X[k] represents X($n$-k), e.g., $v_{\text{e}}$ [1] denotes $v_{\text{e}}(n\text{-}1)$. The parameter $v_{\text{ccR}}$ is utilized to memorize $v_{\text{cc}}(t_{\text{d1}})$ and $v_{\text{cc}}(t_{\text{u1}})$ when the operation mode changes from the conventional VMC mode into the other operation modes. The conventional VMC mode, step-down transient mode, step-up transient mode, and the LTD are programmed in C language as in Figs. 9(a), 9(b), 9(c), and 9(d), respectively. The digital codes consist of a few conditionals and simple math functions such as subtraction and addition, aiming not to burden MCU excessively.

## IV. EXPERIMENTAL RESULTS

A prototype boost converter shown in Fig. 10 was built according to the specifications listed in Table 1 and tested using MCU, LAUNCHXL-280049C, manufactured by Texas Instruments. The load resistance $R$ in Fig. 1 was realized by the electronic load PLZ1005WH from KIKUSUI, while the voltage source $V_{\text{g}}$ in Fig. 1 was by the GEN100-15 from TDK- Lambda. The load change in the following experimental waveforms exhibits a slew rate of 8 A/ms which is the maximum current slew rate provided by PLZ1005WH. Table 2 shows the value of the parameters for DLSC method. The VMC controller was designed to have low bandwidth

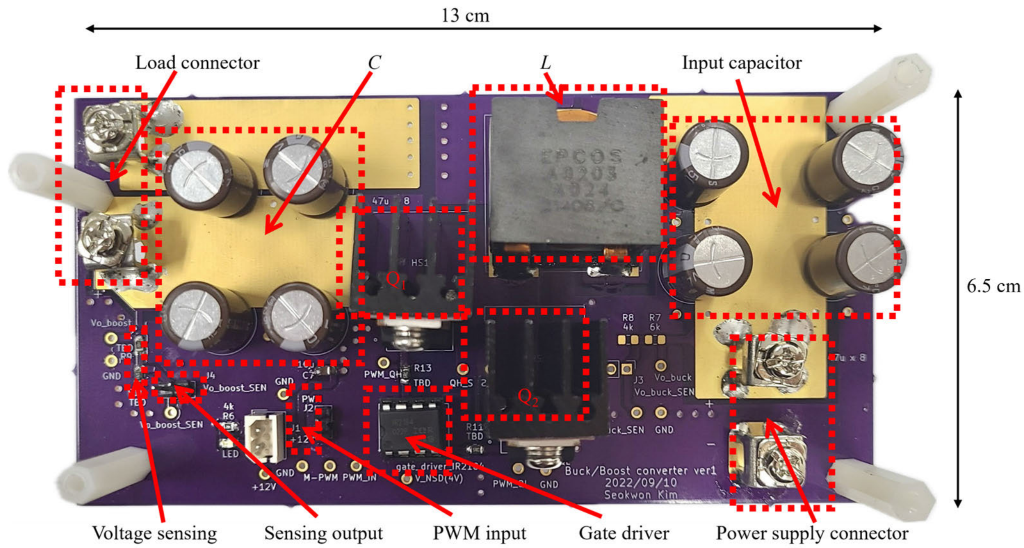


**FIGURE 10.** The photograph of the prototype boost converter to validate the proposed DLSC.

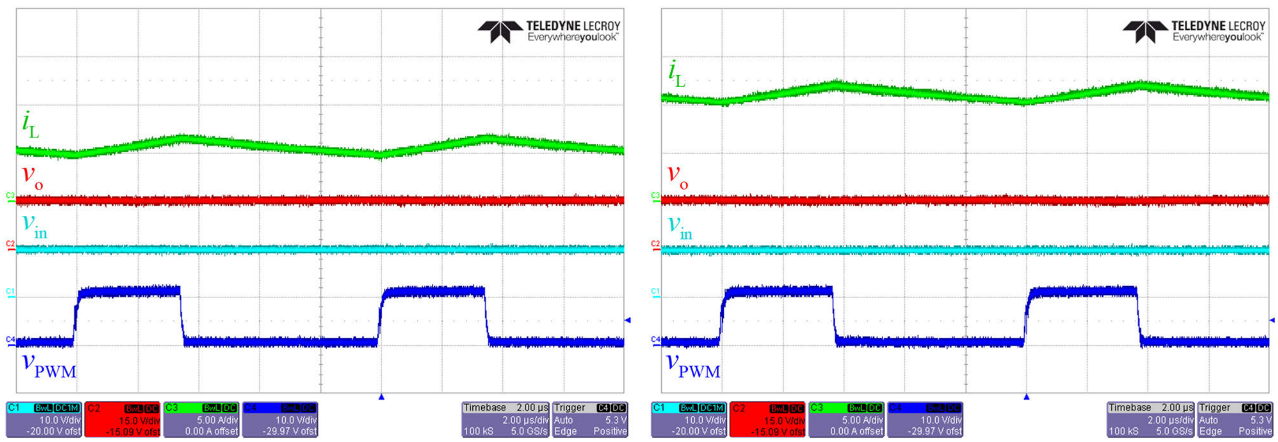


**FIGURE 11.** The experimental waveforms during the steady state at the output power of (a) 50 W and (b) 100 W.

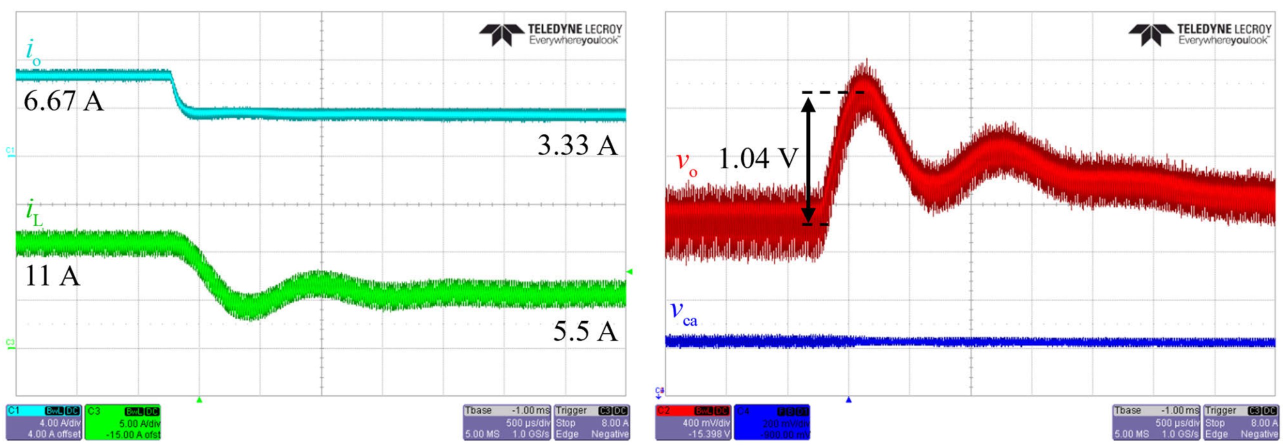


**FIGURE 12.** The experimental waveforms during the step-down load transient when the conventional VMC is applied.

such as a few hundred hertz by setting $b_1$ in Fig. 9(a) to 0.0003. The values of $k_{d1}$ and $k_{d2}$ were assigned 2360 and 2430 to set $V_{thd1}$ and $V_{thd2}$ to 15.22 V and 15.68 V, respectively. The voltages $V_{thu1}$ and $V_{thu2}$ were configured to 14.8 V and 14.3 V by setting $k_{u1}$ and $k_{u2}$ to 2290 and 2220, respectively. The lengths of the blanking windows A and C

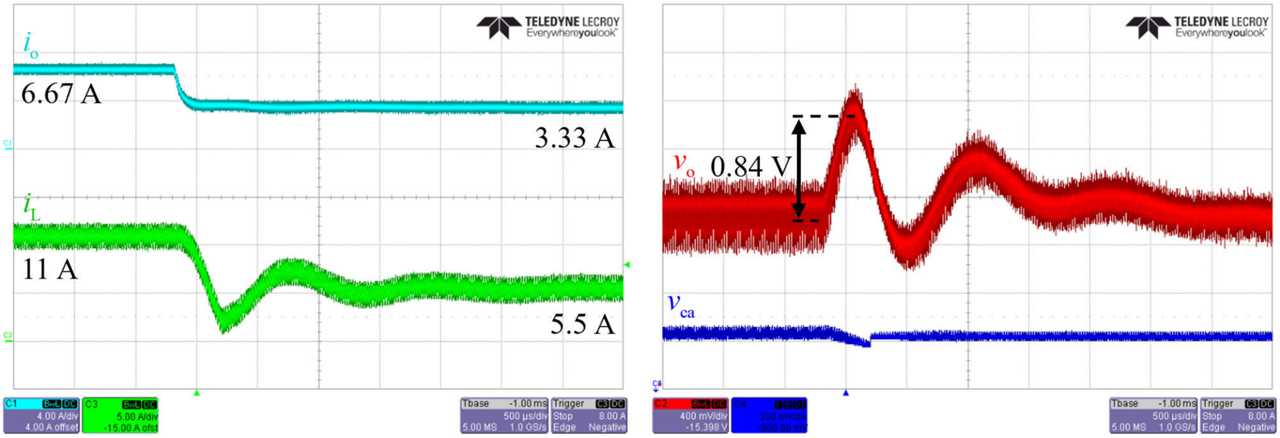


**FIGURE 13.** The experimental waveforms during the step-down load transient when the proposed DLSC is applied with $m_d = 2/T_s$.

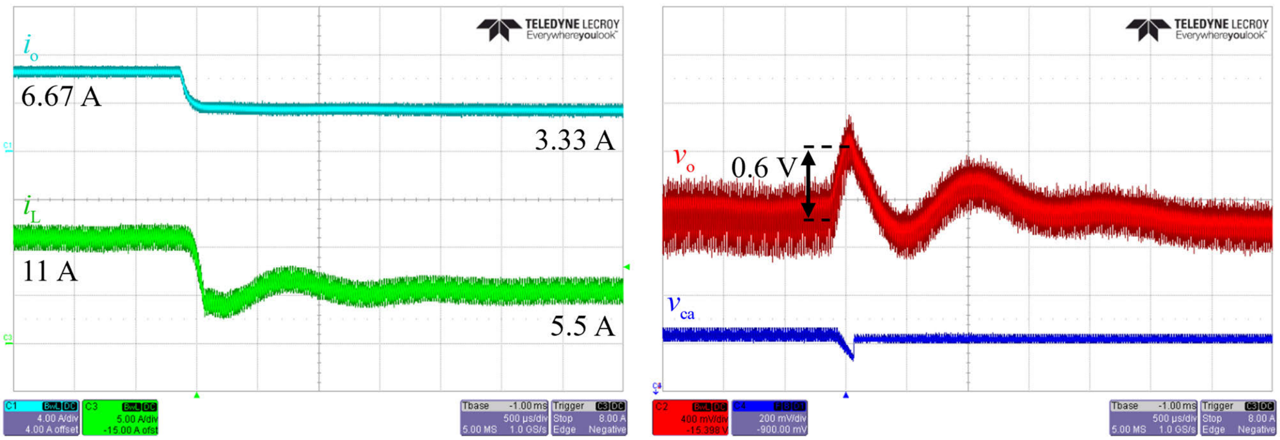


**FIGURE 14.** The experimental waveforms during the step-down load transient when the proposed DLSC is applied at $m_d = 10/T_s$.

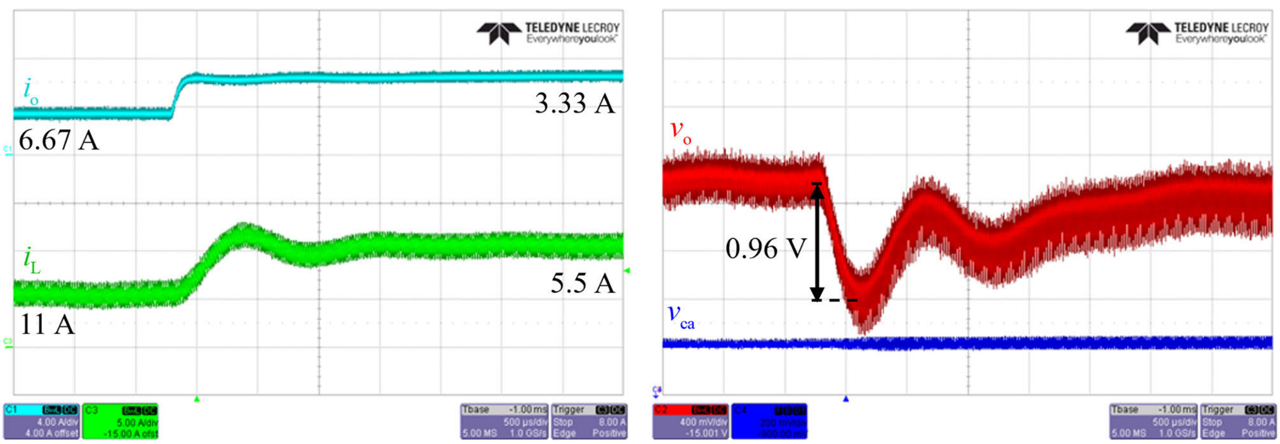


**FIGURE 15.** The experimental waveforms during the step-up load transient when the conventional VMC is applied.

were adjusted to $9T_s$ by setting both $k_{rd1}$ and $k_{rd2}$ to 9, determined by finding $i$ when $v_o$ is larger than $V_{thd2}$ and $V_{thu2}$ using (1)-(20). The lengths of blanking window B and D were set $100T_s$ by setting $k_{rd2}$ and $k_{ru2}$ to 100, which are longer than the settling time of the proposed DLSC.

Figs. 11-17 show the experimental waveforms of the prototype boost converter, demonstrating the performance of the proposed DLSC method. The experimental waveforms during the steady states outputting 50 W and 100 W are depicted in Figs. 11(a) and 11(b), respectively. The green, red, cyan, and blue traces correspond to $i_L$, $v_o$, $v_{in}$, and $v_{PWM}$, respectively. The time scale is 2 $\mu$s/div. Figs. 12-17 display the waveforms during the load transient, all in 500-$\mu$s/div. time scale. The cyan, green, and red traces correspond to

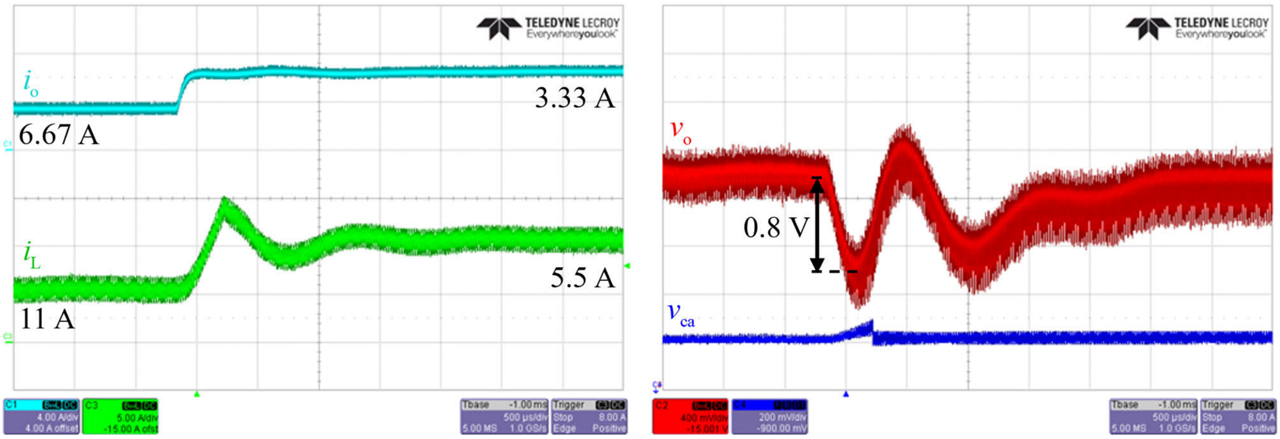


**FIGURE 16.** The experimental waveforms during the step-up load transient when the proposed DLSC is applied with $m_u = 2/T_s$.

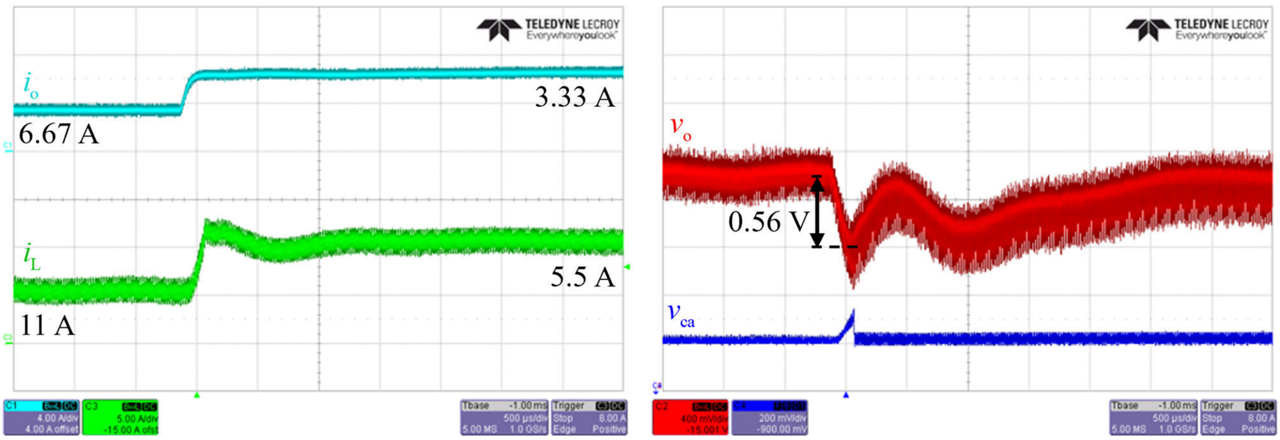


**FIGURE 17.** The experimental waveforms during the step-up load transient when the proposed DLSC is applied with $m_u = 10/T_s$.

**TABLE 3.** Required Circuit Components to Implement Four Control Methods.

| Control method | Conventional VMC [4] | Current mode control [2] | $V^2$ control [15] | Proposed control |
|---|---|---|---|---|
| Voltage sensor | O | O | O | O |
| Current sensor | X | O | X | X |
| High ESR output capacitor | X | X | O | X |

$i_o$, $i_L$, and $v_o$, respectively. The blue trace $v_{ca}$ represents $v_c$, which is converted into an analog signal according to (28).

$$v_{ca}(t) = \frac{3.3}{4096} v_c(t) \tag{28}$$

Figs. 12, 13, and 14 depict the waveforms observed during the step-down load transient from 6.67 A to 3.33 A. The conventional VMC was applied for Fig. 12 and $v_{ca}$ hardly changes during the load transient. This little change of $v_{ca}$ causes the large difference between $i_L$ and $i_o$ and thus considerable $\Delta V_o$ such as 1.04 V in Fig. 12. When the proposed DLSC is applied, $v_{ca}$ decreased with a constant slope $m_d$ during the load transient as shown in Figs. 13 and 14. When $m_d = 2/T_s$, $\Delta V_o$ was measured 0.84 V in Fig. 13, which was 80.8% of $\Delta V_o$ in Fig. 11. When $m_d$ was increased to $10/T_s$, $v_{ca}$ became steeper than when $m_d = 2/T_s$ as shown in Fig. 14. As a result, $i_L$ changes more rapidly to further reduce $\Delta V_o$ to 0.6 V, which represents 57.7% of $\Delta V_o$ by the conventional VMC. The experimental results during the step-down load transient were expressed by red dots in Fig. 5. The experimental results and the analysis conducted in Section II fit well together.

Figs. 15, 16, and 17 depict the waveforms observed during the step-up load transient from 3.33 A to 6.67 A. In Fig. 15, $\Delta V_o$ was measured as 0.96 V using the conventional VMC due to little variation in $v_c$. The operations with the proposed DLSC applied are in Figs. 16 and 17 where $v_{ca}$ linearly increased with the slope of $m_u$ during the step-up load transient. In Fig. 16, $\Delta V_o$ was 0.8 V when $m_u = 2/T_s$, accounting for 87.5% of $\Delta V_o$ in Fig. 15. When $m_u$ was increased to $10/T_s$, $\Delta V_o$ was measured as 0.56 V in Fig. 17, representing 58.3% of $\Delta V_o$ measured in Fig. 15. The experimental results during the step-up load transient were expressed by red dots in Fig. 7. The experimental results and the analysis conducted in Section II fit well together.

Table 3 compares the required circuit components for the four representative control methods: conventional VMC [4], current mode control [2], $V^2$ control [15], and proposed control. The proposed control does not require additional components compared to the conventional VMC as shown in Table 3 while it exhibited better performance as demonstrated in the experimental results.

## V. CONCLUSION

The DLSC method for a boost converter was proposed to reduce $\Delta V_o$ during the load transient. The LTO, step-down transient mode, and step-up transient mode were added to the conventional VMC to realize DLSC. The proposed method was implemented by simple and straightforward program code of addition and subtraction operations, aiming to minimize the extra computational load on MCU. A 10 V-15 V 100-kHz prototype boost converter was built and tested to verify the performance of the proposed DLSC method. During the step-down load transient, $\Delta V_o$ decreased by 19.2% when $m_d = 2/T_s$ and by 42.3% when $m_d = 10/T_s$. The reduction of $\Delta V_o$ was 12.5% when $m_u = 2/T_s$ and 41.7% when $m_u = 10/T_s$ during the step-up load transient. The higher slope of $v_c$ further reduced the undershoot and overshoot of $v_o$ and closely matched the analysis in Section II. The experimental results, which match well with analysis, demonstrated that the proposed method improves the transient response without current sensors and extra circuit components.

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