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Performance Optimization of Fabricated Nanosheet GAA CMOS Transistors and 6T-SRAM Cells via Source/Drain Doping Engineering

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***Abstract*—As gate-all-around nanosheet transistors (GAA NSFETs) replacing current FinFETs for their superior gate control capabilities, it needs various performance optimizations for better transistor and circuit benefits. In this paper, special optimizations to source/drain (S/D) doping engineering including spacer bottom footing (SBF) and refining the lightly doped drain (LDD) implantation process are explored to enhance both fabricated complementary metal oxide semiconductor (CMOS) NSFETs and their 6T-SRAM cells. The experimental results demonstrate that the optimal SBF width increased the static noise margin (SNM) of the SRAM cells by 14.9%, while significantly reducing static power consumption for the balance performance between the NMOS and PMOS and reduced current in all leakage paths of SRAM. Moreover, the LDD optimization significantly reduced off-state leakage current (Ioff) for both NMOS and PMOS due to the reductions of peak electric field in overlap region between the S/D and the channel, leading to a 9.5% improvement in SNM and a substantial reduction in static power consumption. These results indicate that the optimization to S/D doping engineering may achieve substantial performance gains in both the GAA CMOS transistors and the SRAM cells.**

***Index Terms*—gate-all-around nanosheet transistor (GAA NSFET), source/drain (S/D) doping, spacer, lightly doped drain (LDD), 6T static random-access memory (6T-SRAM).**

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I. INTRODUCTION

As technology advances to the 3-nm node and beyond, the gate-all-around nanosheet transistor (GAA NSFET) has emerged as a promising successor to the FinFET [1]. Its vertically stacked nanosheet channels provide superior gate control capability, resulting in improved channel electrostatics and enhanced driving abilities [2], [3], [4], [5], [6], [7]. A series of studies have explored the structural exploration, process realization, and performance optimization of GAA NSFETs [8], [9], [10]. Hans Mertens et al. [11] investigated suppression of the parasitic channel leakage in NSFETs through ground plane engineering. Sylvain Barraud et al. [12] effectively enhanced the drive capability of NSFETs through source/drain stress engineering. On the other hand, static random-access memory (SRAM) cells are extensively utilized in up-to-date chips. The development of SRAM with higher performance and less power consumption is one of the most critical tasks to maintain the scaling of CMOS technology [13]. A series of design optimization technologies for NSFETs building standard 6T-SRAM cells are reported [14], [15], [16], [17]. Taejoong Song et al. [18] optimized the SRAM disturb margin through flexible nanosheet width design. Huynh Bao et al. [19], [20] proposed device threshold voltage retargeting technology to reduce the minimum operating voltage of SRAMs with NSFETs. However, there remains broad technical space to further optimize the performance specification of 6T-SRAM cells through various process technologies. Source/drain (S/D) doping has been extensively utilized to minimize leakage and enhance device performance [21], [22], [23], [24], [25], [26]. Some simulation studies also show that the performance of 6T-SRAM can be enhanced using S/D doping [27] [28]. But the impact of S/D doping engineering on 6T-SRAM made by NSFETs has not yet to be clearly defined. Appropriate S/D doping optimization strategies are required to boost GAA SRAM performance and reduce power consumption.

In this study, the optimization of S/D doping engineering to improve the performance of the fabricated nanosheet GAA CMOS transistors and 6T-SRAM cells were investigated. Key S/D doping engineering techniques are explored, including spacer bottom footing (SBF) and the refinement of the lightly doped drain (LDD) implantation process. The study

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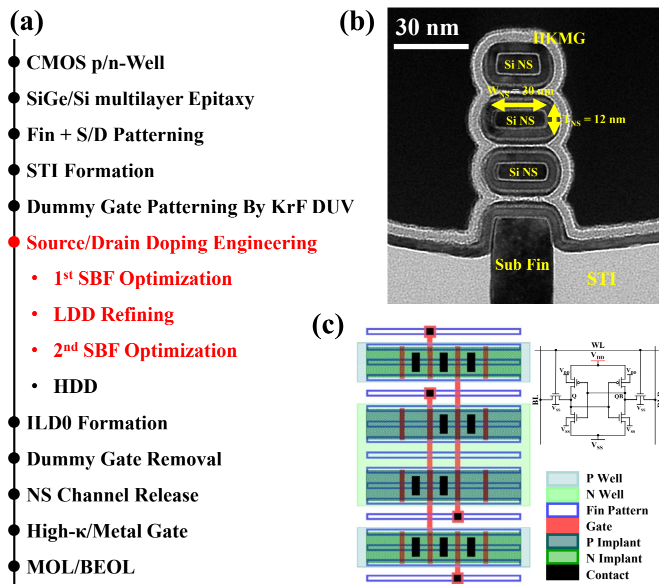

Fig. 1. (a) The integrated process flows of CMOS bulk-Si GAA NSFETs and 6T-SRAM cells. (b) TEM image of GAA NSFETs. (c) The layout and schematic of GAA 6T-SRAM cell.

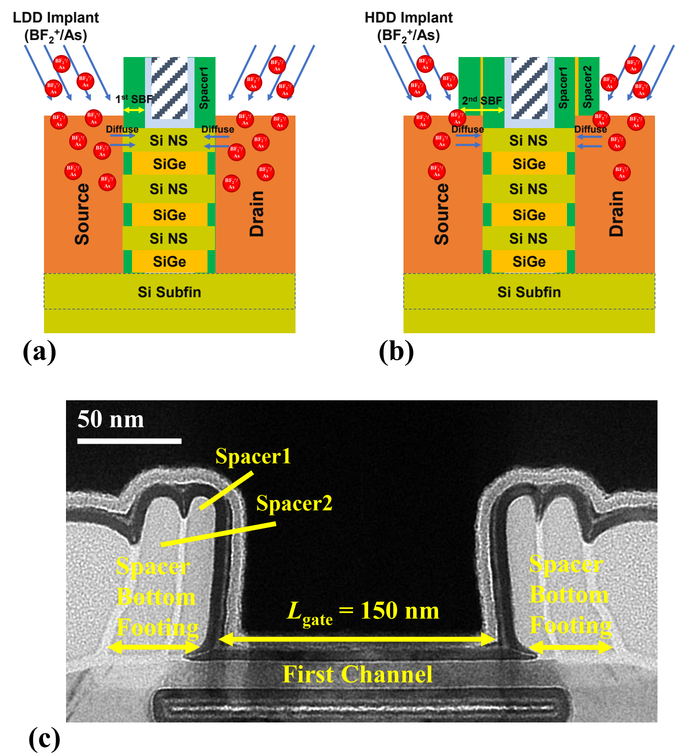

Fig. 2. Strategy of S/D doping optimization. (a) 1st SBF optimization and LDD refining. (b) 2nd SBF optimization and HDD implant. (c) TEM image of spacer bottom footing.

investigates how these S/D doping process optimizations impact transistor characteristics and the behavior of 6T-SRAM cells. By studying the comprehensive impact of S/D doping engineering on devices and circuits, the disturb margin of GAA 6T-SRAM cell is significantly improved, and the static power consumption is substantially reduced.

II. Fabrication and S/D Doping Engineering

A. CMOS Device and 6T-SRAM Fabrication

Stacked Si nanosheet GAA CMOS transistors and 6T-SRAM cells are fabricated on 8-inch p-type bulk-Si (100) wafers. The integrated process flow and key steps of S/D engineering are shown in Fig. 1. At first, the bulk-Si substrate is doped with B and P impurities to form P-wells and N-wells. Then, three periodic SiGe/Si multilayers are grown by reduced pressure chemical vapor deposition (RPCVD). SiN_x spacers are then formed using spacer image transfer techniques to define the fin patterns. S/D patterns are formed using deep ultraviolet (DUV) lithography. Afterward, the defined fin and S/D hybrid patterns are simply transferred below the SiGe/Si stacks and Si substrate by reactive ion etching [29], [30]. Next, shallow trench isolation (STI) and dummy gate were formed. Subsequently, the process advances into S/D doping engineering including spacer formation and implantation doping. SiN_x spacer1 is formed by advanced reactive ion etching (RIE). Lightly doped drain (LDD) process is then carried out with As and BF_2^+ implantation for NMOS and PMOS, respectively. To better control the dopant distribution, NMOS devices use As implant, which has a slower diffusion rate compared to P and helps achieve more precise dopant control and improves the performance. Followed with SiN_x spacer2 formation, the heavy doped drain (HDD) implantation are formed to reduce the parasitic resistance of S/D. After ILD0 formation and dummy gate removal, the stacked NS channel release is formed by the selective wet-etch of SiGe layers. Next, in the replacement metal gate (RMG) process, multilayer CMOS high-k/metal gate (HKMG) stacks were conformally formed by selective pattern and atomic layer deposition (ALD). Finally, the transistor contacts and back-end-of-line (BEOL) process are adopted for the formation of devices and interconnections in SRAM circuits.

B. Strategy of Source/Drain Doping Engineering Optimization

The S/D doping engineering is obtained by the strategy of spacer bottom footing (SBF) and the relevant LDD optimization. In the S/D doping engineering process, critical spacer bottom footing (SBF) optimization was implemented during the spacer1 and spacer2 etching. This approach adjusts the lateral bottom spacer width near the first channel after forming the poly-gate structure by controlling the spacer over-etch ratio in GAA CMOS devices, as shown in Fig. 2. The SBF widths influence the implantation and diffusion behavior of S/D dopants, resulting in different impurity doping profiles, which in turn affect the performance of the devices and 6T-SRAM cells. In addition, the doping profile in the overlap region between the S/D and the gate is one of the most important factors affecting the performance, which can be primarily adjusted through the LDD implantation process in S/D doping engineering. After SBF optimization, devices and 6T-SRAM cells performance can be further improved through LDD refining.

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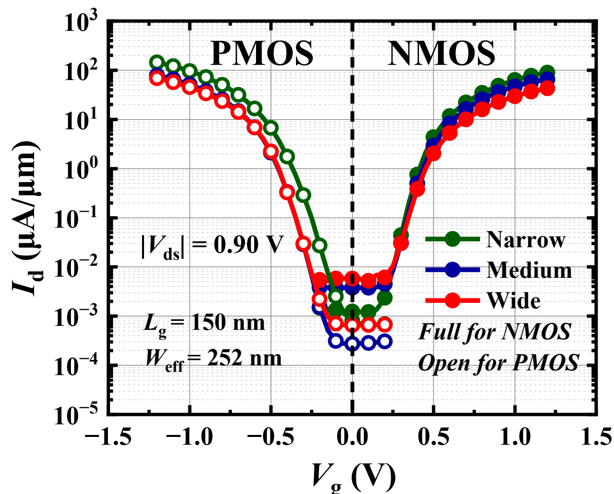

Fig. 3. Transfer characteristics of the fabricated GAA NSFETs with different SBF widths at 0.9 V operating voltage.

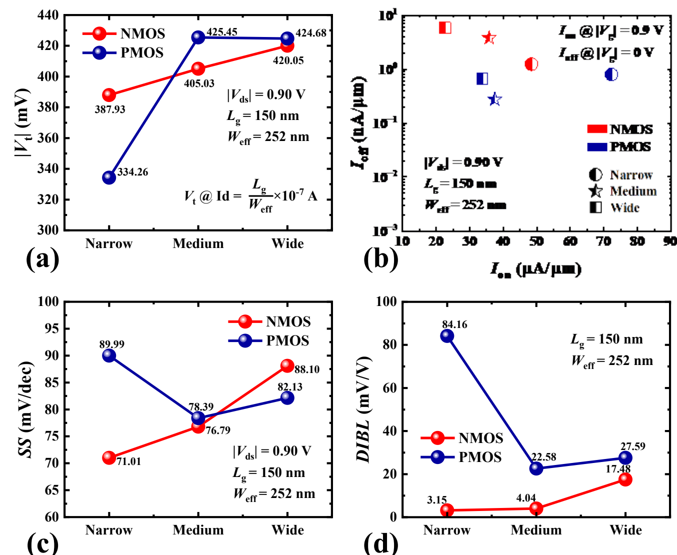

Fig. 4. (a) $|V_t|$, (b) I_{on} & I_{off}, (c) SS, (d) DIBL of the fabricated GAA NSFETs with different SBF widths.

III. CMOS Transistors Characteristics

A. Spacer Bottom Footing Optimization

Experiments were conducted to fabricate with three different SBF widths. The transfer characteristic curves of fabricated devices are presented in Fig. 3. The results show that as the SBF width increases, NMOS and PMOS exhibit distinct characteristics trends. For NMOS, as the SBF width decreases, the transistors characteristics metrics show a consistent trend of improvement. As shown in Fig. 4, the subthreshold characteristics are enhanced, the subthreshold swing (SS) decreases, the off-state current (I_{off}) is reduced, and the on-state current (I_{on}) shows a slight increase. Compared to the wide SBF width, the narrow SBF width exhibits a significant reduction in the I_{off} of NMOS, underscoring its effectiveness in suppressing leakage.

Technical computer-aided design (TCAD) simulations of the S/D doping profiles for NMOS with three different SBF widths are shown in Fig. 5(a). Given that As is used as the NMOS S/D dopant, which has a slow diffusion rate, there is little diffusion of the dopant into the channel. The overlap region between the S/D and the channel remains consistent with the channel doping. However, the electric field control of the gate over this region is weakened due to the isolation effect of the spacer, reducing its effectiveness in controlling the on/off state. Consequently, the narrower SBF width minimizes the region that the gate cannot effectively control, leading to enhanced NMOS characteristics. Moreover, as the SBF width increases, the corresponding lateral resistance also increases, causing a slight reduction in I_{on}.

For PMOS, the characteristics trend is more complex. As the SBF width decreases, the characteristics indicators of the transistor, such as SS, I_{off}, and drain-induced barrier lowering (DIBL), initially improve but then significantly degrade. Compared to the narrow SBF width, the medium SBF width results in a notable reduction in the I_{off} of PMOS. TCAD

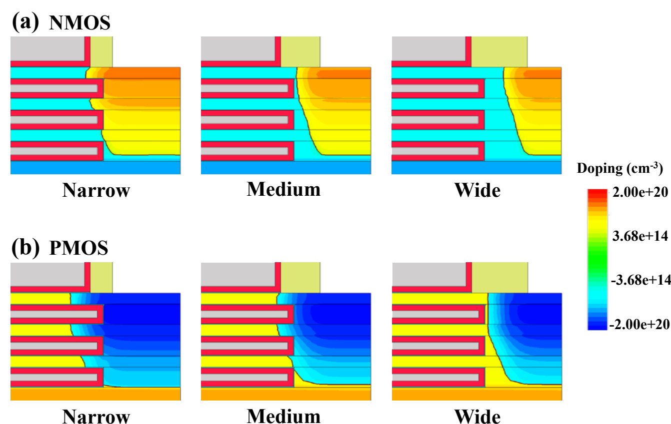

Fig. 5. Doping profile with different SBF widths of (a) NMOS and (b) PMOS.

simulations of the S/D doping profiles for PMOS with the three different SBF widths are shown in Fig. 5(b). As the SBF width decreases slightly, the characteristics improvement in PMOS is similar to that in NMOS—the region where the gate cannot effectively control becomes smaller. However, the PMOS S/D dopant is B, which diffuses rapidly. At the medium SBF width, the doping profile of the S/D reaches the vicinity of the gate and spacer interface. If the SBF width is further reduced, a significant amount of the S/D dopant diffuses into the channel, greatly reducing the effective gate length and worsening the short-channel effects, leading to substantial degradation in device characteristics.

B. Lightly Doped Drain Refining

Using the medium SBF width device as the baseline, GAA devices were fabricated with one-third of the baseline LDD implantation dose and without LDD implantation. The transfer

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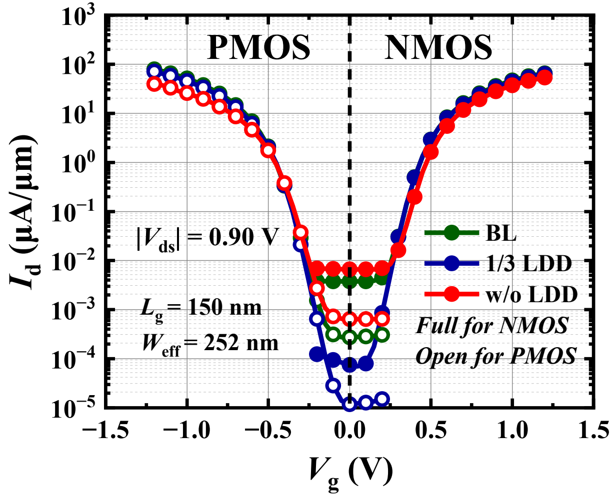

Fig. 6. Transfer characteristics of the fabricated GAA NSFETs with different LDD implantation conditions at 0.9 V operating voltage.

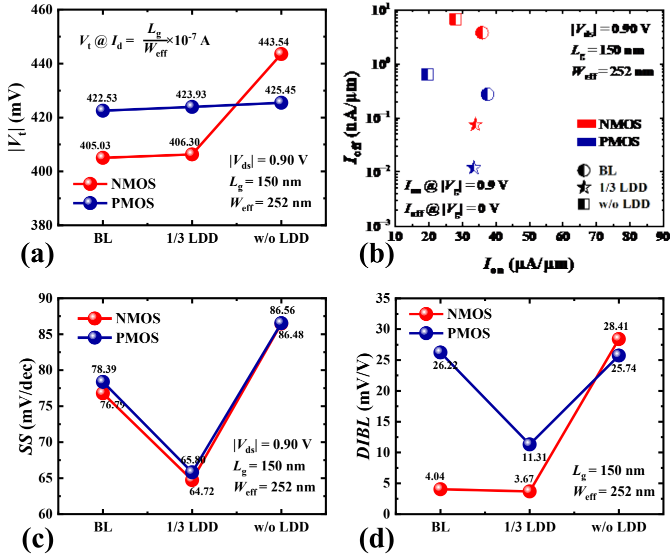

Fig. 7. (a) $|V_t|$, (b) I_{on} & I_{off}, (c) SS, (d) DIBL of the fabricated GAA NSFETs with different LDD implantation conditions.

characteristic curves for fabricated devices under different LDD implantation conditions are shown in Fig. 6. Compared to devices without LDD implantation, GAA transistors with LDD implantation exhibit significantly lower leakage. This reduction in leakage is attributed to the LDD implantation, which reduces the impurity concentration gradient in the overlap region between the S/D and the channel. By mitigating the peak electric field in this region and inhibiting hot carrier effects, LDD implantation effectively reduces leakage. However, as the LDD implantation dose increases, the subthreshold characteristics of the device initially improve and then degrade. Specifically, the SS first decreases and then increases, while the I_{off} decreases and subsequently rises, as shown in Fig. 7. The change in I_{off} is particularly pronounced, compared to the baseline device, the I_{off} of the devices with 1/3 LDD implantation dose is significantly reduced. Leakage

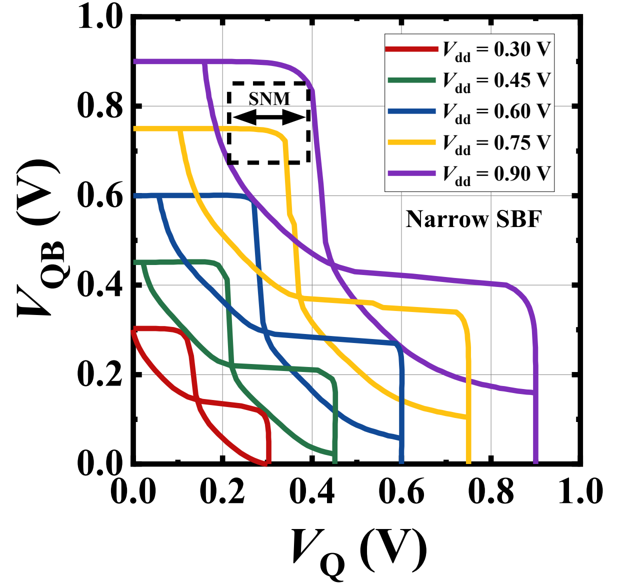

Fig. 8. Butterfly curves of fabricated GAA 6T-SRAM cell with narrow SBF width. The SNM were extracted from the maximum inscribed square of each butterfly curve.

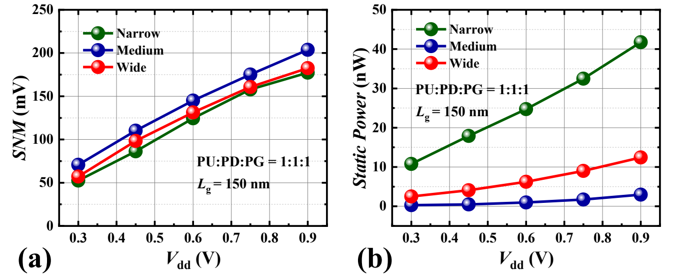

Fig. 9. (a) SNM, (b) static power consumption of fabricated GAA 6T-SRAM cells with different SBF widths.

increases because an excessive LDD implantation dose causes a significant amount of S/D dopant to diffuse into the channel, exacerbating short-channel effects and degrading performance. Additionally, due to the lighter weight and faster diffusion rate of the PMOS S/D dopant, the DIBL effect in PMOS becomes more pronounced at high LDD implantation doses.

IV. 6T-SRAM Cell Performance

A. *SBF Coordinated Optimization of 6T-SRAM Cell*

The static noise margin (SNM) and static power consumption of the fabricated GAA 6T-SRAM cells were evaluated, with the SNM measured using the maximum square method [31], as illustrated in Fig. 8. The SNM for 6T-SRAM cells with three different SBF widths is shown in Fig. 9(a). As the SBF width decreases, the SNM of the 6T-SRAM cells initially increases and then decreases. At the operating voltage of 0.9 V, the SNM of the 6T-SRAM cell with the medium SBF width improves by 14.9% compared to the narrow SBF width. In the design of 6T-SRAM cells, it is advantageous for the drive strength of the

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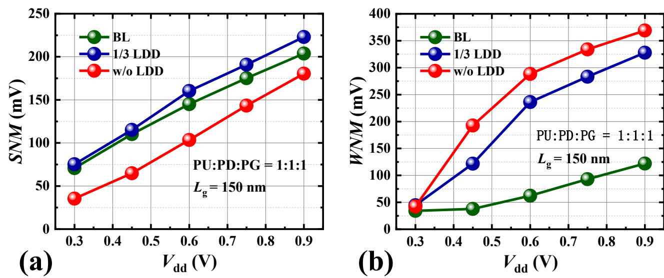

Fig. 10. (a) SNM, (b) WNM of fabricated GAA 6T-SRAM cells with different LDD implantation conditions.

pull-down transistor to exceed that of the access transistor, which should in turn be greater than the drive strength of the pull-up transistor for optimal performance. However, with the narrow SBF width, the PMOS experiences severe short-channel effects, leading to a decrease in threshold voltage and an increase in I_{on}. This results in excessive pull-up transistor drive, significantly reducing the SNM of the 6T-SRAM cell. Conversely, with the wide SBF width, the subthreshold characteristics of both NMOS and PMOS degrade, resulting in slower transitions in the metastable region of the 6T-SRAM cell, a reduced slope in the metastable region, and a lower SNM. In contrast, the medium SBF width provides the best SNM performance due to the balanced drive capabilities of NMOS and PMOS and improved subthreshold characteristics.

The static power consumption of the 6T-SRAM cells with three different SBF widths is shown in Fig. 9(b). As the SBF width decreases, the static power consumption of the 6T-SRAM cells initially decreases significantly and then increases. At the operating voltage of 0.9 V, the medium SBF width demonstrates significantly lower static power consumption compared to the narrow SBF width, indicating an optimal range for minimizing power dissipation. There are two primary leakage paths in the 6T-SRAM cell. Path 1 runs from VDD through the PMOS in the on-state, through the NMOS in the off-state, and finally to GND. Path 2 runs from VDD through the PMOS in the off-state, through the NMOS in the on-state, and then to GND. With the narrow SBF width, the PMOS exhibits high off-state leakage, resulting in substantial leakage current through Path 1 and leading to high static power consumption for the 6T-SRAM cell. In contrast, with the medium SBF width, both NMOS and PMOS show reduced I_{off}, resulting in the lowest static power consumption for the 6T-SRAM cell.

Although the NMOS and PMOS characteristics do not both reach optimal levels with medium SBF width, coordinated optimization results in the 6T-SRAM cell achieving the best SNM and minimal static power consumption.

B. LDD Coordinated Optimization of 6T-SRAM Cell

The SNM of fabricated GAA 6T-SRAM cells under three different LDD implantation conditions is shown in Fig. 10(a). As the LDD implantation dose increases, the SNM of the 6T-SRAM cells initially rises and then falls. At the operating voltage of 0.9 V, the SNM of the 6T-SRAM cell with 1/3 LDD implantation dose improves by 9.5% compared to the baseline, while the SNM of the 6T-SRAM cell without LDD implantation decreases by 11.4%. Without LDD implantation, part of the PMOS S/D dopant continues to diffuse into the channel, resulting in a lower threshold voltage. However, since the NMOS S/D dopant is As, which is heavier and diffuses more slowly, it maintains a higher threshold voltage. This disparity in threshold voltages causes the flipping threshold of the SRAM butterfly curve to deviate from VDD/2, leading to a reduction in SNM. At high LDD implantation doses, the SS of both NMOS and PMOS increases, causing the rate of change in the metastable region of the 6T-SRAM cell to slow down, which reduces the slope and consequently decreases the SNM. Additionally, the DIBL effect is more pronounced for PMOS under high LDD implantation doses compared to NMOS, significantly increasing the threshold voltage and reducing current at lower operating voltages for PMOS. This makes the advantage of the pull-down and access transistor drives over the pull-up transistor drive more evident at lower voltages, resulting in a smaller slope of SNM reduction as VDD decreases. With 1/3 LDD implantation dose, NMOS and PMOS exhibit more symmetrical threshold voltages and optimal device performance, including the best subthreshold characteristics, resulting in the best SNM for the 6T-SRAM cells.

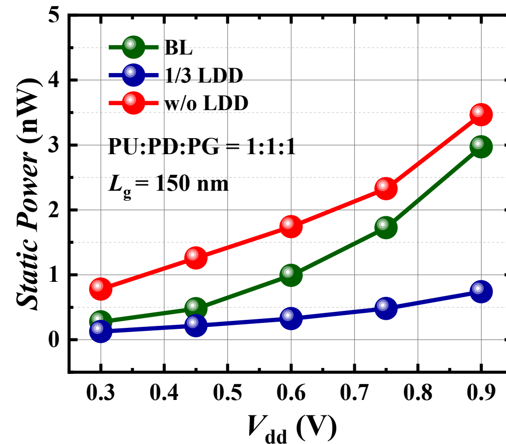

Fig. 11. Static power consumption of fabricated GAA 6T-SRAM cells with different LDD implantation conditions.

The write noise margin (WNM) of fabricated GAA 6T-SRAM cells under three different LDD implantation conditions is shown in Fig. 10(b). At high LDD implantation doses, the lighter weight and faster diffusion rate of the PMOS S/D dopant lead to a higher I_{on} compared to the NMOS, causing the drive strength of the pull-up transistor to surpass that of the access transistor, thereby degrading the WNM. In contrast, without LDD implantation, the reduced PMOS I_{on} due to limited dopant diffusion leads to a higher WNM. However, at lower doses of LDD doping, the main limiting factor for SRAM performance shifts to SNM. Therefore, despite having a higher WNM, the overall performance of the SRAM cell without LDD implantation is inferior to that of the SRAM cell with a 1/3 LDD implantation dose. The 1/3 LDD implant dose achieves the best trade-off between SNM and WNM, resulting in superior SRAM performance.

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TABLE I
COMPARISON OF SNM VALUES

	This work	[31] TED 2024	[32] TED 2023	[33] IEDM 2022	[34] SISPAD 2021
L_{gate}	150 nm	16 nm	50 nm	15 nm	14 nm
V_{dd}	0.9 V	0.7 V	1.0 V	0.7 V	/
SNM	203.69 mV	106.01 mV	100 mV	~160 mV	~153 mV
Device Structure	GAA Nanosheet	GAA Nanosheet	GAA Nanowire	GAA Nanosheet	GAA Nanosheet
Measurement/ Simulation	Measurement	Simulation	Simulation	Simulation	Simulation

The static power consumption of the 6T-SRAM cells under the three LDD implantation conditions is shown in Fig. 11. Due to the minimal off-state leakage of devices with 1/3 LDD implantation dose, the static power consumption of 6T-SRAM cell is significantly reduced. At the operating voltage of 0.9 V, the 6T-SRAM cell with 1/3 LDD implantation dose exhibits a significant reduction in static power consumption compared to the baseline, underscoring the effectiveness of reduced implantation doses in improving power efficiency. In contrast, the devices without LDD implantation exhibit high off-state leakage, resulting in increased static power consumption. At the operating voltage of 0.9 V, the static power consumption of 6T-SRAM cell without LDD implantation increases by 16.7% compared to the baseline.

V. CONCLUSION

This research investigated the optimization of S/D doping engineering to enhance the performance of GAA CMOS transistors and 6T-SRAM cells. Through SBF optimization and the refinement of the LDD implantation process, significant improvements were achieved in both device characteristics and 6T-SRAM cell performance. The optimal SBF width improved the SNM of the 6T-SRAM cell by 14.9% and significantly reduced static power consumption due to the balanced optimization of NMOS and PMOS characteristics and lower leakage paths in the SRAM cell. Furthermore, the LDD refining effectively reduced I_{off} for both NMOS and PMOS for minimizing the peak electric field in the overlap region between the S/D and the channel and mitigated hot carrier effects which led to a 9.5% improvement in SNM and a noticeable reduction in static power consumption. These optimizations are not only crucial for device design at advanced nodes but also provide new directions for developing more efficient and stable SRAM cell designs.

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