Effect of Layout on TDDB in 45-nm PDSOI N-channel FETs under DC and AC Stress

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***Abstract*—This paper investigates the effect of device layout and gate area-to-perimeter ratio on Time-Dependent Dielectric Breakdown (TDDB) in DC and RF FETs fabricated using 45-nm RFSOI technology. The FETs are subjected to both DC and AC gate stress at 125°C, and various TDDB parameters such as breakdown time (T63), Weibull slope (β), voltage acceleration exponent (n), and safe operating voltage (Vsafe) are measured and analyzed. Under both DC and AC stress, RF FETs show better T63 and higher β compared to DC FETs of the same gate oxide thickness. From analysis, it is seen that the Area/Perimeter ratio of gate oxide plays a critical role. The power law voltage acceleration model is used to estimate a 10-year lifetime, based on safe operating voltages, projecting approximately ~1.7 V for RF FETs and ~1.35 V for DC FETs. Our findings reveal the limitations of the current power-area law and highlight the critical understanding required in advanced technology nodes to improve reliability predictions and device design.**

***Index Terms*—CMOS, Gate Area, PDSOI, Poisson Area Law, Power Law Exponent, Reliability, TDDB.**

I. INTRODUCTION

CMOS technology is widely used in the industry because of its high integration density, scalability, low power consumption, and cost-effectiveness. Such features make it appropriate for a wide range of applications, starting from consumer electronics to high-performance computing systems. Among various technologies, PDSOI significantly enhances device performance by minimizing parasitic capacitances, increasing transistor switching speed, and optimizing power consumption [1]. These advantages make PDSOI more crucial for applications in aerospace, IoT sensors, and automotive electronics [2]. However, the reliability of CMOS technology is a major concern despite its several advantages, particularly because devices get smaller and closer to the nanoscale, thus operating at higher electric fields, causing a threat to the device reliability [3-6].

Time-Dependent Dielectric Breakdown (TDDB), one of the major reliability mechanisms, causes the gradual degradation of gate oxide under prolonged stress conditions which ultimately leads to the failure of the device/system. TDDB has been widely studied in several important areas, including the impact of stress conditions, advanced characterization techniques (both AC and DC), material innovations (such as low-k and high-k dielectrics), and process variations [7-14]. However, the impact of layout variation on the TDDB models needs deeper understanding and focus.

To evaluate reliability under TDDB, it is important to accurately determine the effect of electric field on device breakdown time (TBD) and/or failure time of the device (TTF), along with the statistical distribution. For technology qualification, multiple area devices on the chip are chosen to study TDDB. Using area scaling along with weibul distribution, the lifetime prediction data evaluated in small areas is projected to the required standard areas by extrapolating higher failure rate to extremely low percentile (0.001-0.0001%) [15]. This signifies the importance of understanding and accuracy of area scaling law for accurate lifetime prediction, where continuous advancement and frequent changes in device design is the norm.

TABLE I
DEVICE SPECIFICATIONS AND STRESS CHARACTERIZATION METHODOLOGY

DUT & Stress Applied	W_f (µm)	Array Of FETs ($N_f \times My_j$)	Area (A_G) (μm^2)	STI Perimeter (P_{STI}) (µm)	Diffusion Perimeter (P_D) (µm)	AG/P_{STI} (µm)
$D1_{DC}$ (DC, AC& RVS)	0.15	1×5	0.03	0.4	1.52	~0.075
$D2_{DC}$ DC, AC& RVS)	0.15	1×50	0.31	4	15.2	~0.0775
$D3_{DC}$ (DC, AC& RVS)	0.15	1×100	0.61	8	30.4	~0.076
$D4_{RF}$ (DC, AC& RVS)	1	6×6	1.44	2.88	72	~0.5
$D5_{RF}$ (DC&RVS)	1	20×3	2.4	4.8	120	~0.5
$D6_{RF}$ (DC&RVS)	2	20×3	4.8	4.8	240	~1

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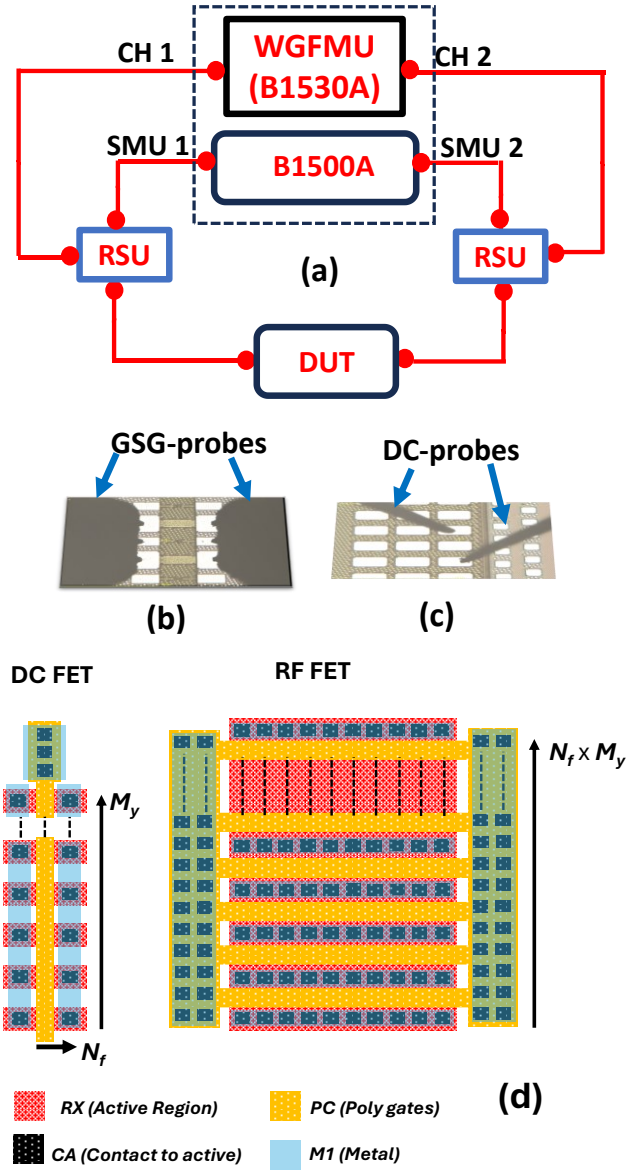

Fig. 1. (a) Measurement setup used for DC and AC TDDB characterization, (b) RF FET with GSG padset, measured using infinity GSG probes, (c) DC FET measured using DC probes, and (d) shows the top layout configuration of DC and RF FET.

The dependence of the TDDB model on gate area is well-reported in the literature [16-17]. Wen Liu provided a well-quantified report on the dependence of TDDB on layout in FinFETs [18]. In this study, the layout effects are addressed by considering PDSOI technology under DC and AC conditions. In this paper, we present a comprehensive experimental analysis of how layout, device design, and gate area-to-perimeter ratio impact gate dielectric breakdown in PDSOI FETs, all featuring the same gate stack and Equivalent Oxide Thickness (EOT). Section II outlines the device specifications and provides details on the characterization setup. Section III presents the key findings, focusing on the variation in breakdown time of the devices in context with the area scaling. Section IV concludes the paper.

II. DEVICE DETAILS AND EXPERIMENTAL SETUP

PDSOI N-channel DC and RF FETs with a gate length (Lg) of 40 nm and an EOT of 1.8 nm are used in this work. These devices are fabricated by GLOBALFOUNDRIES using 45-nm RFSOI technology [19]. Table I shows the device specifications and stress methodology used in this work. These devices are an array of FETs having different fingers and multiplicity (M_y) as described in Table I. While DC FETs ($D1_{DC}$ to $D3_{DC}$) are single-finger devices with varying multiplicities, RF FETs labeled $D4_{RF}$ to $D6_{RF}$ vary in parameters such as finger width (W_f), M_y, and number of gate fingers (N_f). Another key attribute is the area-to-STI perimeter ratio which is captured as A_G/P_{STI} ratio. These devices are fabricated using a similar process technology with SiON gate stacks. The gate oxide is primarily SiO_2-based, with oxide nitridation achieved through decoupled plasma nitridation (DPN) to boost the device performance. This process effectively increases the dielectric constant (k-value) of the oxide from approximately 3.9 to a range of 7.5–9 [20].

FETs were stressed under both DC and AC conditions for the detailed analysis in terms of area scaling and breakdown time. To improve confidence in extracted TDDB parameters, it is important to have enough sample sizes for each stress condition and device type. In this case, we have used 18~32 samples per stress condition along with the different areas.

The characterization setup used for this work is shown in Fig.1. The Keysight B1500A-semiconductor parameter analyzer, along with the B1530A-Waveform Generator Fast Measurement Unit (WGFMU) were used for the DC and AC stress characterization of the devices under test (DUT) respectively, shown in Fig. 1(a). CH1/SMU1 was connected to the gate of the device, and CH2/SMU2 connected to the drain of the device, where CH refers to the channel of WGFMU. To avoid the impact of external resistance effect, the WGFMU's Remote-Sense and Switch Units (RSUs) are used to enable smooth transitions between DC and pulsed stress. The microphotographs in Fig. 1(b) and Fig. 1(c) show the padset device design of RF FET having Ground-Signal-Ground (GSG) padsets and DC FETs using conventional DC pads, respectively. Fig.1(d) shows the top layout configration of DC and RF FETs.

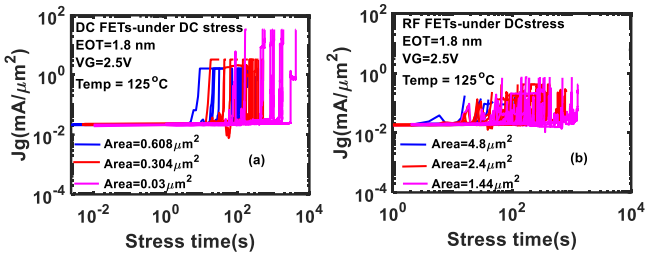

Fig. 2. Gate leakage current density showing breakdown time under VG stress of 2.5V for various areas in (a) DC FETs , and (b) RF FETs

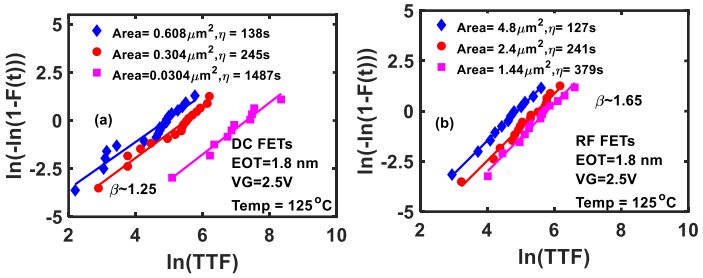

Fig. 3. Impact of area on Weibull distribution of failure time under VG stress of 2.5V in (a) DC FETs, and (b) RF FETs. Higher β is observed for RF FETs than DC FETs.

For reliability characterization, GSG infinity probes were used for the RF FETs, while DC probes were used for the DC FETs. All the measurements were done at an elevated temperature of 125℃. Adequate screening techniques were employed where weak devices and/or t_0 fails (devices that fail at time zero) were eliminated and not considered in this study. Devices with very little to no variability in the pre-stress characterization were considered for each stress condition. Moreover, an analysis based on the breakdown voltage (VBD) of each device was carried out, before selecting the stress voltage conditions.

III. RESULTS AND DISCUSSION

Devices with varying gate area ranging from 1X (0.03 μm²) to ~160X (4.8 μm²) were subjected to initial DC stress with a gate voltage (VG) of 2.5V. The time-dependent evolution of gate leakage current was monitored for both DC and RF FETs as shown in Fig. 2(a) and Fig. 2(b), respectively. For the TDDB analysis, devices were stressed until a hard breakdown was observed. It is observed that devices with larger areas show early breakdown in both DC and RF FETs. Fig. 3 shows the Weibull plots for varying areas providing additional insights into the statistical nature of the breakdown as a function of area and device type. It is observed that the Weibull shape parameter, β shows variation in DC and RF FETs, with $\beta_{DC} < \beta_{RF}$ indicating tighter failure distribution in RF FETs. Using Weibull distribution, the characteristic time, η (or T63) which represents the failure of 63.2% of devices was also determined.

Combining Fig. 2 and Fig. 3 data indicates that the DC and RF FETs together do not follow the area scaling law, as the T63 of RF FETs is expected to be much lower than DC FETs. The results also show the unexpected variation in β.

It is to be noted that both DC and RF devices exhibit area scaling law when they are considered as two different device types but fail to exhibit such area scaling when both devices are combined together.

To further validate the observed trends, AC stress characterization was performed on devices at VG of 2.7V at a frequency of 10 kHz with various duty cycles (DTC). Fig. 4 shows the results under AC stress and compares them with DC stress outcomes. Devices with gate areas of 0.31 μm² ($D2_{DC}$) and 1.44 μm² ($D4_{RF}$) were initially subjected to DC stress at VG

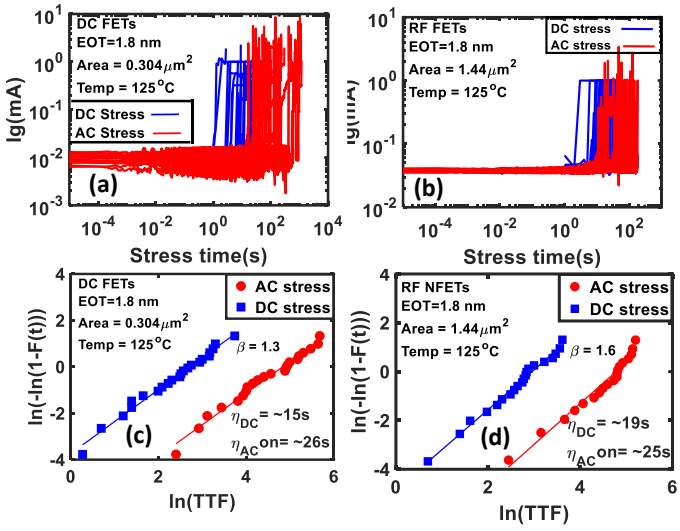

Fig. 4. Gate current under DC (VG=2.7V) and AC stress (VG=2.7, Freq= 10kHz, DTC=20%), in (a) DC FETs, and (b) RF FETs. Weibull distribution in FETs showing no effect of stress type on β, in (c) DC FETs, and (d) RF FETs.

= 2.7V (VD = 0). This was followed by AC stress, using WGFMU at 10 kHz of frequency with a 20% duty cycle, maintaining VG at 2.7V for a fair comparison on fresh dies next to DC-stressed die. A checker board die pattern is used to minimize die-to-die variation. As evident from Fig. 4(a) and 4(b), devices under DC stress exhibit earlier breakdown in both DC and RF FETs. AC-stressed devices demonstrate longer breakdown times (higher $T63_{on}$), consistent with expectations and previous literature [21-22]. The increase in breakdown time under AC stress is attributed to the reduction in both trapping/detrapping and trap generation rates at higher frequencies. The observed decrease in evolution of Stress Induced Leakage Current (SILC) primarily reflects this reduction in trap generation rate [21]. Analysis of Fig. 4(c) and 4(d) reveals that while the characteristic lifetime (η) increases with AC stress for both device types, the β remains unaffected within DC or RF FETs where β_{RF} (~1.6) is consistently higher than that of β_{DC} (~1.3) even under AC stress conditions. The η

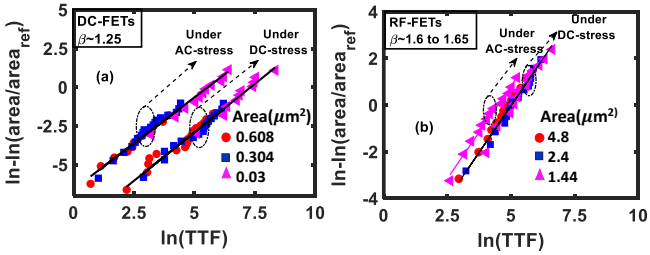

Fig. 5. Area-scaled Weibull distribution (a) under DC (VG=2.5V) and AC stress (VG=2.7V, Freq=10kHz, DTC=80%) at 125℃ for DC FETs, and (b) for RF FETs under DC stress (VG=2.5V) and AC stress (VG=2.7V, Freq=10kHz, DTC=20%).

for AC stress (η_{AC} on) in Fig.4(c) and 4(d) is calculated solely based on the on-time of the stress. It is observed that effect of frequency seems slightly higher in DC FETs compared to the RF FETs.

Understanding the crucial role of sample size in Weibull parameter extraction, the Weibull area Scaled method was used for more accurate determination of the Weibull slope [23]. Fig. 5(a) shows the results for DC FETs under both DC (VG = 2.5V) and AC (VG = 2.7V, 10 kHz, 80% duty cycle) stress conditions, where the area-scaled β values remain consistent with those derived from individual areas. Similarly, Fig. 5(b) demonstrates area-scaled distributions for RF FETs, with β values aligning well with individual area results.

To study the effect of area on T63 in both DC and RF FETs, the conventional power area law shown in (1) is used [24-25].

$$T63 \propto \left(\frac{1}{Area}\right)^{\frac{1}{\beta}} \quad (1)$$

Fig. 6 (a) shows the relationship between T63 and device area, revealing a decrease in T63 with increasing device area for both DC and RF FETs. However, the expected overall area dependence of T63 is not seen if both RF and DC FETs are considered together as clear discontinuity in the T63 vs. area trend is observed in Fig. 6(a). RF FETs with areas of 50X and ~160X exhibit approximately the same failure times as 10X and 20X DC FETs respectively. To further investigate the trend, DC FETs ranging from 1X to 20X area were subjected to AC stress

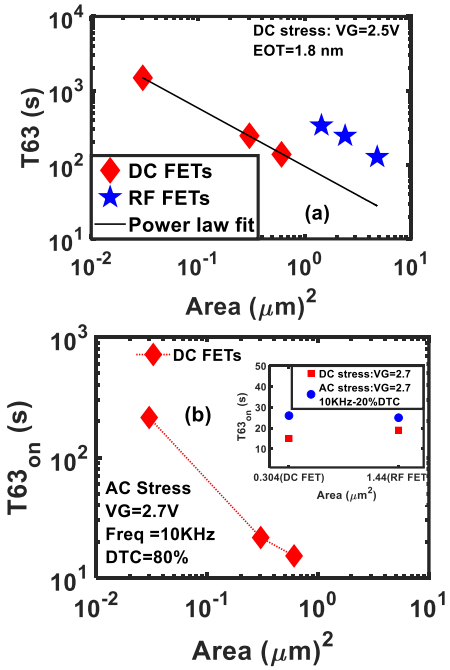

Fig. 6. T63 vs. area on a log-log scale for (a) DC and RF FETs along with expected area scaling power law under DC stress, and (b) of DC FETs under AC stress, where inset shows approximately same breakdown time of RF FET as that of smaller area DC FET, under both AC and DC stress.

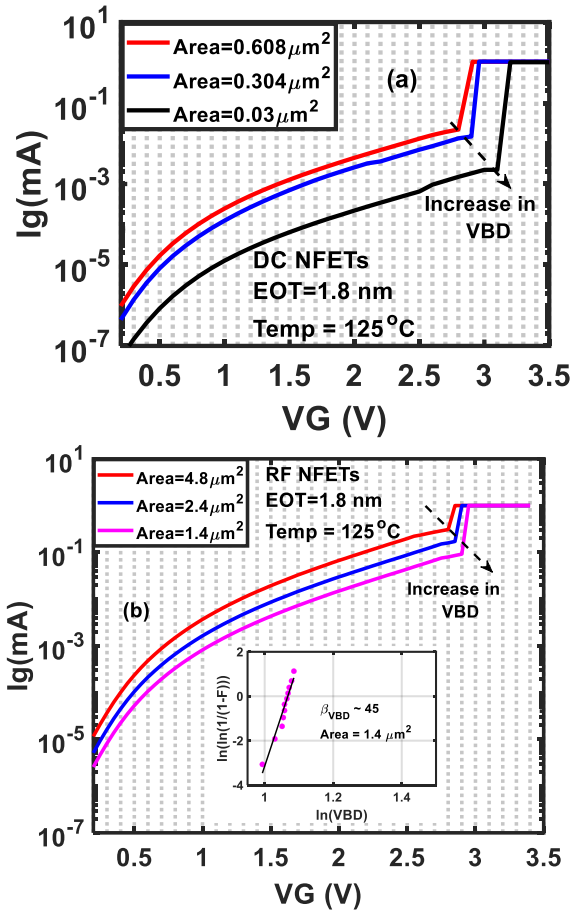

Fig. 7. Gate current vs. gate voltage as function of area, where sharp rise in the current is considerd as breakdown voltage (VBD) in (a) DC FETs, and (b) RF FETs. Inset in (b) shows the VBD Weibull distribution of the device with area 1.4 μm².

(VG=2.7V, 10kHz, DTC=80%), as shown in Fig. 6(b), which further confirms the well-aligned area vs. T63 trend.

A more detailed comparison between a $D4_{RF}$ (area = 1.44 μm²) and a $D2_{DC}$ (area = 0.304 μm²) using DC (VG=2.7V) and AC stress (VG=2.7V, Freq=10kHz, and DTC=20%) revealed approximately similar T63 values for these FETs under both stress conditions, despite the RF FET being approximately 5X larger in area. This observation is highlighted in the inset of Fig. 6(b). This could be because the gate area-to-perimeter ratio is different for both devices as highlighted in Table 1, where particularly, gate area-to-STI perimeter (A_G/P_{STI}) ratio for RF FETs is greater than DC FETs.

To further analyze these devices, ramp voltage stress (RVS) tests were also conducted on devices D1 to D6. The ramp voltage breakdown test is considered the fastest method for assessing the device breakdown [26]. Fig. 7 shows the relationship between breakdown voltage (VBD) and device area. Previous studies [26-27] have established an approximately linear relationship between VBD and T63, with VBD typically being several times smaller than T63, and $\beta_{VBD} >> \beta_{T63}$. The β_{VBD} for VBD distribution is typically very high (e.g β_{VBD} for 1.4 μm² RF FET is ~45,as shown in inset of 7(b))

which significantly reduces the area scaling effect. In Fig. 7(a), we observe 2-6% variation in VBD values when the device area changes from 1X (0.608 µm²) to 20X (0.03 µm²), consistent with the expected scaling behavior for high β_{VBD}. However, a comparable VBD (~2.96V) is observed for $D4_{RF}$ (area = 1.4 µm²) and $D2_{DC}$ (area = 0.31 µm²), despite the significant difference in their areas. This could either be because of low impact of the area on VBD or a possible influence of the device layout on VBD behavior. Nevertheless, this hypothesis requires further detailed validation.

The observation for the increased failure time and higher β measured and extracted in RF FETs can be attributed to the variation in gate area to perimeter ratio in RF and DC FETs. While the gate area-to-Diffusion Perimeter ratio (A_G/P_D) is comparable in both DC and RF FETs, the gate area-to-STI Perimeter ratio (A_G/P_{STI}) ratio is significantly higher in RF FETs than in DC FETs (as shown in Table I). This hints that the STI edge may play a more critical role in the breakdown mechanism of these devices. Devices with a higher A_G/P_{STI} ratio are likely to exhibit a more uniform electric field distribution across both the central region and the STI edge, potentially delaying breakdown and resulting in a narrower Weibull distribution (higher β_{RF}). In contrast, devices with a lower A_G/P_{STI} ratio experience a more non-uniform electric field distribution, potentially intensifying the influence of STI-edge-related defects in DC FETs. In DC FETs, higher contribution of the STI edge-related defects (weaker oxide) in device failure might be the reason for wider failure distribution, hence lower β_{DC}.

Fig. 8 shows the pre-stress gate leakage current density characteristics across various areas. This leakage is attributed to the probability of process-induced defects playing a role in breakdown within larger gate dielectrics. These defects serve as potential leakage paths, contributing to increased current flow.

The impact of voltage acceleration was analyzed using the power-law voltage acceleration model, which is fundamentally based on the Anode Hydrogen Release (AHR) mechanism [27]. The power law model is particularly suitable for ultrathin

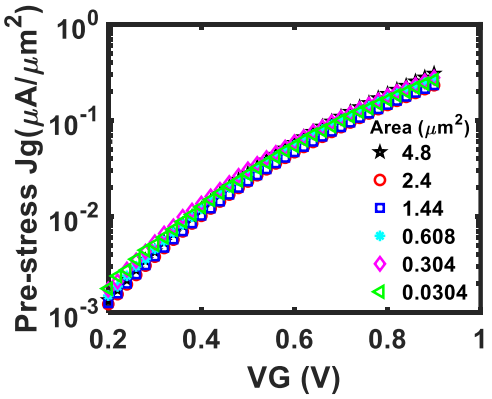

Fig. 8. Pre-stress gate leakage current density as a function of gate area.

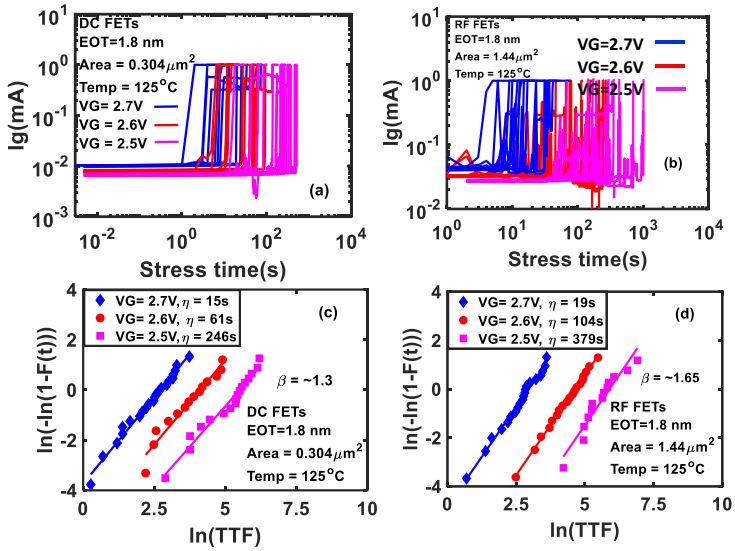

Fig. 9. Gate current as a function of various DC gate voltage stress, in (a) DC FETs, and (b) RF FETs. Weibull distribution in FETs under various gate stress voltages, showing no effect of voltage on β in (c) DC FETs, and (d) RF FETs

oxides, as it captures a thickness-independent voltage acceleration exponent for TBD (or T63) , avoiding the inaccuracies of the exponential model that can overestimate the lifetime of thinner oxides [27]. Our findings align with the power-law model, highlighting that the release and accumulation of hydrogen-induced defects, especially in the weaker oxide regions near the STI edge, play a critical role in accelerating breakdown.

Both RF and DC FETs were subjected to a range of stress voltages, VG=2.5V, 2.6V, and 2.7V. Fig. 9 (a) and (b) shows that both kinds of FETs exhibit accelerated breakdown with increasing gate voltage. Weibull distributions under various gate stress voltages are shown in Fig. 9(c) and Fig. 9(d), indicating similar voltage acceleration for both device types.

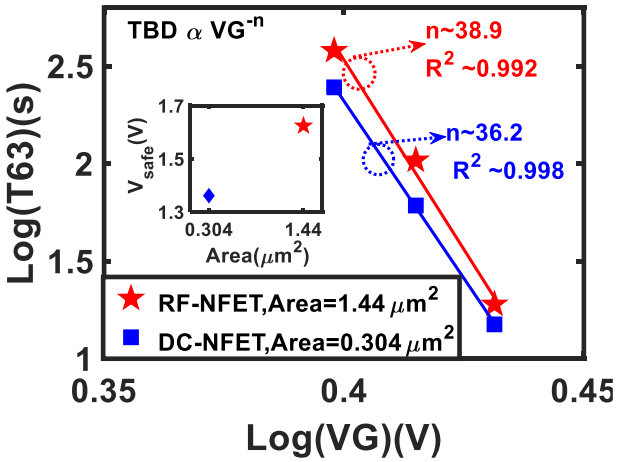

Fig. 10. T63 as function of gate voltage stress, following the power law. Inset shows safe operating voltage of RF and DC FETs for 10-years of lifetime.

TABLE II
PARAMETER COMPARISON FOR DC AND RF FETS

S.No	Parameters	DC FETs	RF FETs
1	**Area scaled Weibull slope (under DC stress)**	~1.25	~1.65
2	**Area scaled Weibull slope (under AC stress)**	~1.25	~1.65
3	**VAE**	36.2	38.9
4	**Vsafe**	~1.35V	~1.7V
5	**VBD**	~2.96V	~2.96V
6	**T63 under DC stress (VG=2.7V)**	15s	19s
7	**T63 under AC stress, considering only on-stress time (VG=2.7V, Freq= 10kHz, DTC = 20%)**	~26s	~25s
8	**β_{DC} (VG=2.7V)**	~1.25-1.3	~1.6-1.65
9	**β_{AC} (VG=2.7V, Freq= 10kHz, DTC = 20%)**	~1.25-1.3	~1.6-1.65

Analysis reveals that the voltage acceleration exponent (n) is slightly higher in RF FETs (~38.9 $\pm$ 18%) compared to DC FETs (~36 $\pm$ 10%), as shown in Fig. 10. However For RF FETs with an area of 1.44 μm², the safe operating voltage is determined to be ~1.7 V, assuming a ten-year lifespan and a 0.01% failure rate. In contrast, DC FETs with a smaller area (approximately 0.304 μm²) exhibit a maximum safe operating voltage (Vsafe/Vmax) of only about 1.35 V under the same conditions. The results indicate that the RF FETs show higher Vmax than DC FETs. The overall parameter comparison of DC and RF FETs are shown in Table II, with parameters 3 to 9 particularly extracted using $D2_{DC}$ and $D4_{RF}$ for comparison.

Overall, results show superior reliability of RF FETs compared to DC FETs based on TDDB Weibull parameters under DC and AC stress. The difference is attributed to layout difference between these two devices. More specifically, the A_G/P_{STI} ratio are different indicating non-uniformity of gate oxide within the device could turn out to be potential reason for different breakdown mechanisms.

IV. CONCLUSION

TDDB analysis of 45nm based RFSOI DC and RF FETs is presented in this work using Weibull distribution parameters. Stress characterization techniques, like DC, AC, and RVS were used in this study.

RF FETs have a higher gate area-to-STI perimeter (A_G/P_{STI}) ratio, resulting in delayed breakdown time than DC FETs. Under various stress conditions, using both DC and AC stress, RF FETs also show higher β values than DC FETs. In addition, a little higher voltage acceleration is noticed for RF FETs than DC FETs. The projected safe operating voltage for RF FETs over a 10-year lifespan is approximately 1.3 times higher than that of DC FETs, with a minimum safe operating voltage (V_{safe}) of 1.35V. Based on the T63 and V_{safe} values obtained for RF FETs, it is concluded that FETs with larger area-to-STI perimeter ratios, in our case, the RF FETs, show superior reliability compared to DC FETs. This enhanced reliability is hypothesized to arise from a more uniform electric field distribution in RF FETs, as opposed to the non-uniform field distribution in DC devices, where the STI edge becomes a critical weak link for breakdown. This detailed analysis highlights the importance of considering layout-dependent factors in FET design and reliability assessment even for similar device types of the same process technology.

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