A New 13T4C LTPO MicroLED Pixel Circuit Producing Highly Stable Driving Current by Minimizing Effect of Parasitic Capacitors and Stabilizing Capacitor Nodes

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Abstract— **In this paper, we proposed a new low-temperature polycrystalline oxide (LTPO) thin-film transistor (TFT) pixel circuit for micro light-emitting diode (μLED) displays that produces a highly stable and uniform driving current. The proposed pixel circuit suppresses the current level change along with the sweep signal due to the parasitic capacitances and compensates for the TFT's threshold voltage (V_{TH}) variation-induced current error, including even falling shape. In addition, the proposed circuit produces a constant current regardless of the data voltage. As a result, a relative current error rate of less than 2% was achieved across all gray levels under the ±0.5 V V_{TH} fluctuation. The proposed circuit was verified using HSPICE with a low-temperature polycrystalline silicon (LTPS) TFT and amorphous indium-gallium-zinc-oxide (a-IGZO) TFT model based on the measured data. The simulation analysis confirmed that the optimal sweep signal input position and pulse width modulation (PWM) and constant current generation (CCG) parts connecting method were key design points for stable and uniform performance.**

Index Terms—**MicroLED (μLED), pixel circuit, a low-temperature polycrystalline oxide (LTPO) thin-film transistor (TFT), threshold voltage (V_{TH}), compensation, falling time, parasitic capacitor, coupling effect.**

I. INTRODUCTION

Micro light-emitting diode (μLED) is gaining extensive attention as the next generation of display due to its superior characteristics compared to the organic light-emitting diode (OLED), such as high brightness, wide color gamut, low power consumption, and resistance to burn-in [1]–[4]. Despite its superior characteristics, μLED has a significant problem in wavelength shift according to current

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density [5], [6]. Therefore, a conventional driving method for OLED, which changes the luminance by adjusting the current level with fixed emission time, can cause color distortion according to the gray level when applied to μLED display. Hence, μLED has adopted the pulse width modulation (PWM) to change the luminance by adjusting the emission time with the constant current [7]–[9].

Generally, a conventional thin-film transistor (TFT)-based μLED pixel circuit consists of a PWM part that adjusts emission time and a constant current generation (CCG) part that produces a constant current to the μLED [10], [11]. The emission time is determined when the ramp-shaped sweep voltage signal (V_{SWEEP}) changes the on/off state of the driving TFT in the PWM part (DRT_PWM) based on the PWM data voltage. However, the subthreshold characteristics of TFTs and the slope of the sweep signal cause a significant delay in the μLED current turning off, i.e., falling time [12]. Therefore, a circuit compensating for even falling wave-shape variation is necessary for uniform operation. In addition, due to the parasitic capacitors of TFTs between the gate and drain node (C_{GD}) or between the gate and source node (C_{GS}) [13], [14], continuously varying gate voltage can negatively influence the threshold voltage (V_{TH}) compensation accuracy and the constant current supply. Therefore, both the circuit structure and operation scheme should be carefully designed to achieve more stable circuit performance, independent of the parasitic capacitance and sweep signal.

Therefore, we proposed a new 13T4C low-temperature polycrystalline oxide (LTPO) pixel circuit based on PWM driving that supplies a stable amplitude of the square current pulse to μLED and compensates for even falling wave-shape under TFT's V_{TH} variation. We chose the LTPO backplane because recent high-performance display devices have mainly adopted LTPO [15], [16]. The low-temperature polycrystalline (LTPS) TFT offers high mobility and stability, which is suitable for driving transistors, while amorphous indium-gallium-zinc-oxide (a-IGZO) TFT shows low leakage current, which provides an advantage to switching transistors by minimizing voltage loss from the storage capacitors [17]. The proposed circuit consists of 6 TFTs and 2 capacitors in the PWM part, and 7 TFTs and 2 capacitors in the CCG part. For the stable driving current for μLED, we suggest three key design points: the input position of sweep signal, the
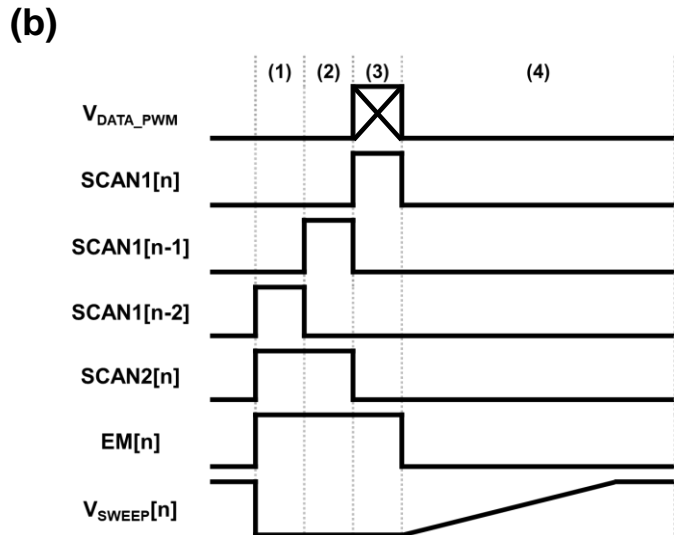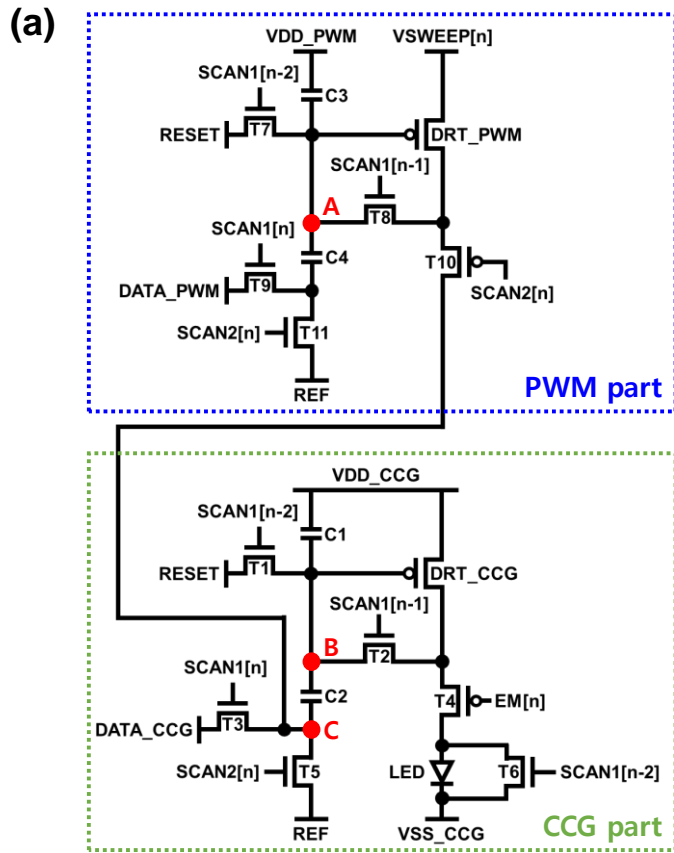
(a)

(b)

Fig. 1. (a) The proposed 13T4C μLED pixel circuit structure, and (b) its signal timing diagram.

connection position between PWM and CCG parts, and the connection timing between PWM and CCG parts. Moreover, we verified the effectiveness of these design strategies by comparing proposed circuit with three slightly modified circuits. The relative current error remains below 2% across all gray levels in the proposed circuit, even with the ±0.5 V V_{TH} fluctuation in both the driving TFTs of the PWM and CCG parts.

Table1. Comparison of the proposed pixel circuit with conventional μLED pixel circuit.

Category	[10]	[18]	[19]	Proposed
Backplane	LTPS	LTPO	LTPS	LTPO
Falling wave-shape compensation	X	X	X	O
Sweep signal-dependent temporal variation in μLED current	O	O	O	X
PWM data-dependent peak level variation in μLED current	O	O	O	X

II. PROPOSED PIXEL CIRCUIT

Typically, TFT-based μLED circuits [10], [18], [19] consist of four stages: initialization, data input, V_{TH} compensation, and emission. In the first three stages, the PWM and CCG parts are separated by a switching transistor and concurrently operated. Then, the two parts are connected in the emission stage. In this stage, the drain node of DRT_PWM is connected to the gate node of driving TFT in the CCG part (DRT_CCG), enabling DRT_PWM to directly control the on/off state of DRT_CCG. The V_{SWEEP} changes the source-to-gate voltage (V_{SG}) of DRT_PWM so that DRT_PWM turns from an off to an on state at a certain point based on data voltage. This state change makes the gate node of DRT_CCG have a high voltage to turn off, enabling the operation of PWM. Typically, V_{SWEEP} is applied directly to the gate node of DRT_PWM to modulate its V_{SG} directly.

In contrast, we can differentiate the proposed circuit in three aspects: the connection of the PWM and CCG parts during the data input stage, applying V_{SWEEP} to the source node of DRT_PWM, and the indirect connection of the PWM part to the gate node of DRT_CCG. Here, we compared the proposed pixel circuit with a conventional TFT-based pixel circuit in the Table 1.

Fig. 1(a) and (b) are the proposed pixel circuit structure and its signal timing diagram. The proposed pixel circuit consists of 13 TFTs and 4 capacitors. DRT_PWM and DRT_CCG are the driving transistors of PWM and CCG parts, respectively, while T1 to T11 are the switching transistors. DRT_PWM and DRT_CCG are LTPS TFTs, and all switching transistors except for T4 and T10 are a-IGZO TFTs to prevent stored voltage loss in the capacitor utilizing a-IGZO's extremely low off-current characteristic. C1 to C4 are the storage capacitors that store the data voltage and V_{TH} of each part. In particular, C2 and C4 contribute to increasing the input data voltage range by voltage dividing. The size of all TFTs is 3 μm/3 μm. The capacitance of C1 and C3 is 20 fF, while that of C2 and C4 is 50 fF. Moreover, the voltage signal range for SCAN1[n], SCAN2[n], and EM[n] is set to -8.5 V to 12.5 V. V_{DD_CCG} is set to 5 V, and both V_{SS_CCG} and the data
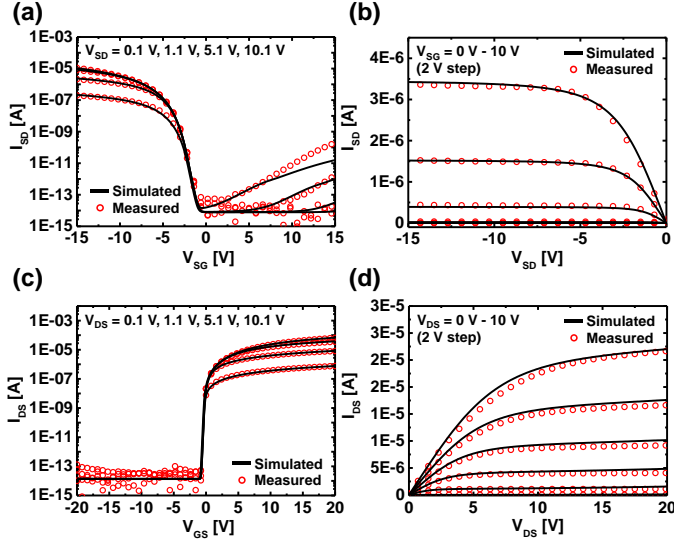
Fig. 2. Measured and simulated results of (a) the transfer curve and (b) the output curve of LTPS TFT, and (c) the transfer curve and (d) the output curve of a-IGZO TFT (dotted symbol represents measured results, and black line represents simulated results).

voltage of CCG part (V_{DATA_CCG}) are set to -2 V. Furthermore, V_{DD_PWM}, V_{REF}, and V_{RESET} are set to 2 V. $V_{SWEEP}[n]$ is swept from 6 V (V_{SWEEP_L}) to 11 V (V_{SWEEP_H}), and the data voltage range of PWM part (V_{DATA_PWM}) for adjusting emission time is set to 3 V to 10 V. Moreover, we set $C_{GD} = C_{GS} = 0.273$ fF for LTPS TFT and $C_{GD} = C_{GS} = 0.2$ fF for a-IGZO TFT, considering an overlap length of 0.1 μm and the gate insulator thickness of each type of TFTs.

The proposed circuit adopts progressive emission driving, which has lower power consumption than the simultaneous one [20]. The circuit operation is divided into four stages: (1) reset, (2) V_{TH} compensation, (3) data input, and (4) emission.

(1) Reset stage: T1, T6, and T7 are turned on with SCAN1[n–2], and T5 and T11 are turned on with SCAN2[n] for the initialization. Hence, the voltage stored in capacitors C1 to C4 from the previous frame is initialized as follows: $V_{DD\_CCG} − V_{RESET}$ for C1, $V_{RESET} − V_{REF}$ for C2, $V_{DD\_PWM} − V_{RESET}$ for C3, and $V_{RESET} − V_{REF}$ for C4.

(2) V_{TH} compensation stage: T1, T6, and T7 are turned off, while T2 and T8 are turned on with SCAN1[n–1]. Subsequently, the current flows through DRT_CCG and DRT_PWM until the drain node of both TFTs reaches $V_{DD\_CCG} − V_{TH\_DRT\_CCG}$ and $V_{SWEEP\_L} − V_{TH\_DRT\_PWM}$, respectively. Here, $V_{TH\_DRT\_CCG}$ and $V_{TH\_DRT\_PWM}$ represent the V_{TH} of DRT_CCG and DRT_PWM, respectively. Moreover, V_{SWEEP_L} represents the low voltage level of the sweep signal. As a result, C1 and C3 store V_{TH} of DRT in both CCG and PWM parts.

(3) Data input stage: SCAN2[n] decreases to a low voltage to turn off T5 and T11, and SCAN1[n–1] also decreases to a low voltage to turn off T2 and T8. Subsequently, T3 and T9 are turned on with the SCAN1[n] to apply the data voltage for each part. Therefore, node A voltage becomes $V_{SWEEP\_L} − V_{TH\_DRT\_PWM} + (V_{DATA\_PWM} − V_{REF}) \times C4/(C3 + C4)$, and node

B voltage becomes $V_{DD\_CCG} − V_{TH\_DRT\_CCG} + (V_{DATA\_CCG} − V_{REF}) \times C2/(C1 + C2)$. Usually, PWM and CCG parts are connected in the emission stage [18], [19]. However, our circuit connects PWM and CCG parts through the SCAN2[n] signal before the emission stage to keep the stored voltage in C1 stable. The effect of the pre-connection of two parts before the emission stage will be discussed in the next section.

(4) Emission stage: SCAN1[n] and EM[n] decrease to a low voltage, so all switching TFTs are turned off except for T4 and T10. Consequently, the current flowing through the μLED current can be expressed by the following equation due to the stored voltage in C1.

$$I_{\mu LED} = 0.5\mu_n C_{ox}(W/L) \cdot (V_{SG\_DRT\_CCG} − V_{TH\_DRT\_CCG})^2 \ (1)$$
$$I_{\mu LED} = 0.5\mu_n C_{ox}(W/L) \cdot \{(V_{REF} − V_{DATA\_CCG}) \times \frac{C2}{C1 + C2}\}^2 \ (2)$$

, where $I_{\mu LED}$ represents the μLED current during the emission stage, μ_n is mobility of DRT_CCG, C_{ox} is oxide capacitance, W is width of DRT_CCG, and L is length of DRT_CCG. As indicated by equation (2), the $I_{\mu LED}$ is independent of the $V_{TH\_DRT\_CCG}$, so the proposed pixel circuit can compensate for the $V_{TH\_DRT\_CCG}$ variation and supply constant current. Note that $V_{SWEEP}[n]$ is supplied to the source node of DRT_PWM in the proposed circuit, while it is usually supplied to the gate node. This structure minimizes the effect of $V_{SWEEP}[n]$ on the shape of the square current pulse, which is caused by the coupling effect of the DRT_PWM's parasitic capacitor. The next section also verifies how the V_{SWEEP} connection affects the pulse amplitude.

When $V_{SWEEP}[n]$ increases and exceeds $V_{TH\_DRT\_PWM}$, DRT_PWM is turned on, and the $V_{SWEEP}[n]$ is applied to node C through T10, so the node C voltage also increases. Subsequently, when $V_{SG\_DRT\_CCG}$ decreases and becomes smaller than $V_{TH\_DRT\_CCG}$, DRT_CCG turns off, leading to the termination of light emission. Meanwhile, the equation determining the end of emission can be expressed as follows:

$$V_{SG\_DRT\_PWM} + V_{SWEEP}[n] > V_{TH\_DRT\_PWM} \ (3)$$
$$V_{SWEEP}[n] > (V_{DATA\_PWM} - V_{REF}) \times \frac{C4}{C3 + C4} \ (4)$$

Consequently, according to equation (4), emission time can be adjusted by comparison between V_{DATA_PWM} and $V_{SWEEP}[n]$, regardless of the $V_{TH\_DRT\_PWM}$. If the PWM part is connected to node B, a stored voltage loss in C1 will occur at the falling time, increasing the compensation error rate due to the falling shape deviation.

III. SIMULATION RESULTS AND DISCUSSIONS

The proposed pixel circuit was verified using HSPICE by Synopsys. We assumed 340 × 422 resolution with a 60 Hz frame rate. Additionally, the total emission time is set to 2 ms. We developed the libraries of the LTPS TFT and a-IGZO TFT based on the measured data. The fabricated LTPS TFT has a size of 300 μm/400 μm, and for a-IGZO TFT, the size is
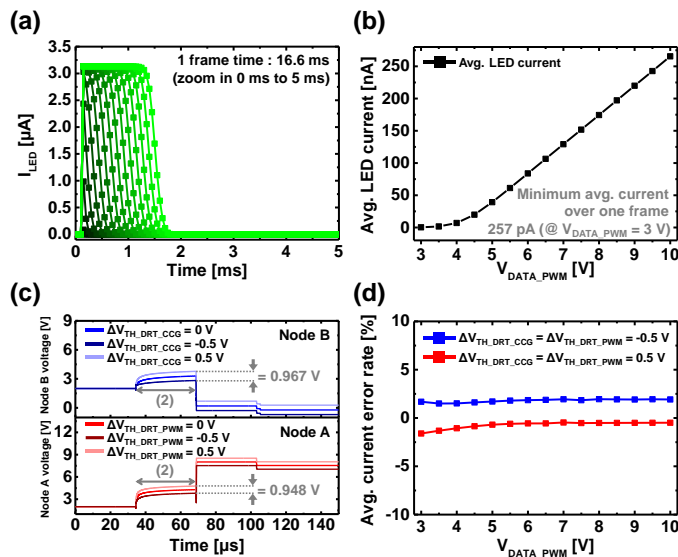
Fig. 3. The simulated results of (a) μLED current, (b) the average μLED current, (c) the change of node A voltage and node B voltage over time (V_{DATA_PWM} = 8 V), and (d) the relative average current error rate.

24 μm/21 μm. The measured characteristics for LTPS TFT are V_{TH} = -1.53 V, mobility = 80.1 cm^2/V·s, and subthreshold swing (S.S) = 396.6 mV/dec. For a-IGZO TFT, the corresponding values are V_{TH} = -0.46 V, mobility = 17.7 cm^2/V·s, and S.S = 81.6 mV/dec. As shown in Fig. 2, the simulated data was well fitted based on the measured data, achieving a coefficient of determination over 0.9996.

As shown in Fig. 3(a) and (b), the proposed pixel circuit can control the emission time and luminance of μLED by adjusting V_{DATA_PWM} based on the constant current driving. Here, the minimum average current over one frame at V_{DATA_PWM} = 3 V is 257 pA. We applied simultaneous variations of ±0.5 V to both $V_{TH\_DRT\_CCG}$ and $V_{TH\_DRT\_PWM}$ to verify the stability of the proposed circuit. Fig. 3(c) demonstrates the voltage variations of nodes A and B over time. After storing the $V_{TH\_DRT\_CCG}$ and $V_{TH\_DRT\_PWM}$ in stage (2), the node voltage difference of about 1 V between before and after the V_{TH} fluctuation should be maintained until the end of the frame. This value represents the difference in V_{TH} fluctuation for DRT_CCG and DRT_PWM. Therefore, the proposed circuit enables stable operation even in the V_{TH} variations, having less than a 2% relative current error rate across all gray levels, as shown in Fig. 3(d). We compared three different circuits with proposed circuit to verify these stable results based on three key factors.

A. Input position of sweep signal

Fig. 4(a) depicts the circuit (I) where applying point of the sweep signal and V_{DD_PWM} are interchanged compared to the proposed pixel circuit while the CCG part is the same as the proposed one. During emission stage of the circuit (I), the $V_{SG\_DRT\_PWM}$ increases as the $V_{SWEEP}[n]$ signal continuously decreases. When it surpasses $V_{TH\_DRT\_PWM}$, DRT_PWM is
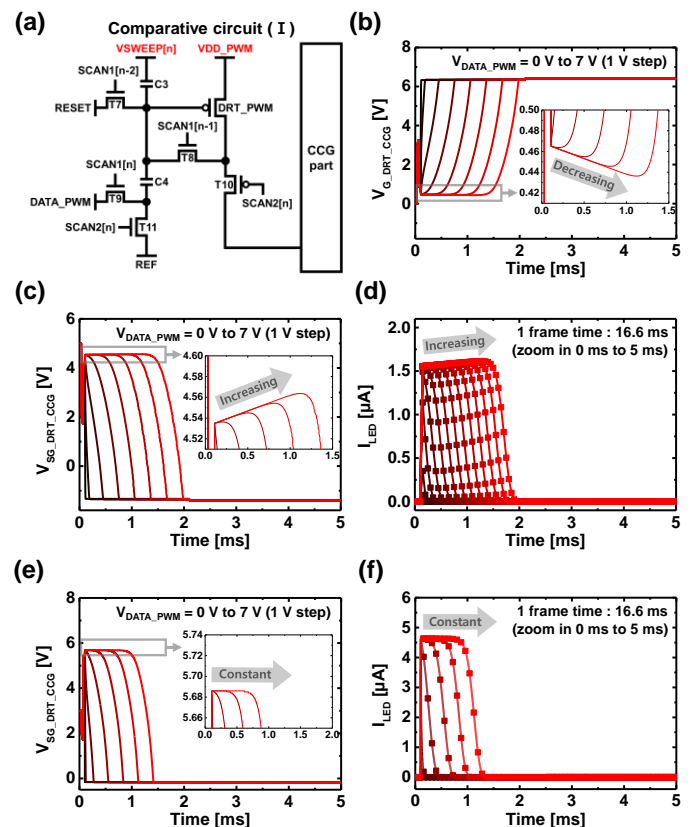

Fig. 4. (a) The schematic of comparative circuit (I) applying $V_{SWEEP}[n]$ at the gate node of DRT_PWM, the simulation result of (b) the gate node voltage of DRT_CCG, (c) V_{SG} of DRT_CCG, (d) μLED current (V_{DATA_PWM} = 0 V to 7 V), (e) V_{SG} of DRT_CCG when $C_{GD} = C_{GS} = 0$, and (f) μLED current when $C_{GD} = C_{GS} = 0$ (V_{DATA_PWM} = 0 V to 7 V).

turned on to terminate light emission. This operation closely resembles the emission stage of the proposed circuit. However, as $V_{SWEEP}[n]$ decreases during the emission stage, the gate node voltage of DRT_CCG decreases ($V_{G\_DRT\_CCG}$) due to the C_{GD} of DRT_PWM, causing an increase in $V_{SG\_DRT\_CCG}$, as shown in Fig. 4(b) and (c). Consequently, as illustrated in Fig. 4(d), the μLED current does not remain constant but increases during emission time. Such current level variation during the light emission induces wavelength shift in the μLED and results in image distortion. We also adjusted the parasitic capacitance-related parameters in the TFT model library to modify $C_{GD} = C_{GS} = 0$ and simulated on comparative circuit (I). As can be seen from Fig. 4 (e) and (f), $V_{SG\_DRT\_CCG}$ and μLED current are not affected regardless of the change in $V_{SWEEP}[n]$ when $C_{GD} = C_{GS} = 0$. Therefore, we confirm that the parasitic capacitances significantly affect the circuit operation. Therefore, it is effective to apply $V_{SWEEP}[n]$ at the source node of DRT_PWM to minimize the impact of sweep signal through the parasitic capacitor to achieve high image quality.
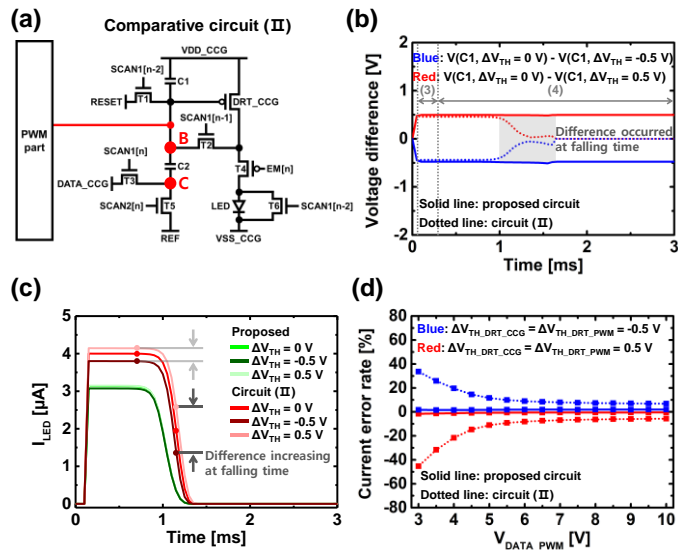
Fig. 5. (a) The schematic of comparative circuit (II) where the PWM part is connected to the gate node of DRT_CCG, (b) stored voltage difference at C1 when the $\Delta V_{TH} = 0$ V and when the $\Delta V_{TH} = \pm 0.5$ V, (c) the simulation result of µLED current ($V_{DATA\_PWM} = 8$ V), and (d) the relative current error rate of proposed circuit and comparison circuit.

B. Connection position between PWM and CCG parts

Fig. 5(a) illustrates the circuit (II) where the PWM part is connected to node B instead of node C of the CCG part. The PWM of circuit (II) has the same circuit structure as the proposed one. Fig. 5(b) shows the simulation results of the stored voltage difference in C1 caused by V_{TH} change (ΔV_{TH}) as much as ± 0.5 V. The stored voltage difference in C1, corresponds to the change in $V_{TH\_DRT\_CCG}$, should be maintained 0.5 V until the end of the emission, including the falling time, if the V_{TH} compensation is as successful as the proposed one. However, in the case of a circuit (II) where the PWM part is connected to gate node of DRT_CCG (node B), the stored voltage difference of 0.5 V could not be maintained. $V_{SWEEP}[n]$ is directly applied to node B through DRT_PWM and T10 at the emission stage, so it affects the stored $V_{TH\_DRT\_CCG}$ and V_{DATA_CCG} in C1 during falling time leading to stored voltage loss. Eventually, circuit (II) has a larger µLED current difference during falling time as shown in Fig. 5(c). As a result, it leads to a much higher relative current error rate compared to the proposed circuit, as depicted by the dotted line in Fig. 5(d). This error rate tends to increase, particularly in low gray levels where the falling time affects µLED current dominantly due to shorter emission time. Therefore, compensation accuracy can be improved by indirectly connecting the CCG part.

C. Connection timing between PWM and CCG parts

As shown in Fig. 6(a), during the emission stage, the circuit (III) connects the PWM and CCG parts by applying the EM[n] signal to T10 instead of the SCAN2[n] signal. All other
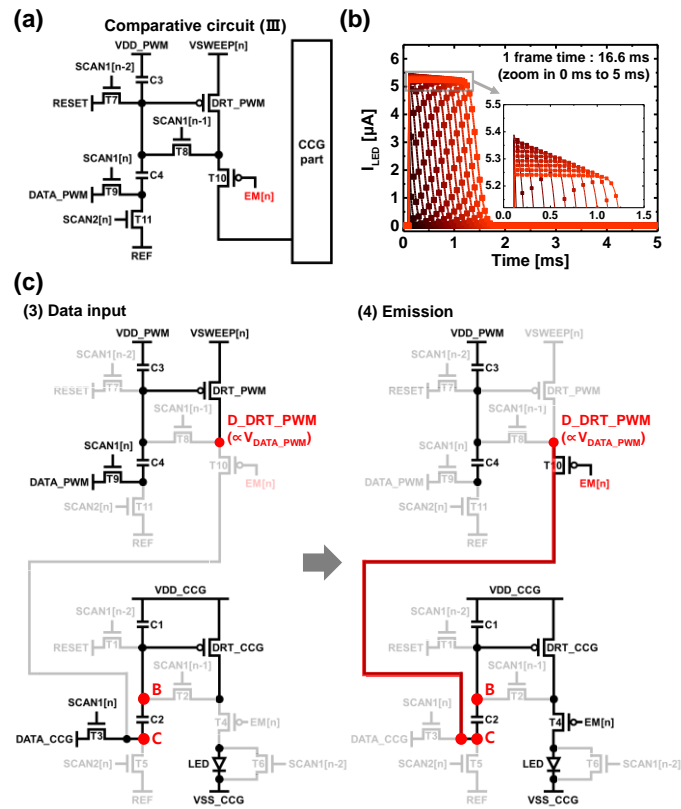

Fig. 6. (a) The schematic of comparative circuit (III) connecting PWM and CCG parts at emission stage, (b) the simulation result of µLED current ($V_{DATA\_PWM} = 3$ V to 10 V), and (c) operation in data input and emission stage of circuit (III).
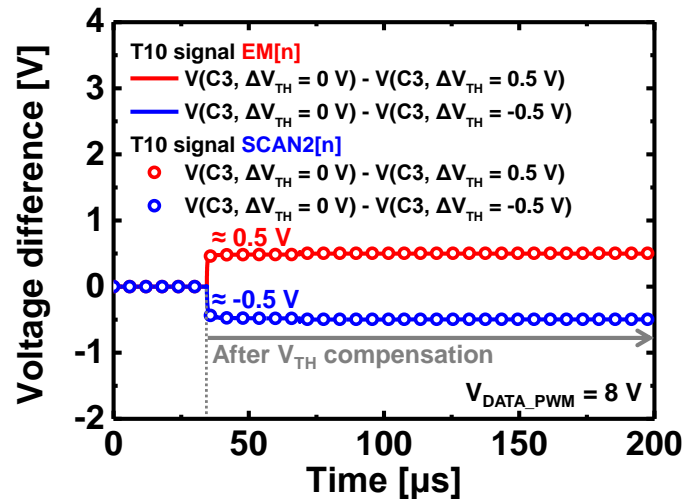

Fig. 7. Stored voltage difference at C3 when the $\Delta V_{TH} = 0$ V and when the $\Delta V_{TH} = \pm 0.5$ V ($V_{DATA\_PWM} = 8$ V).

circuit parameters and operations are the same as the proposed one. The simulation results show that the circuit (III) produces different current levels depending on the gray level, which can cause color distortion, as depicted in Fig. 6(b). During the V_{TH} compensation stage, the drain node of DRT_PWM (D_DRT_PWM) voltage becomes $V_{SWEEP}[n] + V_{TH\_DRT\_PWM}$, and this node maintains a floating state. Subsequently, during

the data input stage, this node voltage changes proportionally to V_{DATA_pwm} due to the coupling effect of DRT_PWM's C_{GD}. When EM[n] becomes a low voltage, the PWM and CCG parts are connected, and the light emission begins until DRT_PWM is turned on. Meanwhile, the D_DRT_PWM voltage affects the stored voltage in C1. This is because the stored voltage value in C1 changes due to charge conservation, similar to the principle of the data input as depicted in Fig. 6(c). In contrast, the proposed circuit pre-connects PWM and CCG parts through the SCAN2[n] signal during the data input stage, and it ensures the stable node C voltage without causing voltage fluctuations in C1. Meanwhile, when the PWM and CCG parts are connected at the data input stage, the voltage at the source and drain nodes of DRT_PWM have constant voltage value. As a result, the $V_{TH\_DRT\_pwm}$ stored in C3 is preserved without any voltage loss due to parasitic capacitances. As shown in Fig. 7, the voltage difference stored in C3 between $\Delta V_{TH\_DRT\_PWM} = \Delta V_{TH\_DRT\_CCG} = 0$ V and $\Delta V_{TH\_DRT\_pwm} = \Delta V_{TH\_DRT\_CCG} = \pm 0.5$ V is consistent with the difference in threshold voltage, regardless of the control signal applied to T10. Therefore, connecting at the data input stage does not significantly affect the compensation accuracy of the proposed pixel circuit.

IV. CONCLUSIONS

In this paper, we proposed a new 13T4C LTPO µLED pixel circuit that ensured a highly stable and uniform driving current with less than 2% relative errors throughout all gray levels. We suggested three key design points for stable operation. Firstly, the effect of parasitic capacitors can be minimized by applying the $V_{SWEEP}[n]$ signal to the source node of DRT_PWM so that the circuit can provide a stable square current pulse independent of the $V_{SWEEP}[n]$ signal. Secondly, we designed the circuit that indirectly connects the PWM part and the gate node of DRT_CCG to maintain the compensated stored V_{TH} in the capacitor even during falling time. Hence, the circuit can maintain not only a constant current level but also a uniform falling wave-shape under the variations of $V_{TH\_DRT\_CCG}$. Lastly, we connect the PWM and CCG parts during the data input stage to stabilize node voltage, so the circuit can ensure reliable voltage storage in C1. Thus, the current amplitude remains constant regardless of the gray level.

Through HSPICE simulation, we have systematically analyzed the proposed circuit design strategies to prove its structural advantages. In conclusion, our proposed pixel circuit can generate a constant current amplitude even during falling time, minimize the influence of the sweep signal, and ensure stable circuit operation despite variations in V_{TH}.

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