Received 25 October 2024; revised 2 December 2024 and 25 December 2024; accepted 7 January 2025. Date of publication 10 January 2025; date of current version 27 January 2025. The review of this article was arranged by Editor J. Kumar.

Digital Object Identifier 10.1109/JEDS.2025.3528073

TCAD Simulation Study of Cylindrical Vertical Double-Surrounding-Gate a-InGaZnO FETs and Geometric Parameter Optimization

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This work was supported in part by the National Key Research and Development Program under Grant 2021YFB3600704; in part by the National Natural Science Foundation of China under Grant 62274178 and Grant 92264204; and in part by the CAS Interdisciplinary Innovation Team under Grant JCTD-2022-07.

ABSTRACT Threshold control of amorphous In-Ga-Zn-O field-effect transistor (a-IGZO FET) is generally a critical issue through material composition adjustment. Instead, this work reports a cylindrical vertical double-surrounding-gate (DSG) a-IGZO FET, featuring flexibility of threshold modulation, by the 3-D technology computer-aided design (TCAD) simulation. Firstly, physics-based parameters are calibrated to single-gated vertical transistor experiments. Thereafter, the performance is simulated by sweeping inner gate (G_1) bias voltages under the various outer gate (G_2) voltages, indicating the ability of threshold modulation. Length-scaling and position-variation of G_2 significantly impact the transistor performance metrics. For in-depth understanding of dimensional dependence, the surface potential of the channel and the electric field distribution near electrode are systematically investigated for an ultra-thin outer gate electrode, via considering spatial and geometric effects. These results will boost a design technology co-optimization flow of the future DSG-a-IGZO-FET-based extremely large-scale and high-density M3D memory.

INDEX TERMS Vertical transistor, double-surrounding-gate, TCAD, a-IGZO, gate length, gate position, scaling behavior.

I. INTRODUCTION

Recently, amorphous In-Ga-Zn-O field-effect transistor (a-IGZO FET) has received considerable interest and been actively explored for applications in display drivers, flexible electronics and artificial synapse/neuron emulation, owing to its several remarkable advantages, such as high mobility in amorphous state, ultra-low leakage current and back-end-of-line (BEOL) compatibility [1], [2], [3]. Moreover, a-IGZO FET exhibits distinguishable sensitivity to a range of physical parameters, including light, pressure and gases, making it a promising candidate for sensor applications [4], [5], [6]. Notably, a-IGZO FETs have also been increasingly reported to be applied in high-performance capacitor-less dynamic random-access memory (DRAM) [7], [8], [9], [10]. Compared to a large 2T0C bit-cell area about $20F^2$ constructed by common planar FET structure, using vertical Channel-All-Around (CAA) IGZO FET, a 3D monolithic integrated bit cell merely requires $4F^2$ area for future extremely large-scale and high-density applications [11], [12], [13], [14]. However, threshold voltage control and sub-threshold optimization of a-IGZO FETs are generally critical issues due to complex material composition [15], [16], [17]. Moreover, the reliability issues on the cycle-to-cycle and device-to-device variations have been reported in the previous work [18]. To overcome such issues, a planar dual-gate IGZO transistor has been employed to compensate the threshold variations [19]. Thus, to incorporate a dual-gate structure into the vertical device can further enhance the gate control ability of transistors, mitigate the short-channel effects (SCEs), and

TABLE 1. Critical simulation parameters.

Symbol	Parameter	Value
CD	Critical Dimension	500 nm
t_{igzo}	Thickness of IGZO	3 nm
t_{ox1}	Thickness of GI_1	5 nm
t_{ox2}	Thickness of GI_2	4 nm
	Thickness of bottom electrode	100 nm
	Thickness of top electrode	70 nm

enable dynamic threshold voltage control, which provides the basis for some future technologies such as multi-value storage and multi-bit programming in 3D integrated DRAMs [19], [20]. It can also be applied in active-matrix organic light-emitting diode (AMOLED) pixel circuit to compensate threshold voltage variation, as well as shifting the operation characteristics of devices from enhancement mode to depletion mode to realize logic circuits at low voltages [21], [22], [23]. However, current discussions on vertical DSG FETs mainly focus on the optimization of Gate-All-Around (GAA) structure, with the channel material being silicon nanowire [24], [25], [26]. Generally, GAA device is another type of single-gate transistor. Compared to CAA, the GAA device is not proper in 2T0C vertical stacking due to its unique electrode position [27], [28]. Vertical dual-gate structures compatible with IGZO technology and CAA-device-based DRAM application have been barely reported due to the difficulty in device fabrication, which hinders further device optimization and associated DRAM's storage density.

In this article, towards future high-reliability and high-density memory application, a distinguishing cylindrical vertical double-surrounding-gate (DSG) a-IGZO FET is successfully proposed. Based on the previous CAA FET, an extra ultra-thin electrode is inserted as an outer gate inside the insulator layer between the drain and source electrodes. Via sweeping the bias voltages on the inner gate under various outer gate voltages, we observe a distinct threshold voltage control of this structure using a 3-D TCAD simulation tool. Performance metrics are investigated under different geometry parameters, including length scaling and position variation of the outer gate. Underlying physical mechanisms are studied in detail for the structural variations. These results will provide guidance for structural optimization of vertical dual-gate FETs for the cross-layer design of M3D applications.

II. DEVICE STRUCTURE AND FABRICATION

A. DSG FET STRUCTURE

The structure of proposed cylindrical vertical DSG a-IGZO FET is shown in Fig. 1(a). The vertical and horizontal (at the outer gate) 2D cross-sections are presented in Fig. 1(b) and (c), respectively. Fig. 1(d) shows the TCAD simulation structure with actual device dimensions. Different from the previous CAA structure, an additional ring gate is inserted into the spacer layer between S and D to enhance the control over the channel. The spacer material is also used as outer gate insulator (GI_2) material. The possible fabrication process of the proposed DSG structure is similar to CAA FET [12], [13], [14]. Particularly, the fabrication of G_2 is a critical step that is not included in the CAA process. Its possible fabrication approach can be referenced from relevant experiments, such as the 'C'-shaped outer gate oxide process reported in 2024 *VLSI* [29] and the metal gate electrode self-aligned oxidation process reported in 2024 *IEDM* [30]. Moreover, the channel length is determined by the thickness of the spacer layer and etching angle. The diameter of etched hole is defined as the critical dimension (CD), and its perimeter is nearly regarded as the channel width. In the simulation, hafnium dioxide HfO_2 is considered for the inner gate insulator (GI_1) and SiO_2 for the outer gate insulator (GI_2), the material of spacer. The source and drain electrodes are composed of TiN and two gates are made up of InZnO. The critical design parameters for the proposed DSG FET are listed in Table 1.

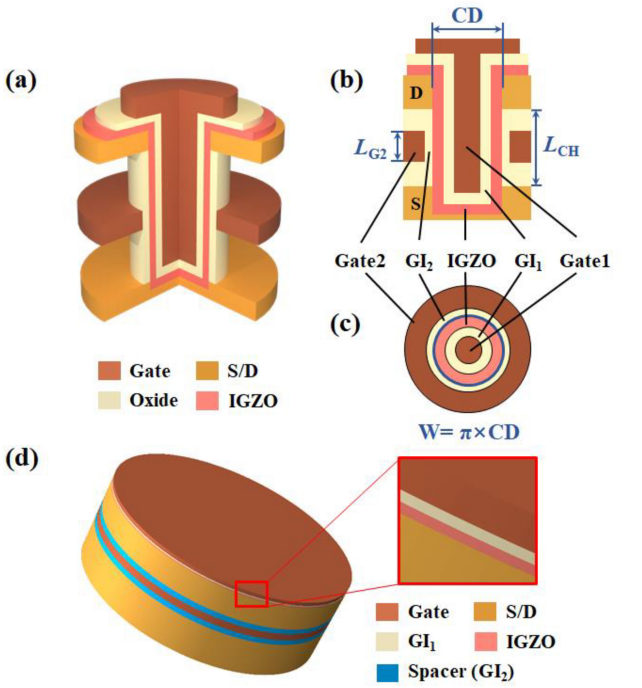

FIGURE 1. (a) The structure of proposed cylindrical vertical double-surrounding-gate (DSG) a-IGZO FET. (b) The vertical and (c) horizontal (at the outer gate) two-dimensional cross-sections of DSG structure. (d) TCAD simulation structure of DSG a-IGZO FET.

B. CAA FET FABRICATION

In order to establish an accurate simulation model and optimize the parameters, a group of CAA FETs were fabricated and tested for experimental data. The fabrication

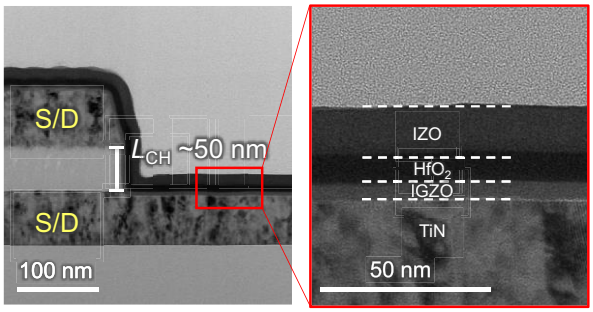

FIGURE 2. Cross-sectional TEM images of the fabricated CAA device with 500-nm CD and 50-nm channel length.

process flow is as follows: First, a TiN layer is deposited and patterned as the bottom S/D electrode. A silicon oxide spacer layer and the top TiN as another S/D electrode are deposited and patterned sequentially, forming the MIM structure. Then, a hole in MIM structure is etched to obtain the vertical channel by dry etching process. Finally, an IGZO film as channel, a hafnium oxide film as gate insulator and an In-Zn-O film as gate electrode are sequentially deposited by plasma-enhanced atomic layer deposition (PEALD) at 250°C. Fabrication process details can refer to our previous publication [13]. Fig. 2 shows the cross-sectional TEM images of the fabricated CAA device with 500-nm CD and 50-nm channel length.

C. MODEL CALIBRATION

Fig. 3(a) and (b) show the transfer characteristic curves and transconductance of 10 fabricated CAA device samples from the same process batch, respectively. The statistical distribution of the extracted threshold voltages is inset. Device-to-device variations can be clearly observed for vertical CAA transistors. In our previous work [19], an independent dual-gate complementation scheme is utilized to improve the circuit reliability, which indicates the essentiality of introducing the dual-gate structure for threshold modulation to ensure the uniformity of device performance. Thus, on this basis, a vertical dual-gate transistor is proposed to overcome the reliability issues in the CAA devices for future circuit applications.

All 3-D simulations are performed by VICTORYDEVICE simulator of SILVACO TCAD. Density of states (DOS) model, Fermi-Dirac model and Abe's electron mobility model [31] are employed for carrier distribution and transport mechanism in the IGZO channel, respectively. The calibration results between simulation device model and tested experimental data of CAA FETs are shown in Fig. 3(c). The asymmetric characteristics of source and drain electrodes are examined by exchanging electrodes, which was investigated in another work [32]. The simulated transfer characteristic curves match well with the experimental data, which proves the validity of simulation environment. Besides extracted parameters, the G_2 with 30 nm length (L_{G2} = 30 nm) is incorporated, transfer curves with a V_{g1} sweep under various

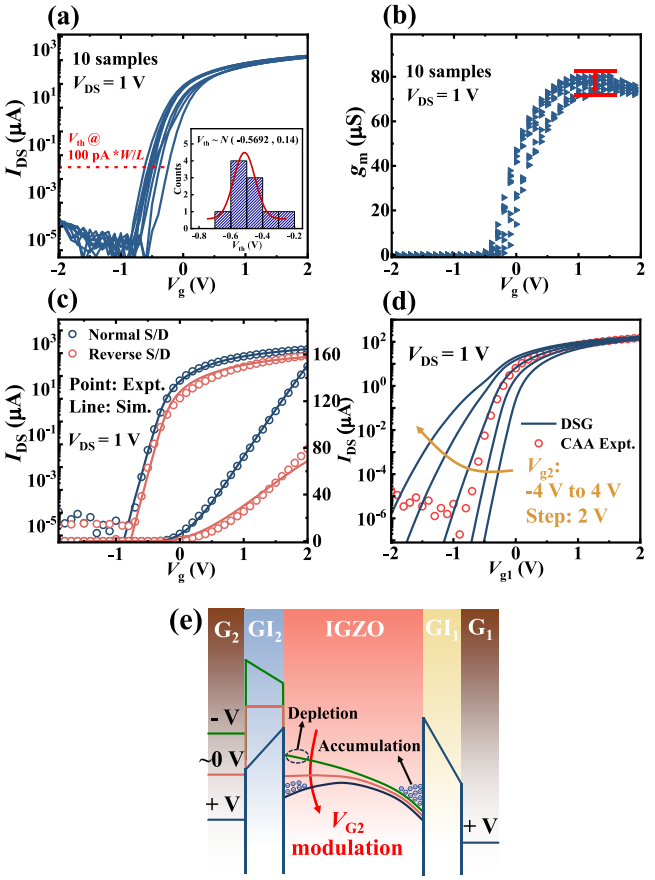

FIGURE 3. (a) Transfer curves of 10 fabricated CAA device samples and insert the statistical distribution of the threshold voltages. (b) Transconductance extracted from I-V curves of 10 samples. (c) Simulation calibration to experiments for CAA a-IGZO FETs with V_{DS} = 1 V and L_{CH} = 50 nm. (d) The transfer characteristic curve simulation of DSG a-IGZO FETs when V_{g2} varies from −4 V to 4 V based on extracted parameters. Besides extracted parameters, L_{G2} = 30 nm and G_2 is located at the center. (e) Energy band diagrams and carrier concentration distributions under different G_2-voltage conditions.

V_{g2} are shown in Fig. 3(d), demonstrating an ability of threshold modulation. Here G_2 is located at the center of the channel, with V_{DS} = 1 V and normal S/D. V_{th} (V) is defined as the V_{g1} given by I_{DS} (A) of $W/L \times 100$ pA. For independent dual-gate devices, under the effect of positive V_{G1}, electrons accumulate at the interface of GI_1/ IGZO and form the main channel. Considering the significant double-gate coupling effect, G_2 can control the electrons accumulation or depletion at the interface of GI_1/ IGZO, which in turn affects the carrier concentration of the whole channel as well as the degree of energy band bending, as shown in Fig. 3(e).

III. GEOMETRIC PARAMETER OPTIMIZATION

A. THE OUTER GATE LENGTH (LG2)

To investigate the impact of the outer gate length L_{G2} on device performance, several designs of experiments are simulated [33]. Firstly, the channel length L_{CH} is fixed at 50 nm and L_{G2} varies from 2 nm to 40 nm. The transfer characteristic curves of CAA FET and DSG FET as L_{G2}

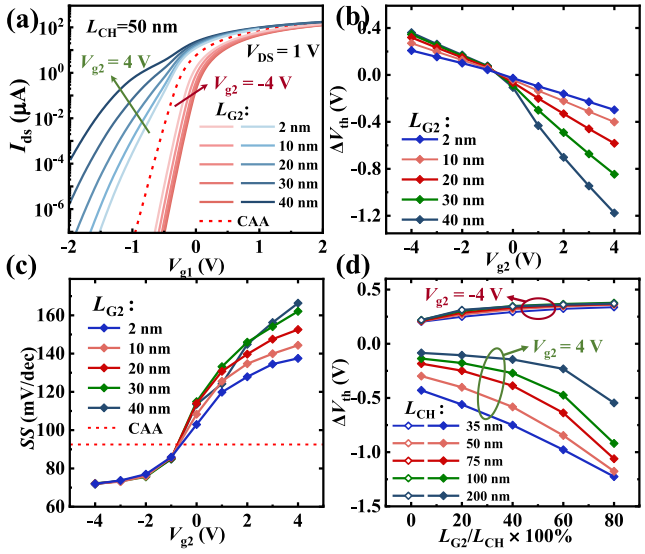

FIGURE 4. (a) The transfer characteristic curves of CAA FET and DSG FETs as L_{G2} scaling down when V_{g2} is set to 4 V and −4 V (b) ΔV_{th} and (c) SS vs. V_{g2} curves under different L_{G2} with L_{CH} = 50 nm. (d) ΔV_{th} vs. L_{G2}/L_{CH} curves with V_{g2} = −4 V and 4 V at different channel lengths.

scaling down when V_{g2} is set to 4 V and −4 V are shown in Fig. 4(a), and performance differences of dual-gate devices are obvious. Fig. 4(b) and (c) show the threshold voltage shift ($\Delta V_{th} = V_{th,DSG}$-$V_{th,CAA}$) and subthreshold swing (SS) vs. V_{g2} curves under different L_{G2}, respectively. As L_{G2} decreases, the absolute value of ΔV_{th} decreases at the same V_{g2}, which indicates a weak G_2-control over the channel. The degradation effect is severer at a positive V_{g2} than that at a negative V_{g2}. The deterioration of SS with increase of the V_{g2} is also alleviated with L_{G2} decreasing. Particularly, even when L_{G2} is scaled down to 2 nm, an obvious threshold voltage shift is still observed via altering V_{g2}. Furthermore, Fig. 4(d) shows the impact of L_{G2} scaling (L_{G2}/ L_{CH}=4%, 20%, 40%, 60%, 80%) on the threshold voltage control ability at different channel lengths (L_{CH} = 35, 50, 75, 100, 200 nm). It can be clearly observed that at a fixed L_{G2}/L_{CH}, as L_{CH} increases, the absolute value of ΔV_{th} decreases notably under the condition of $V_{g2} = 4$ V, and remains almost unchanged under the condition of $V_{g2} = -4$ V. In general, the extremely scaled G_2 holds a more acceptable ability of channel control in short-channel devices than long-channel devices.

To deeply analyze the influence of L_{G2} extreme scaling on the threshold modulation ability of dual-gate devices, the electric field distribution under L_{CH}=50 nm, L_{G2}=2 nm, V_D=1 V and V_{g2}=−4 V is shown in Fig. 5. It can be clearly observed that except for the region directly below G_2, fringe electric field from the upper and lower surfaces of G_2 provides additional control over the channel, allowing the device to still retain appreciable threshold modulation ability and leading to a feasible extreme L_{G2} scaling [34], [35], [36]. Compared to the case of short channel length, an additional channel control length covered by the fringe electric field (L_{Fr}) is nearly fixed for long

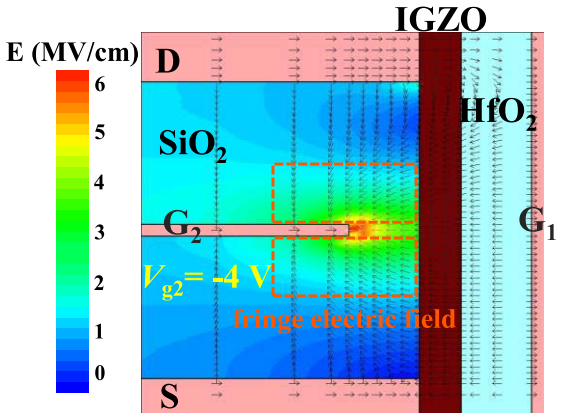

FIGURE 5. Electric field distribution in SiO_2 spacer layer for the DSG a-IGZO FET with L_{G2} = 2 nm, L_{CH} = 50 nm, V_D = 1 V and V_{g2} = −4 V.

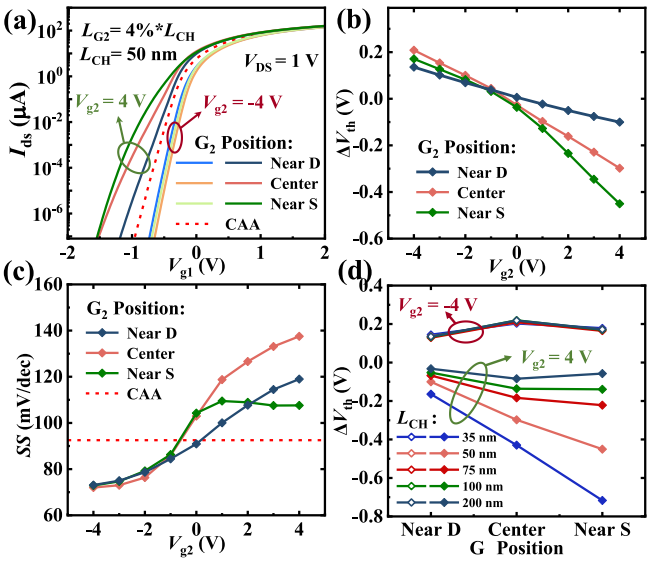

FIGURE 6. (a) The transfer characteristic curves of CAA FET and DSG FETs with different G_2 positions (L_{CH} = 50 nm, L_{G2} = 4%*L_{CH}=2 nm, V_{DS}=1 V, V_{g2} = −4 V and 4 V). (b) ΔV_{th} and (c) SS vs. V_{g2} curves with different G_2 positions (L_{CH} = 50 nm). (d) ΔV_{th} vs. L_{G2}/L_{CH} curves with V_{g2} = −4 V and 4 V at different channel lengths.

channel. Since L_{Fr}/L_{CH} increases at a decreased L_{CH}, presence of the fringe electric field will greatly enhance the G_2 gate control in short-channel devices.

B. THE OUTER GATE POSITION

The position of the outer gate relative to the channel is an important geometric parameter considering asymmetric electric field distribution. Hence, the performance of DSG FETs with various G_2 positions is also investigated. The rate of L_{G2}/L_{CH} is fixed at 4% and three different gate positions are considered for comparison: Near Drain (4 nm from drain), Center (equal distance from the source and drain) and Near Source (4 nm from source). Fig. 6(a) shows the transfer characteristic curves of CAA FET and DSG FETs with different G_2 positions (at L_{CH}=50 nm), and obvious performance variations are observed. Fig. 6(b) and

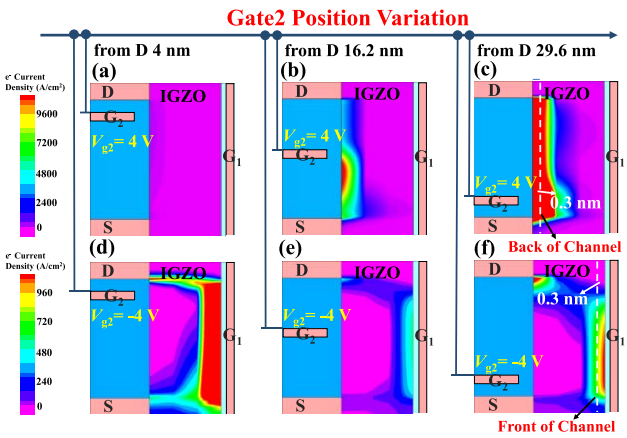

FIGURE 7. The current density distribution when G_2 is located at the (a) Near-D, (b) Center and (c) Near-S positions in a-IGZO channel for DSG FETs with L_{CH} = 35 nm, L_{G2} = 1.4 nm, V_{g1} =−0.7 V and V_{g2} = 4 V. These results indicate the formation of back channel when G_2 is applied by a large positive voltage. The current distribution of the three G_2-position devices at L_{CH} = 35 nm, L_{G2} = 1.4 nm, V_{g1} = −0.3 V and V_{g2} = −4 V are then shown in (d-f), indicating the depletion of the front channel. Contour cutline in a-IGZO layer with 0.3 nm from the inner (outer) surface is utilized to estimate the electron concentration and current density distribution of front (back) channel [37].

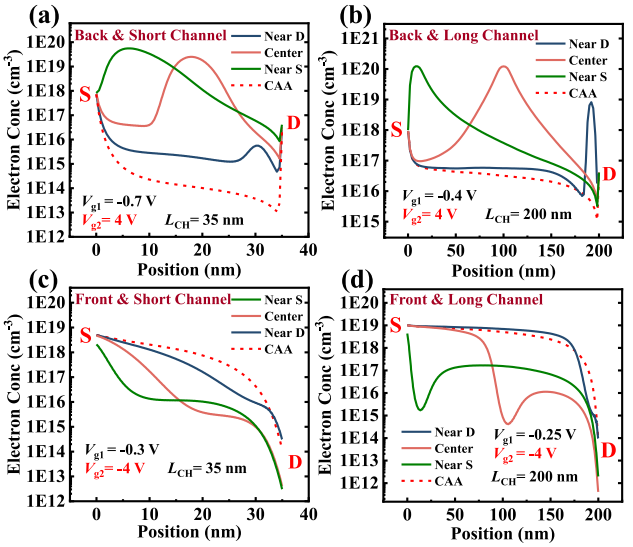

FIGURE 8. (a) The electron concentration distribution along the back surface of channel with L_{CH} = 35 nm V_{g1} = −0.7 V and V_{g2} = 4 V; (b) along the back surface with L_{CH}=200 nm, V_{g1} =−0.4 V and V_{g2} =4 V; (c) along the front surface with L_{CH} =35 nm, V_{g1} = −0.3 V and V_{g2} =-4 V; (d) along the front surface with L_{CH}= 200 nm, V_{g1} =−0.25 V and V_{g2} = −4 V.

(c) further indicate ΔV_{th} and SS vs. V_{g2} curves considering spatial dependence of G_2, respectively. In the negative region of V_{g2}, the variation of ΔV_{th} induced by positions is not large. Additionally, the Center-gate configuration presents a largest ΔV_{th}. However, when V_{g2} is converted to positive region, the ΔV_{th} in all three gate configurations becomes more pronounced. Moreover, the largest threshold voltage shift is found in Near-S gate device, while the smallest one presents in Near-D gate device. In addition, among three configurations, the SS shows non-monotonic increase for Near-S gate device. To further comprehend the working principles, device simulations under various channel lengths are also performed, as shown in Fig. 6(d). When V_{g2}=−4 V, the results of threshold voltage shift are nearly independent on L_{CH}. However, when V_{g2}=4 V, as L_{CH} increases, the strength of gate controllability for modulating the threshold voltage gradually changes from "Near S > Center > Near D" to "Center > Near S ≈ Near D". The performance differences induced by various gate positions are extremely pronounced in short-channel devices.

In order to investigate the underlying physical mechanisms, the current density and electron concentration distribution in a-IGZO channel layer are projected in different configurations near the threshold voltage. As shown in Fig. 7(a-c), in short-channel devices at L_{CH}=35 nm, V_{g2}=4 V and V_{g1}=−0.7 V, a higher current density corresponds to the more negatively shifted threshold voltage, due to the formation of back channel when G_2 is applied by a large positive voltage. Given by a large negative voltage on G_2 in devices at L_{CH}=35 nm, V_{g2}=−4 V and V_{g1}=−0.3 V, it manifests a depletion of the front channel and a lower current density represents the more positively shifted threshold voltage, as shown in Fig. 7(d-f). The different modulation mechanisms of G_2 on the conductivity of IGZO channel under positive and negative voltages, particularly the dominant transport mechanism and carrier density profile variations, which are dependent on the gate voltage, lead to a significant asymmetry in the electrical characteristic curves at the same voltage magnitude [38], [39], [40]. Meanwhile, the effective gate capacitance of G_2 (C_{g2}) varies with different bias conditions. Under positive voltage, the C_{g2} is composed only of the outer gate insulator capacitance (C_{ox2}). However, under negative bias, the electric field lines emitted by G_2 need to vertically traverse the active layer to reach the front channel, resulting in the C_{g2} being comprised of the series combination of C_{ox2} and active layer capacitance (C_{igzo}). This is also the reason for the asymmetry of device's electrical characteristic curves [41].

Furthermore, the electron concentration distribution on the a-IGZO channel surfaces is analyzed. According to Fig. 8(a), in the case of short channel and positive V_{g2}, the electron concentration at the back surface of channel for Near-S gate is significantly higher than the other, attributed to the lower surface potential [42], [43]. And the area covered by the fringe electric field takes a large portion of the entire channel length. Therefore, the Near-S gate device shows a superior performance. When L_{CH} is extended to 200 nm, electron concentrations of Near-S and Center gate devices are almost equal. Unlike Near-S gate, the performance of Center-gate shows better gate control with electric field distribution on both sides, as shown in Fig. 8(b). Figs. 8(c), (d) illustrate the electron concentrations along the front

surface of channel for short-channel (L_{CH}=35 nm) and long-channel (L_{CH}=200 nm) devices at V_{g2} =−4 V, respectively. Due to ultra-thin a-IGZO layer, a strong depletion of the channel is observed in all three cases with little difference in performance as mentioned above. Particularly, when G_2 is set chose to the drain, the electric field from the drain will weaken the gate's control over the channel. Hence the Near-D gate devices indicate the worst threshold modulation in all cases.

IV. CONCLUSION

In summary, a cylindrical vertical double-surrounding-gate amorphous IGZO field-effect transistor is proposed. Via 3-D TCAD simulations, effects of critical geometry parameters, including the gate length and position of the outer gate as well as channel length, on device performance are investigated. It is found that an extremely scaled gate exhibits better gate control in short-channel devices. For the case of short-channel and positive V_{g2}, the Near-S gate shows the best controllability of threshold voltage. Instead, among other cases, the center gate will take advantage in threshold voltage control. These characteristics are explained by potential and electric field predictions, showing a great potential for threshold-modulated high-density M3D capacitor-less DRAM applications.

REFERENCES

[1] M. Aman et al., "Reliability improvement of IGZO-TFT in hybrid process with LTPS," *J. Soc. Inf. Display*, vol. 29, no. 5, pp. 416–427, May 2021, doi: 10.1002/jsid.1032.

[2] B. Bao et al., "Flexible IGZO TFT technology for shift register drivers," *Adv. Electron. Mater.*, vol. 10, no. 10, Oct. 2024, Art. no.2400036, doi: 10.1002/aelm.202400036.

[3] Y. He, S. Nie, R. Liu, S. Jiang, Y. Shi, and Q. Wan, "Dual-functional long-term plasticity emulated in IGZO-based photoelectric neuromorphic transistors," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 818–821, May 2019, doi: 10.1109/LED.2019.2908727.

[4] Y. Lai, I. Wang, and T. Hou, "Giant photoresponsivity and external quantum efficiency in a contact-engineered broadband a-IGZO phototransistor," *Adv. Funct. Mater.*, vol. 32, no. 24, Jun. 2022, Art. no. 2200282, doi: 10.1002/adfm.202200282.

[5] C. Xin et al., "Highly sensitive flexible pressure sensor by the integration of microstructured PDMS film with a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1073–1076, Jul. 2018, doi: 10.1109/LED.2018.2839595.

[6] D. Lee et al., "Highly sensitive oxygen sensing characteristics observed in IGZO based gasistor in a mixed gas ambient at room temperature," *ACS Sens.*, vol. 7, no. 9, pp. 2567–2576, Sep. 2022, doi: 10.1021/acssensors.2c00484.

[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488–92, Dec. 2004, doi: 10.1038/nature03090.

[8] J.-Y. Kwon, D.-J. Lee, and K.-B. Kim, "Review paper: Transparent amorphous oxide semiconductor thin film transistor," *Electron. Mater. Lett.*, vol. 7, no. 1, pp. 1–11, Mar. 2011, doi: 10.1007/s13391-011-0301-x.

[9] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, Jun. 2012, doi: 10.1002/adma.201103228.

[10] P. Houshmand et al., "Opportunities and limitations of emerging analog in-memory compute DNN architectures," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA: IEEE, Dec. 2020, pp. 29.1.1–29.1.4, doi: 10.1109/IEDM13553.2020.9372006.

[11] A. Belmonte et AL., "Capacitor-less, long-retention (>400s) DRAM cell paving the way towards low-power and high-density monolithic 3D DRAM," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2020, p. 28.2.1–28.2.4. doi: 10.1109/IEDM13553.2020.9371900.

[12] X. Duan et al., "Novel vertical channel-all-around (CAA) In-Ga-Zn-O FET for 2T0C-DRAM with high density beyond 4F ^{2} by monolithic stacking," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2196–2202, Apr. 2022, doi: 10.1109/TED.2022.3154693.

[13] C. Chen et al., "Inter-layer dielectric engineering for monolithic stacking 4F ^{2}-2T0C DRAM with channel-all-around (CAA) IGZO FET to achieve good reliability (>10^4 s bias stress, >10^{12} cycles endurance)," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2022, pp. 26.5.1–26.5.4, doi: 10.1109/IEDM45625.2022.10019502.

[14] C. Chen et al., "First demonstration of stacked 2T0C-DRAM bit-cell constructed by two-layers of vertical channel-all-around IGZO FETs realizing 4F^2 area cost," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413790.

[15] J.-H. Kim et al., "Bias and illumination instability analysis of solution-processed a-InGaZnO thin-film transistors with different component ratios," *Thin Solid Films*, vol. 645, pp. 154–159, Jan. 2018, doi: 10.1016/j.tsf.2017.09.054.

[16] Y. Park et al., "Defect engineering for high performance and extremely reliable a-IGZO thin-film transistor in QD-OLED," *Adv. Electron. Mater.*, vol. 8, no. 7, Jul. 2022, Art. no. 2101273, doi: 10.1002/aelm.202101273.

[17] D.-H. Lee, S.-M. Park, D.-K. Kim, Y.-S. Lim, and M. Yi, "Effects of Ga composition ratio and annealing temperature on the electrical characteristics of solution-processed IGZO thin-film transistors," *J. Semicond. Technol. Sci.*, vol. 14, no. 2, pp. 163–168, Apr. 2014, doi: 10.5573/JSTS.2014.14.2.163.

[18] J. Guo et al., "Compact modeling of IGZO-based CAA-FETs with time-zero-instability and BTI impact on device and capacitor-less DRAM retention reliability," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Honolulu, HI, USA, Jun. 2022, pp. 300–301, doi: 10.1109/VLSITechnologyandCir46769.2022.9830482.

[19] L. Xu et al., "Reliability-aware ultra-scaled IDG-InGaZnO-FET compact model to enable cross-layer co-design for highly efficient analog computing in 2T0C-DRAM," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413757.

[20] K. Chen et al., "Improved multi-bit statistics of novel dual-gate IGZO 2T0C DRAM with in-cell V_{TH} compensation and ΔV_{SN} /ΔV_{DATA} boosting technique," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413770.

[21] Y.-H. Tai, L.-S. Chou, H.-L. Chiu, and B.-C. Chen, "Three-transistor AMOLED pixel circuit with threshold voltage compensation function using dual-gate IGZO TFT," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 393–395, Mar. 2012, doi: 10.1109/LED.2011.2179282.

[22] S. H. Nam, P. J. Jeon, Y. T. Lee, S. R. A. Raza, and S. Im, "NOT and NOR logic circuits using passivation dielectric involved dual gate in a-InGaZnO TFTs," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1527–1529, Dec. 2013, doi: 10.1109/LED.2013.2285185.

[23] Y. V. Li, J. I. Ramirez, K. G. Sun, and T. N. Jackson, "Low-voltage double-gate ZnO thin-film transistor circuits," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 891–893, Jul. 2013, doi: 10.1109/LED.2013.2263193.

[24] Y. Chen and W. Kang, "Experimental study and modeling of double-surrounding-gate and cylindrical silicon-on-nothing MOSFETs," *Microelectron. Eng.*, vol. 97, pp. 138–143, Sep. 2012.

[25] S. Rewari, S. Haldar, V. Nath, S. S. Deswal, and R. S. Gupta, "Numerical modeling of Subthreshold region of junctionless double surrounding gate MOSFET (JLDSG)," *Superlatt. Microstruct.*, vol. 90, pp. 8–19, Feb. 2016, doi: 10.1016/j.spmi.2015.11.026.

[26] V. M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF switch," *Microelectron. J.*, vol. 42, no. 10, pp. 1124–1135, Oct. 2011, doi: 10.1016/j.mejo.2011.07.003.

[27] S. Fujii et al., "Oxide-semiconductor channel transistor DRAM (OCTRAM) with 4F2 architecture," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2024, pp. 6.1.1–6.1.4.

[28] W. Zhao et al., "High-performance vertical gate-all-around oxide semiconductor transistors with 6 nm ALD IGZO channel and scaled contact CD down to 28 nm," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2024, pp. 1–11.

[29] Z. Liu et al., "A dual-gate vertical channel IGZO transistor for BEOL stackable 3D parallel integration for memory and computing applications," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Honolulu, HI, USA, Jun. 2024, pp. 1–2, doi: 10.1109/VLSITechnologyandCir46783.2024.10631472.

[30] F. Liao et all., "Novel $4F^2$ multi-bit dual-gate 2T0C for high-density dram with improved vertical-channel IGZO TFTs by self-aligned single- step process," in *Proc. Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2024, pp. 6.7.1–6.7.4.

[31] K. Abe, A. Sato, K. Takahashi, H. Kumomi, T. Kamiya, and H. Hosono, "Mobility- and temperature-dependent device model for amorphous In–Ga–Zn–O thin-film transistors," *Thin Solid Films*, vol. 559, pp. 40–43, May 2014, doi: 10.1016/j.tsf.2013.11.066.

[32] Q. Chen et al., "Investigation of asymmetric characteristics of novel vertical channel-all-around (CAA) In-Ga-Zn-O field effect transistors," *IEEE Electron Device Lett.*, vol. 43, no. 6, pp. 894–897, Jun. 2022, doi: 10.1109/LED.2022.3168059.

[33] S. Subhechha et al., "First demonstration of sub-12 nm Lg gate last IGZO-TFTs with oxygen tunnel architecture for front gate devices," in *Symp. VLSI Technol. Tech. Dig.*, 2021, pp. 1–2.

[34] F. Wu et al., "Vertical MoS2 transistors with sub-1-nm gate lengths," *Nature*, vol. 603, no. 7900, pp. 259–264, Mar. 2022, doi: 10.1038/s41586-021-04323-3.

[35] P. Cadareanu, J. Romero-Gonzalez, and P.-E. Gaillardon, "Parasitic capacitance analysis of three-independent-gate field-effect transistors,"*IEEE J. Electron Devices Soc.*, vol. 9, pp. 400–408, 2021, doi: 10.1109/JEDS.2021.3070475.

[36] T. Mizuno, T. Kobori, Y. Saitoh, S. Sawada, and T. Tanaka, "High dielectric LDD spacer technology for high performance MOSFET using gate-fringing field effects," in *Proc. Int. Tech. Dig. Electron Devices Meeting*, Washington, DC, USA, 1989, pp. 613–616. doi: 10.1109/IEDM.1989.74355.

[37] M. M. Billah et al., "Effect of grain boundary protrusion on electrical performance of low temperature polycrystalline silicon thin film transistors," *J. Electron Devices Soc.*, vol. 7, pp. 503–511, 2019, doi: 10.1109/JEDS.2019.2911088.

[38] S. Lee et al., "Temperature dependent electron transport in amorphous oxide semiconductor thin film transistors," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 2011, pp. 14.6.1–14.6.4, doi: 10.1109/IEDM.2011.6131554.

[39] M. Chun, M. D. H. Chowdhury, and J. Jang, "Semiconductor to metallic transition in bulk accumulated amorphous indium-gallium-zinc-oxide dual gate thin-film transistor," *AIP Adv.*, vol. 5, no. 5, May 2015, Art. no. 57165, doi: 10.1063/1.4922005.

[40] S. H. Park, M. Mativenga, and J. Jang, "Increase of mobility in dual gate amorphous-InGaZnO4 thin-film transistors by pseudo-doping," *Appl. Phys. Lett.*, vol. 103, no. 4, Jul. 2013, Art. no. 43509, doi: 10.1063/1.4816587.

[41] M. Moradi, A. A. Fomani, and A. Nathan, "Effect of gate dielectric scaling in nanometer scale vertical thin film transistors," *Appl. Phys. Lett.*, vol. 99, no. 22, Nov. 2011, Art. no. 223503, doi: 10.1063/1.3664217.

[42] H. A. El Hamid, B. Iniguez, and J. Roig Guitart, "Analytical model of the threshold voltage and subthreshold swing of undoped cylindrical gate-all-around-based MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 572–579, Mar. 2007, doi: 10.1109/TED.2006.890595.

[43] Z.-H. Liu et al., "Threshold voltage model for deep-submicrometer MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 86–95, Jan. 1993, doi: 10.1109/16.249429.