Received 17 July 2024; revised 12 September 2024; accepted 12 September 2024. Date of publication 23 September 2024; date of current version 7 October 2024. The review of this article was arranged by Editor C.-H. Kim.

*Digital Object Identifier 10.1109/JEDS.2023.3465669*

# High-Performance Carbon Nanotube Optoelectronic Transistor With Optimized Process for 3D Communication Circuit Applications

**SHUANG LIU [1,2,3], HEYI HUANG[1,2,3], YANQING LI[1,2,3], YADONG ZHANG [1,2,3], FEIXIONG WANG [1,2,3], ZHAOHAO ZHANG [1,2,3], QINGZHU ZHANG [1,2,3] (Member, IEEE), JIALI HUO [1,2,3], JIAXIN YAO [1,2,3] (Associate Member, IEEE), JING WEN[1,2,3], AND HUAXIANG YIN [1,2,3] (Senior Member, IEEE)**

1 Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences, Beijing 100029, China
2 Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
3 School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing 100049, China

CORRESPONDING AUTHORS: H. HUANG AND H. YIN (e-mail: huangheyi@ime.ac.cn; yinhuaxiang@ime.ac.cn)

This work was supported by the National Key Research and Development Plan "Nano Frontier" Key Special Project under Grant 2021YFA1200502.

**ABSTRACT** One-dimensional carbon nanotube field-effect transistors (CNFETs) have offered a solution for obtaining high transistor performance in a compatible low-temperature BEOL process, enabling monolithic 3D integration benefits for more functional circuits. Currently, CNT transistors need to further improve their performance with a more stable process and explore the most suitable circuit application scene. In this study, we successfully enhanced the performance of CNFETs through special $Y_2O_3$ film passivation and vacuum annealing processes. The on-state current of the optimized device was improved by 36.6× compared to the device without these processes. Besides, the subthreshold swing (SS) was notably reduced from 259 mV/dec to 215 mV/dec and the threshold voltage was decreased from 2.02 V to 1.79 V due to the reduction of the interface state. Meanwhile, the devices' optoelectronic characteristics were significantly improved and exhibited a 72× increase in $\Delta I_{ds}$ under identical illumination. With an improved annealing process, the $\Delta I_{ds}$ were further increased to 231× compared to the original device because of the reduction of defects within the device. Finally, the tentative Morse code communication applications all by the optimized CNFETs were obtained. These technologies and functional implementations provided a promising approach for future 3D functional communication systems with CNT technology.

**INDEX TERMS** Carbon nanotube field-effect transistors (CNFETs), optoelectronic devices, Morse code communication.

## I. INTRODUCTION

Silicon-based complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) have driven the rapid advancement of microelectronic technology over the past six decades [1], [2]. As the industry evolves, the integration of innovative materials into integrated circuit (IC) design has become increasingly prevalent. The pursuit of novel semiconductors with extraordinarily thin thickness and superior carrier mobility has been a key strategy [2], [4]. In the burgeoning field of semiconductor materials, carbon nanotubes have distinguished themselves as a compelling material due to their exceptional physicochemical stability, superior electron mobility [5], direct gap [6], and amenability to low-temperature device fabrication processes [7], [8]. These intrinsic attributes have rendered CNTs one of the interesting materials for the development of high-performance and

© 2023 The Authors. This work is licensed under a Creative Commons Attribution 4.0 License.
For more information, see https://creativecommons.org/licenses/by/4.0/

multi-functional transistors for advanced monolithic 3D circuits [9], [10], [11], [12]. Furthermore, the development of carbon nanotube-based room-temperature transistors was successfully accomplished in 1998 [13], marking a significant milestone in the evolution of CNFET research.

Although carbon nanotubes possess intrinsic advantages, additional enhancements in the performance of carbon nanotube transistors are essential to guarantee process stability and optimize their integration into 3D circuit applications. To address these needs, the research has proposed using oxide passivation to enhance the ON/OFF current ratio [14]. Moreover, the implementation of annealing processes across a range of temperatures is known to exert variable influences on the optimization of CNFETs [15]. However, these studies have predominantly concentrated on electrical aspects of device performance enhancement, with few reports on improvements in multimodal aspects. Optoelectronic modulation is another important research direction for device applications due to its advantages such as fast response speed, separation of read and write operations, and reduced crosstalk. To enhance the optoelectronic performance of a device, refining the surface properties of the channel material is a pivotal strategy. Yu Huang et al. have shown that the assembly of ZnPc molecules on the surface of $MoS_2$ can significantly improve the device's response speed [16]. Furthermore, the integration of Au nanoparticles onto the surface of black phosphorus-based photodetectors has been demonstrated to substantially boost light absorption due to the localized surface plasmon resonance effect [17]. In terms of CNT-based optoelectronic research, C Torres-Torres et al. have reported the observation of photoconductivity and light absorption response of carbon nanotubes [18], followed by Alexandra L. Gorkina et al. who have reported the enhancement of optoelectronic properties of thin films by hybridizing carbon nanotubes with graphene [19]. The complex optimization process is not compatible with CMOS technology, limiting its application scope. Thus, we need a new method that enhances both the electrical and optoelectronic properties of CNFETs while being compatible with CMOS technology.

In the paper, we dedicated efforts toward enhancing the performance of CNFETs through targeted $Y_2O_3$ passivation and vacuum annealing process optimizations and achieved a significant enhancement in device performance of electrical properties. The on-state current of the optimized CNFETs was amplified 36.6× and the subthreshold swing was reduced by 17% when compared to the transistors without an optimized process. In addition, the optoelectronic characteristics of the optimized CNFETs were investigated in detail and got a pronounced enhancement. Under consistent illumination conditions, the devices with $Y_2O_3$ passivation film and those with vacuum annealing process demonstrated a 72× and 231× increase in $\Delta I_{ds}$, respectively. With these device advancements, we successfully demonstrated on tentative circuit for Morse code communication all by CNFETs, showcasing their versatility in functional system applications. These lay a solid and promising groundwork for the future of transistor optimization and the pursuit of 3D multifunctional integrated circuits with CNT devices.

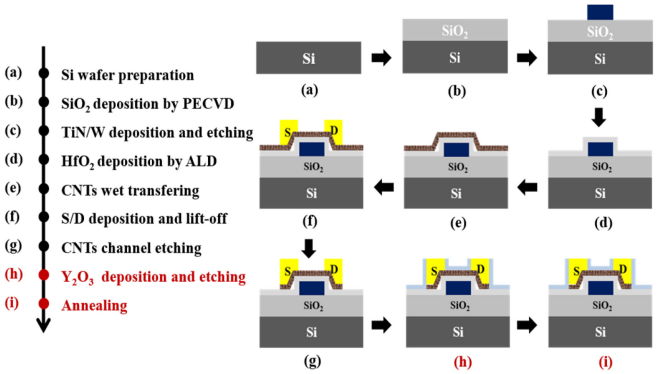


**FIGURE 1. Fabrication process flow of carbon nanotube thin-film field-effect transistors (CNFETs). (a) Si wafer preparation. (b) Insulating layer formation: $SiO_2$ deposition. (c) Back-gate formation: TiN/W deposition and etching. (d) Back-gate dielectric formation: $HfO_2$ deposition. (e) CNT channel formation. (f) The source and drain electrode formation: Ti/Pd deposition and lift-off. (g) CNT channel etching. (h) Passivation layer formation: $Y_2O_3$ deposition and etching. (i) Device annealing.**

## II. EXPERIMENT

### A. FABRICATION PROCESS

In our study, carbon nanotube thin-film field-effect transistors (CNFETs) were executed through a meticulous nine-step process, as shown in **Figure 1**. The process began with the preparation of a p-type silicon wafer **(Figure 1a)**, onto which a 200 nm $SiO_2$ insulating layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) to reduce the risk of device leakage **(Figure 1b)**. Subsequently, a 20 nm layer of TiN and a 75 nm layer of W were deposited by physical vapor deposition (PVD), followed by pattern photolithography and reactive ion etching (RIE) to form the back-gate electrode **(Figure 1c)**. In the lithography process described, AZ6112 positive photoresist was utilized. The photoresist was coated and homogenized to achieve a thickness of approximately 1 μm, which was then subjected to a soft bake at 90 °C for 5 minutes to ensure uniformity and stability. Post-alignment, the exposure dose was calibrated to approximately 50 mJ, followed by a post-exposure bake for 10 minutes at 110 °C. Subsequently, development was carried out using KMP PD238-II developer for a duration of 18 s and then dried using $N_2$. The final step involved a hard bake at 110 °C for approximately 3 minutes to remove the photoresist solvent, thereby completing the lithography process. We then proceeded with the atomic layer deposition (ALD) of a 15 nm $HfO_2$ film at 300 °C, which functions as the high-k dielectric for the back gate **(Figure 1d)**. A networked carbon nanotube thin film, which acts as the device channel, was prepared using a solution deposition method **(Figure 1e)**. The fabrication of the carbon nanotube thin film encompassed the following steps: (i) In an ultra-clean environment, a high-concentration dispersion of

semiconducting carbon nanotubes was meticulously mixed with an xylene solution at a 1:10 ratio, yielding a diluted solution tailored for the precise density of the carbon nanotube film required. (ii) A substrate featuring a pre-cleaned back-gate structure was submerged in this diluted solution for 48 hours under static conditions at ambient temperature. The CNTs were tightly deposited on the surface of the $HfO_2$ layer by hydrogen bonding. This was succeeded by a series of baths in acetone and anhydrous ethanol for 5 minutes each to ensure thorough cleaning. (iii) Subsequently, the substrate was dried using high-purity nitrogen, effectively concluding the fabrication of the carbon nanotube thin film, ready for its role as the device channel. Afterward, a 2 nm Ti and a 230 nm Pd layer were deposited by electron-beam evaporation (EBE) after defining the source-drain electrode positions by photolithography, followed by a lift-off process to fabricate the source and drain electrodes (**Figure 1f**). For the delineation of source and drain electrodes, AR-N 4340 negative photoresist was utilized. Following application and homogenization, the photoresist was uniformly set to a thickness of approximately 1.68 μm. To ensure homogeneity and stability, a soft bake was implemented at 110 °C for 120 s. Post-alignment, the photoresist was exposed to a dose of 123 mJ, succeeded by a post-exposure bake at 100 °C for 80 s. Development was performed using AR 300-475 developer for 90 s, after which the photoresist was dried with $N_2$. The photolithography process was finalized with a hard bake at 100 °C for approximately 3 minutes to solidify the film. In the lift-off process, the photoresist is initially subjected to an extended immersion in an acetone solution for over 10 hours. Following this, a brief immersion in anhydrous ethanol for approximately 10 minutes is applied to ensure the thorough removal of any residual photoresist. Then, the channel area was defined through photolithography, and dry etching was employed to prepare the channel, completing the original device fabrication (**Figure 1g**). The lithography and debonding processes described adhere to the same protocols as those detailed in the preceding section for positive photoresist lithography and the lift-off process. To enhance the device performance, a 5 nm Y layer was deposited using EBE onto the original device, which was immediately annealed in air at 250 °C for 30 minutes to facilitate the conversion to $Y_2O_3$, establishing a passivation layer. This step completed the fabrication of the passivation-optimized devices (**Figure 1h**). Finally, the device was annealed under vacuum conditions at 300 °C for 15 minutes to complete the passivation and annealing optimization of the device fabrication process (**Figure 1i**). Upon completion of this process step, the device optimization is finalized. It is important to note that standard UV lithography at 365 nm was utilized for all lithography stages in the fabrication of CNFETs. Moreover, to prevent CNT debonding, mechanical forces, such as ultrasonication, were deliberately avoided during the lift-off and debonding phases.

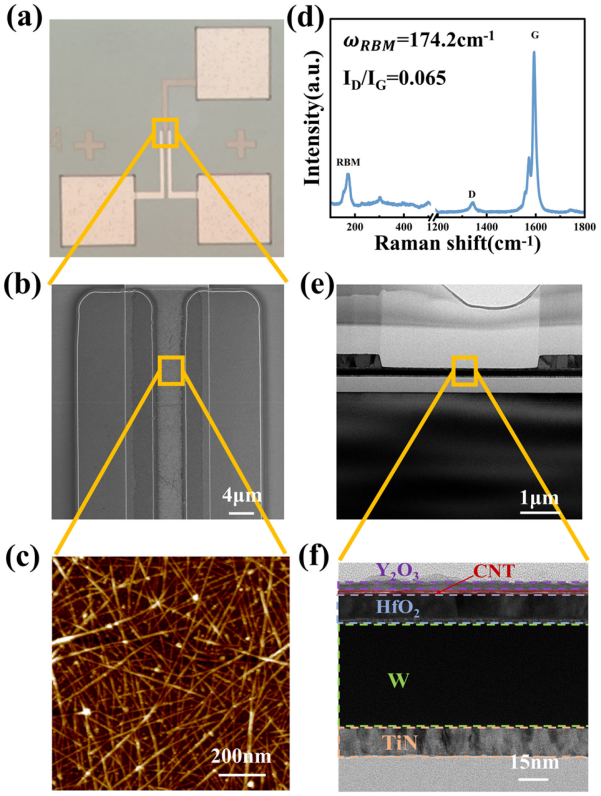


**FIGURE 2. Structural characterization of carbon nanotube thin-film field-effect transistors. (a) Structural view of the device under an optical microscope. (b) The FIB image of the source, drain, back gate, and channel sections of the original device. (The scale bar is 4 μm.) (c) The AFM image of CNT film characterization at the device channel. (The scale bar is 200 nm.) (d) The RAMAN characterization of CNT film corresponds to a radial breathing mode position of 174.2 cm$^{-1}$ and a D/G band ratio of 0.065. (e) TEM image of the optimized device and (f) EDS elemental analysis elucidates the elemental composition of the entire device channel. (The scale bar is 1 μm and 15 nm for Figure 1e and Figure 1f, respectively.)**

### *B. DEVICE STRUCTURES AND MORPHOLOGIES*

We conducted a comprehensive structural and morphological characterization of the devices fabricated through the process mentioned above. The overall device structure, as observed under an optical microscope, is depicted in **Figure 2a**. Further detailed analysis was performed using a focused ion beam (FIB) to scrutinize the core components of the original device, including the source-drain electrodes, gate electrode, and channel area, as presented in **Figure 2b**. Atomic Force Microscopy (AFM) was employed to examine the carbon nanotubes in the channel region, as shown in **Figure 2c**. The networked disordered CNT film exhibits a density of approximately 36 tubes/μm. The AFM images reveal an excellent overall morphology of the carbon nanotube film, characterized by low surface impurity content, long tube lengths, and uniform diameters. This indicates that our fabrication process minimally impacts the CNT film, preserving its intrinsic properties and laying a solid foundation for the device's promising performance. Raman spectroscopy was utilized to further characterize the CNT film, with

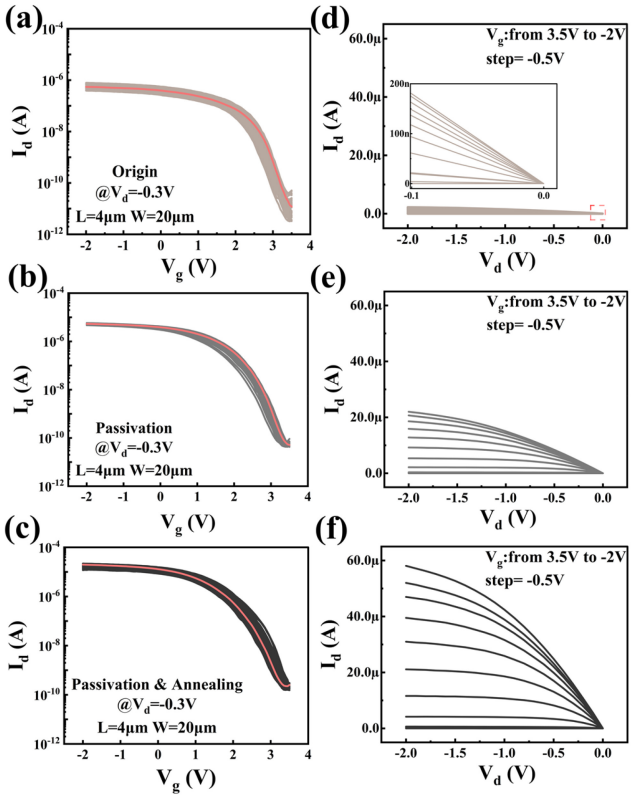


**FIGURE 3.** Comparison of electrical characteristics of original (O), passivated (P), and passivated and annealed (P&A) CNFETs. (a)Statistical images of the transfer characteristic curves of 35 original CNFETs. (b) Statistical images of the transfer characteristic curves of 35 passivated CNFETs. (c) Statistical images of the transfer characteristic curves of 35 passivated and annealed CNFETs. The highlighted curves are the transfer characteristic curves for the most representative devices of the three devices. The transfer characteristics were measured for devices with a channel length (L) of 4 μm and width (W) of 20 μm at $V_{ds} = -0.3$ V. (d)The output characteristic curve of the most representative device (highlighted curve) of the original CNFETs. (e) The output characteristic curve of the most representative device (highlighted curve) of the passivated CNFETs. (f) The output characteristic curve of the most representative device (highlighted curve) of the passivated and annealed CNFETs. The output characteristic curves illustrate $V_d$ sweeping from 0 V to −2 V, while $V_g$ is stepped from 3.5 V to −2 V in intervals of −0.5 V.

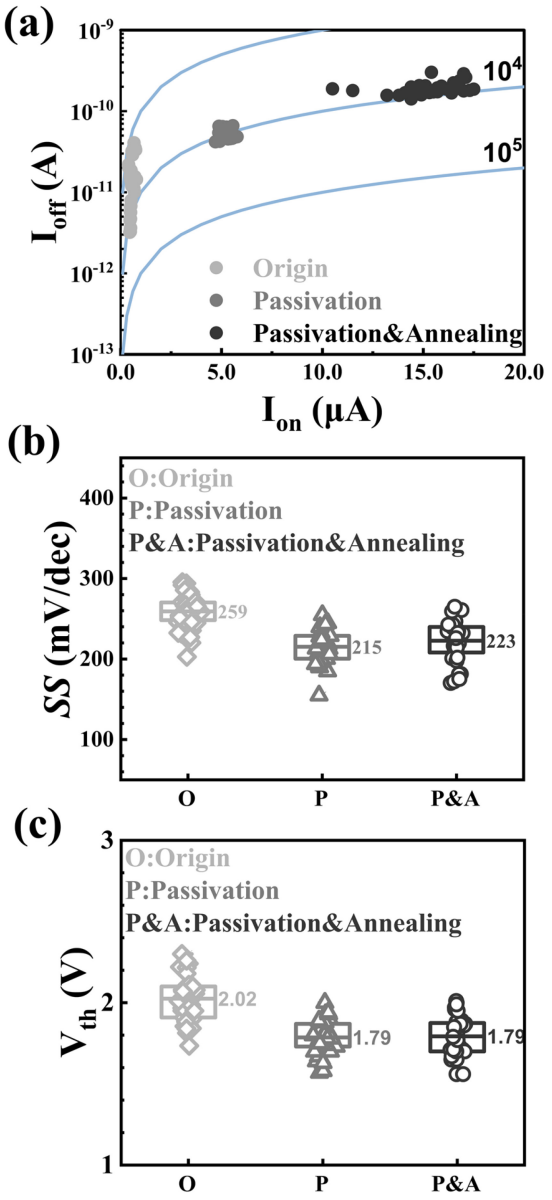


**FIGURE 4.** Performance comparison of original (O), passivated (P), and passivated and annealed (P&A) CNFETs. (a) $I_{on}/I_{off}$ distribution (b) SS and (c) threshold voltage statistical diagrams for the original, passivated, and passivated and annealed 35 CNFETs at $V_{ds} = -0.3$V.

the identification of a radial breathing mode (RBM) band at 174.2 $cm^{-1}$, as illustrated in **Figure 2d**. According to the CNT diameter calculation formula specified in GB/T 32871-2016:

$$\omega_{RBM} = \frac{234}{d} + 10 \tag{1}$$

The CNT diameter is calculated to be 1.4 nm. Employing a 532 nm laser wavelength and an energy of 2.33 eV for the Raman measurement, indicative of a semiconducting type. The low D/G band ratio suggests a minimal presence of defects and amorphous carbon within the CNTs, signifying high-quality CNT material [20]. **Figures 2e-f** showcase the transmission electron microscopy (TEM) characterization of the optimized device's overall structure and the energy-dispersive X-ray spectroscopy (EDS) elemental analysis of the channel's film layers, respectively. Among them, **Figure 2e** illustrates the TEM schematic of the TEM sample that was prepared using a FIB device. The schematic is presented at a low magnification to provide an overview of the device's structure. These analyses confirm the device's gate length (L) to be 4 μm. The precise delineation of elemental distribution within the channel, as revealed by EDS analysis, confirms the precise fabrication of carbon nanotube thin-film field-effect transistors with a superior structure. Such structural excellence is fundamental to the device's capability to serve as a high-performance advanced CNFET, highlighting its potential for future applications.

**TABLE 1. Electrical performance of different CNFETs.**

| Device | $I_{on}$ (A) | $I_{off}$ (A) | $I_{on}/I_{off}$ | SS (mV/dec) | $V_{th}$ (V) | μ ($cm^2/V{\cdot}s$) |
|---|---|---|---|---|---|---|
| O | $5.57\times10^{-7}$ | $1.22\times10^{-11}$ | $4.6\times10^{4}$ | 247.15 | 2.24 | 0.04 |
| P | $5.56\times10^{-6}$ | $6.03\times10^{-11}$ | $9.2\times10^{4}$ | 217.89 | 1.90 | 0.95 |
| P&A | $2.04\times10^{-5}$ | $2.75\times10^{-10}$ | $7.4\times10^{4}$ | 180.44 | 1.88 | 3.47 |

## III. RESULTS AND DISCUSSION

### A. OPTIMIZATION OF ELECTRICAL PERFORMANCE IN CNFETS

Electrical measurements were conducted on all devices under ambient conditions to elucidate the electronic properties of the CNFETs. For each category, 35 CNFETs, identical in structure, dimensions, and parameters, were subjected to random testing. The results are depicted in **Figures 3a-c**, illustrating the transfer characteristic curves for original **(O)**, passivation-optimized **(P)**, and passivation-and-annealing-optimized **(P&A)** CNFETs, respectively. These curves represent the variation in $I_{ds}$ as a function of $V_g$ from 3.5 V to −2 V, with $V_{ds} = -0.3$ V. The presented transfer curves underscore the high-performance p-type FET characteristics of the devices. The initial assessment reveals that the back-gate CNFETs demonstrate exceptional uniformity and a high fabrication yield. Compared to the original devices, depicted in **Figure 3a**, the on-state current of the devices after $Y_2O_3$ passivation, as illustrated in **Figure 3b**, exhibited a significant enhancement. At $V_{ds} = -0.3$ V, the maximum on-state current surpassed 4 μA. A direct comparison between the most representative devices from each group indicates that the $Y_2O_3$ passivation-optimized device achieved an $I_{on}$ of $5.56 \times 10^{-6}$ A, marking an approximate order of magnitude increase relative to the original device's current of $5.57 \times 10^{-7}$A, as detailed in **Table 1**. Further optimization through annealing led to an additional increase in $I_{on}$. All of the 35 randomly selected devices tested exhibit $I_{on}$ exceeding 10 μA. Notably, a representative device's $I_{on}$ reaches $2.04 \times 10^{-5}$ A, nearly 3.5× greater than before annealing and almost 36.6× larger than the original device. According to the formula:

$$\mu_{FE} = \frac{L}{WC_{OX}V_{DS}} \cdot \frac{dI_{DS}}{dV_{GS}} \tag{2}$$

The mobility increases from 0.04 to 0.95 and then to 3.47 $cm^2/(V{\cdot}s)$. Furthermore, the output characteristic curves depicted in **Figure 3d-f** illustrate a progressive enhancement in device current in correlation with the device's incremental optimization. Specifically, at $V_d = -2$ V and $V_g = -2$ V, the current value escalates from 2.2 μA in the original devices to 22 μA post-passivation, culminating in a significant increase to 58μA following the annealing process. Although there is a slight increase in the off-state current throughout the optimization process, it remains minimal. The device's ON/OFF current ratio ($I_{on}/I_{off}$) is consistently maintained at approximately $10^4$, as evidenced in **Figure 4a**.

In the $Y_2O_3$ passivation process, the optimization of the CNT/Air interface is significantly enhanced due to the excellent wetting properties of yttrium metal with CNTs and the low-density interfacial trap states of the $Y_2O_3$ film [21]. This results in a reduction of interfacial state density [22] and a concomitant decrease in carrier scattering [23]. Furthermore, the presence of negative charges at the $Y_2O_3$/CNT interface potentially induces a more pronounced p-type doping effect compared to water or oxygen adsorbents [14], as demonstrated in **Figures 5a** and **5b**. The proliferation of trapping states within the energy band structure of CNTs leads to an increased number of holes transitioning to the valence band. Additionally, the passivation of the device results in a reduced Schottky barrier, enabling more holes to tunnel through and effectively enhancing the hole concentration within the CNTs. The contact between the source-drain metal and the CNT is also optimized during the annealing process at 250 °C in the formation of the $Y_2O_3$ layer. This step is crucial for reducing contact resistance. Consequently, the $Y_2O_3$ passivation optimization enhances the on-state current of the device. Additionally, a high-temperature vacuum annealing process further refines the metal-semiconductor contact at the source-drain electrode and reduces defects within the CNT, so that the hole concentration is further increased, as shown in **Figure 5c**. This process contributes to a further increase in the on-state current.

Furthermore, the passivation process results in a comprehensive enhancement of the CNFETs' performance compared to the original devices. This improvement is particularly evident in SS, which is reduced from approximately 259 mV/dec to 215 mV/dec, and a shift in $V_{th}$ from 2.02 V to 1.79 V, as displayed in **Figure 4b, c**. Notably, the SS and $V_{th}$ values remain unchanged after annealing, indicating the stability of the passivation treatment. The observed reduction in SS is indicative of an enhanced gate control efficiency. This decrease in SS, along with the lowering of $V_{th}$, is primarily attributed to the optimization of the $Y_2O_3$ film, which results in a diminished density of interfacial states during the passivation process. By integrating the statistical data of $I_{on}$, SS, and $V_{th}$, our analysis reveals that passivation optimization significantly augments the device's $I_{on}$ and concurrently refines the SS and $V_{th}$. Furthermore, the subsequent annealing optimization is observed to provide an additional increment in $I_{on}$ without adversely impacting the SS and $V_{th}$, thereby preserving the optimized performance parameters.

### B. ENHANCEMENT OF OPTOELECTRONIC PERFORMANCE IN CNFETS

Furthermore, in order to fully demonstrate the potential of CNFETs for multifunctional applications, an in-depth analysis of their optimized optoelectronic response characteristics has been performed. This analysis aims to enhance the versatility of the devices, ensuring their suitability for a wide range of applications within dense, multi-layered sensor arrays. Measurements of the $I_{ds}$ were conducted under various lighting conditions and voltage configurations. **Figures 6a-c** illustrate the transfer characteristic curves for

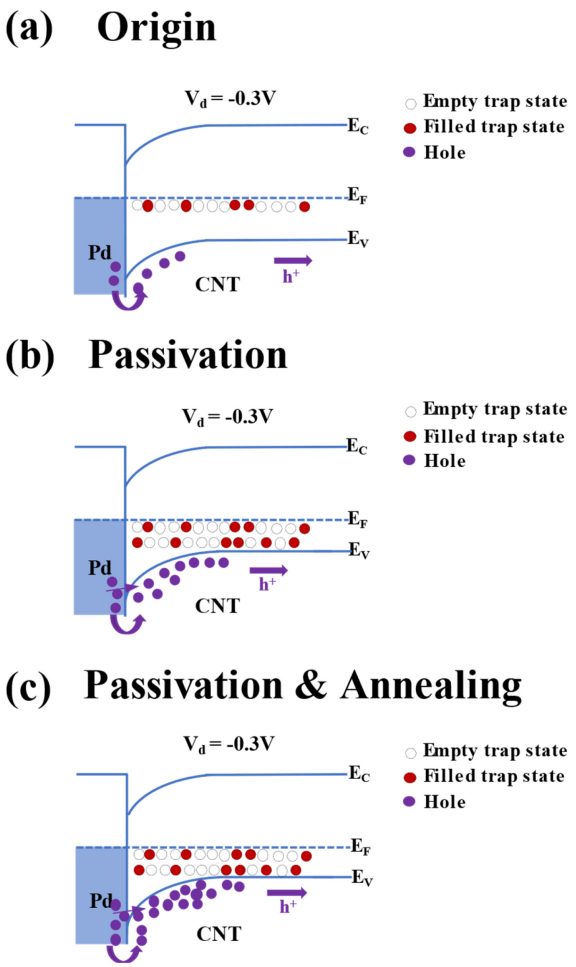


**FIGURE 5.** Schematic diagram of the energy band structure of the CNFETs. (a) Schematic diagram of the energy band structure of the original CNFET. (b) Schematic diagram of the energy band structure of the $Y_2O_3$ passivation optimized CNFET. (c) Schematic diagram of the energy band structure of the $Y_2O_3$ passivated and annealed optimized CNFET. The drain voltage is -0.3 V.

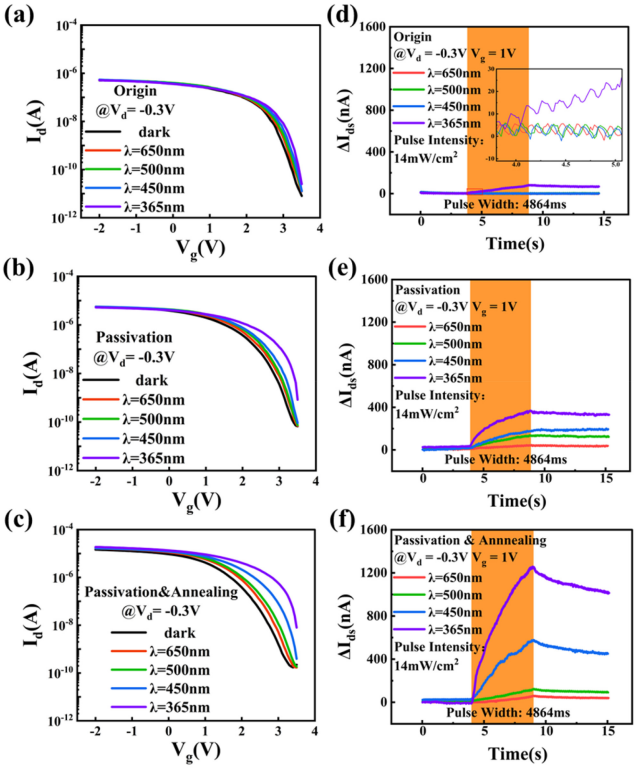


**FIGURE 6.** Optoelectronic response comparison of original, passivated, and passivated and annealed CNFETs. (a) The transfer curves of the original devices under different light wavelengths. (b) The transfer curves of the passivated devices under different light wavelengths. (c) The transfer curves of the passivated and annealed devices under different light wavelengths. (d) Comparison of the photocurrent of the original devices under different wavelengths with the same pulse width, and the right inset shows the enlarged photocurrent of the device. (e) Comparison of the photocurrent of the passivated devices under different wavelengths with the same pulse width. (f) Comparison of the photocurrent of the passivated and annealed devices under different wavelengths with the same pulse width.

the original and progressively optimized CNFETs under dark and different wavelength light illumination. The experimental setup involves four distinct light wavelengths: 650 nm, 500 nm, 450 nm, and 365 nm, each with an intensity of 14 mW/cm$^2$. The corresponding transfer characteristic curves were derived by incrementally varying the gate voltage from 3.5 V to −2 V, under the condition of a constant drain voltage at −0.3 V and with continuous light exposure. Combined with the photoelectric response of the original device and the progressively optimized device under four different wavelengths of light pulses with the same light intensity (14 mW/cm$^2$) and the same duration (4864 ms) as shown in **Figure 6d-f**. As shown in **Figure 6d**, the original device exhibited current increments of 0.7 nA, 1.3 nA, 2.5 nA, and 81.4 nA upon exposure to red, green, blue, and UV light, respectively. The passivated device, depicted in **Figure 6e**, demonstrated significantly enhanced current growth, reaching 45.3 nA, 133.3 nA, 180.8 nA, and 365.2 nA under identical conditions. Utilizing the photocurrent response elicited by 450 nm blue light as a baseline, the photocurrent response of passivated devices is approximately 72× greater than that of the original devices. Moreover, the passivated and annealed devices, as represented in **Figure 6f**, exhibited even more pronounced current increases, with values of 60.1 nA, 120.6 nA, 577.5 nA, and 1257.0 nA, respectively. The photocurrent response of these devices is remarkably amplified to about 231× that of the original devices. Our investigations reveal a progressive enhancement in the photoelectric response characteristics of CNFETs as they undergo the optimization process. Furthermore, **Figure 7** presents the absorption spectra of both the CNT film and the passivated CNT & $Y_2O_3$ film across a wavelength range spanning from 200 nm to 700 nm. The passivated CNT & $Y_2O_3$ film demonstrates a significantly enhanced light absorption capacity compared to the original CNT film under identical wavelength conditions.

The observed enhancement in photoresponse current can be ascribed to two principal factors. Firstly, it is attributed to the enhanced light absorption capability of the passivated CNT & $Y_2O_3$ films, which is a direct consequence of the

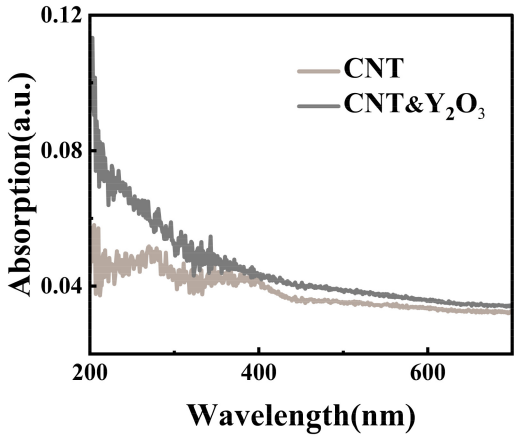


**FIGURE 7.** **Comparison of absorption spectra of CNT films and passivated CNT & $Y_2O_3$ films.**

passivation process. Secondly, the passivation optimization process is instrumental in significantly diminishing the defect density on the CNT surfaces. Furthermore, the subsequent annealing treatment is crucial as it continues this reduction, this time focusing on the interior of the carbon nanotubes. This dual process leads to a significant decrease in the defect energy levels in the energy bands and increases the excitation of electron-hole pairs near the Fermi energy levels, as illustrated in **Figures 8a-c**. As a result, this contributes to an increase in photocurrent and enhances the overall photo responsiveness of the device. Remarkably, the optoelectronic current for all devices does not fully relax post-stimulation, suggesting a memory effect and indicating the potential for non-volatile memory functionality. The device's non-volatile memory functionality is primarily attributed to the difficult recombination of electrons and holes at the deep impurity energy levels within the energy band of the CNTs. Thereby enhancing the retention capability of the charge carriers and endowing the device with its non-volatile characteristics. This behavior underscores the promising potential of optimized CNFETs for applications in-memory technology.

Subsequently, we conducted an exhaustive investigation of the optimized devices, which exhibited amplified opto-electronic responses, to assess their viability for practical applications. **Figure 9a** demonstrates the modulation of the $I_{ds}$ by seven different pulse widths (76 ms, 152 ms, 304 ms, 912 ms, 1824 ms, 2432 ms, and 4864 ms), under the fixed conditions of a wavelength of 450 nm and a light intensity of 14 mW/cm$^2$. The results indicate that an increase in light pulse width corresponds to a higher change in $I_{ds}$ ($\Delta I_{ds}$). **Figure 9b** further demonstrates that varying light pulse intensities, from 6 mW/cm$^2$ to 14 mW/cm$^2$, can elicit $\Delta I_{ds}$ of different magnitudes when applied for a fixed duration of 152 ms. Higher intensities result in larger $\Delta I_{ds}$. Moreover, **Figure 9c** discloses a relationship between the frequency of light pulses and the amplitude of $\Delta I_{ds}$. Seven sets of light pulses, consistent in wavelength (450 nm), pulse width (190 ms), and intensity (14 mW/cm$^2$), are administered to

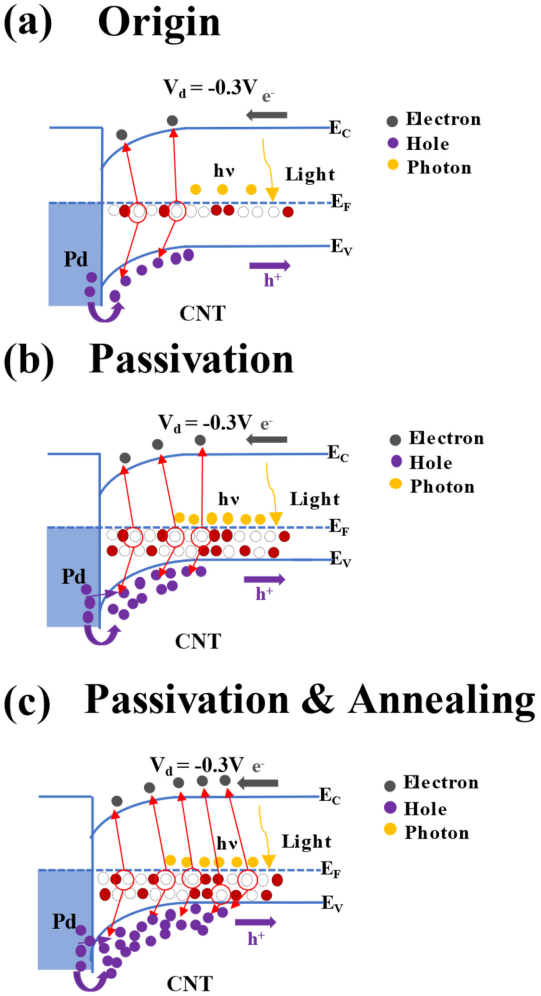


**FIGURE 8.** **Schematic diagram of the energy band structure of the CNT optoelectronic transistors. (a) Schematic diagram of the energy band structure of the original CNT optoelectronic transistor and the jumping of electrons and holes under light stimulation. (b) Schematic diagram of the energy band structure of the passivation-optimized CNT optoelectronic transistor and the jumping of electrons and holes under light stimulation. (c) Schematic diagram of the energy band structure of the passivation and annealing-optimized CNT optoelectronic transistor and the jumping of electrons and holes under light stimulation.**

the CNT optoelectronic transistors at frequencies ranging from 0.025 Hz to 2.63 Hz. The findings show that an escalation in pulse frequency is associated with a progressive enhancement in $\Delta I_{ds}$.

Additionally, **Figures 9a-c** collectively demonstrate that the device's current rises during light stimulation, indicative of its sensing capabilities. Notably, the current does not return to baseline levels post-stimulation, suggesting a retention of current that implies the device's capacity for information memorization.

### C. CNT MORSE CODE COMMUNICATION SIMULATION

The optoelectrical characteristics of CNFETs make them suitable for light-based wireless communication applications [24], [25]. **Figure 10** showcases the modulation of

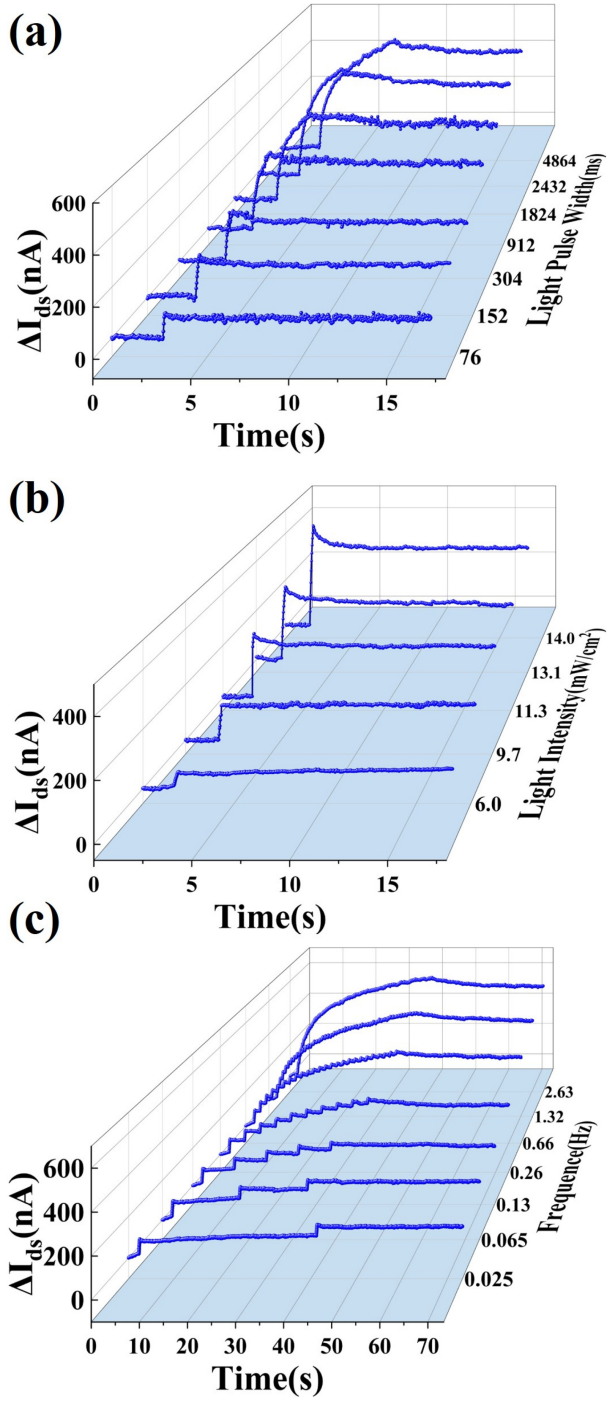


**FIGURE 9.** Optoelectronic characteristics of passivated and annealed CNFETs. (a) $\Delta I_{ds}$ triggered by different optical pulse widths. (b) $\Delta I_{ds}$ triggered by different optical pulse intensities; (c) $\Delta I_{ds}$ triggered by different optical pulse frequencies.

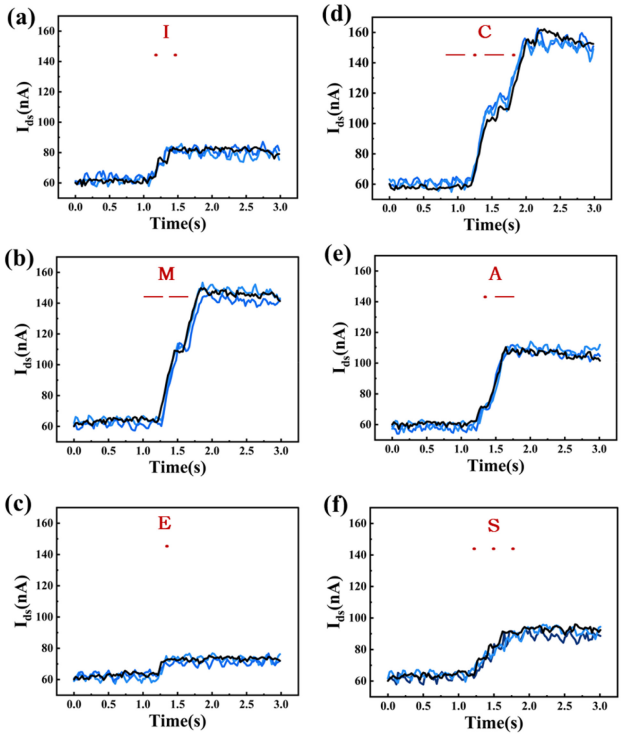


**FIGURE 10.** Transmitting the word "IMECAS" by optical wireless communication using light stimulated three different CNFETs. $I_{ds}$ images of optical signal modulation corresponding to (a) "I", (b) "M", (c) "E", (d) "C", (e) "A", (f) "S".

the word "IMECAS" using Morse code with the incident light, where the $I_{ds}$ response of each letter is measured for three identically-sized CNT optoelectronic transistors. Dots and dashes in the Morse code are represented by encoding pulse widths of 38 ms and 190 ms, respectively, at a constant wavelength and intensity of 450 nm and 14 mW/cm$^2$. **Figures 10a** through **10f** detail the specific $I_{ds}$ responses associated with each letter: "I" is represented by a current value of 83 nA, "M" by 148 nA, "E" by 69 nA, "C" by 161 nA, "A" by 110 nA, and "S" by 91 nA. The distinct $I_{ds}$ responses accurately reflect the unique Morse code for each letter, underscoring the device's proficiency in modulating and detecting light signals. Furthermore, the $I_{ds}$ responses, as exhibited by the various devices under identical modulation conditions, exhibit a remarkable degree of consistency. Our results underscore the exceptional reproducibility of the $I_{ds}$ responses in CNT optoelectronic transistors when subjected to distinct Morse-coded letters. This highlights the robustness and reliability of CNT optoelectronic transistors for potential applications in communication systems.

## IV. CONCLUSION

We employed a special passivation and annealing technique to enhance the intrinsic performance of CNFETs significantly. Through these optimizations, we successfully improved $I_{on}$, reduced SS, and optimized $V_{th}$ of the CNFETs. Furthermore, our research demonstrated a progressive refinement in the optoelectronic performance of these devices. Moreover, we demonstrated the feasibility of Morse code communication circuits all by the optimized CNFETs, showcasing their versatility and potential for integration into monolithic 3D circuits with heterogeneous materials. The achievements lay a promising groundwork for the future novel electronic systems with CNT devices.

## REFERENCES

[1] C. Macilwain, "Silicon down to the wire," *Nature*, vol. 436, pp. 22–23, Jul. 2005, doi: 10.1038/436022a.
[2] J. S. C. Kilby, "Turning potential into realities: The invention of the integrated circuit (Nobel Lecture)," *ChemPhysChem*, vol. 2, nos. 8–9, pp. 482–489, 2001, doi: 10.1002/1439-7641(20010917)2:8/9<482::AID-CPHC482>3.0.CO;2-Y.
[3] A. D. Franklin, "Nanomaterials in transistors: From high-performance to thin-film applications," *Science*, vol. 349, no. 6249, 2015, Art. no. aab2750, doi: 10.1126/science.aab2750.
[4] S. Wang, X. Liu, and P. Zhou, "The road for 2D semiconductors in the silicon age," *Adv. Mater.*, vol. 34, no. 48, 2022, Art. no. 2106886, doi: 10.1002/adma.202106886.
[5] G. Hills et al., "Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital VLSI," *IEEE Trans. Nanotechnol.*, vol. 17, no. 6, pp. 1259–1269, Nov. 2018, doi: 10.1109/tnano.2018.2871841.
[6] P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nat. Nanotechnol.*, vol. 2, pp. 605–615, Sep. 2007, doi: 10.1038/nnano.2007.300.
[7] R. An et al., "A hybrid computing-in-memory architecture by monolithic 3D integration of BEOL CNT/IGZO-based CFET logic and analog RRAM," in *Proc. Int. Electron Devices Meet. (IEDM)*, 2022, pp. 18.1.1–18.1.4, doi: 10.1109/IEDM45625.2022.10019473.
[8] S. Wang, Z. Zhang, and L. Peng, "Doping-free carbon nanotube optoelectronic devices," *Chin. Sci. Bull.*, vol. 57, nos. 2–3, pp. 149–156, 2011, doi: 10.1007/s11434-011-4806-3.
[9] L. Liu. et al., "Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics," *Science*, vol. 368, no. 6493, pp. 850–856, 2020, doi: 10.1126/science.aba5980.
[10] M. Kim et al., "Human and environmental safety of carbon nanotubes across their life cycle," *Nat. Rev. Mater.*, vol. 9, pp. 63–81, Nov. 2023, doi: 10.1038/s41578-023-00611-8.
[11] L. Ding et al., "CMOS-based carbon nanotube pass-transistor logic integrated circuits," *Nat. Commun.*, vol. 3, no. 1, p. 677, 2012, doi: 10.1038/ncomms1682.
[12] M. Yin et al., "Wafer-scale carbon-based CMOS PDK compatible with silicon-based VLSI design flow," *Nano Res.*, vol. 17, pp. 7557–7566, Aug. 2024, doi: 10.1007/s12274-024-6583-8.
[13] S. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 49–52, May 1998, doi: 10.1038/29954.
[14] J. Xia et al., "Performance enhancement of carbon nanotube thin film transistor by yttrium oxide capping," *Nanoscale*, vol. 10, no. 9, pp. 4202–4208, 2018, doi: 10.1039/c7nr08676h.
[15] Y. Deng, Y. Wu, and M. Zhang, "Annealing temperature optimization for high-performance carbon nanotube thin film transistors," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, 2015, pp. 672–675, doi: 10.1109/EDSSC.2015.7285205.
[16] Y. Huang et al., "Van der Waals coupled organic molecules with monolayer $MoS_2$ for fast response photodetectors with gate-tunable responsivity," *ACS Nano*, vol. 12, no. 4, pp. 4062–4073, Apr. 2018, doi: 10.1021/acsnano.8b02380.
[17] S. Jeon, J. Jia, J. H. Ju, and S. Lee, "Black phosphorus photodetector integrated with Au nanoparticles," *Appl. Phys. Lett.*, vol. 115, no. 18, 2019, Art. no. 183102, doi: 10.1063/1.5119833.
[18] C. Torres-Torres, N. Peréa-López, H. Martínez-Gutiérrez, M. Trejo-Valdez, J. Ortíz-López, and M. Terrones, "Optoelectronic modulation by multi-wall carbon nanotubes," *Nanotechnology*, vol. 24, no. 4, 2013, Art. no. 045201, doi: 10.1088/0957-4484/24/4/045201.
[19] A. L. Gorkina et al., "Transparent and conductive hybrid graphene/carbon nanotube films," *Carbon*, vol. 100, pp. 501–507, Apr. 2016, doi: 10.1016/j.carbon.2016.01.035.
[20] Y. Park et al., "Reinterpretation of single-wall carbon nanotubes by Raman spectroscopy," *J. Phys. Chem. C*, vol. 123, no. 22, pp. 14003–14009, 2019, doi: 10.1021/acs.jpcc.9b02174.
[21] Z. Wang et al., "Growth and performance of yttrium oxide as an ideal high-$\kappa$ gate dielectric for carbon-based electronics," *Nano Lett.*, vol. 10, no. 6, pp. 2024–2030, 2010, doi: 10.1021/nl100022u.
[22] L. Xu, N. Gao, Z. Zhang, and L.-M. Peng, "Lowering interface state density in carbon nanotube thin film transistors through using stacked $Y_2O_3$/$HfO_2$ gate dielectric," *Appl. Phys. Lett.*, vol. 113, no. 8, 2018, Art. no. 83105, doi: 10.1063/1.5039967.
[23] H. Xiao et al., "Interface and border traps in the gate stack of carbon nanotube film transistors with an Yttria dielectric," *ACS Appl. Electron. Mater.*, vol. 5, no. 7, pp. 3908–3916, 2023, doi: 10.1021/acsaelm.3c00613.
[24] Y. Lee et al., "Stretchable organic optoelectronic sensorimotor synapse," *Sci. Adv.*, vol. 4, no. 11, 2018, Art. no. eaat7387, doi: 10.1126/sciadv.aat7387.
[25] H. Huang et al., "Pt/TiOx/Ti-based dynamic optoelectronic memristor for neuromorphic computing," in *Proc. 6th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, 2022, pp. 310–312, doi: 10.1109/EDTM53872.2022.9798290.