Received 9 May 2024; revised 4 June 2024 and 11 July 2024; accepted 29 August 2024. Date of publication 2 September 2024; date of current version 11 September 2024. The review of this article was arranged by Editor N. Collaert.

Digital Object Identifier 10.1109/JEDS.2024.3453408

An Approach to Determine Noise Model Parameter for Submicron MOSFET from RF Noise Figure Measurement

HANQI GAO, JING JIN (Senior Member, IEEE), AND JIANJUN ZHOU (Senior Member, IEEE)

Center for Analog/RF Integrated Circuits, School of Microelectronics, Shanghai Jiao Tong University, Shanghai 200240, China

CORRESPONDING AUTHOR: J. JIN (e-mail: jinjing@sjtu.edu.cn)

This work was supported by the National Natural Science Foundation of China under Grant 62122051.

ABSTRACT An extraction method to obtain the noise model parameter T_d in deep submicron MOSFETs directly from radio frequency (RF) scattering parameters and noise figure measurements is presented. A simplified noise equivalent circuit, along with closed-form solutions to calculate the RF noise figure of MOSFET is developed. On-wafer experimental verification is presented and a comparison with tuner based method is given. Good agreement is obtained between simulated and measured results for $16\times1\times2\mu$m (number of gate fingers $\times$ unit gatewidth $\times$ cells) gatelength MOSFETs.

INDEX TERMS Equivalent circuits, MOSFET, parameter extraction, noise model, small signal model, noise figure measurement.

I. INTRODUCTION

Thanks to recent advances in CMOS technology, the MOSFET offers the advantages of low cost, high integration, and the possibility of a single-chip solution. The understanding and modeling of thermal noise is crucial since it is the dominant noise source in the device at RF frequencies [1], [2], [3]. From the circuit point of view, the MOSFET device can be treated as a closed box of a noisy two port. The noise behavior of a linear noisy two-port network can be characterized by the four noise parameters, minimum noise figure $F_{\min}$, noise resistance R_n, optimum source conductance G_{opt} and optimum source susceptance B_{opt} [4].

The common used methods for determination of noise parameters for semiconductor devices can be categorized into the tuner-based methods and 50Ω noise figure measurement system based methods. The tuner-based methods rely on the source–pull measurement technique to extract the noise parameters from a large set of parameters (source impedances and noise figures) at a single frequency, and normally 16 impedance points are required. Although this method gives accurate results, it is time consuming and requires an expensive automatic broadband microwave tuner that involves complex calibration procedures [5], [6], [7], [8], [9]. Alternatively, 50Ω noise figure measurement system is less complicated to use and easier to calibrate, and it is desirable to determine four noise parameters by using the equivalent transistor noise model (such as Pospieszalski [10] and Cappy models [11]) to provide additional information. Unfortunately, this kind of methods heavily relies on the complex noise and signal correlation matrix computations to embed the parasitic to obtain the four noise parameters, and the analytical expression between noise figure and channel noise model parameter T_d is not available directly [12], [13], [14], [15], [16], [17].

In order to overcome the limitations of previous literature, we have developed an extraction method to obtain the channel noise model parameter T_d based on Pospieszalski model in submicron MOSFETs directly from RF scattering parameters and noise figure measurements. Noted noise parameter extraction is based on Pospiesczalski noise model, which neglects correlation between induced gate current noise and channel noise. The main advantage of this method is based on the common used circuit thermal noise calculation without complicated matrix computations. An extraction method to obtain the noise model parameter T_d in deep submicron MOSFETs directly from RF scattering parameters and noise figure measurements is presented. A simplified

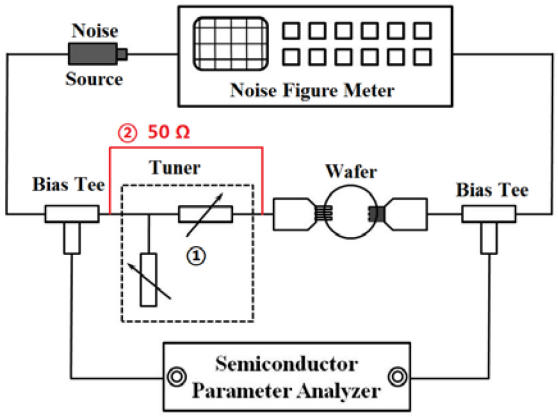

FIGURE 1. Tuner-based noise measurement system and 50 ohm noise measurement system.

noise equivalent circuit, along with closed-form solutions to calculate the RF noise figure of MOSFET is developed.

This paper is organized as follows. Section II gives the simplified noise equivalent circuit model of the MOSFET. Sections II and III are dedicated to the derivation of analytical expressions for the corresponding noise figure based on a simplified noise model. A comparison between the new expressions and experimental data measured on MOSFETs is presented in Section IV. The conclusion is given in Section IV.

II. EQUIVALENT CIRCUIT MODEL

A. CONVENTIONAL EQUIVALENT CIRCUIT MODEL

The complete MOSFET small signal and noise equivalent circuit model is shown in Fig. 2. Fig. 2 (a) shows the extrinsic network and Fig. 2 (b) the intrinsic network, respectively. where L_g, L_d and L_s represent the feedline inductances, respectively. In Pospieszalski's model, the equivalent temperature parameters T_g and T_d are assigned to the resistances R_{gs} and g_{ds}. Both resistances contribute uncorrelated thermal noise.

These two noise sources are characterized by their mean quadratic value in a bandwidth Δf centered on the frequency f, and can be expressed as following [10]:

$$\overline{e_{gs}^2} = 4kT_gR_{gs}\Delta f \tag{1}$$

$$\overline{i_{ds}^2} = 4kT_d/R_{ds}\Delta f \tag{2}$$

The output current noise source models a noise process which produces noise current only a drain circuit. The noise temperature T_g can be simply equal to the ambient temperature under low noise application bias condition (i.e., $T_g = T_o$).

The six noise sources $\overline{e_{oxg}^2}$, $\overline{e_{oxd}^2}$, $\overline{e_{sub}^2}$, $\overline{e_g^2}$, $\overline{e_d^2}$ and $\overline{e_s^2}$ represent the noisy behavior of the access resistances R_{oxg}, R_{oxd}, R_{sub}, R_g, R_d and R_s, and are simply given by

$$\overline{e_i^2} = 4kT_oR_i\Delta f \ \ (\mathrm{i} = \mathrm{oxg, oxd, sub, g, d, s}) \tag{3}$$

where q is the electronic charge, k is Boltzmann's constant, T_o is the ambient temperature.

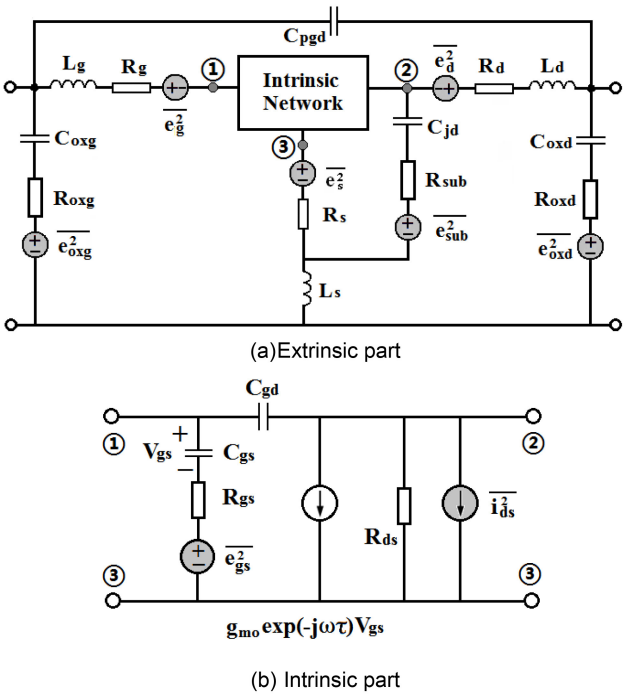

FIGURE 2. Conventional noise circuit model for MOSFET.

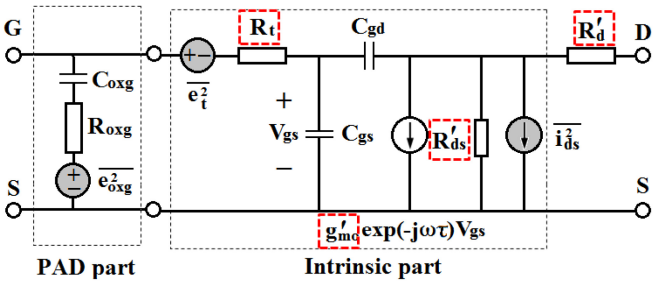

FIGURE 3. Simplified noise circuit model for MOSFET noise factor calculation.

B. SIMPLIFIED EQUIVALENT CIRCUIT MODEL

From the point of view of MOSFET noise factor calculation, four features can be used to simplify the conventional noise circuit model:

1) In the low frequency range, the contribution of extrinsic inductances can be neglected due to the length of device feedlines are kept as short as possible normally.
2) Based on the noise circuit node analysis method, the extrinsic thermal noise sources $\overline{e_{gs}^2}$, $\overline{e_g^2}$ and $\overline{e_s^2}$ can be regards as a single noise source which generated by single resistance. It is very useful to calculation of the noise figure of the device.
3) The noise sources $\overline{e_d^2}$, $\overline{e_{oxd}^2}$ and $\overline{e_{sub}^2}$ are ignored duo to the contributions to noise figure are reduced by device available power gain.
4) The extrinsic drain resistance R_d can be regards as a load resistance in series with the input impedance of next stage.

Based on the noise circuit node analysis method, the noise factor can be expressed as following [18], [19]:

$$F_{50} = 1 + \frac{\overline{v_{no}^2}}{4kT_oR_o|A_V|^2} \tag{4}$$

Fig. 2 shows the simplified noise circuit model for MOSFET noise factor calculation, where $R_t = R_g + R_s + R_{gs}$, and the thermal noise is $\overline{e_t^2} = 4kT_gR_t\Delta f$. The detail procedure consists of two steps: 1) combination of R_s and R_g, and the transconductance and output resistance have been changed. 2) combination of intrinsic resistance R_{gs} and extrinsic resistances.

In order to guarantee the voltage gain A_V (the ratio from output port voltage to the source voltage) must be remain invariant. i.e. : $A_V^s \approx A_V$. The corresponding transconductance and output resistance become:

$$g'_{mo} = g_{mo}/(1 + g_{mo}R_s) \tag{5}$$

$$R'_{ds} = R_{ds}(1 + g_{mo}R_s). \tag{6}$$

with

$R'_{\rm d} = R_{\rm d} + R_s$

$\overline{v_{no}^2}$ is the total output noise voltage density without source impedance, which consists of the noise contribution from R_{ds}, R_t and R_{oxg}., i.e.:

$$\overline{v_{no}^2} = \overline{v_{ds}^2} + \overline{v_t^2} + \overline{v_{oxg}^2} \tag{7}$$

A_V is the voltage gain:

$$A_V = \frac{1}{R_o\left(M_1\ M_3 - M_2/R_t\right)} \tag{8}$$

with

$$M_1 = \left[1 + j\omega\left(C_{gs} + C_{gd}\right)R_t\right]M_2 + j\omega C_{gd}R_t$$

$$M_2 = \frac{1 + j\omega C_{gd}R_L}{\left(g_{mo} - j\omega C_{gd}\right)R_L}$$

$$M_3 = \frac{1}{R_t} + \frac{1}{R_o} + Y_{oxg}$$

$$Y_{oxg} = \frac{j\omega C_{oxg}}{1 + j\omega C_{oxg}R_{oxg}}$$

Normally, the source impedance and load impedance are set to 50 Ω (i.e., $R_o = R_L = 50\Omega$) in standard microwave system.

The noise voltage contributed at the output port by R_{ds} can be expressed as:

$$\overline{v_{ds}^2} = \frac{4kT_{\rm d}}{R'_{ds}}\left|\frac{R_L}{N}\right|^2 \tag{9}$$

$$R_L = \frac{R_{ds}\left(R'_{\rm d} + R_o\right)}{R_{ds} + R'_{\rm d} + R_o}$$

$$N = 1 + j\omega C_{gd}R_L + \frac{j\omega C_{gd}g'_{mo}R_L(R_o + R_t)}{1 + j\omega\left(C_{gs} + C_{gd}\right)(R_o + R_t)}$$

The noise voltage contributed at the output port by R_t can be expressed as:

$$\overline{v_t^2} = 4kT_oR_t|A_V|^2 \tag{10}$$

TABLE 1. The MOSFET parasitic parameters.

Parameters	Values	Units	Parameters	Values	Units
C_{oxg}	115	fF	R_g	7	Ω
C_{oxd}	110	fF	R_d	5	Ω
C_{pgd}	1.1	fF	R_s	3.5	Ω
R_{pg}	8.2	Ω	R_{sub}	250	Ω
R_{pd}	8	Ω	C_{jd}	12	fF
L_g	75	pH	L_s	4	pH
L_d	65	pH			

TABLE 2. Intrinsic parameters (V_{ds} = 1.0V).

Parameters	V_{gs} =0.6V	V_{gs} =0.8V	V_{gs} =1.0V	V_{gs} =1.2V
I_{ds} (mA)	1.67mA	6.3mA	12.3mA	18.4mA
C_{gs} (fF)	30	32	33	34
C_{gd} (fF)	15.5	16	16.5	17
C_{ds} (fF)	14	14	14	14
g_m (mS)	16.5	32	35	35.5
g_{ds} (mS)	1.22	2.5	3.33	4.54
R_i (Ω)	7	9	11	13

The noise voltage contributed at the output port by R_{oxg} can be expressed as:

$$\overline{v_{oxg}^2} = 4kT_oR_{oxg}|A_{VP}|^2 \tag{11}$$

$$A_{VP} = \frac{Y_{oxg}}{M_1M_3 - M_2/R_t}$$

It is obviously that noise model parameter $T_{\rm d}$ can be directly determined from noise figure measurement.

$$\frac{T_{\rm d}}{T_o} = \frac{[(F_{50} - 1)R_o - R_t]|A_V|^2 - R_{pg}|A_{VP}|^2}{|R_L/N|^2}R_{ds} \tag{12}$$

Noted the equation (12) is only valid in the low frequency range (normally, less than 26 GHz).

III. EXPERIMENTAL VERIFICATION

In order to verify the above derived expression for channel noise model parameter T_d, a 16×1×2μm (number of gate fingers × unit gatewidth × cells) with 90nm gate-length NMOSFET transistor has been measured up to 50GHz for S parameters. High frequency noise parameter measurements are carried out on wafer over the frequency range 1-26GHz using an ATN microwave noise measurement system NP5.

A. SMALL SIGNAL MODEL VERIFICATION

Table 1 gives the MOSFET parasitic parameters, and the extracted values of the small signal elements at a constant drain-source voltage V_{ds} = 1.0V with different gate-source voltage V_{gs} are summarized in Table 2. Fig. 4 compares the measured and modeled S parameters for the 16×1×2 μm

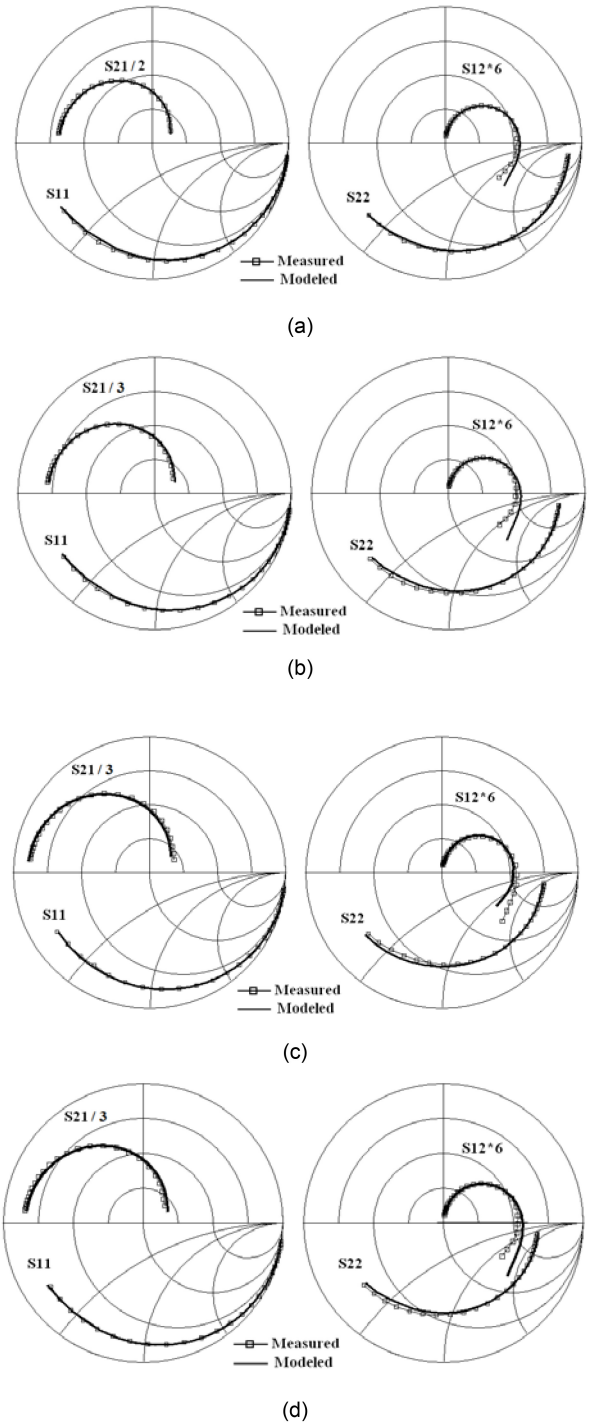

FIGURE 4. Comparison of modeled and measured S parameters for the 16×1×2μm MOSFET. (a) Bias: V_{gs} =0.6 V, V_{ds} =1.0V (b) Bias: V_{gs} =0.8 V, V_{ds} =1.0V (c) Bias: V_{gs} =1.0 V, V_{ds} =1.0V (d) Bias: V_{gs} =1.2 V, V_{ds} =1.0V.

MOSFET in the frequency range of 1GHz to 50GHz under four different bias conditions. The modeled S parameters agree very well with the measured ones to validate the accuracy of the model. We observed the contribution of non-quasi-static (NQS) resistance R_{gs} leads to significant improvements of the MOSFET small signal and noise model simulations, especially at high frequencies.

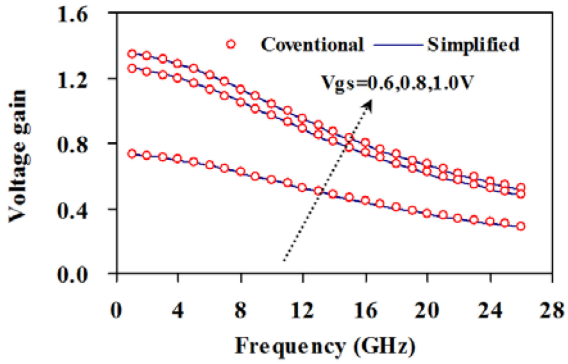

FIGURE 5. Comparison of voltage gain between conventional model and simplified model.

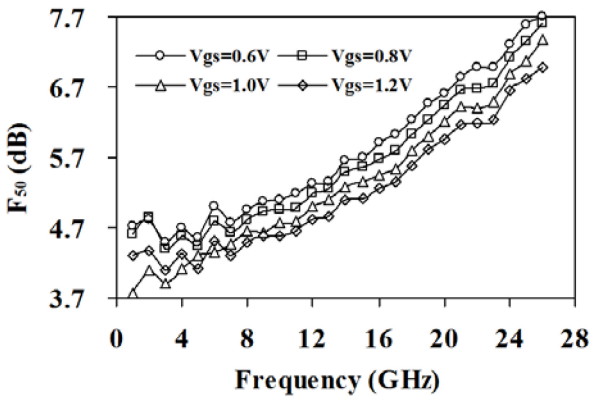

FIGURE 6. 50Ω noise figure measured results for the 16×1.0×2 μm MOSFET. Bias: V_{ds} =1.0V.

B. COMPARISON OF VOLTAGE GAIN

In order to verify the validity of the simplified equivalent model as shown in Fig. 3, Fig. 5 gives the comparison of the voltage gain between conventional model and simplified model. It can be seen that the voltage gain are very close.

C. NOISE MODEL VERIFICATION

Fig. 6 shows the 50Ω noise figure measured results for the 16×1.0×2 μm MOSFET. Due to the large variation of noise figure at low frequencies, the drain noise model parameter $T_{\rm d}$ should be determined in the high frequency range.

Fig. 7 and Fig. 8 show the plot of normalized drain current noise model parameter T_d ($T_{\rm d}/T_o$) versus frequency under four different bias conditions (I_{ds} = 1.67mA, 6.28mA, 11.0mA, and 16.73mA). Rather T_d constant values can be observed from 8GHz to 26GHz to verify the validity of the proposed method.

Fig. 9 shows the ratio of noise model parameter T_d and output resistance $R_{\rm ds}$ versus gate-source voltage V_{gs} and drain-source voltage V_{ds}, It is obviously that $T_{\rm d}/R_{ds}$ remain invariant with V_{ds}, and increases with increase of V_{gs}. Because of the drain current noise is proportional to $T_{\rm d}/R_{ds}$ as shown in Eq. (2), that means drain current noise only dependent on the gate-source voltage V_{gs} and independent on the drain-source voltage V_{ds} roughly.

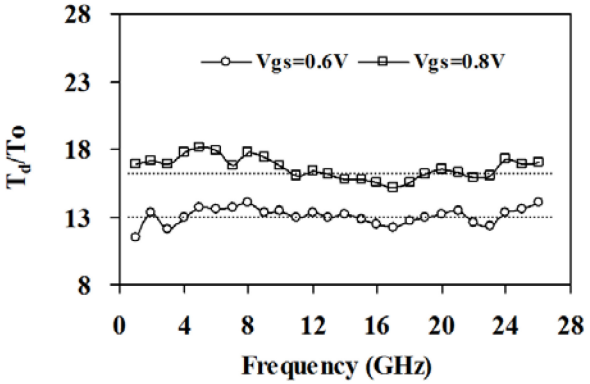

FIGURE 7. Extracted noise model parameter for the 16×1.0×2 μm MOSFET. Bias: V_{ds} =1.0V.

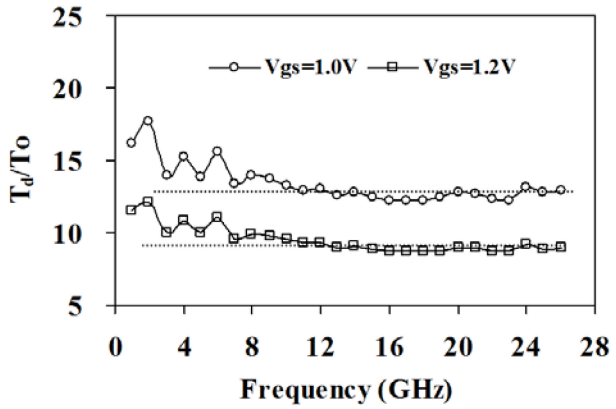

FIGURE 8. Extracted noise model parameter for the 16×1.0×2 μm MOSFET. Bias: V_{ds} =0.6V.

Once the channel noise model parameter T_d is determined, the four noise parameters of whole device can be calculated using the conventional noise model as shown in Fig. 1. Fig. 10 shows the comparison of measured and modeled noise parameters for the 16×1.0×2 μm MOSFET under bias condition V_{gs} = 0.8 V and V_{ds} = 1.0 V. An excellent agreement over the whole frequency range is obtained.

Fig. 11 shows the comparison of measured and simulated noise parameters versus gate-source voltage V_{gs} and drain-source voltage V_{ds}. The small discrepancy between modeled and measured $F_{\min}$, especially under larger V_{gs} bias condition. The largest discrepancy is 0.4 dB for $V_{gs} = V_{ds} = 1.2$V bias condition. The reason may be the correlation of gate and drain current noise is neglected under high V_{gs} bias condition. It is noticed that the range of optimum bias point V_{gs} is 0.8∼0.9V roughly for low noise amplifier design, the phase of optimum reflection coefficient Γ_{opt} remains invariant with respect to V_{gs} and V_{ds} due to the variation of gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} is very small.

The S-parameter and noise analyses of the devices were performed on the basis of a classical MOSFET small-signal equivalent circuit, as shown in Fig. 1. Such an equivalent circuit keeps valid for advanced node technology (such as

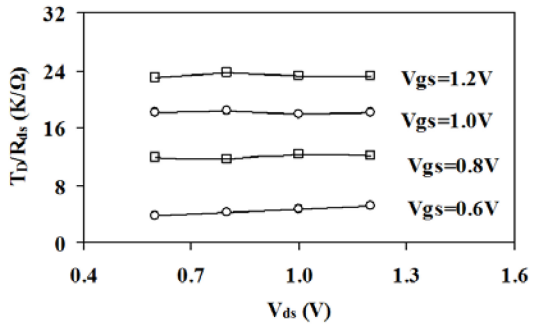

FIGURE 9. Extracted channel noise parameter versus V_{gs} and V_{ds}.

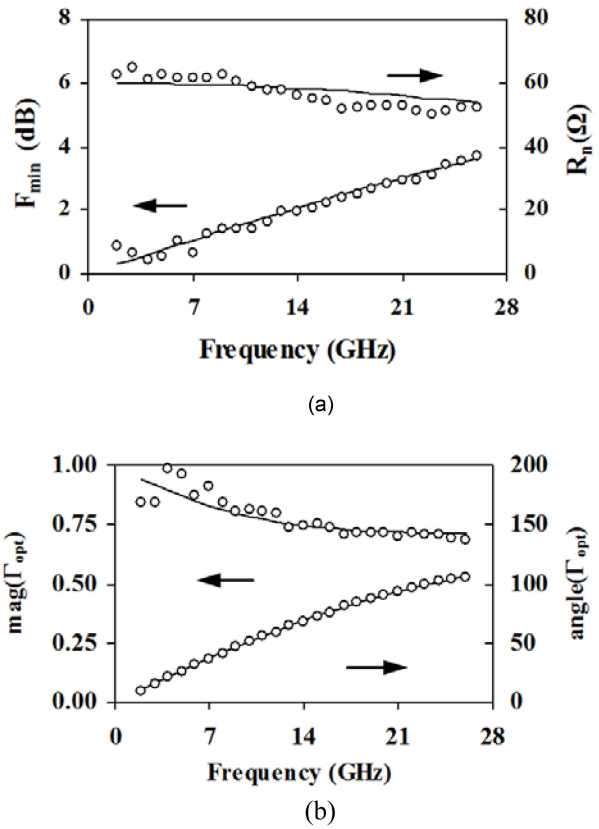

FIGURE 10. Comparison of measured and modeled noise parameters for the 16×1×2 μm MOSFET. Bias: V_{gs} = 0.8 V, V_{ds} =1.0V.

FinFETs), as demonstrated in [20] and [21]. Therefore, we believe the proposed method is very useful for the noise modeling and parameter extraction for the device fabricated by current node technology.

IV. CONCLUSION

In this paper, we have proposed an approach for determination of the channel noise model parameter Td in deep submicron MOSFETs directly from radio frequency (RF) scattering parameters and noise figure measurements. The expression of T_d is derived from a simplified noise equivalent circuit. On-wafer experimental verification is presented and a comparison with tuner based method is given. The validity of the new approach is proved by comparison with measured

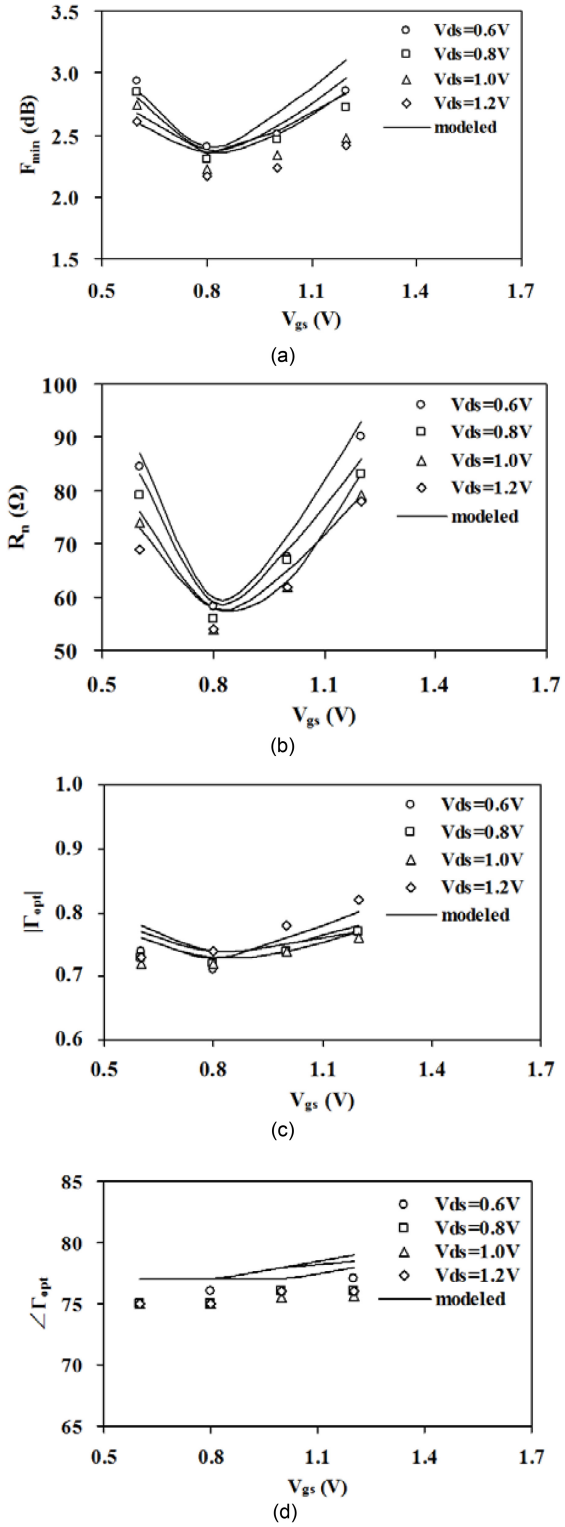

FIGURE 11. Comparison of measured and simulated noise parameters versus V_{gs} and V_{ds} at 16GHz.

S-parameter up to 50GHz and noise parameters up to 26GHz in multi-bias region. Good agreement is obtained between simulated and measured results up to 26GHz for $16\times1\times2\mu$m (number of gate fingers × unit gatewidth × cells) 90 nm gatelength MOSFETs.

REFERENCES

[1] X. Chen, C. Chen, and R. Lee, "Fast evaluation of the high-frequency channel noise in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1502–1509, Apr. 2018, doi: 10.1109/TED.2018.2808184.

[2] I. Myeong, J. Kim, H. Ko, I. Song, Y. Kim, and H. Shin, "A simple and accurate modeling method of channel thermal noise using BSIM4 noise models," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 39, no. 12, pp. 4351–4358, Dec. 2020, doi: 10.1109/TCAD.2020.2974339.

[3] G. D. J. Smit, A. J. Scholten, R. M. T. Pijper, L. F. Tiemeijer, R. van der Toorn, and D. B. M. Klaassen, "RF-noise modeling in advanced CMOS technologies," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 245–254, Feb. 2014.

[4] M. W. Pospieszalski, "Interpreting transistor noise," *IEEE Microw. Mag.*, vol. 11, no. 6, pp. 61–69, Oct. 2010.

[5] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2884–2892, Dec. 2001.

[6] S.-C. Wang et al., "Comprehensive noise characterization and modeling for 65-nm MOSFETs for millimeter-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 740–746, Apr. 2010.

[7] L. Belostotski, "On the number of noise parameters for analyses of circuits with MOSFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 877–881, Apr. 2011.

[8] M. Emam, P. Sakalas, D. Vanhoenacker-Janvier, J.-P. Raskin, T. C. Lim, and F. Danneville, "Thermal noise in MOSFETs: A two- or a three-parameter noise model?" *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 1188–1191, May 2010.

[9] A. J. Scholten et al., "Accurate thermal noise model for deep-submicron CMOS," in *Int. Electron Devices Meeting Tech. Dig.*, 1999, pp. 155–158, doi: 10.1109/IEDM.1999.823868.

[10] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microw. Theory Techn.*, vol. 37, no. 9, pp. 1340–1350, Sep. 1989.

[11] A. Cappy, "Noise modeling and measurements techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 1, pp. 1–10, Jan. 1988.

[12] H. Hillbrand and P. H. Russer, "An efficient method for computer-aided noise analysis of linear amplifier networks," *IEEE Trans. Circuits Syst.*, vol. CAS-23, no. 4, pp. 235–238, Apr. 1976.

[13] J. Gao and A. Werthof, "Scalable small-signal and noise modeling for deep-submicrometer MOSFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 4, pp. 737–744, Apr. 2009.

[14] G. Dambrine, H. Happy, F. Danneville, and A. Cappy, "A new method for on wafer noise measurement," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 3, pp. 375–381, Mar. 1993.

[15] S. Asgaran, M. J. Deen, C.-H. Chen, G. Ali Rezvani, Y. Kamali, and Y. Kiyota, "Analytical determination of MOSFET's high-frequency noise parameters from NF50 measurements and its application in RFIC design," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1034–1043, May 2007.

[16] A. Caddemi, A. Di Paola, and M. Sannino, "Determination of HEMT's noise parameters versus temperature using two measurement methods," *IEEE Trans. Instrum. Meas.*, vol. 47, no. 1, pp. 6–10, Feb. 1998.

[17] J. Gao, "Direct parameter-extraction method for MOSFET noise model from microwave noise figure measurement," *Solid-State Electron.*, vol. 63, no. 1, pp. 42–48, 2011.

[18] J. Ortiz and C. Denig, "Noise figure analysis using SPICE," *Microw. J.*, vol. 35, no. 4, pp. 89–94, 1992.

[19] J. Gao, "Fast calculation of transimpedance gain and equivalent input noise current density for high-speed optical preamplifier design," *Microw. J.*, vol. 54, no. 5, pp. 188–204, 2011.

[20] J.-P. Raskin et al., "High-frequency noise performance of 60-nm gatelength FinFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2718–2727, Oct. 2008.

[21] G. Crupi, D. M. M.-P. Schreurs, J.-P. Raskin, and A. Caddemi, "A comprehensive review on microwave FinFET modeling for progressing beyond the state of art," *Solid-State Electron.*, vol. 80, pp. 81–95, Feb. 2013.