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Plasma-Enhanced Atomic Layer Deposition-Based Ferroelectric Field-Effect Transistors

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ABSTRACT The use of the plasma-enhanced atomic layer deposition (ALD) technique for the deposition of HfO_2-based ferroelectrics has received attention in recent years primarily due to wake-up free operation. However, these studies have primarily focused on metal-ferroelectric-metal (MFM) structures. In this work, we investigate the characteristics of ferroelectric field-effect transistors (FEFETs) in which the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) gate stack is deposited using the plasma-enhanced atomic layer deposition (PEALD) technique. We observe that PEALD FEFET requires a higher write voltage for the same memory window compared to an equivalent FEFET with thermal ALD (THALD)-grown HZO. The increase in write voltage in PEALD FEFET occurs primarily due to the increase of the interfacial oxide layer using the plasma process. In addition, we observe that the SiO_2 interfacial layer underneath the ferroelectric (FE) HZO layer eliminates the wake-up behavior in both THALD and PEALD FEFETs.

INDEX TERMS FEFET, memory window, thermal atomic layer deposition, plasma-enhanced atomic layer deposition.

I. INTRODUCTION

SINCE the discovery of ferroelectric characteristics in HfO_2, FEFETs have gathered significant attention as promising candidates for non-volatile memory applications [1], [3], [4], [5], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17]. Studies on ferroelectric properties of such compounds such as $Hf_xZr_{1-x}O_2$ (HZO) in metal-insulator-metal (MIM) capacitors have revealed that characteristics such as wake-up behavior and endurance vary significantly with the deposition method used, namely thermal atomic layer deposition (THALD) and plasma-enhanced atomic layer deposition (PEALD) [18], [19], [20]. It has been observed that PEALD HZO exhibits less wake-up compared to THALD HZO, attributed to the presence of lesser t-phase

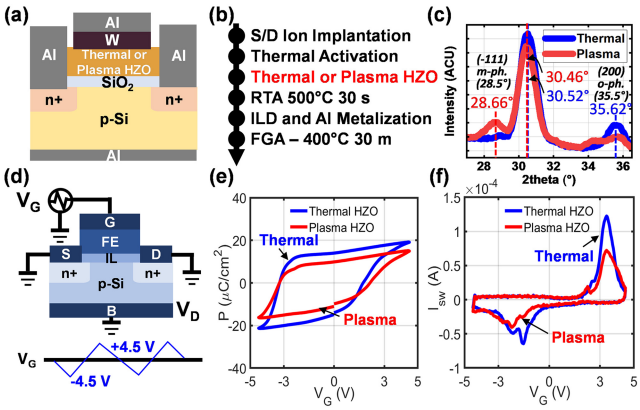

FIGURE 1. **(a) Device schematic of FEFETs. (b) Fabrication process flow (c) GIXRD spectrum of PEALD and THALD Ferroelectric HZO metal-ferroelectric-semiconductor (MFS) structures. (d) Measurement schematic for polarization vs. voltage (P-V) characteristics. (e, f) Comparison of P-V characteristics (e), current vs voltage (I-V) characteristics (f) of PEALD and THALD-based HZO FEFETs.**

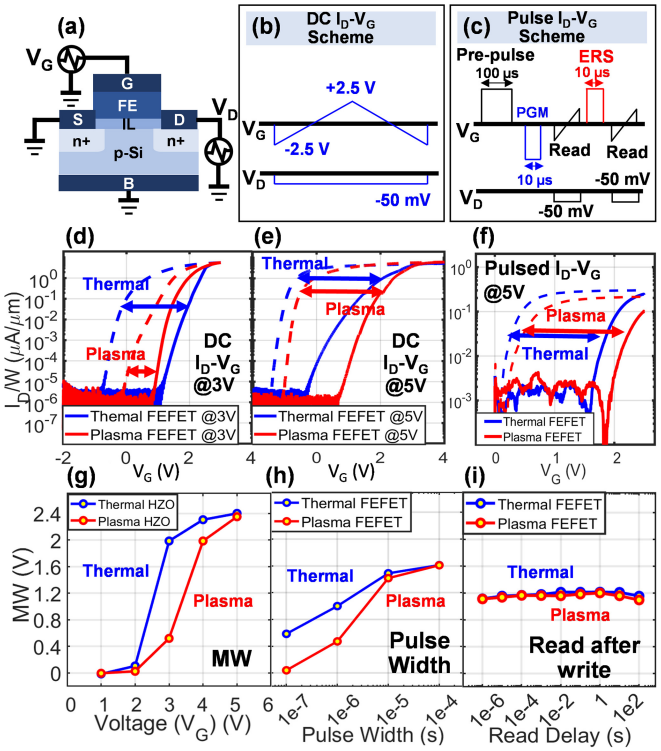

FIGURE 2. **(a) Schematic of the circuit connection for the measurement. (b) Pulse scheme for DC I_D-V_G. (c) Pulse scheme for Pulsed I_D-V_G. (d, e) DC I_D-V_G characteristics of PEALD and THALD nFEFETs for a sweep range of ±3 V (d) and ±5 V (e). (f) Pulsed I_D-V_G characteristics of PEALD and THALD FEFETs at V_{write} = ±5 V. (g-i) Evolution of MW as a function of write voltage (g), pulse width (h), and read delay after write (i).**

[21], [22]. Despite these findings, it is important to note that the impact of the use of PEALD technique on the characteristics and performance of Ferroelectric Field-Effect Transistors (FEFETs) has not been studied in details [23], [24], [25].

In this brief, we present a comparative study between FEFETs with HZO deposited via the THALD and PEALD techniques. We investigate the electrical characteristics such as memory window (MW), polarization-voltage/current-voltage (P-V/I-V), capacitance-voltage (C-V), and endurance characteristics. We further use high-resolution transmission electron microscopy (HRTEM) and grazing incidence x-ray diffraction (GIXRD) to support the inferences from the electrical characterization.

II. EXPERIMENTAL DETAILS

Fig. 1(a) to (b) illustrates the device schematic and fabrication process flow of both THALD and PEALD Si-nFEFETs. The source (S) and drain (D) regions are established through ion-implantation (BF_2, 15 keV), followed by dopant activation. Silicon wafers (B-doped Si, 1-10 ohm·cm) are cleaned using a solution of 20:1 HF and SC1, during which a chemical oxide layer forms. The HZO film is then deposited at 250°C either through THALD or PEALD at a power of 300 W, followed by crystallization via rapid thermal annealing with a W capping layer at 500°C for 30 seconds. The thickness of the HZO layer is 10 nm. For further details on the fabrication procedure of the FEFETs, one may refer to our previous publication [26]. All FEFET characterizations were conducted using a Keysight B1500A semiconductor device analyzer and C-V characteristics were measured at 10 kHz using a Keysight E4990A impedance analyzer.

III. RESULTS AND DISCUSSION

Fig. 1(c) shows glancing incidence X-ray diffraction spectrum the ferroelectric HZO layer in the FEFETs grown using the THALD and the PEALD techniques. Each XRD peak of PEALD and THALD FEFET was found to be at 30.46° and 30.52°, respectively. Considering that the O-phase is at 30.5° and the t-phase is at 30.7°, it can be concluded that both PEALD and THALD FEFETs are crystallized in the o-phase. Fig. 1(e) and 1(f) present the polarization (P) vs. gate voltage (V_G) and switching current (I) vs. V_G characteristics of the THALD and PEALD FEFETs. In this measurement, the source (S), the drain (D), and the body terminal (D) were connected together, and the measurement was performed between the shorted S-D-B terminal and the gate terminal (Fig. 1(d)). The remanent polarization ($2P_r$) of the THALD FEFET is found to be slightly larger than its PEALD counterpart (27.8 μC/cm^2 for THALD vs. 19.6 μC/cm^2 for PEALD). The coercive voltage ($2V_c$) is 4.96 V for THALD FEFET and 5.44 V for PEALD FEFET, respectively. Similar difference in remnant polarization and coercive voltage between THALD and PEALD-growth HZO in the MIM structure was observed in Ref. 18.

We measured drain current (I_D) vs. V_G characteristics of the FEFETs under DC and pulsed bias. Fig. 2(a), 2(b) and 2(c) depict the measurement scheme for DC and pulsed I_D-V_G. Fig. 2(d) and 2(e) show DC I_D-V_G characteristics for sweep ranges of ±3 V and ±5 V, respectively. Fig. 2(f) show the pulsed I_D-V_G characteristics for write voltage of

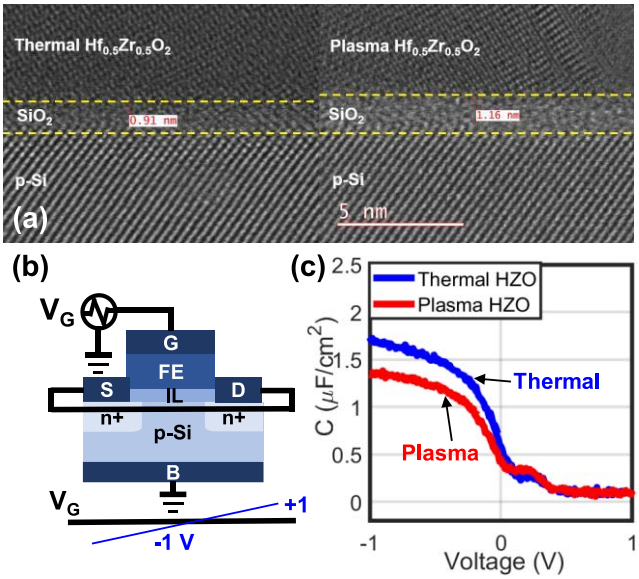

FIGURE 3. (a) Comparison of HRTEM cross-sections of the gate stacks of THALD and PEALD FEFETs. (b) Measurement schematic for the capacitance vs. voltage (C-V) measurement. (c) Comparison of split C-V characteristics of PEALD and THALD-based HZO FEFETs

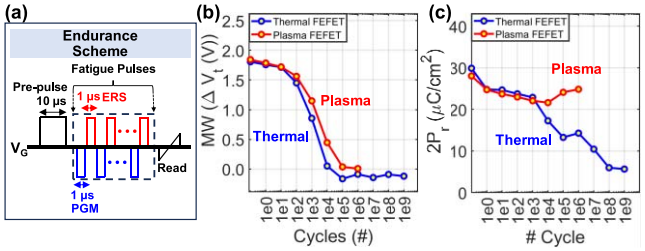

FIGURE 4. (a) Measurement scheme for endurance characteristics. (b) Evolution of MW under iso-MW condition ±4 V (THALD) and ±4.5 V (PEALD). (c) Evolution of 2Pr under iso-MW condition ±4 V (THALD) and ±4.5 V (PEALD).

TABLE 1. Comparison of the electrical characteristics in FEFETs between thermal-ALD HZO and plasma-ALD HZO.

Parameters	Thermal HZO FEFET	Plasma HZO FEFET
Maximum Memory window (MW)	2.4 V	2.35 V
Write voltage @Max MW	5 V	5 V
MW @write voltage 3V	2 V	0.4 V
Write voltage @1.8V MW	4 V	4.5 V
Coercive voltage	1.72(+), -3.24(-)	2.16(+), -3.28(-)
Polarization ($2P_r$)	13.9(+), -13.9(-)	9.86(+), -9.78(-)
Capacitance	1.73	1.33
Endurance (MW)	1e4	1e5
Endurance (Polarization)	1e9	1e6

±5 V and pulse width of 10 μs. Fig. 2(g) plots the MW as a function of the sweep range. It is clearly observed in Fig. 2(g) that while both PEALD and THALD FEFETs show similar values of maximum MW, for a given MW, PEALD requires a larger voltage sweep range for the same MW. Fig. 2(h) plots MW measured from the pulsed I_D-V_G measurement as a function of pulse width. At lower pulse widths, THALD FEFETs exhibit a larger MW compared to PEALD FEFET. Fig. 2(i) plots the MW as a function of a delay for read after write operation. It is observed that both THALD and PEALD demonstrate similar read-after-write behavior.

To understand the origin of larger write voltage requirement for a given MW in PEALD FEFETs compared to that in its THALD counterpart, we performed cross-sectional high-resolution transmission electron microscopy (HRTEM) images of the FEFET gate stacks, as presented in Fig. 3(a). It is observed that the PEALD process contributes to a thickening of the SiO_2 interfacial oxide layer. Specifically, the thickness increases to 1.16 nm for the PEALD FEFET compared to 0.91 nm for the THALD FEFET. Fig. 3(c) shows the gate capacitance C_G vs. V_G characteristics of the PEALD and THALD FEFETs. C_G was measured using the split capacitance method, between the gate terminal and shorted S-D terminal (Fig. 3(b)). THALD FEFET exhibits a higher ON-capacitance (1.73 μF/cm^2) in comparison to 1.33 μF/cm^2 in the case of PEALD FEFET. A lower value of C_G in PEALD FEFET further confirms the existence of a thicker SiO_2 layer in the PEALD FEFET. A thicker IL in turn also leads to a larger voltage drop across it during the write process, thereby leading to a larger write voltage for a given MW in PEALD FEFETs compared to its THALD counterpart. The increase in SiO_2 thickness in PEALD FEFET is presumed to be due to oxygen, which received plasma energy, diffusing into the substrate Si and forming additional SiO_2.

To assess the reliability of the FEFETs, their endurance is evaluated using the measurement scheme depicted in Fig. 4(a), Fig. 4(b) and 4(c) illustrates the evolution of MW and $2P_r$ with cycling, respectively. The MW in FEFETs have been known to be realized by neutralizing charged traps and the MW closes when the density of permanently charged traps increases [23], [24]. While in the THALD FEFET, the MW drops to zero at 1e4 cycles, the PEALD FEFET undergoes MW closure at 1e5 cycles. The faster MW closure of THALD FEFET compared to PEALD FEFET can be attributed to increased trap generation rate.

Table 1 summarizes the performance characteristics of the THALD FEFET and PEALD FEFET highlighting the trade-off between write voltage and MW endurance.

It is notable that neither the THALD FEFET nor its PEALD counterpart show any wake-up behavior, as depicted in Fig. 4(b, c). This is in contrast to the observation that in MFM structures, THALD leads to a strong wake-up behavior while PEALD does not. This suggests that the existence of the SiO_2 underneath the FE layer plays an important role in eliminating the wake-up behavior in the THALD technique for HZO growth. Further studies are required to understand

the role of the SiO_2 IL in controlling both the wake-up and the cycling endurance of FERAM and FEFET devices.

IV. CONCLUSION

In conclusion, we performed a comparative study of FEFETs wherein the 10 nm FE $Hf_{0.5}Zr_{0.5}O_2$ layer is deposited using either plasma-enhanced or thermal ALD technique (THALD or PEALD), respectively. Our main observation is that PEALD FEFET require a larger write to achieve a given memory window, due to the existence of a thicker SiO_2 interfacial layer therein compared to that in the THALD FEFET. Our study also uncover that the SiO_2 interfacial layer may play an important role for eliminating the wake-up effect in THALD and PEALD FEFET which would require further studies.

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