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Demonstration of SA TG Coplanar IGZO TFTs With Large Subthreshold Swing Using the Back-Gate Biasing Technique for AMOLED Applications

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ABSTRACT We demonstrate that the shorter channel self-aligned top-gate (SA TG) coplanar indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs), with negative voltage applied to the back-gate, exhibit superior characteristics as driving transistors in organic light-emitting diode (OLED) pixels compared to their longer channel counterparts. The shorter channel IGZO TFTs (with a channel length (L) of 3 μm) biased with a back gate voltage of -3.5 V showed a larger subthreshold swing (SS = 0.21 V/dec) than the longer channel ones (with L = 5 μm, SS = 0.16 V/dec) with a similar threshold value (V_{TH} = 0.7–0.8 V). A large SS is beneficial for controlling grayscale levels, especially at low gray levels, when IGZO TFTs are used as driving transistors in OLED pixels. Furthermore, the negatively back-gate-biased shorter channel SA TG coplanar IGZO TFTs exhibited significantly enhanced electrical stability compared to the longer channel ones under both positive gate bias and hot carrier stresses. The findings of this study are expected to be useful in expanding the utility of IGZO TFTs in OLED displays.

INDEX TERMS Self-aligned top-gate coplanar IGZO TFTs, back-gate biasing technique, short channel, subthreshold swing, electrical stability.

I. INTRODUCTION

OVER the last decade, indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs) have become extensively employed as the backplane in organic light-emitting diode (OLED) displays [1], [2]. This widespread adoption can be attributed to the numerous appealing features offered by IGZO TFTs, such as high field-effect mobilities (μ_{FE}s), good large-area uniformity, and low leakage currents [3], [4], [5], [6]. In OLED displays, IGZO TFTs are mainly employed in the implementation of pixel and peripheral circuits [7]. For switching transistors in the pixel and peripheral circuits of OLED displays, it is desirable for TFTs to have a high current on-off ratio with a small subthreshold swing (SS). However, for the driving transistors in OLED pixels, a large SS is advantageous because these transistors are used to control the gradation of the OLED displays [7], [8]. A large SS contributes to better grayscale level controllability, especially at low gray levels where the human eye is highly sensitive [8]. Generally, IGZO TFTs have smaller SS values than silicon-based TFTs due to the relatively small subgap density of states (DOS) near the conduction band edge [9]. While this is advantageous when using them as switching transistors in OLED displays, it can be disadvantageous when using them as driving transistors in OLED pixels.

The SS value of IGZO TFTs can be easily increased by increasing the subgap DOS within the IGZO, but this generally leads to deterioration in the electrical stability

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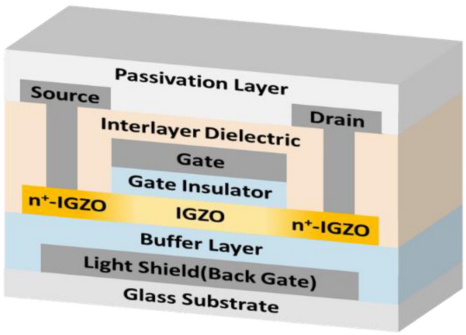

FIGURE 1. **Cross-sectional schematic of the fabricated SA TG coplanar IGZO TFTs.**

of the devices. In recent years, several studies have been conducted to increase the *SS* values of IGZO TFTs while maintaining the μ_{FE} values and electrical stabilities of the devices [8], [10]. However, these previous studies have shown the drawback of complex processes and device structures, such as fabricating multi-channel TFTs based on plasma-enhanced atomic layer deposition techniques. In this study, we demonstrate that the shorter channel self-aligned top-gate (SA TG) coplanar IGZO TFTs, with negative voltage applied to the back-gate, can exhibit larger *SS* values and significantly better electrical stability than their longer channel counterparts. The SA TG coplanar structure is widely utilized in fabricating IGZO TFTs for AMOLED applications due to its small parasitic capacitance and excellent process controllability [11], [12]. In this work, we experimentally confirmed our observations using commercially available SA TG coplanar IGZO TFTs with channel lengths (*Ls*) ranging from 3 to 5 μm. Considering that the back gate biasing technique has already been utilized in implementing OLED pixel circuits using IGZO TFTs [13], [14], [15], the results of this study are anticipated to further enhance the applicability of IGZO TFTs in OLED displays.

II. EXPERIMENTS

Fig. 1 shows a schematic cross section of the fabricated SA TG coplanar IGZO TFT. The fabrication process for the SA TG coplanar IGZO TFT is described as follows. First, Al layer was deposited and patterned to form the back gate electrode (i.e., a light shield) on a glass substrate. Next, a 300-nm-thick SiO_x layer was formed using plasma-enhanced chemical vapor deposition (PECVD) at 350 °C as a buffer layer. A 30-nm-thick IGZO (In:Ga:Zn = 1:1:1 at %) was deposited via radio-frequency magnetron sputtering as a channel layer, and then a 120-nm-thick SiO_x gate insulator was deposited via PECVD at 200 °C, followed by the deposition of a metal (Mo) as a gate electrode. After deposition and patterning of the Mo gate electrode and SiO_x gate insulator, a SiO_x and SiN_x layer was sequentially deposited as an interlayer dielectric (ILD) using PECVD and pattered to form via holes. The source and drain electrodes of Al were deposited and patterned on the n^+-IGZO source/drain extension regions, where, the hydrogen diffused from the

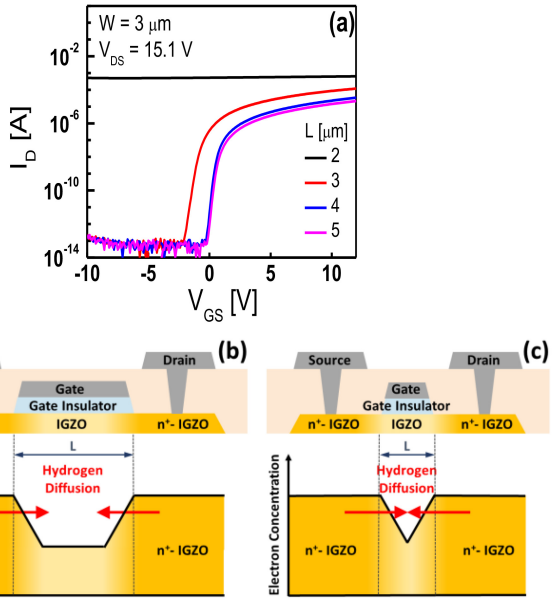

FIGURE 2. **(a) Transfer characteristics of the SA TG coplanar IGZO TFTs with various *Ls* (W/L = 3 μm/2, 3, 4, 5 μm) measured in the saturation region (V_{DS} = 15.1 V). Here, both the source and back gate electrodes were grounded. Schematic of the electron distribution across the channel for SA TG coplanar IGZO TFTs with (b) long and (c) short channel.**

PECVD-deposited ILD acts as electron donors in IGZO and forms the source/drain extension regions [16], [17]. Finally, the TFTs were passivated with a SiO_2 layer and thermally annealed at 340 °C to achieve stable and uniform electrical performances.

III. RESULT AND DISCUSSION

Fig. 2(a) depicts the semi-logarithmic scale transfer curves (I_D–V_{GS} plot) of the SA TG coplanar IGZO TFTs with *Ls* ranging from 2 to 5 μm and a constant channel width (W = 3 μm), where I_D represents the drain current, and V_{GS} corresponds to the gate-to-source voltage. The measurements were performed in the saturation region with a drain-to-source voltage (V_{DS}) of 15.1 V. Throughout the measurements, both the source and back gate electrodes were grounded. Fig. 2(a) shows that the transfer curve shifts in the negative direction and *SS* increases as L decreases from 5 to 3 μm. I_D was hardly modulated by V_{GS} in the TFT with L = 2 μm. These phenomena are mainly attributed to the hydrogen diffusion from the n^+-IGZO source/drain extension region to the channel region in the SA TG coplanar structure IGZO TFT, which results in higher electron concentration within the channel especially in short channel SA TG coplanar IGZO TFTs [18], [19]. Figs. 2(b) and (c) compare the schematic of the electron distribution across the channel for SA TG coplanar IGZO TFTs with long and short channel, respectively. The increase in the electron concentration promotes the formation of the percolation conduction path in IGZO, making it difficult to turn off the TFT. Moreover, a higher electron concentration within the channel and a shorter effective channel length impedes the modulation of I_D by the electric field induced

TABLE 1. V_{TH}, SS, and μ_{SAT} values extracted from the fabricated SA TG coplanar IGZO TFTs with every L (L = 2, 3, 4, 5 μm).

L [μm]	V_{TH} [V]	SS [V/dec]	μ_{SAT} [cm^2/V·s]
2	–	–	–
3	−0.91	0.21	21.01
4	0.59	0.16	13.61
5	0.74	0.16	10.85

by the applied V_{GS}; which increases the SS value of the IGZO TFT [19], [20], [21].

Table 1 lists the threshold voltage (V_{TH}), SS, and saturation mobility (μ_{SAT}) values extracted from IGZO TFTs with every L, where V_{TH} was extracted by using the linear extrapolation method, and SS was obtained at I_D in the range of 10^{-11}–10^{-10} A according to the equation:

$$SS = (d(\log I_D)/dV_{GS})^{-1}. \quad (1)$$

μ_{SAT} values were calculated in the saturation region as follows

$$\mu_{SAT} = \frac{2L}{WC_I}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2, \quad (2)$$

where C_I is the gate insulator capacitance per unit area. Fig. 2(a) and Table 1 show that the fabricated SA TG coplanar IGZO TFTs operate as enhancement-type devices with V_{TH} larger than 0 V when L is not smaller than 4 μm, where the enhancement type operation provides various advantages for circuit implementation in OLED displays [22].

However, for IGZO TFTs with L = 4 or 5 μm, the SS value is small at 0.16 V/dec, making it somewhat challenging to utilize them as driving transistors in OLED pixels. The larger μ_{SAT} values in the shorter channel SA TG coplanar IGZO TFTs in Table 1 are possibly attributed to both the enhanced electron percolation conduction due to the increase in channel electron concentration [9], and to a phenomenon where the μ_{SAT} value calculated through Eq. (2) exhibits larger values than the actual values when the effective channel length is significantly smaller than the drawn channel length, especially in short channel devices, as observed in Fig. 2(c) [23].

Fig. 3(a) depicts the transfer characteristics of the short channel SA TG coplanar IGZO TFT (L = 3 μm) measured at various back-gate biases (V_{BG}s). From Fig. 3(a), it is observed that as V_{BG} becomes more negative, the transfer curve undergoes a positive shift, and the TFT operates in the enhancement mode at V_{BG} = −3.5 V with a positive V_{TH} of 0.78 V. This is because negative V_{BG} impedes the formation of the accumulation layer in IGZO TFTs, thus necessitating a higher voltage on the top gate to form the accumulation layer [24], [25]. Table 2 presents the V_{TH} and SS values extracted from the short channel IGZO TFT (L = 3 μm) with every V_{BG}. Unlike V_{TH}, no significant change is observed in SS with respect to the applied V_{BG}.

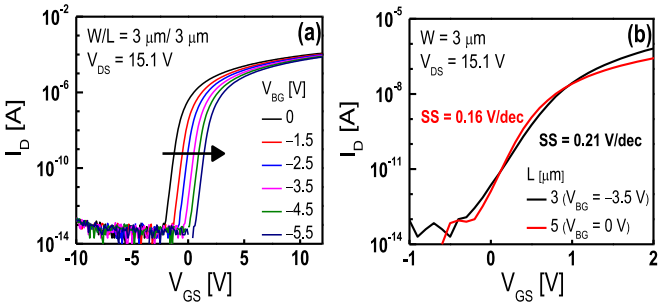

FIGURE 3. (a) Transfer characteristics of the shorter channel SA TG coplanar IGZO TFT (L = 3 μm) measured at various V_{BG}s. (b) Comparison of the transfer characteristics measured from the longer channel SA TG coplanar IGZO TFT (L = 5 μm, V_{BG} = 0 V) and negative back-gate-biased shorter channel SA TG coplanar IGZO TFT (L = 3 μm, V_{BG} = −3.5 V).

TABLE 2. V_{TH} and SS values extracted from the short channel SA TG coplanar IGZO TFT (L = 3 μm) with every VBG ranging from −5.5 to 0 V.

V_{BG} [V]	V_{TH} [V]	SS [V/dec]
0	−0.91	0.21
−1.5	−0.19	0.21
−2.5	0.29	0.21
−3.5	0.78	0.21
−4.5	1.27	0.21
−5.5	1.75	0.21

Fig. 3(b) compares the transfer characteristics measured from the longer channel SA TG coplanar IGZO TFT (L = 5 μm, V_{BG} = 0 V) and negative back-gate-biased shorter channel SA TG coplanar IGZO TFT (L = 3 μm, V_{BG} = −3.5 V). Fig. 3(b) indicates that V_{TH} is similar in both transfer characteristics; however, the transfer curve measured from the negative back-gate-biased shorter channel SA TG coplanar IGZO TFT exhibits larger values for SS and on current (I_{ON}). The results in Fig. 3(b) clearly demonstrates that the shorter channel SA TG coplanar IGZO TFTs with an appropriate negative V_{BG} can provide more favorable characteristics when utilized as a driving transistor in OLED pixels, compared to the longer channel SA TG coplanar IGZO TFTs.

Figs. 4(a) and (b) compare the time dependencies of the transfer curves measured at V_{DS} = 15.1 V under positive bias stress (PBS (V_{GS} = 20 V, V_{DS} = 0 V) for longer channel (L = 5 μm, V_{BG} = 0 V) and negative back-gate-biased shorter channel (L = 3 μm, V_{BG} = −3.5 V) IGZO TFTs, respectively. Fig. 5 summarizes the ΔV_{TH} obtained from both TFTs under different positive bias temperature stress (PBTS) conditions at 60 °C after a stress time of 60 minutes. The results in Figs. 4 and 5 demonstrate that the negative back-gate-biased shorter channel IGZO TFT (L = 3 μm, V_{BG} = −3.5 V) exhibits superior electrical stability compared to the longer channel IGZO TFT (V_{GS} = 20 V, V_{DS} = 0 V) under PBTS conditions.

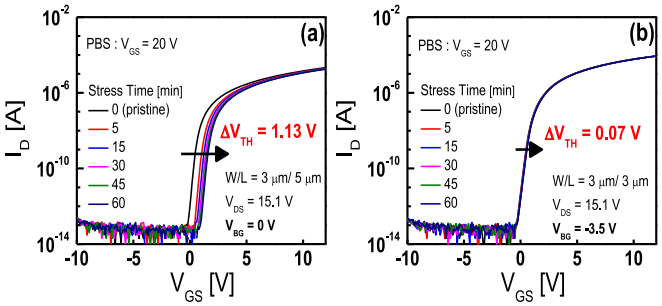

FIGURE 4. Time dependencies of the transfer curves measured at V_{DS} = 15.1 V under PBS (V_{GS} = 20 V, V_{DS} = 0 V) for (a) longer channel (L = 5 μm) and (b) negative back-gate-biased shorter channel (L = 3 μm, V_{BG} = −3.5 V) SA TG coplanar IGZO TFTs.

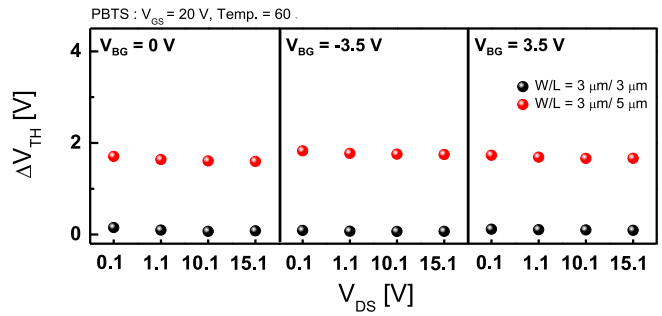

FIGURE 5. ΔV_{TH} extracted from long-channel (L = 5 μm) and short-channel (L = 3 μm) SA TG coplanar IGZO TFTs under different PBTS conditions at 60 °C after a stress time of 60 minutes.

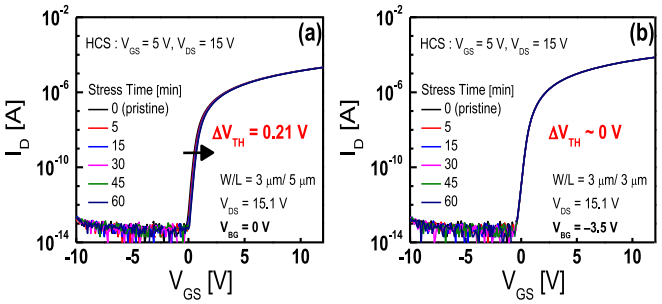

FIGURE 6. Time dependencies of the transfer curves measured at V_{DS} = 15.1 V under HCS (V_{GS} = 5 V, V_{DS} = 15 V) for (a) longer channel (L = 5 μm) and (b) negative back-gate-biased shorter channel (L = 3 μm, V_{BG} = −3.5 V) SA TG coplanar IGZO TFTs.

Figs. 6(a) and (b) compare the time dependencies of the transfer curves measured at V_{DS} = 15.1 V under hot carrier stress (HCS (V_{GS} = 5 V, V_{DS} = 15 V)), demonstrating that the negative back-gate-biased shorter channel IGZO TFT (L = 3 μm, V_{BG} = −3.5 V) exhibits superior electrical stability compared to the longer channel IGZO TFT (L = 5 μm, V_{BG} = 0 V) not only under PBTS but under HCS conditions. These phenomena are likely attributed to the more efficient passivation of electrical defects within the IGZO channel by hydrogen diffusing from the n^+-IGZO source/drain extension region in the shorter channel device. Hydrogen within IGZO has been reported not only to act as an electron donor but also to passivate various defects such as oxygen deficiencies, oxygen interstitials, and others [26], [27].

IV. CONCLUSION

In this study, we showed that the shorter channel SA TG coplanar IGZO TFTs, with an appropriately negative V_{BG}, can exhibit similar V_{TH}, larger SS and I_{ON}, as well as superior electrical stability in comparison to the longer channel counterparts by comparing the electrical properties of commercially available SA TG coplanar IGZO TFTs with Ls ranging from 3 to 5 μm. The large SS and superior electrical stability are beneficial for controlling grayscale levels when IGZO TFTs are utilized as driving transistors in OLED pixels.

Although the obtained SS value (0.21 V/dec) is still somewhat insufficient for use in driving transistors in OLED pixels, it is expected that SA TG coplanar IGZO TFTs with sufficiently high SS values can be fabricated through optimization of the device structure and process based on the proposed methodology in subsequent research.

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