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# The Endurance and Reliability Mechanisms Investigation of InGaZnO and InSnO Thin Film Transistors

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**ABSTRACT** Amorphous oxide semiconductor-thin film transistors (AOS-TFTs) have attracted considerable attention due to their impressive performance in various applications. However, there is a limited amount of study available on the reliability of AOS-TFTs. This work investigates the endurance and reliability mechanisms of Indium Gallium Zinc Oxide (IGZO) and Indium Tin Oxide (ITO) TFTs. The devices underwent a range of test conditions to evaluate their endurance properties. The study utilized Zero-Bias Endurance Tests (ZBET) to examine the fluctuating behaviors of threshold voltage, revealing valuable insights into the causes of electrical instability. The study highlights the crucial importance of electron depletion and restoration dynamics in affecting the reliability of TFTs. Additionally, the study found differences in the performance of IGZO-TFTs and ITO-TFTs, suggesting that the differing features of the materials have a significant impact on the endurance and reliability of TFTs.

**INDEX TERMS** InGaZnO thin film transistor, InSnO thin film transistor, endurance test, electron depletion and restoration.

## I. INTRODUCTION

Amorphous oxide semiconductor-thin film transistors (AOS-TFTs) have garnered considerable interest since their introduction by Nomura et al. [1] in 2004, with the use of InGaZnO (IGZO). In 2006, Yabuta et al. [2] conducted research on IGZO-TFTs which were suitable for high-performance and low-temperature applications, thereby paving the way for their manufacture in a compatible manner. Later, in 2012, Sharp started producing liquid crystal displays using IGZO-TFTs. Currently, there is a significant increase in the research of AOS-TFTs for various applications such as DRAM, SRAM, FeRAM, and 3D heterogeneous integration [3], [4], [5], [6], [7], [8], [9], [10]. This growth is attributed to their exceptional performance, adaptable design architecture, and strong potential for integration. The endurance and reliability of AOS-TFTs are essential for their efficient utilization in analog circuit applications. However, studies on the reliability of AOS-TFTs have only focused on negative bias stress (NBS) instability, positive bias stress (PBS) instability, negative bias illumination stress (NBIS) instability, and other associated aspects [11], [12], [13], [14], [15], [16], [17], [18]. To promote the wider adoption of AOS-TFTs, it is essential to assess their endurance performance and gain a comprehensive understanding of the underlying mechanism.

In their study, Nomura et al. [11] examined the positive shifts in the threshold voltage ($V_{TH}$) of IGZO-TFTs. They

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found that these shifts were caused by deep acceptor-type traps in annealed TFTs and an increase in shallow traps in unannealed TFTs during constant current stress. Additional research, such as the study conducted by You et al. [12], specifically examined the employment of Ti-doped IGZO and HfAlO gate dielectric layers. The purpose of this investigation was to minimize defects and prevent surface scattering in order to enhance the performance of NBS, PBS, and NBIS. In addition, Kim et al. [13] conducted study on the build-up of deep states at the channel/dielectric interface under NBIS, whereas Uraoka et al. [14] examined F-doped SiN gate dielectric layers in order to decrease interface states. The experiments conducted by Kang et al. [15] and Park et al. [16] investigated the adsorption of oxygen and water on IGZO surfaces. These adsorptions resulted in the creation of depletion layers and defects that vary in thickness. Koretomo et al. [17], [18] demonstrated the use of techniques such as improving sputtering procedures, and adding annealing and passivation layers to decrease flaws and improve the reliability of AOS-TFTs. To summarize, the main factor for AOS-TFT instability is the presence of shallow or deep oxygen vacancy defects, which can either create or remove various types of oxygen vacancies. Nevertheless, these investigations fail to completely elucidate the variations in stability caused by variations in channel thickness and AOS materials. Additionally, they do not conduct exhaustive endurance tests for AOS-TFTs, which is essential for their optimal utilization in advanced applications.

IGZO is a significant material that has undergone extensive research and has reached a stage of mature uses. On the other hand, ITO is a highly conductive substance that finds extensive application in liquid crystal displays and OLED displays. Both IGZO and ITO possess well-established manufacturing techniques and exhibit a remarkably low cost. Hence, conducting a comparative analysis of IGZO and ITO is advantageous for large-scale manufacturing. This work investigates the endurance and reliability mechanism of AOS-TFTs by comparing the characteristics of IGZO and indium tin oxide (ITO) channel materials. TFTs with varying channel thicknesses are fabricated under different annealing conditions. Data was gathered from the endurance tests, Zero-Bias Endurance Tests (ZBET), to examine the causes of AOS instability and to understand the variations in endurance among the devices. The primary factor responsible for the differences in endurance among 10 nm IGZO, 20 nm IGZO, and 5 nm ITO TFTs is the disparity in electron depletion. 10 nm IGZO-TFTs exhibit a higher susceptibility to be depleted compared to both 20nm IGZO and 5nm ITO TFTs. The endurance characteristics vary for IGZO and ITO TFTs under different annealing conditions due to the dominant effect of annealing on deep oxygen vacancy defects in IGZO materials and on electron concentration in ITO materials.

## II. EXPERIMENT

IGZO-TFTs and ITO-TFTs were created as inverted staggered planar transistors, as shown in **Fig. 1**. **Fig. 2** displays the microscopic view of an ITO-TFT. The gate electrode was created by depositing a layer of 60 nm thick molybdenum (Mo) using magnetron sputtering. Afterwards, a 10 nm layer of silicon dioxide was used as the gate insulator (GI) and was produced using the plasma-enhanced chemical vapor deposition (PECVD) technology. The precursors employed were $SiH_4$ and $N_2O$, and the process was done under a temperature of 400°C for a duration of 6 seconds. The active layers (ALs) composed of IGZO or ITO were deposited using a radio-frequency (RF) sputtering system. The sputtering target employed was either an In:Ga:Zn = 1:1:1 target or a target doped with 10%wt of Tin Oxide ($SnO_2$) in Indium Oxide ($In_2O_3$). Device A and B had IGZO ALs with thicknesses of 10 nm and 20 nm respectively, whilst device C had a 5 nm ITO AL. The patterning of IGZO and ITO was achieved by employing a 3.3% nitric acid etchant for IGZO and a 3.3% nitric acid-17.6% hydrochloric acid mixed etchant for ITO. Subsequently, a 60 nm layer of Mo was applied as the metal for the source and drain by magnetron sputtering deposition. It was then shaped using a dry etch method. Following that, passivation layers with a thickness of 100 nm were created using a PECVD method at a temperature of 200°C. These devices were then subjected to annealing at temperatures of 250°C and 300°C, with various durations, in the presence of $O_2$ or $N_2$. The unannealed IGZO-TFTs and ITO-TFTs were labeled as A1, B1, and C1, whereas devices A4, B4, and C4 were subjected to annealing at 300°C in an oxygen-rich atmosphere for a duration of 80 minutes. Devices A2, B2, C2, or A6, B6, C6 were fabricated by modifying the annealing temperature from 300°C to 250°C or by switching the ambient environment from $O_2$ to $N_2$. In addition, devices A3, B3, C3, A5, B5,

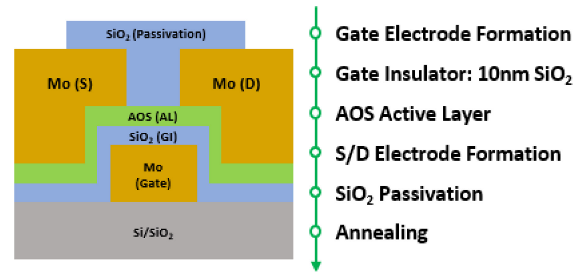


**FIGURE 1. The fabrication flow of the inverted staggered AOS-TFTs in this work.**

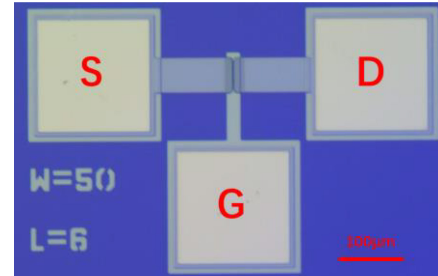


**FIGURE 2. The microscopic image of an ITO-TFT.**

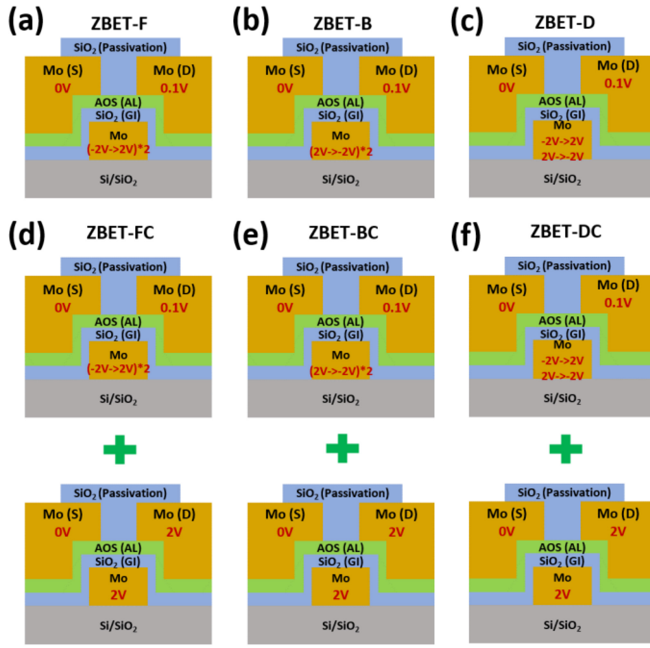


FIGURE 3. The Zero-Bias Endurance Tests (ZBET) included two times forward sweeping, two times backward sweeping, and double-direction sweeping, marked as (a) ZBET-F, (b) ZBET-B and (c) ZEBT-D, then followed by a constant current, marked as (d) ZBET-FC, (e) ZBET-BC and (f) ZBET-DC.

TABLE 1. Listing the annealing conditions for the 10nm IGZO, 20nm IGZO and 5nm ITO devices in this experiment.

| Annealing Conditions | 10nm IGZO (Device A) | 20nm IGZO (Device B) | 5nm ITO (Device C) |
|---|---|---|---|
| Unannealed | A1 | B1 | C1 |
| 250°C, $O_2$, 80 minutes | A2 | B2 | C2 |
| 300°C, $O_2$, 40 minutes | A3 | B3 | C3 |
| 300°C, $O_2$, 80 minutes | A4 | B4 | C4 |
| 300°C, $O_2$, 120 minutes | A5 | B5 | C5 |
| 300°C, $N_2$, 80 minutes | A6 | B6 | C6 |

and C5 were manufactured at a temperature of 300°C in an atmosphere with $O_2$ for annealing periods of 40 minutes and 120 minutes. The device configurations are specified in **Table 1**.

The electrical properties were assessed utilizing a semiconductor parameter analyzer (Keysight B1500). The experiments were performed at the room temperature (RT), and the threshold voltages, defined as the gate voltage at which the drain current reaches 100 pA, a constant current technique. A novel approach for investigating the mechanisms of reliability is the Zero-Bias Endurance Tests (ZBET). This method involves two forward scans, two backward scans, and a double-direction scan, denoted as ZBET-F, ZBET-B, and ZBET-D, respectively. Some tests are followed by a constant current stress, denoted as ZBET-FC, ZBET-BC, and ZBET-DC, as shown in **Fig. 3**. The implementation of constant current stress required the establishment of a drain voltage and gate voltage of 2V for a duration of half a second.

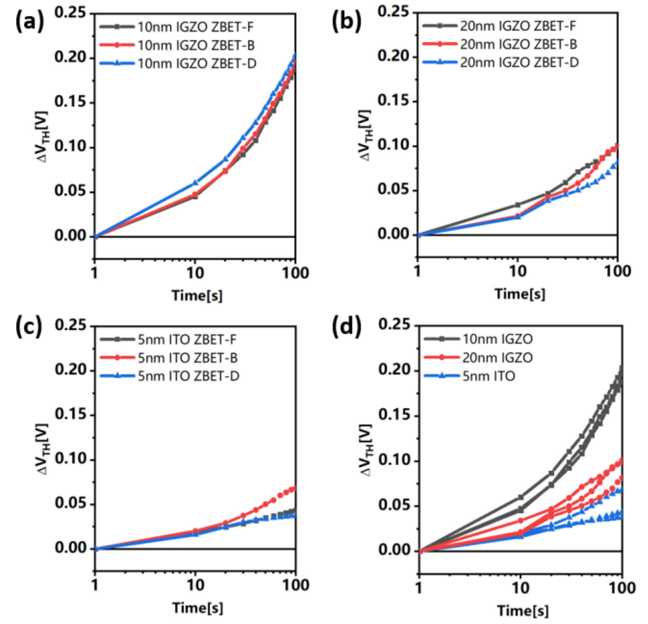


FIGURE 4. The ZBET of device A1, B1 and C1. The two times forward sweeping, two times backward sweeping and double directions sweeping, marked as ZBET-F, ZBET-B and ZBET-D, were used every 10 seconds. The threshold voltage shifts of device A1, B1 and C1 are plotted in (a), (b) and (c). (d) integrates all the data and categorizes by different devices.

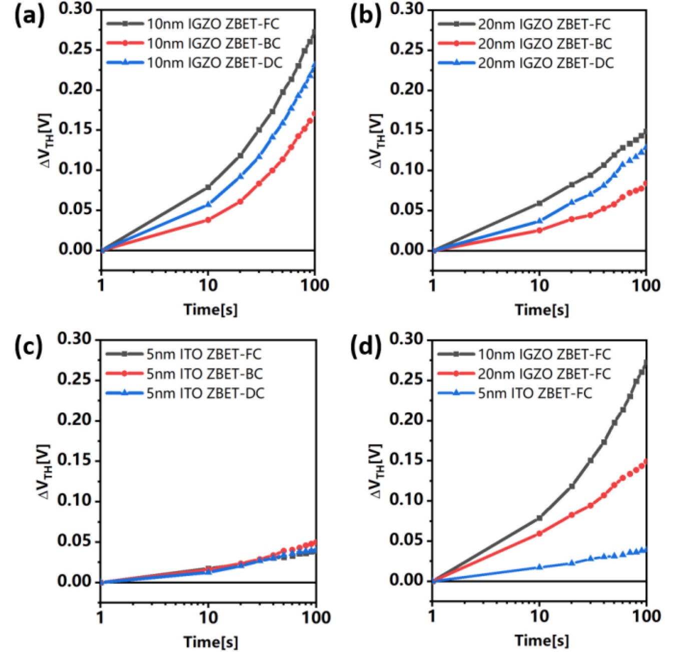


FIGURE 5. The ZBET with a constant current of device A1, B1 and C1. The two times forward sweeping, two times backward sweeping, double directions sweeping and followed by a constant current, marked as ZBET-FC, ZBET-BC and ZBET-DC, were used every 10 seconds. The threshold voltage shifts of device A1, B1 and C1 are plotted in (a), (b) and (c).

## III. RESULTS AND DISCUSSION

The Zero-Bias Endurance Tests (ZBET) results for devices A1, B1, and C1 were gathered, as shown in **Fig. 4 and 5**. Every device was subjected to $I_d V_g$ sweeping at a frequency

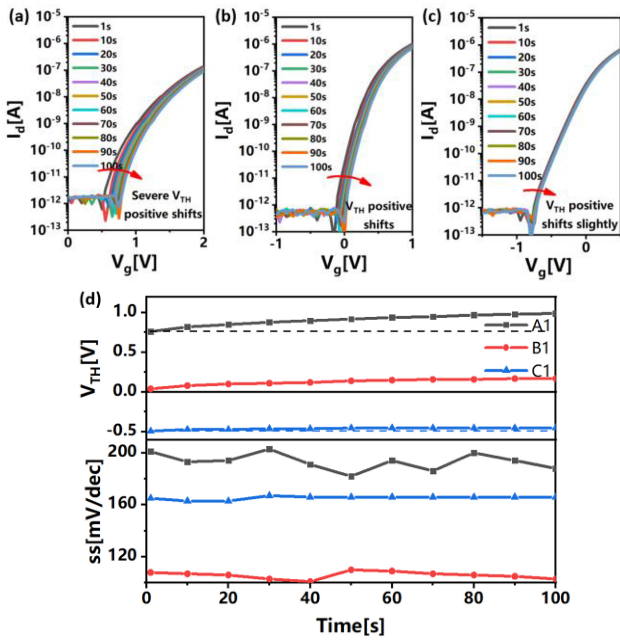


FIGURE 6. The $I_dV_g$ curve of (a) A1, (b) B1 and (c) C1 with ZBET-DC. (d) summarized the threshold voltage and subthreshold swing (ss) of (a)(b)(c).

of 10 seconds. The $I_dV_g$ sweeping involved three types of sweeping: forward sweeping, backward sweeping, and double-direction sweeping, referred to as ZBET-F, ZBET-B, and ZEBT-D, respectively. Although there was a noticeable variation in endurance amongst the devices, the variance caused by the different testing techniques was rather modest, as shown in **Fig. 4**. After ZBET tests, a constant current stress was followed for a duration of 0.5 seconds. Those tests were referred to as ZEBT-FC, ZEBT-BC, and ZEBT-DC. **Fig. 5** revealed the results of ZEBT-FC, ZEBT-BC, and ZEBT-DC for devices A1, B1, and C1. The threshold voltage shifting curves of devices A1 and B1 were separated. This study examined the consistent positive shifts in threshold voltage caused by current, as previously explored by Nomura et al. [11]. However, Nomura's explanation could not fully account for the disparity between IGZO-TFTs and ITO-TFTs. Also, it does not provide a comprehensive elucidation for the variations in reliability caused by varied channel thicknesses, as shown in **Fig. 6**.

This research proposes that the discrepancies in endurance and reliability across different devices can be attributed to electron depletion [15] and subsequent restoration. The Random Band-Edge Model (RBEM) is a model used to study carrier transport in AOSs [19]. According to **Fig. 7**, the model shows many valleys with distinct depths below the conductive band. Based on this concept, $I_dV_g$ sweeping results in a reduction of electrons in the valleys by drain current. However, the restoration of electrons is impeded by AOS barriers, causing a positive change in threshold voltages. The presence of In-rich (lower and less barriers) in ITO TFTs reduces the induced electron depletion in transfer

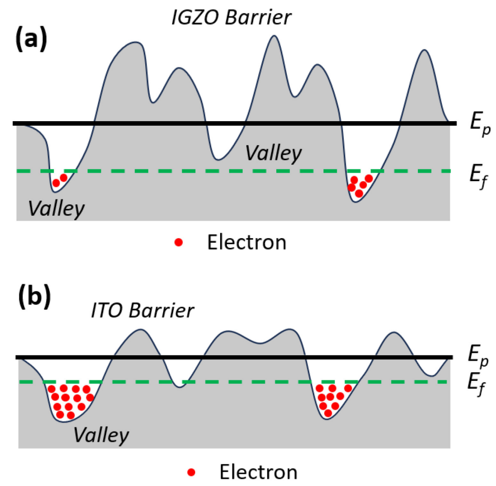


FIGURE 7. Band structure of (a) IGZO material and (b) ITO material based on Random Band-Edge Model. comparing to ITO material, IGZO has higher barriers due to its lower In element concentration. That causes the difficulty of IGZO channel electron restoration. The $E_p$ is the percolation band minimum and the $E_f$ is the Fermi level.

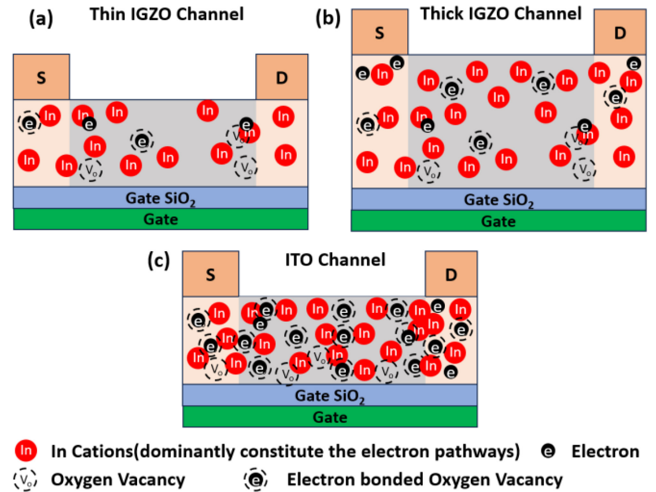


FIGURE 8. (a) The thin IGZO channel has limited electrons which is easier to be depleted than (b) the thicker one. (c) The ITO channel has more electrons due to its material characteristics which hinders the channel depletion.

characteristic tests. Thicker channel IGZO TFTs have a challenging depletion process [25], as illustrated in **Fig. 7 and 8**. The data presented in **Fig. 4** aligns closely with the predictions of this hypothesis. The idea suggests that the results of endurance tests conducted with a consistent electric current, as shown in **Fig. 5**, can be readily comprehended. Forward sweeping results in a greater accumulation of electrons at the gate isolator and channel interface compared to backward sweeping. And the followed constant current stress partially removes these accumulated electrons, as seen in **Fig. 9**. Forward sweeping, in combination with constant current stress, significantly reduces the number of electrons in the channel region of TFTs. Then, this depletion causes a significant positive change in the threshold voltage. The alleviation and potential elimination of this issue in

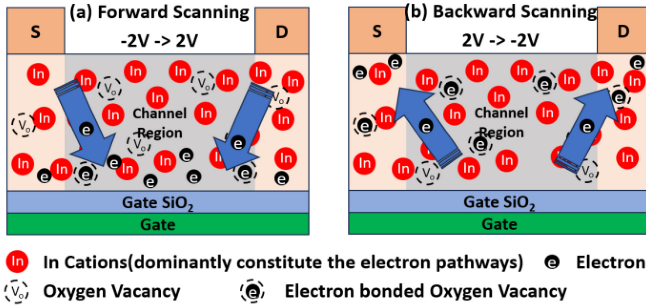


**FIGURE 9. (a) Forward sweeping will accumulate electrons at the end of the scanning and the electrons are partly removed by following constant current test and cause severe electron depletion. (b) Backward sweeping will disperse the electrons back into channel. The following constant current induced electron depletion is limited.**

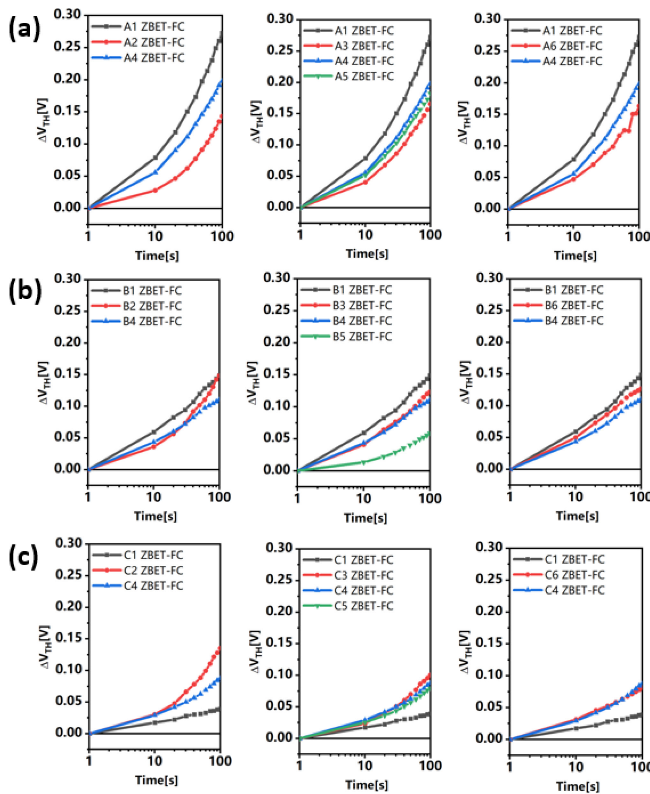


**FIGURE 10. The ZBET-FC of (a) 10nm IGZO, (b) 20nm IGZO and (c) 5nm ITO devices with different annealing conditions. The IGZO-TFTs demonstrated improved endurance performance post-annealing processes. Conversely, ITO-TFTs did not exhibit improvement similar to IGZO-TFTs under the same annealing conditions.**

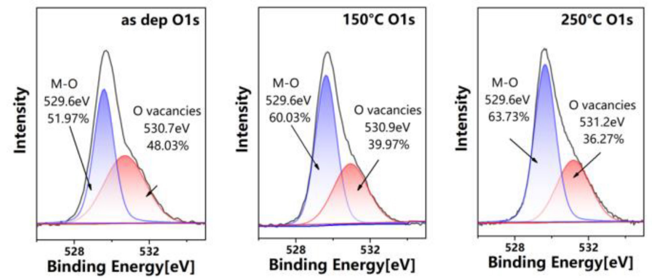


**FIGURE 11. Characterization of the X-ray photoelectron spectroscopy (XPS) of ITO channel material at various annealing temperatures.**

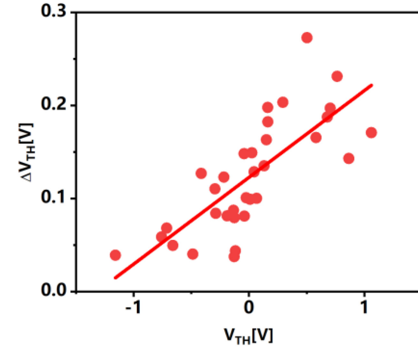


**FIGURE 12. The threshold voltages of IGZO and ITO devices are positively related their threshold voltage shifts under each endurance tests.**

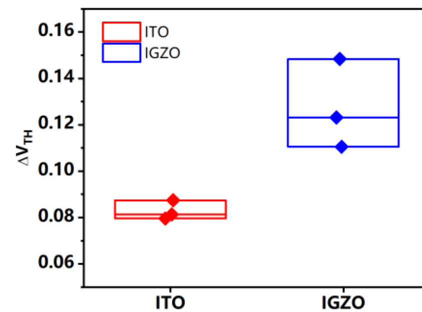


**FIGURE 13. The threshold voltage shifts of IGZO and ITO devices with the same initial threshold voltage level to eliminate the electron concentration induced reliability effect. ITO-TFTs show the superior reliability comparing to IGZO-TFTs.**

ITO TFTs can be attributed to the low barriers and high electron concentration present in the conductive band of ITO channels.

In addition, a forward sweeping ZBET was performed using constant currents for devices A2-6, B2-6, and C2-6. The results of this experiment are displayed in **Fig. 10**. Similar to IGZO, the presence of oxygen vacancies in the ITO channel material decreases after undergoing annealing processes, as seen in **Fig. 11**. In contrast, ITO-TFTs did not show a similar improvement as IGZO-TFTs, suggesting a degradation that could not be fully explained by flaws and traps in ITO-TFTs. The endurance behaviors of ITO-TFTs under different annealing conditions is dominated by electron concentration. In order to verify this hypothesis, the threshold voltages of various devices and their threshold voltage shifts during each endurance test are correlated and illustrated in **Fig. 12**. In **Fig. 12**, there is a positive correlation between the shift in threshold voltage and the threshold voltage (electron concentration) of different devices. So, annealed ITO-TFTs have less electron concentration which induces large threshold voltage shifts.

By conducting a comparison of the threshold voltage shifts among devices that have the same threshold voltage,

any reliability discrepancies that be affected by electron concentration was avoided. This is clearly demonstrated in **Fig.** 13. It provides evidence of the better endurance and reliability of ITO-TFTs.

## IV. CONCLUSION

This study has provided insight into the mechanisms that determine the reliability of AOS-TFTs and has identified differences in the endurance and reliability of IGZO-TFTs and ITO-TFTs when subjected to various test conditions. These findings demonstrate the relationship between material properties and channel characteristics. By employing ZBET testing methodologies, specifically ZBET-F, ZBET-FC, ZBET-B, ZBET-BC, ZBET-D, and ZBET-DC, we discovered difference in endurance between IGZO and ITO TFTs. The results of our research indicate that the depletion and restoration of electrons within the devices play a crucial role in causing the shifting of the threshold voltage. This study emphasized the essential significance of material composition and channel thickness in affecting the reliability of TFT devices. ITO-TFTs demonstrated better endurance performance due to their high electron concentration and low barriers in conductive band, which prevents electron depletion and enhances its restoration. In addition, the increased thickness of the IGZO channel ensures a sufficient number of electrons and channel space, which prevents electron depletion and results in outstanding endurance performance. In summary, utilizing AOS material with a simple elemental composition and a significant electron concentration can result in excellent endurance and reliability performance.

The results yield useful insights into the parameters that influence the stability of AOS-TFT and enhance comprehension of the materials. Furthermore, it indicates that ITO possesses the capability to be utilized in sophisticated applications.

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