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Reduction of Low Frequency Noise of Buried Channel PMOSFETs With Retrograde Counter Doping Profiles

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ABSTRACT The impacts of retrograde counter doping (RCD) profiles on low frequency noise (LFN) of buried channel (BC) PMOSFETs were investigated. RCD profiles were formed using heavy ion implantation. The RCD profile reduced LFN by more than 50%. The origin of LFN reduction in the RCD device was investigated using TCAD simulation. It was found that both RCD profile itself and the polarity of Si surface contributed to the deeper channel position and larger energy barrier between Si surface and channel position.

INDEX TERMS Buried channel, epitaxial, low frequency noise, PMOS, retrograde counter doping profile.

I. INTRODUCTION

Drain current (I_d) noise of MOSFETs is one of the critical problems in scaled logic LSI [1], analog LSI [2], [3], and memory devices [4]. Since I_d noise is induced by capture and emission of carriers at gate insulator/Si interfaces [5], [6], reduction of interface state density (N_{ss}) is effective to reduce I_d noise [7], [8], [9]. Recently, the concept of channel percolation has been proposed to understand the reliability of scaled devices based on device simulation [10], [11] and experiments using transient enhanced diffusion of channel dopants [12], [13], [14]. The degree of channel percolation can be modulated by random discrete doping [15], metal gate granularity [16], electric field concentration at active corner [11], and gate insulator/Si interface roughness [17], [18]. It has been reported that N_{ss} becomes larger as gate width (W_g) becomes narrower since the active corner region has higher N_{ss} than the channel center [14]. In simulation studies, it has been proposed that I_d noise can be suppressed using nonuniform doping profiles along W_g direction [19], [20]. By increasing threshold voltage (V_{th}) near the active corner where N_{ss} is higher than the channel center, channel is likely not to be formed near the active corner.

To separate the channel position from traps in the depth direction, buried channel (BC) structures are used in analog LSI such as CMOS image sensors [21]. I_d noise can be reduced as channel position becomes deeper [22]. However, V_{th} becomes lower as counter doping region becomes deeper [23]. The tradeoff between I_d noise and V_{th} makes it difficult to reduce I_d noise further by simply making the counter doping region deeper.

It has been reported that retrograde counter doping (RCD) profiles can provide the matched V_{th} with conventional counter doping profiles [24]. In the previous work, RCD profiles were fabricated using heavy ion implantation. The purpose was to make the counter doping region shallower for suppression of short channel effect in BC PMOSFETs [24]. However, the impacts of RCD profiles on channel position and low frequency noise (LFN) have not been reported.

In this study, BC PMOSFETs with RCD profiles were fabricated using heavy ion implantation. The impact of RCD profiles on LFN was experimentally investigated. Mechanism of LFN reduction by RCD profiles was investigated using TCAD simulation.

II. EXPERIMENTS

BC PMOSFETs with n^+-poly-Si gate electrodes were fabricated on p-type Si (100) wafers. Fig. 1 shows the process flow. After STI formation, phosphorus ions (P^+)

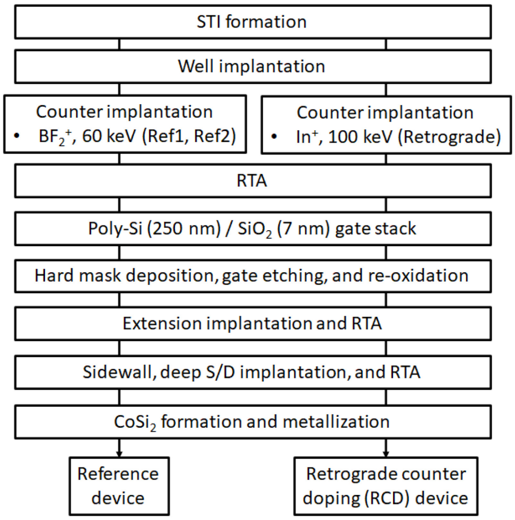

FIGURE 1. Process flow of the fabricated BC PMOSFETs.

were implanted into the well region with the acceleration energy of 140 keV. BF_2^+ ions were implanted into counter doping region of reference devices with two dose conditions (Ref1, Ref2). The acceleration energy was 60 keV. Indium ions (In^+) were implanted into counter doping region of RCD devices with the acceleration energy of 100 keV which was higher than the reference paper [24]. However, the final doping profiles were determined by the high thermal budget in gate stack formation to reduce N_{ss}. It is known that In^+ implantation induce kink in I_d – gate voltage (V_g) curves [24]. To suppress kink in I_d-V_g curves, low In^+ dose condition was used. Gate SiO_2 film was thermally grown at 800°C with the thickness of 7 nm. N^+-poly-Si gate thickness was 250 nm. LFN was evaluated using B1500A, E4727A (Keysight), and PA200 semiauto prober (Formfactor). All the measurements were carried out at room temperature. Since LFN has variation among the samples, median values were used for characterization [16], [25]. For TCAD simulation, Sentaurus tools (Synopsys) were used.

III. EXPERIMENTAL RESULTS

Fig. 2 shows simulated channel doping profiles. Although the polarity of Si surface of the reference devices was P-type, that of RCD device was N-type. Junction position between counter doping region and N-well region of RCD device was deeper than that of the reference devices.

N_{ss} was extracted from maximum absolute values of charge pumping current [26]. Fig. 3 shows measured N_{ss} values of BC PMOSFETs with different counter doping ions. Median values of 15 samples were plotted. N_{ss} values of the reference devices and RCD devices were 2.1×10^9 and 2.3×10^9 cm^{-2}, respectively. It was confirmed that channel dopants did not impact on N_{ss}. Fig. 4 shows measured I_d-V_g curves of BC PMOSFETs with channel doping profiles in Fig. 2. W_g was 10 μm. Gate length (L_g) was 0.4 μm. Drain voltage (V_d) was −1.5 V. Substrate voltage (V_{sub}) was 0 V. V_{th} values of Ref1, Ref2, and RCD devices were −0.97, −0.87, and −1.01 V, respectively. V_{th} of RCD device was almost the same with Ref1 device (lower BF_2^+ dose condition). Subthreshold swing (SS) of Ref1, Ref2, and RCD devices were 93, 97, and 118 mV/dec, respectively. RCD device showed the largest SS among the three devices although V_{th} of Ref2 device (higher BF_2^+ dose condition) was lower than that of RCD device. I_d values of Ref1, Ref2, and RCD devices were −1.88 mA, −2.05 mA, −1.86 mA, respectively at V_g=−3 V and V_d=−1.5 V. I_d of RCD device was also almost the same with that of Ref1 device.

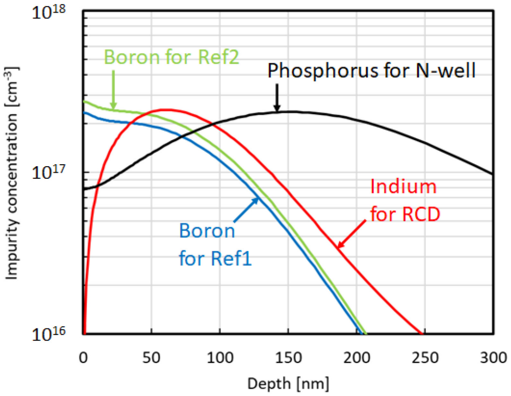

FIGURE 2. Simulated channel doping profiles for the fabricated devices. 0 nm is SiO_2/Si interface.

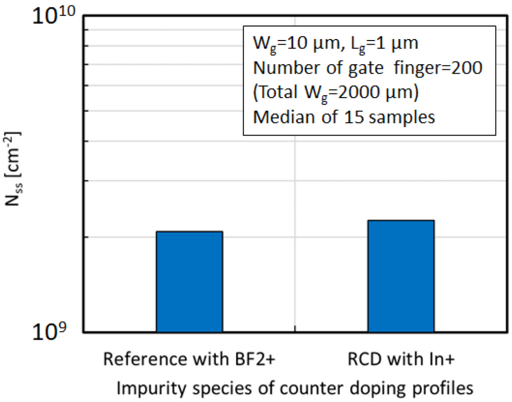

FIGURE 3. Measured N_{ss} values of BC PMOSFETs with different counter doping ions.

Fig. 5 shows simulation results of valence band energy along depth direction for BC PMOSFETs with channel doping profiles in Fig. 2. I_d was −1 μA. The valence band energy was extracted at the channel center. Although channel position of Ref1 device was almost at Si surface, channel positions of Ref2 and RCD devices were buried. RCD device showed the deepest channel position. It should be noted that channel position depends on bias condition [27]. Although the channel position of Ref1 device was almost at Si surface in Fig. 5, the channel position of Ref1 device can be buried with lower $|I_d|$ condition like Ref2 and RCD devices. It has been reported that SS becomes larger due to deeper

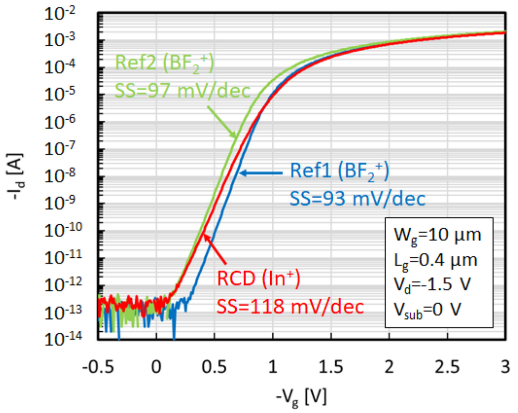

FIGURE 4. Measured I_d-V_g characteristics of BC PMOSFETs with channel doping profiles in Fig. 2.

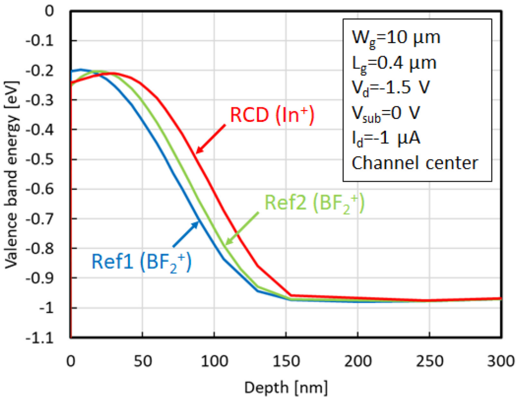

FIGURE 5. Valence band energy along depth direction for BC PMOSFETs with channel doping profiles in Fig. 2.

epitaxially grown counter doping region which makes gate capacitance smaller [23]. It was considered that the origin of larger SS for RCD device was the deeper channel position.

It has been reported that drain current noise (S_{Id}) depends on I_d [28]. According to the equations shown in [28], S_{Id} increases as I_d becomes larger. Therefore, lower V_{th} devices may show larger S_{Id} than higher V_{th} devices at the fixed V_g condition. However, it is accepted that lower V_{th} buried channel devices show lower noise than higher V_{th} devices [21], [22]. In realistic analog LSI applications such as source follower circuits, the devices are biased with current source components [21]. It is considered that S_{Id} dependences on I_d is more important than those on V_g from the viewpoint of realistic usage. Therefore, in this study, S_{Id} characteristics were compared at the fixed I_d conditions.

Fig. 6 shows measured drain current noise (S_{Id}) dependence on frequency (F) of BC PMOSFETs at $I_d=-1$ µA. V_d was -1.5 V. V_{sub} was 0 V. Median values of 255 samples were plotted. The sample size was chosen to be close to [25]. Median values of S_{Id} of Ref1, Ref2, and RCD devices were 2.9×10^{-23}, 2.1×10^{-23}, and 8.5×10^{-24} A^2/Hz, respectively. S_{Id} became lower as the channel position became deeper. RCD device showed more than 50% reduction of median S_{Id} compared with Ref1 device at F=100 Hz. Fig. 7 shows cumulative plots of S_{Id} at F=100 Hz in (a) log normal distribution plots and (b) Gumbel plots. It should be noted that the horizontal axis was log scale in Fig. 7. The plots in Fig. 7(a) were not straight lines. Although it has been reported that LFN characteristics follow log normal distribution [16], [29], the plots in Fig. 7(a) did not follow log normal distribution. Instead of log normal distribution plots, Gumbel plots are used for LFN and random telegraph noise (RTN) analysis [22], [25], [30], [31]. In Fig. 7(b), the

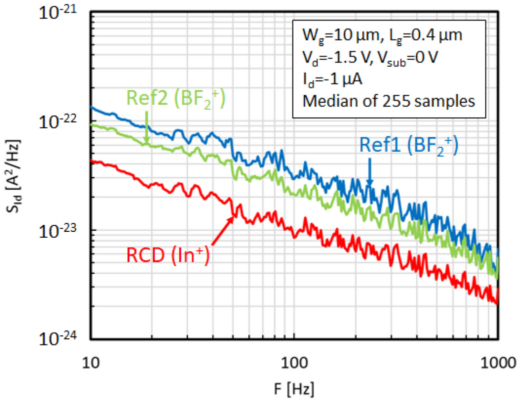

FIGURE 6. Measured S_{Id} dependences on F of BC PMOSFETs with channel doping profiles in Fig. 2. 255 samples were measured. I_d was -1 µA.

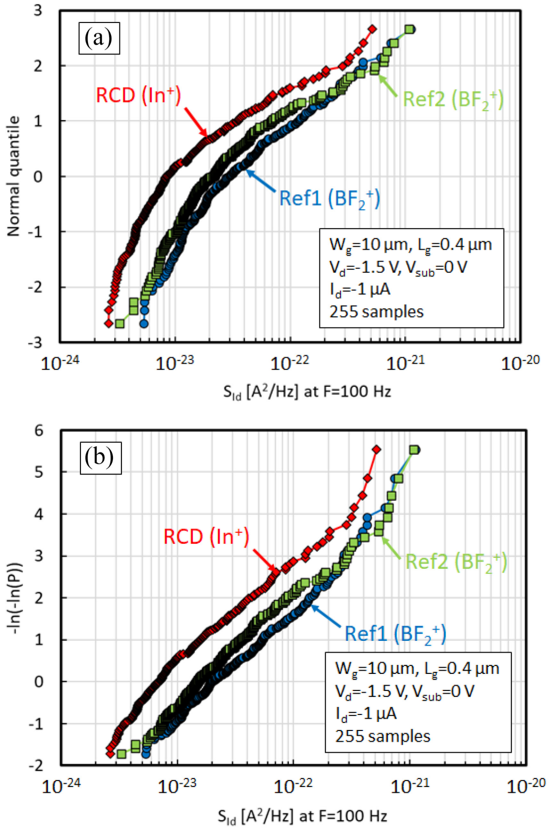

FIGURE 7. Measured cumulative plots of S_{Id} of BC PMOSFETs with channel doping profiles in Fig. 2. 255 samples were measured. F was 100 Hz. I_d was -1 µA. (a) Log normal plots and (b) Gumbel plots.

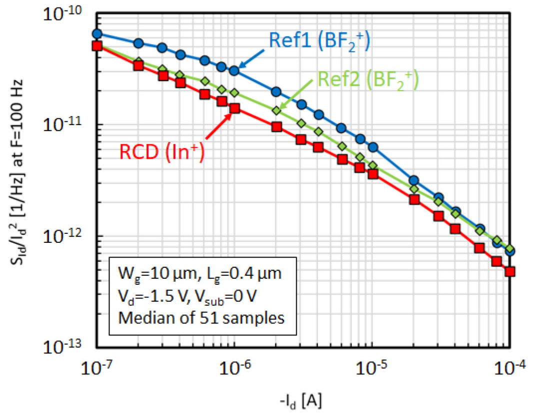

FIGURE 8. **Measurement results of normalized S_{Id} dependences on I_d of BC PMOSFETs with channel doping profiles in Fig. 2. 51 samples were measured. F was 100 Hz.**

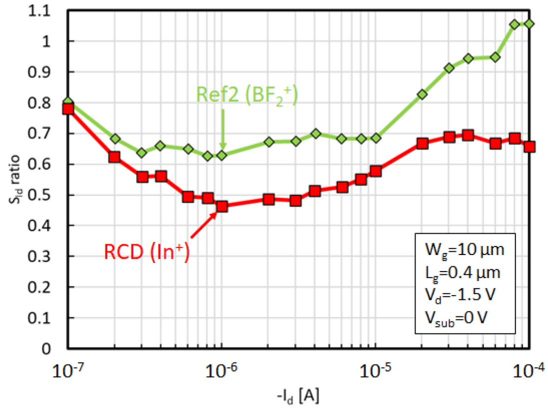

FIGURE 9. **S_{Id} ratio dependence on I_d. S_{Id} ratio was defined as S_{Id} of RCD or Ref2 device divided by S_{Id} of Ref1 device.**

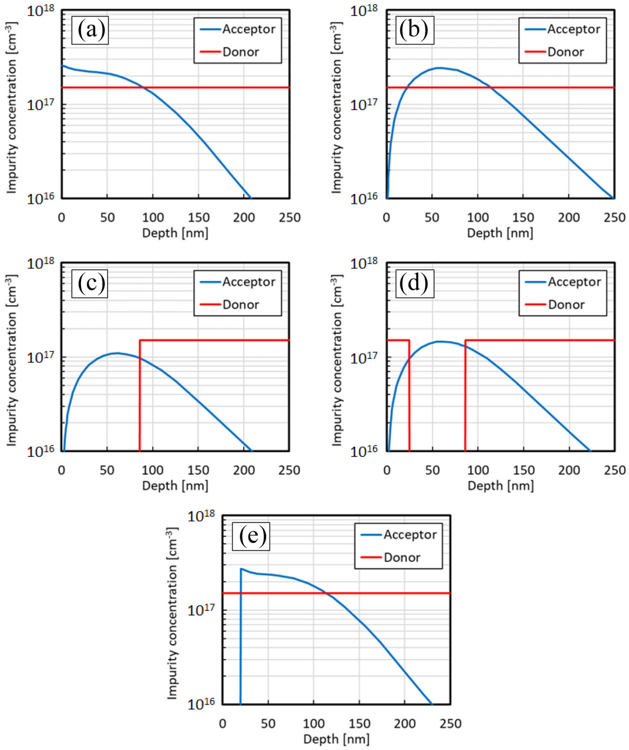

FIGURE 10. **Various channel doping profiles for BC PMOSFETs with n^+-poly-Si gate electrodes. The profiles were generated using TCAD structure editor tool. (a) Conventional, (b) RCD, (c) RCD+RW, (d) RCD+RW+NS, and (e) Conv+NS. 0 nm is SiO_2/Si interface.**

plots for all the samples were nearly straight lines up to -ln(-ln(P))∼4, where P is cumulative probability. Tails were not observed for all the samples. To discuss the impacts of channel doping profiles on the spread in detail, it is needed to increase sample size or measure smaller devices. Since it has been reported that deeper channel position makes RTN spread smaller [22], it is expected that RCD devices will show smaller spread of S_{Id} than the reference devices. Fig. 8 shows normalized S_{Id} dependence on I_d at F=100 Hz. I_d was controlled by V_g. Median values of 51 samples were plotted because 51 samples were enough to discuss the effect of the channel doping profiles on median of LFN. RCD device showed the lowest normalized S_{Id} for all measured I_d conditions. From these results, it was found that RCD profile can reduce LFN of BC PMOSFETs while suppressing V_{th} reduction. Fig. 9 shows S_{Id} ratio dependence on I_d. S_{Id} ratio was defined as median value of S_{Id} of RCD or Ref2 device divided by that of Ref1 device. S_{Id} ratio of RCD device depended on I_d. The reason can be understood as follows. The impact of RCD profiles became smaller as $|I_d|$ became lower than 1 μA since channel positions of both devices were buried. S_{Id} ratio became smallest near I_d=−1 μA. The impact of RCD profiles became largest near I_d=−1 μA because the channel position of Ref1 device was near SiO_2/Si interface whereas channel of RCD device was buried as shown in Fig. 5. As $|I_d|$ became higher, the channel positions of both devices approach to SiO_2/Si interface. The impact of RCD profiles became smaller in higher $|I_d|$ region. Although Ref2 device showed worse S_{Id} ratio than RCD device, Ref2 device showed the similar tendency with RCD device. S_{Id} ratio dependency of Ref2 device was also understood by the same reason with RCD device.

IV. DISCUSSION

In the previous section, it was found that LFN became lower as the degree of buried channel was enhanced. However, the origin of the enhancement of the degree of buried channel has not been clarified. To investigate the origin, various channel doping profiles were generated using TCAD structure editor tool. The degree of buried channel was investigated using TCAD device simulation. Fig. 10 shows the generated channel doping profiles for BC PMOSFETs with n^+-poly-Si gate electrodes. Figs. 10 (a), (b), (c), (d), (e) show Conventional, RCD, RCD+retrograde well (RW), RCD+RW+N-type surface (NS), conventional+NS (Conv+NS), respectively. It can be assumed that acceptor profiles of Figs. 10 (a) and (e) correspond to boron profiles while those of Figs. 10 (b), (c), and (d) correspond to indium profiles. The concentration of donor dopants (N-well

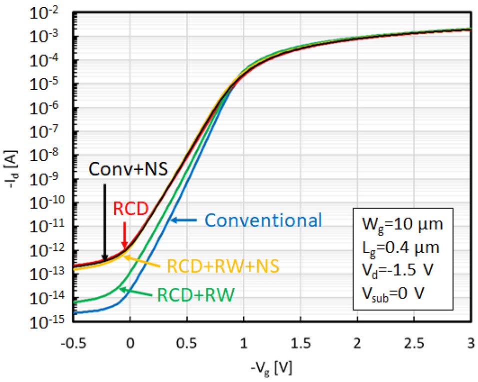

FIGURE 11. **Simulation results of I_d-V_g characteristics of BC PMOSFETs with channel doping profiles in Fig. 10.**

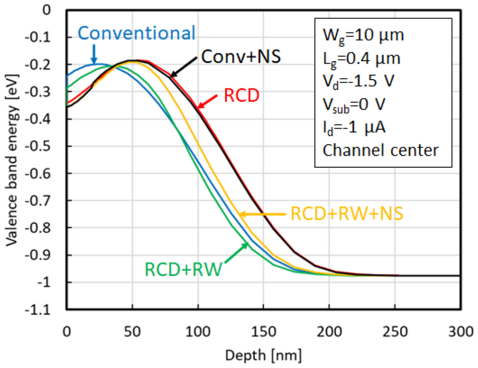

FIGURE 12. **Valence band energy along depth direction for BC PMOSFETs with channel doping profiles in Fig. 10.**

dopants) was 1.5×10^{17} cm^{-3}. The concentration of acceptor dopants (counter dopants) was tuned to match V_{th}. Counter doping region depth was 94, 118, 86, 86, and 118 nm for Figs. 10 (a), (b), (c), (d), and (e), respectively.

Fig. 11 shows simulated I_d-V_g characteristics of BC PMOSFETs with channel doping profiles in Fig. 10. It was found that RCD, RCD+RW+NS, and Conv+NS showed larger SS than Conventional and RCD+RW. Fig. 12 shows simulation results of valence band energy of BC PMOSFETs with channel doping profiles in Fig. 10. I_d was -1 μA. The degree of buried channel was enhanced in RCD, RCD+RW+NS, and Conv+NS. As shown in Figs. 4 and 5, the origin of larger SS in RCD, RCD+RW+NS, and Conv+NS was the deeper channel position.

To evaluate the degree of buried channel, channel depth and energy barrier were investigated. The definition of channel depth was the depth where valence band energy became maximum. The definition of energy barrier was the difference between valence band energy at SiO_2/Si interface and that at the channel depth. Fig. 13 shows channel depth dependence on counter doping region depth. RCD+RW showed deeper channel depth than Conventional although counter doping region depth of RCD+RW was shallower than that of Conventional. It was found that RCD increased channel depth. Furthermore, RCD+RW+NS and Conv+NS also showed deeper channel depth. It was found that polarity of Si surface also contributed to enhancement of channel depth. Fig. 14 shows energy barrier dependence on counter doping region depth. This result also suggested that energy barrier was enhanced by both RCD itself and polarity of Si surface. From these results, it was concluded that the origin of reduction of LFN using RCD profiles were RCD itself and polarity of Si surface.

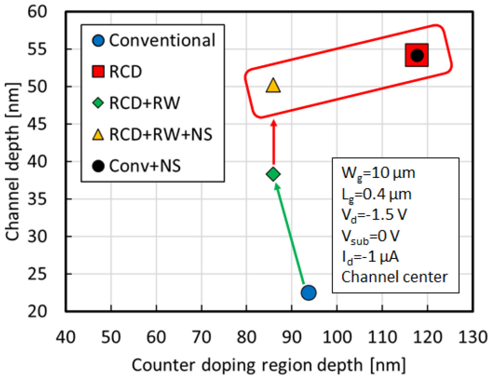

FIGURE 13. **Channel depth dependence on counter doping region depth for BC PMOSFETs with channel doping profiles in Fig. 10. Channel depth was extracted from Fig. 12.**

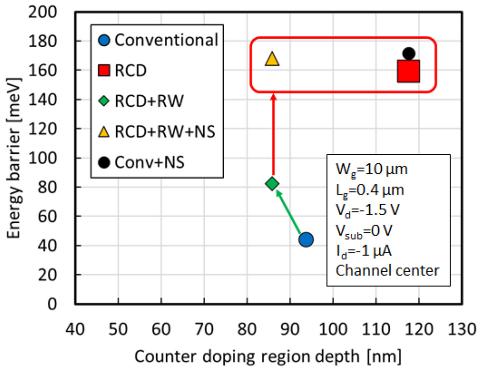

FIGURE 14. **Energy barrier dependence on counter doping region depth for BC PMOSFETs with channel doping profiles in Fig. 10. Energy barrier was extracted from Fig. 12.**

Since In^+ implantation may induce kink in I_d-V_g curves of BC PMOSFETs [24], B^+ or $BF_2{}^+$ implantation should be used for realistic applications. However, it is difficult to form RCD profiles (Fig. 10 (b)) using B^+ or $BF_2{}^+$ implantation. Therefore, Conv+NS (Fig. 10 (e)) will be one of the realistic approaches for reduction of LFN of BC PMOSFETs. It is considered that the doping profile can be fabricated as follow. After N-well region is formed, counter doping region should be formed with B^+ or $BF_2{}^+$ implantation. Then, N-type Si surface can be formed by epitaxial growth of Si film (doped Si film or undoped Si film with additional implantation). To suppress boron diffusion toward the epitaxial Si region, diffusion block layers using carbon [32] or oxygen atoms [33], [34], [35] which can trap interstitial Si atoms should be used before epitaxial Si growth. Although the diffusion block layers are used for surface channel devices in [32], [33], [34], [35], it is possible to apply the diffusion block layers to buried channel devices if channel and gate implantation conditions are modified. In this study, LFN reduction by RCD profiles was demonstrated at L_g=0.4 μm. In [22], RTN was reduced by buried channel structures at L_g=0.22 μm. Since LFN is the result of a superposition of RTN [36], it is expected that our findings will be effective to at least L_g=0.22 μm.

V. CONCLUSION

It was demonstrated that RCD profiles enhanced the degree of buried channel and reduced LFN of BC PMOSFETs by more than 50% while suppressing reduction of V_{th}. From TCAD simulation, it was found that both RCD itself and the polarity of Si surface contributed to the enhancement of the degree of buried channel. The findings in this study will be useful for design of low noise BC MOSFETs.

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REFERENCES

[1] T. Matsumoto, K. Kobayashi, and H. Onodera, "Impact of random telegraph noise on CMOS logic delay uncertainty under low voltage operation," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2012, pp. 581–584.

[2] X. Wang, P. R. Rao, A. Mierop, and A. J. P. Theuwissen, "Random telegraph signal in CMOS image sensor pixels," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2006, pp. 1–4.

[3] Y. Kikuchi et al., "Noise performance improvements of 2-layer transistor pixel stacked CMOS image sensor with non-doped pixel-FinFETs," in *Proc. IEEE Symp. VLSI Technol. Circuits*, 2023, pp. 1–2.

[4] S. Aritome, T. Takahashi, K. Mizoguchi, and K. Takeuchi, "RTN impact on data-retention failure/recovery in scaled (∼1Ynm) TLC NAND flash memories," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. PM-13.1–PM-13.4.

[5] H. E. Maes, S. H. Usmani, and G. Groeseneken, "Correlation between 1/f noise and interface state density at the Fermi level in field effect transistors," *J. Appl. Phys.*, vol. 57, no. 10, pp. 4811–4813, 1985.

[6] M. Toita, S. Sugawa, A. Teramoto, T. Akaboshi, H. Imai, and T. Ohmi, "1/f noise degradation caused by Fowler-Nordheim tunneling stress in MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2003, pp. 313–317.

[7] G. Kapila, N. Goyal, V. D. Maheta, C. Olsen, K. Ahmed, and S. Mahapatra, "A comprehensive study of flicker noise in plasma nitrided SiON p-MOSFETs: Process dependence of pre-existing and NBTI stress generated trap distribution profiles," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2008, pp. 1–4.

[8] S. Fujii et al., "Impacts of depth and lateral profiles of fluorine atoms in gate oxide films on reliability," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2021, pp. 1–5.

[9] S. Fujii, I. Maru, S. Morita, and T. Miyazaki, "Experimental analysis of process impacts on fluorine incorporated gate oxide film properties near gate edge region," in *Proc. IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, 2022, pp. 268–270.

[10] J. Franco et al., "Impact of individual charged gate-oxide defects on the entire I_D–$V_G$characteristic of nanoscaled FETs," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 779–781, Jun. 2012.

[11] Z. Zhang et al., "New approach for understanding 'random device physics' from channel percolation perspectives: Statistical simulations, key factors and experimental results," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2016, pp. 172–175.

[12] S. Fujii et al., "Analyzing the effects of boron transient enhanced diffusion on low frequency noise in NMOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. XT-3.1–XT-3.5.

[13] S. Fujii, I. Maru, S. Morita, and T. Miyazaki, "Experimental study on effects of boron transient enhanced diffusion on channel size dependences of low frequency noise in NMOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2019, pp. 1–5.

[14] S. Fujii, S. Morita, and T. Miyazaki, "Experimental understanding of the impact of channel percolation on low frequency noise using transient enhanced diffusion of channel dopants," in *Proc. IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, 2021, pp. 1–3.

[15] A. Ghetti, M. Bonanomi, C. M. Compagnoni, A. S. Spinelli, A. L. Lacaita, and A. Visconti, "Physical modeling of single-trap RTS statistical distribution in flash memories," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2008, pp. 610–615.

[16] T. Matsukawa et al., "Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2014, pp. 299–302.

[17] R. Kuroda, T. Suwa, A. Teramoto, R. Hasebe, S. Sugawa, and T. Ohmi, "Atomically flat silicon surface and silicon/insulator interface formation technologies for (100) surface orientation large-diameter wafers introducing high performance and low-noise metal–insulator–silicon FETs," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 291–298, Feb. 2009.

[18] R. Kuroda, A. Teramoto, and S. Sugawa, "Random telegraph noise measurement and analysis based on arrayed test circuit toward high S/N CMOS image sensors," in *Proc. IEEE Int. Conf. Microelectron. Test Struct. (ICMTS)*, 2016, pp. 46–51.

[19] A. Ghetti, S. M. Amoroso, A. Mauri, and C. M. Compagnoni, "Impact of nonuniform doping on random telegraph noise in flash memory devices," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 309–315, Feb. 2012.

[20] Y. Higashi et al., "Unified transient and frequency domain noise simulation for random telegraph noise and flicker noise using a physics-based model," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4197–4203, Dec. 2014.

[21] Y. Chen, X. Wang, A. J. Mierop, and A. J. P. Theuwissen, "A CMOS image sensor with in-pixel buried-channel source follower and optimized row selector," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2390–2397, Nov. 2009.

[22] A. Yonezawa, A. Teramoto, R. Kuroda, H. Suzuki, S. Sugawa, and T. Ohmi, "Statistical analysis of random telegraph noise reduction effect by separating channel from the interface," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2012, pp. 3B.5.1–3B.5.7.

[23] T. Ohguro et al., "0.15-μm buried-channel p-MOSFET's with ultrathin boron-doped epitaxial Si layer," *IEEE Trans. Electron Devices*, vol. 45, no. 3, pp. 717–721, Mar. 1998.

[24] I. C. Kizilyalli, F. A. Stevie, and J. D. Bude, "n^+-Polysilicon gate PMOSFET's with indium doped buried-channels," *IEEE Electron Device Lett.*, vol. 17, no. 2, pp. 46–49, Feb. 1996.

[25] M. Saitoh, K. Ota, C. Tanaka, and T. Numata, "Systematic understanding of channel-size dependence of low-frequency noise in 10nm-diameter tri-gate nanowire MOSFETs," in *Proc. Symp. VLSI Technol.*, 2013, pp. T228–T229.

[26] D. Okamoto, H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, "Analysis of anomalous charge-pumping characteristics on 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2013–2020, Aug. 2008.

[27] R. A. Wilcox, J. Chang, and C. R. Viswanathan, "Low-temperature characterization of buried-channel NMOST," *IEEE Trans. Electron Devices*, vol. 36, no. 8, pp. 1440–1447, Aug. 1989.

[28] P. Gaubert, A. Teramoto, W. Cheng, and T. Ohmi, "Relation between the mobility, 1/f noise, and channel direction in MOSFETs fabricated on (100) and (110) silicon-oriented wafers," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1597–1607, Jul. 2010.

[29] P. Srinivasan and S. Dey, "New and critical aspects of 1/f noise variability in advanced CMOS SoC technologies," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2012, pp. 458–461.

[30] N. Tega et al., "Anomalously large threshold voltage fluctuation by complex random telegraph signal in floating gate flash memory," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2006, pp. 1–4.

[31] K. Abe et al., "Random telegraph signal statistical analysis using a very large-scale array TEG with 1M MOSFETs," in *Proc. Symp. VLSI Technol.*, 2007, pp. 210–211.

[32] A. Hokazono et al., "25-nm gate length nMOSFET with steep channel profiles utilizing carbon-doped silicon layers (A P-type dopant confinement layer)," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1302–1310, May 2011.

[33] H. Takeuchi et al., "Punch-through stop doping profile control via interstitial trapping by oxygen-insertion silicon channel," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 481–486, 2018.

[34] D. Connelly et al., "Suppressing oxidation-enhanced diffusion of boron in silicon with oxygen-inserted layers," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1173–1178, 2018.

[35] S. Fujii et al., "Analysis of the effects of boron transient enhanced diffusion on threshold voltage mismatch in steep retrograde doping NMOSFETs with inserted oxygen layers," in *Proc. IEEE Int. Symp. Phys. Fail. Anal. Integr. Circuits (IPFA)*, 2020, pp. 1–4.

[36] M. J. Uren, D. J. Day, and M. J. Kirton, "1/f and random telegraph noise in silicon metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 47, no. 11, pp. 1195–1197, 1985.