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# Scaling Challenges of Nanosheet Field-Effect Transistors Into Sub-2 nm Nodes

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**ABSTRACT** The scaling of nanosheet (NS) field effect transistors (FETs) from the **12** nm gate length to the ultimate gate length of **10** nm for sub-2 nm nodes brings additional technological challenges. Here, 3D finite element Monte Carlo simulations are employed to explore how to alter the NS architecture to increase the drive current ($I_{DD}$) because the gate scaling to 10 nm results in a decline of the current (by **10.7**%). $I_{DD}$ of the **10** nm gate length NS FET will increase by **11**% if the maximum *n*-type source/drain doping reaches $1 \times 10^{20}$cm$^{-3}$, or increase by **3.8**% if the high-$\kappa$ dielectric layer equivalent oxide thickness (EOT) is less than **1.0** nm. The reduction in the channel width below **40** nm or the reduction in the channel thickness below **5** nm will substantially decrease $I_{DD}$. The sub-threshold figures of merit like the sub-threshold slope (SS) will decrease from **75** to **73** mV/dec, while the drain-induced barrier lowering (DIBL) will increase from **32** to **77** mV/V. Finally, the effect of strain to increase the drive current is strongly limited by quantum confinement. $I_{DD}$ will increase by **3**% and by **14**% in the 10 nm gate NS FET with the ⟨110⟩ and ⟨100⟩ channel orientations, respectively, when a strain of **0.5**% is applied to the channel, with a negligible increase for larger strain values (**0.7**% and **1.0**%).

**INDEX TERMS** Scaling, gate-all-around, nanosheet FET, 2 nm node, Monte Carlo.

## I. INTRODUCTION

Nanosheet field effect transistors (NS FETs) emerged as a winning transistor architecture [1] to continue the CMOS technology scaling at and beyond the 3 nm technology node. While FinFET dominated the CMOS technology from the 22 nm node to the 5 nm node [2], the architecture reached its end of life. The end of FinFETs is dictated by increased capacitance and external resistance imposed by the limits of fin scaling (fin height and separation) [3] and a larger dissipated power than the power dissipated by equivalent NS FETs [4].

To overcome the FinFET limitations, a gate-all-around (GAA) design is required to fully encompass the transistor channel by a gate [1]. The wide channel body of the NS provides a larger channel carrier mobility than that of nanowire FETs suffering from interface roughness-induced mobility degradation and the self-heating [4], [5]. The advantage of the NS architecture is an epitaxial fabrication [6] producing high-quality lateral interfaces which minimise the interface roughness-induced mobility reduction in the channel [7]. Furthermore, GAA transistors must be vertically stacked to create parallel channels [8] to provide the required drive current [9]. The GAA NS architecture thus delivers a large drive current and minimal variability in device characteristics [10], [11] leading to its acceptance for the chip mass production by Samsung (3 nm Process Technology) [12]. The drive current of 1082 $\mu$A/$\mu$m has been demonstrated at an overdrive of 0.7 V from the 12 nm gate length silicon NS FETs [6]. However, further scaling predicts a decline in the drive current and in the sub-threshold figures of merit (FoM) [13].

In this paper, the gate length is scaled from 12 nm to an ultimate 10 nm [9] to evaluate the impact of this scaling on the subsequent technology node aiming to manufacture denser transistors per chip area. The scaled, 10 nm gate length NS FET, schematically shown in Fig. 1, is studied

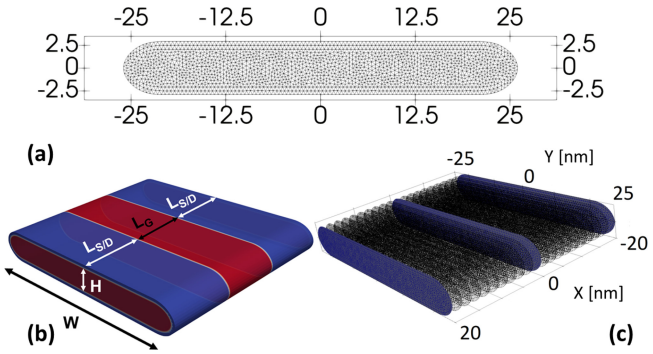


**FIGURE 1.** (a) A finite element mesh of the two-dimensional (2D) slice through the nanosheet (NS) channel for Schrödinger equation solutions. (b) A schematic 3D view of the device simulation domain with dimension parameters: a channel height (H) and width (W), a source/drain length ($L_{S/D}$), and a gate length ($L_G$). (c) A 3D representation of the nanosheet displaying the 2D slices utilised to solve the Schrödinger equation along the channel.

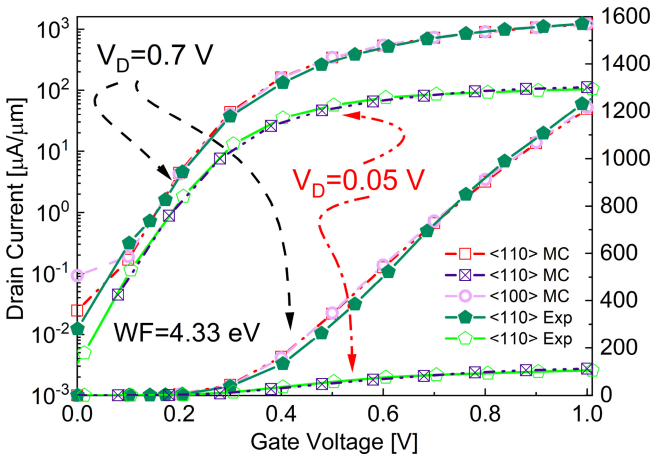


**FIGURE 2.** $I_D$-$V_G$ characteristics at low and high drain biases, obtained from the simulations (MC), for the 12 nm gate NS FET with the 5 nm thick and 50 nm wide channel in the ⟨110⟩ channel orientation NS FET (squares) compared against experimental data (Exp) [6] (diamonds) [27]. The ⟨100⟩ (circles) channel orientation of the 12 nm gate NS FET at $V_{D=0.7}$ V is simulated for comparison.

by using an in-house-developed, state-of-the-art 3D finite-element (FE) ensemble Monte Carlo (MC) device simulation toolbox VENDES [14]. The scaling study investigates how the decline in the device performance [15] might be avoided by changing the channel width, thickness, the high-$\kappa$ dielectric layer, doping profile, and strain; and how the device FoM like on-current, threshold voltage ($V_T$), sub-threshold slope (SS), and drain induced barrier lowering (DIBL) are affected with the variation in the NS architecture.

The paper is organised as follows: Section II details the FE MC & drift-diffusion (DD) simulations. Section III describes the scaling approach for the 10 nm gate GAA NS FET, and Section IV gives essential FoM. Section V summarises the main results of this work.

## II. MONTE CARLO SIMULATIONS BY VENDES

The VENDES toolbox uses a FE mesh to represent the real shape of NS FETs. Its MC and DD transport models incorporate 2D Schrödinger equation (SchE) based quantum corrections (QC) solved in cross-sections along the NS channel defined by a 2D FE mesh to accurately determine quantum-mechanical confinement in the channel [16], [17]. The VENDES' MC uses a non-parabolic and anisotropic band structure of Si with three valleys ($\Gamma$, $L$, and $X$), and includes all relevant-to Si electron scatterings with acoustic and non-polar optical (intra-valley & inter-valley) phonons [18], ionised impurities via the third-body exclusion [19], [20] and interface roughness (IR) using Ando's model [21]. The screening in the electron-ionised impurity scattering uses a static approximation [22] with a self-consistent calculation of Fermi energy ($E_F$) and electron temperature ($T_e$) from the average electron concentration and energy at electron position in the 3D device domain at each time step. The size of the S/D regions included in the simulation domain allows for an exact reproduction of the S/D resistance in the physically based 3D ensemble Monte Carlo technique. Therefore, the MC engine [23] will realistically simulate electron transport in the source/drain to obtain a drain current without adding contact resistances by data post-processing [21], [24], [25]. The effective electric field for the electron-IR scattering is also calculated at every electron position in 3D real-space. More details on the VENDES toolbox can be found in [17], [21], [26].

## III. SCALED NANOSHEET FET ARCHITECTURES

The scaling starts by verifying simulated $I_D$-$V_G$ characteristics of the 12 nm gate length GAA NS FETs for one nanosheet at low and high drain biases against experimental data [6] in Fig. 2 [27]. The drain current ($I_D$) of one nanosheet accounts for the average $I_D$ of the triple NS FETs used in the experimental work [6]. Note that the drain current ($I_D$) obtained from the MC simulations and experimental data are normalised by the respective channel perimeter. The transistor $n$-type S/D doping profile has to be extracted from experimental work using a reverse-engineering method [10], [11], [25], [28]. The device channel is assumed to have a uniform $p$-type doping of $1 \times 10^{15}$cm$^{-3}$, while the source/drain (S/D) regions are assumed to have an $n$-type Gaussian doping profile with a maximum concentration of $5 \times 10^{19}$cm$^{-3}$. This maximum doping concentration also considers the eventual access resistance present in the S/D, which remains uncertain for future technology nodes. Once the S/D doping profile is verified for the 12 nm gate length device [25], the same doping profile is assumed for the 10 nm gate length NS FET. This calibrated single-device doping profile represents an average from the triple nanosheet field effect transistor [6]. Fig. 2 also illustrates that the change of the channel orientation from ⟨110⟩ to ⟨100⟩ would increase the drain current negligibly compared to the original drain current of the NS FET with the ⟨110⟩ channel orientation. The underlying cause is the quantum-mechanical confinement that limits carrier

**TABLE 1. Dimensions and parameters for the 12 nm and the 10 nm gate NS FETs.**

| Device dimensions | | |
|---|---|---|
| Gate length ($L_G$) [nm] | 12 | 10 |
| S/D region length ($L_{S/D}$) [nm] | 14 | 14 |
| High-$\kappa$ thickness (EOT) [nm] | 1.5 (1) | 1.5 (1) |
| Channel thickness [nm] | 5 | $7 \rightarrow 5, 4, 3$ |
| Channel width [nm] | $50 \rightarrow 40, 30, 20$ | $50 \rightarrow 40, 30, 20$ |
| Channel orientation | $\langle 110 \rangle, \langle 100 \rangle$ | $\langle 110 \rangle$ |
| **Doping parameters** | | |
| Minimum $n$-type S/D [$cm^{-3}$] | $5 \times 10^{19}$ | |
| Maximum $n$-type S/D [$cm^{-3}$] | $1 \times 10^{20}$ | |
| Uniform $p$-type channel [$cm^{-3}$] | $1 \times 10^{15}$ | |

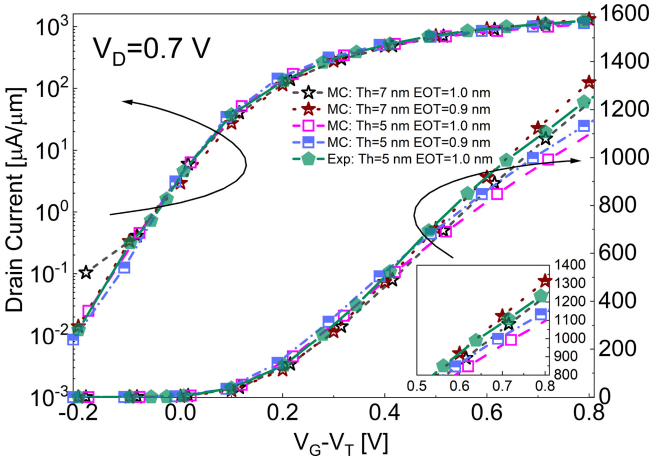


**FIGURE 3.** **$I_D$-($V_G$-$V_T$) characteristics for the 10 nm gate length NS FETs with two channel thicknesses (Th) of 5 nm and 7 nm in the ⟨110⟩ orientation at two equivalent oxide thicknesses (EOT) of 1.0 nm and 0.9 nm obtained from the simulations (MC). The gate workfuction (WF) of 4.33 eV is assumed to be the same in each NS FET. The experimental $I_D$-$V_G$ characteristics (Exp) of the 12 nm NS FET (green diamonds) [6] are shown for comparison.**

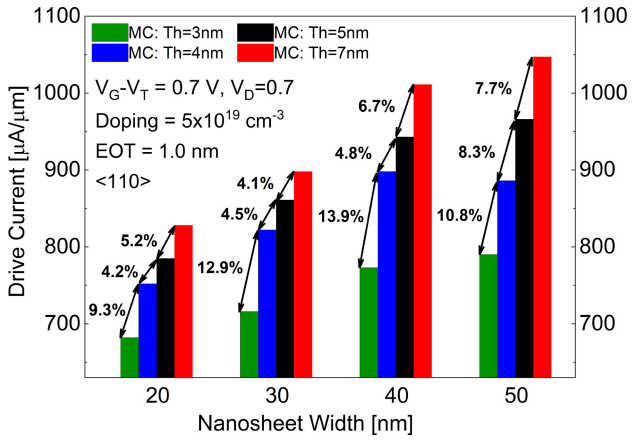


**FIGURE 4.** **The effect of varying the thickness (Th) on the drive current at $V_G - V_T = 0.7V$ and $V_D = 0.7V$ for the 10 nm gate length NS FETs with the <110> channel orientation when the width (W) of NS changes as the doping profile ($5 \times 10^{19} cm^3$) and EOT (1 nm) are kept fixed.**

mobility, which is observed in nanoscale devices along the ⟨100⟩ crystallographic orientation [29]. Furthermore, this negligible change is due to the strong quantum confinement of the channel in GAA architectures [30] and allows for seamless integration of the ⟨110⟩ $n$MOS with the ⟨110⟩ $p$MOS on a die. A subsequent scaling of the 12 nm gate length NS FET must be carried out with careful trade-offs in NS FET dimensions while increasing or preserving device performance. Therefore, the gate of 12 nm is scaled to 10 nm to assure only a small increase in the source-to-drain tunnelling [31]. Table 1 collects all device parameters used in the simulations of the scaled NS FET.

## IV. FIGURES OF MERIT FOR THE SCALED NS FETS

Fig. 3 shows simulated $I_D$-$V_G$ characteristics of the 10 nm gate length NS FETs at $V_D = 0.7$ V and the experimental data [6] of the 12 nm gate length NS FET for comparison. When the 12 nm gate length NS FET is scaled to the 10 nm gate length (keeping the 5 nm thick and 50 nm wide channel), the drive current ($I_{DD}$) will decrease by 10.7% at $V_G$-$V_T$ = 0.7 V and $V_D$ = 0.7 V. The current decrease starts at a relatively large gate bias of $V_G$-$V_T \geq 0.4$ V. The reason for the $I_{DD}$ reduction despite the gate length scaling to 10 nm is as follows: The primary reason for the increase of the drive current when the gate length is scaled down is an increase in the average carrier velocity along the channel. This increase does not occur in the 10 nm gate length NS FET. We conduct an analysis of the electron velocity, plotted in Figs. 7 and 8, along the channel of NS FETs later. Additionally to the limited electron velocity, the number of electrons injected from the source is reduced due to the effect of Fermi-Dirac statistics in the $n$-type doped source/drain as the electric field increases due to the gate scaling. The kinetic energy of electrons thus increases as the electrons are more accelerated by this increased electric field. This reduction in the injection of electrons will reduce the overall electron density in the channel which leads to the reduction in the drive current in the 10 nm NS FET.

When the channel thickness is increased to 7 nm (for 10 nm gate length), keeping the EOT equivalent to 1.0 nm, the drain current decreases only 3% when compared to the 12 nm gate length device. However, this will result in a larger off current ($I_{OFF}$) because the channel with this thickness will have a weaker quantum confinement. The effective oxide thickness (EOT) can be also further reduced from 1.0 nm to 0.9 nm by replacing $HfO_2$ with $HfLaO_x$ [32] or so. $I_{DD}$ will then increase from 1082 $\mu$A/$\mu$m (for 12 nm gate length) to 1123 $\mu$A/$\mu$m (for 10 nm gate length), by 3.8% (at the 7 nm channel thickness). While the $I_{DD}$ shows a slight increase (at the 5 nm channel thickness) to 1015 $\mu$A/$\mu$m when the EOT of 0.9 nm is deployed (less by 6.2% compared to the 12 nm gate length). To further increase the drain current, the EOT can be reduced to as low as 0.8 nm [33].

The channel variations of the 10 nm gate length NS FET in the thickness and width, and the reduction in the EOT from 1.0 nm to 0.9 nm, are plotted in Figs. 4 and 5 showing the MC simulated drive current ($I_{DD}$). When the thickness of the 50 nm-width channel is reduced from 5 nm to 4 nm and 3 nm, $I_{DD}$ is significantly reduced by 8.3% and 10.8%, respectively [34]. However, a reduction in the channel width

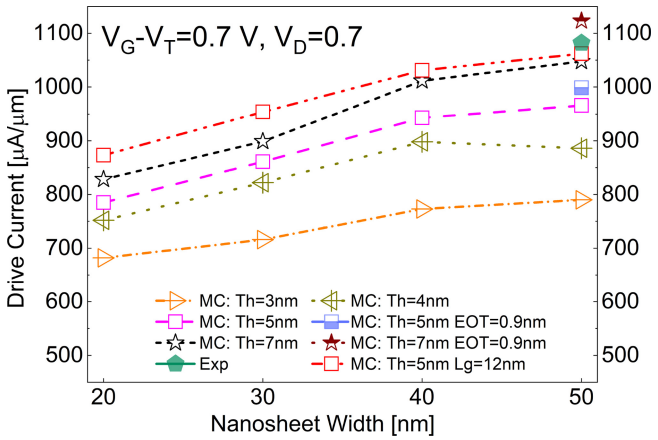


**FIGURE 5.** Simulated (MC) drive current at $V_G$-$V_T$ = 0.7 V and $V_D$=0.7 V versus the NS width with variable NS thicknesses (Th) of 7 nm, 5 nm, 4 nm, and 3 nm for the 10 nm gate NS FETs with the ⟨110⟩ channel orientation. The simulated (MC) and experimental (Exp) data for the 12 nm gate NS FET are included for comparison.

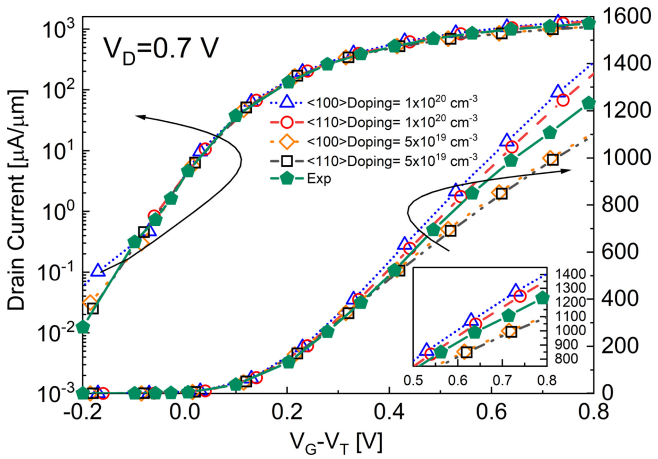


**FIGURE 6.** $I_D$-($V_G$-$V_T$) characteristics at $V_D$ = 0.7 V for the 10 nm gate length, 50 nm wide channel NS FETs in the ⟨110⟩ and ⟨100⟩ orientation obtained from the simulations (MC) for two maximum doping concentrations in the S/D. The experimental data (Exp) are also shown for comparison.

from 50 nm to 40 nm, allowing for a denser transistor integration, will not reduce $I_{DD}$ substantially (2.3%). But if the channel width is decreased further to 30 nm and 20 nm, $I_{DD}$ reduces by 10.8% and 18.7%, respectively. The $I_{DD}$ reduction is due to the decrease in electron density of the channel and electron mobility degradation from the increased interface roughness scattering. This behaviour was also reported in FinFETs [5]. However, an improved gate control and less short-channel effects are achieved by a stronger quantum confinement as the channel thickness decreases. Consequently, an improved $I_{ON}/I_{OFF}$ ratio can be obtained but these smaller channel thicknesses lower $I_{ON}$ substantially.

Fig. 6 illustrates the effect of increasing the doping concentration on the drain current [25]. An increase of 17% in the drive current is observed when the maximum *n*-type

**TABLE 2.** Sub-threshold characteristics for the 10 nm gate NS FETs. The sub-threshold slope (SS) is shown at $V_D$ = 0.05 V (low) and 0.7 V (high).

| | | | | |
|---|---|---|---|---|
| 10 nm Gate length - Channel thickness of 5 nm | | | | |
| Channel width [nm] | 50 | 40 | 30 | 20 |
| Perimeter [nm] | 110 | 90 | 70 | 50 |
| $SS^{low}$ [mV/dec] | 75 | 75 | 74 | 73 |
| $SS^{high}$ [mV/dec] | 73 | 80 | 77 | 75 |
| DIBL [mV/V] | 77 | 78 | 86 | 85 |
| $I_{DD}$ [$\mu A/\mu m$] | 966 | 943 | 861 | 785 |
| $I_{OFF}$ [$nA/\mu m$] | 68 | 67 | 52 | 40 |
| $I_{DD}/I_{OFF}$ ($\times 10^5$) | 0.14 | 0.14 | 0.17 | 0.20 |
| 10 nm Gate length - Channel thickness of 4 nm | | | | |
| Channel width [nm] | 50 | 40 | 30 | 20 |
| Perimeter [nm] | 108 | 88 | 68 | 48 |
| $SS^{low}$ [mV/dec] | 70 | 70 | 70 | 69 |
| $SS^{high}$ [mV/dec] | 71 | 71 | 70 | 70 |
| DIBL [mV/V] | 58 | 60 | 69 | 67 |
| $I_{DD}$ [$\mu A/\mu m$] | 886 | 898 | 822 | 752 |
| $I_{OFF}$ [$nA/\mu m$] | 8 | 7 | 6 | 5 |
| $I_{DD}/I_{OFF}$ ($\times 10^5$) | 1.17 | 1.21 | 1.49 | 1.42 |
| 10 nm Gate length - Channel thickness of 3 nm | | | | |
| Channel width [nm] | 50 | 40 | 30 | 20 |
| Perimeter [nm] | 106 | 86 | 66 | 46 |
| $SS^{low}$ [mV/dec] | 66 | 67 | 66 | 66 |
| $SS^{high}$ [mV/dec] | 67 | 67 | 66 | 66 |
| DIBL [mV/V] | 45 | 40 | 38 | 40 |
| $I_{DD}$ [$\mu A/\mu m$] | 790 | 773 | 716 | 682 |
| $I_{OFF}$ [$nA/\mu m$] | 0.39 | 0.33 | 0.35 | 0.42 |
| $I_{DD}/I_{OFF}$ ($\times 10^5$) | 20.0 | 22.9 | 20.3 | 16.0 |

S/D doping concentration is increased from $5 \times 10^{19}$cm$^{-3}$ to $1 \times 10^{20}$cm$^{-3}$. This maximum doping concentration increase in the 10 nm gate length device results in the 11% increase in $I_{DD}$ when compared to the 12 nm gate length NS FET [6].

Table 2 collects FoM for the 10 nm gate NS FETs with different channel thicknesses and widths. The SS practically does not change with the width decrease from 50 nm to 20 nm and at smaller channel thicknesses of 4 nm and 3 nm due to the strong quantum confinement. The DIBL in the 10 nm gate NS FET increases to 77 mV/V compared to the DIBL of 32 mV/V in the 12 nm gate FET obtained from the $I_D$-$V_G$ characteristics of [6]. The DIBL increase is caused by the increase in fringing electric fields under the gate [35] as the gate length of 12 nm is shortened to 10 nm. The reductions in the NS cross-section width (50 nm → 20 nm) will slightly increase the DIBL (from 77/58 mV/V to 85/67 mV/V) in the 5/4 nm thick NSs because the impact of interface roughness on the channel transport increases. The narrower NS width leads to an increase in the electron scattering with interface roughness [36] because of its exponential spatial dependency from the interface. As the NS width becomes smaller, the electrons at large kinetic energies (when a high drain bias is applied) will be confined into a narrower channel of 30 nm and 20 nm increasing the effect of quantum capacitance on the threshold voltage, especially at the high drain bias. The impact of interface roughness on the channel diminishes as the channel thickness decreases, mainly due to stronger quantum confinement. As the channel thickness is reduced to 4 nm and further to 3 nm, the quantum confinement intensifies further, resulting in an enhanced gate control.

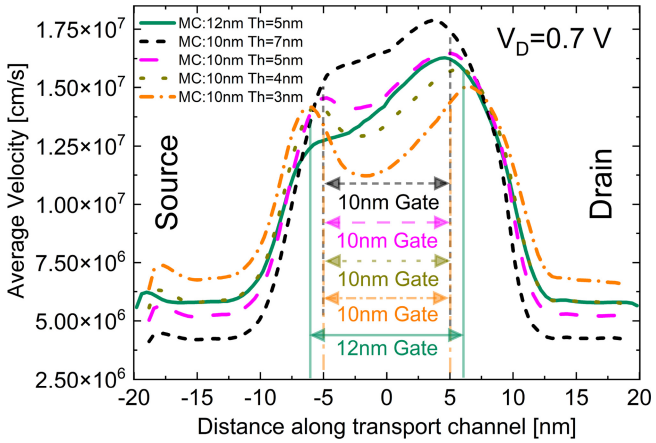


**FIGURE 7.** Average electron velocity along the 12/10 nm gate length, 50 nm wide channel NS FETs in the ⟨110⟩ orientation for different NS thicknesses at $V_G$-$V_T$ = 0.7 V and $V_D$ = 0.7 V obtained from the MC simulations. The arrows indicate the gate length.

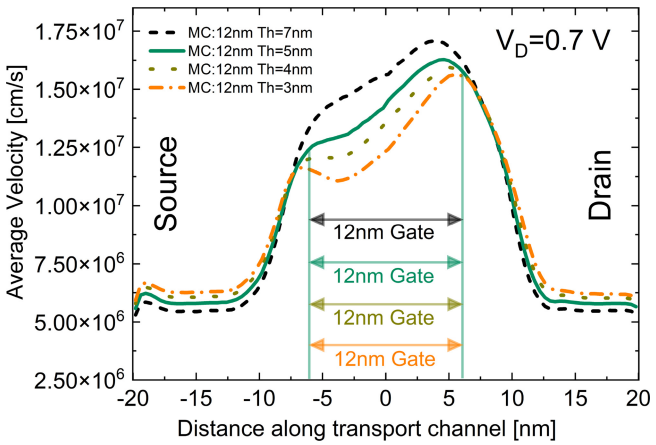


**FIGURE 8.** Average electron velocity along the 12 nm gate length, 50 nm wide channel NS FETs in the ⟨110⟩ orientation for different NS thicknesses at $V_G$-$V_T$ = 0.7 V and $V_D$ = 0.7 V obtained from the MC simulations. The arrows indicate the gate length.

Consequently, the DIBL in NS FETs with reduced channel thickness shows a slight decrease, dropping from 45 mV/V to 40 mV/V. While the decrease in the channel width and thickness reduces the drive current ($I_{DD}$), the off-current ($I_{OFF}$) lowers since the quantum-mechanical confinement becomes stronger, resulting also in an improved on-off ratio ($I_{DD}/I_{OFF}$).

Fig. 7 shows that the peak average electron velocity in the scaled 10 nm gate NS FETs substantially increases only in the 7 nm thick channel to $1.78 \times 10^7$ cm/s, 8.5% increase from its peak value of $1.62 \times 10^7$ cm/s in the 12 nm gate NS FET. When the channel thickness is 5 nm, the increase in the peak electron velocity in the scaled 10 nm gate NS FETs is negligible, and when the channel thickness is reduced below 5 nm, the peak average electron velocity decreases. These reductions in the peak electron velocity in the narrow channel thicknesses are due to the increased electron scattering with interface roughness as the channel thickness is reduced from 7 nm to 3 nm. The gate scaling from the 12 nm gate to the 10 nm one will also increase fringing electric fields beneath the gate. This large fringing electric field will accelerate electrons resulting in the increase of their velocity by about 20.6% at the source side of the gate. However, at the same time, strong electron-phonon interaction with acoustic and non-polar optical phonons governing the transport at large electron kinetic energies in Si [37] is limiting the velocity increase. The additional interface roughness scattering will further limit the electron transport in very narrow channels.

Fig. 8 presents the average velocity along the channel of the 12 nm gate length NS FET with varying thicknesses (ranging from 7 nm to 3 nm) in the ⟨110⟩ orientation at $V_G$-$V_T$ = 0.7 V and $V_D$ = 0.7 V, with a 50 nm width NS. The 7 nm thickness exhibits a higher velocity peak compared to other thicknesses, attributed to its less frequent electron scattering with interface roughness. Together with a larger carrier density this results in a higher drain current. However, this thickness suffers from weaker quantum confinement and electrostatic integrity, leading to the increased OFF current, thereby raising power consumption and heat dissipation in the logical circuits. Conversely, the average velocity peak decreases with thinner thicknesses such as 4 nm and 3 nm, exhibiting similar behaviour to the 10 nm gate length with 4 nm and 3 nm thicknesses (see Fig. 7).

**TABLE 3.** Energy-edge shifts for Si Δ-valleys along the *x*-, *y*- and *z*-k-space directions for increasing strengths of tensile strain and for two channel orientations [38].

| Strain | Uniaxial ⟨100⟩ | | | Uniaxial ⟨110⟩ | | |
|---|---|---|---|---|---|---|
| Strength | 0.5% | 0.7% | 1.0% | 0.5% | 0.7% | 1.0% |
| $\Delta_x$ [eV] | +0.03 | +0.042 | +0.06 | -0.01 | -0.014 | -0.02 |
| $\Delta_y$ [eV] | -0.045 | -0.063 | -0.09 | -0.01 | -0.014 | -0.02 |
| $\Delta_z$ [eV] | -0.045 | -0.063 | -0.09 | -0.065 | -0.091 | -0.13 |

Finally, we investigate the effect of strain in the Si channel which might be induced by using SiGe sacrificial layers [39]. A combination of quantum-mechanical confinement and strain has the potential to boost device performance to its optimum level even at the small nanoscale dimensions [40], [41], [42], even though, as we show, the effect of the strain is quite limited [43]. The effect of strain is modelled by lifting the Si conduction valleys by $\Delta E_C$ according to the strain type and the strain strength [38], [44] as collected in Table 3. When the uniaxial strain is applied to the ⟨110⟩ channel orientation, we also account for the split of transverse effective masses ($m_t$) in $\Delta_z$ valley caused by a bandstructure warping, leading to a lighter $m_t$ in the transport direction [38]. We investigate the effect of strain in both ⟨110⟩ and the ⟨100⟩ channel orientations since the strain impact on the drive current is very different compared to the negligible difference of drive currents obtained from the ⟨110⟩ and the ⟨100⟩ channels with no strain applied as shown in Fig. 2.

The simulated $I_D$-$V_G$ characteristics (plotted against $V_G$-$V_T$ to make a straightforward comparison due to shifts in $V_T$) are collected in Fig. 9 for the ⟨110⟩ channel NS FETs.

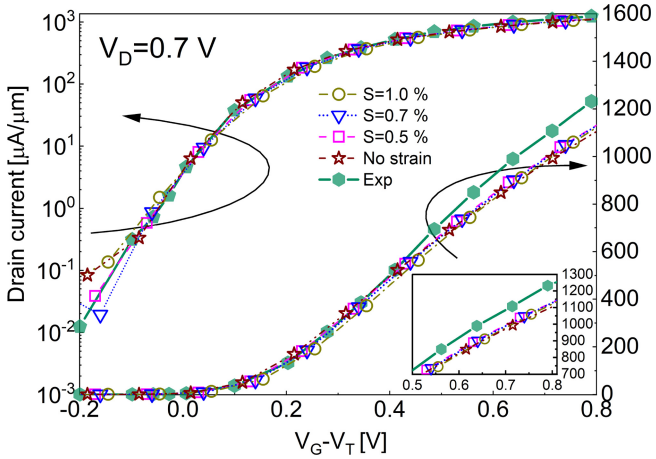


**FIGURE 9.** $I_D$-($V_G$-$V_T$) characteristics versus $V_G$-$V_T$ at $V_D$ = 0.7 V in the ⟨110⟩ channel orientation showing the effect of strain applied in the channel of the 10 nm gate length, 5 nm of thick and 50 nm wide channel NS FETs. The gate workfunction (WF) of 4.33 eV assumes the same gate stack is used in every NS FET.

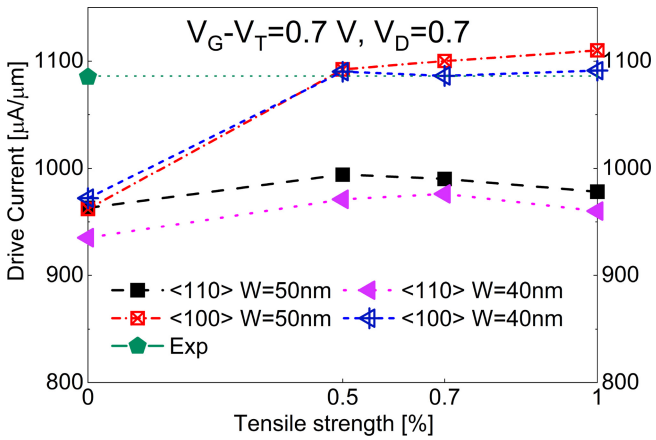


**FIGURE 10.** Simulated (MC) drive current at $V_G$-$V_T$ = 0.7 V and $V_D$ = 0.7 V in the ⟨100⟩ and the ⟨110⟩ channel orientations showing the effect of strain for the 10 nm gate length NS FETs with a fixed thickness of 5 nm and for two widths (W) of 50 nm and 40 nm. The experimental data (Exp) are again shown for comparison.

The limited effect of strain is illustrated in Fig. 10 which shows the drive current $I_{DD}$ versus applied strain for two significant NS channel widths and two channel orientations. While the channel orientation has a negligible effect on the drive current in the 50 nm wide channels with no strain applied, the strain will impact the ⟨100⟩ channel orientation NS FETs more than the ⟨110⟩ channel orientation devices as shown in Fig. 10. When the 0.5% strain is applied to the channel, the drive current $I_{DD}$ increases by 14% for the ⟨100⟩ orientation and by only 3% for the ⟨110⟩ orientation. The impact of strain above 0.5% is strongly limited by the quantum-mechanical confinement [44], [45] in the devices with the ⟨100⟩ channel orientation and even eliminated in the ⟨110⟩ orientation. The limitation and the elimination are larger in the narrower, 40 nm width NS channel due to a stronger quantum confinement.

## V. CONCLUSION

Scaling challenges of the 12 nm gate length Si NS FETs to an ultimate gate length of 10 nm have been thoroughly investigated by a 3D FE MC simulation toolbox with 2D FE SchE QCs. When the gate length is scaled down to 10 nm, the normalised-to-perimeter drive current ($I_{DD}$) will decline by 10.7%. The NS FET architecture must be modified to maintain or increase $I_{DD}$ using two possible strategies. One option is to increase the maximum *n*-type source/drain doping to $1 \times 10^{20}$cm$^{-3}$ or more [25], that will increase $I_{DD}$ by 11%. Another option is to reduce the EOT at least to 0.9 nm, increasing $I_{DD}$ by 3.8% (compared to the 12 nm gate length NS FET). The SS of the 10 nm gate length scaled device will slightly improve from 75 to 73 mV/dec at a high drain bias but the DIBL worsens from 32 mV/V to 77 mV/V. While the channel thickness has to stay at least at 5 nm, the channel width can be decreased from 50 nm to 40 nm, but further decrease will substantially deteriorate $I_{DD}$.

The effect of uniaxial strain applied to the channel in order to increase $I_{DD}$ is strongly limited by quantum-mechanical confinement. $I_{DD}$ will increase only by 3% in the NS FET with the ⟨110⟩ channel orientation and by 14% in the ⟨100⟩ channel orientation when a strain of 0.5% is applied. However, any further increase of strain to 0.7% or 1.0% results in a negligible increase in the drive current. The scaled 10 nm gate GAA NS FETs deliver the needed performance, but a larger increase in $I_{DD}$ has to be achieved by replacing the Si channel with a SiGe channel.

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