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Partially Isolated Dual Work Function Gate IGZO TFT With Obviously Reduced Leakage Current for 3D DRAMs

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ABSTRACT In this article, a partially isolated dual work function (PIDWF) gate In-Ga-Zn-O (IGZO) thin-film transistor (TFT) is proposed to reduce the off-state current (I_{off}) obviously, which also provides a feasible integration method for stacking IGZO TFT on Si-based devices. It is found that compared with the general back gate IGZO TFT structure, the I_{off} of the proposed IGZO TFT reduces from 2.57×10^{-14}A/μm to 7.57×10^{-16} A/μm, achieving two orders of magnitude improvement. This breakthrough has the potential to increase the retention time of DRAM applications by nearly 100 times. Moreover, the pronounced novel structure has mitigated parasitic capacitance, thereby leading to a notable 47.7% reduction in write latency within dynamic-random-access-memory (DRAM) circuits. The relevant operation mechanism is carefully demonstrated and verified by the simulation of the electric field and potential barrier results by technical computer-aided design (TCAD). Furthermore, the impacts of the dual gate work function level, the length, and the type of isolation dielectric between dual work function gates are systematically investigated. The results show that the off-state leakage is further reduced by increasing the difference of the work function levels between in dual gates, the dielectric length (L_D) and using the isolation layer with a lower dielectric constant. The PIDWF gate IGZO TFT exhibits scalability and is capable of achieving an 84.6% reduction in leakage current even with ultra-short channel lengths, which offers a promising application for future 3D DRAM applications with little extra cost.

INDEX TERMS Dual work function gate, In-Ga-Zn-O (IGZO) thin-fifilm transistor (TFT), isolation dielectric, off-state current (I_{off}), partially isolated.

I. INTRODUCTION

Artificial Intelligence (AI) and Machine Learning (ML) applied to visual recognition, natural language processing, self-driving vehicles, and prediction need strong hardware system supporting with numerous dynamic random access memory (DRAM) storages packaged on arithmetic-logic units (ALUs) [1], [2]. However, the data transfer bandwidth and speed between the memory and the ALU have become a bottleneck in the hardware systems [3]. Stacking the random dynamic memory on the logic unit with a sequential 3-D integration for forming 3D embedded DRAM (3D eDRAM) may avoid inter-chip propagation delays and expand the bandwidth for a great promotion on the AI calculation performance and efficiency [4], [5]. For eDRAM, it always suffers from the challenge of short retention times, resulting in a high refresh power consumption and then whole

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performance degradation of the overall AI system. Therefore, improving eDRAM cell retention time and operating speed through revolutionary 3D processes and device structure obtains widespread attention [6], [7].

Since In-Ga-Zn-O (IGZO) thin-film transistors (TFTs) show extremely low off-state current (I_{off}), low-thermal process-integration budget and excellent BEOL compatibility [8], [9], it becomes one of the most promising candidates for 3D eDRAM toward the realization of high-performance AI system. Regarding the application of IGZO-based eDRAM, there are 1T1C or 2T0C storage cell structures, both requiring ultra-low off-state current in the devices for achieving a long memory retention time. In recent years, the thermal annealing process is often used to reduce the leakage current of IGZO TFTs [10]. However, the approach of thermal annealing has reached its limits in further decreasing leakage due to the inherited film and interface defect reasons [11]. Especially for sequential 3-D integration in 3D eDRAM, the thermal annealing process introduces an extra thermal budget, which may take a side effect to the bottom devices [12]. Meanwhile, it often causes an unpredictable threshold voltage (V_{th}) shift in the IGZO TFTs [16], [17] and makes the threshold matching between the top-tier devices and the bottom-tier devices turn worse. In addition, recent reports have shown some structure innovations in IGZO devices for less channel leakages. However, the proposed structure and fabrication process is relatively complex and incompatible with sequential 3-D integration. In addition, the large size of IGZO devices and the source-drain overlap contribute to the issue of low integration density. To address the size compatibility challenge between IGZO and GAA devices, significant efforts have been directed towards the development and fabrication of IGZO devices with ultra-short channel. There are currently studies showing that IGZO has the ability to shrink in size [18], [19]. However, the electric field in the channel of these miniature IGZO TFTs is significantly intensified, complicating the optimization of such small devices. Due to the lower leakage of IGZO TFTs compared to GAA FETs, stacking them on top of GAA devices has been investigated to have advantages in circuit structure [20]. Furthermore, IGZO TFTs have lower process temperatures than GAA FETs, which makes IGZO devices more suitable for multilayer stacking to increase device integration density, yet the thermal budget required for extreme multilayer stacking remains a considerable challenge. Therefore, the more advanced structure suitable for the 3D eDRAM application with less additional thermal budget is needed in development [21].

In this article, a partially isolated dual work function (PIDWF) gate IGZO TFT is proposed for the first time to reduce the leakage in a large extent with the simple integration process. Through the help of technical computer-aided design (TCAD) simulation, the reductions of the transistor leakages with the segmented bottom gate-electrode with different work function levels in different gate sections are systematically explored. The critical process and structure parameters impacting on the electrical properties are extracted and one transistor leakage lowering model induced by overlapped gate work function control is proposed. With the indication of the model, a novel partially isolated dual work function gate IGZO TFT with more feasible process flow under a low thermal budget is designed, which shows a further two orders of magnitude decrease than general back gate TFTs. With optimized gate work function, partially isolated length, and dielectric constant, the devices may obtain further reduction of the leakage for better 3D eDRAM applications.

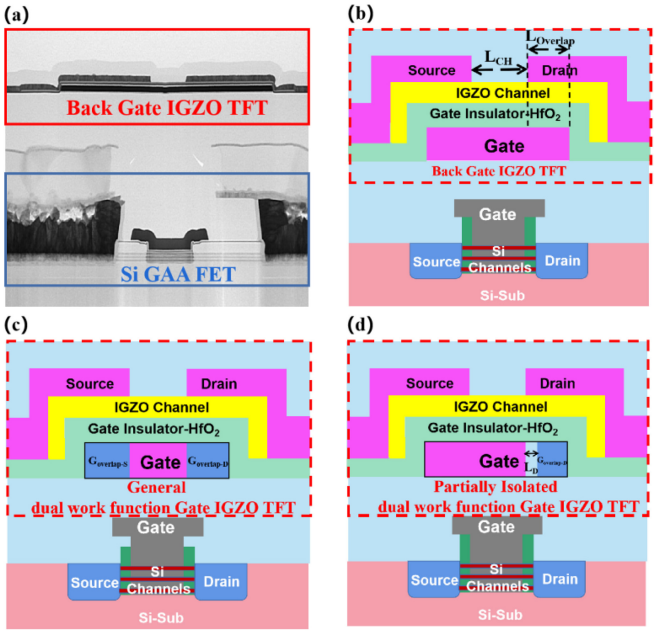

FIGURE 1. (a) The experimental image of the back gate IGZO TFT sequential heterogeneous 3D integration on Si gate-all-around (GAA) FET MOSFET for 3D eDRAM application and the schematic of (b) the regular back gate IGZO TFT as a top tier device, (c) the general dual work function gate IGZO TFT, and (d) partially isolated dual work function (PIDWF) gate IGZO TFT.

II. DEVICE DESIGN AND SIMULATION

A. DEVICE STRUCTURES

Fig. 1 (a) demonstrates the application of IGZO TFT stacking on bottom Si-based MOSFET for potential 3D eDRAM integrations. Experimental data obtained from the top-layer IGZO TFT with conventional structures were utilized to calibrate the simulation results for more meaningful simulation and design investigations. Fig. 1 (b) and (c) show the schematics of a conventional back gate IGZO TFT and the general dual work function (GDWF) gate IGZO TFT, respectively. The distance between the source and the drain is defined as the channel length (L_{CH}). There often exists a large overlapped distance ($L_{Overlap}$) between the bottom gate electrode and top source or drain electrodes for good transistor performance. In GDWF gate IGZO TFT, the bottom gate is separated into three segments with two overlapped gate sections and one un-overlapped gate section.

The Gate-source overlapped section and Gate-drain overlapped section are defined as $G_{Overlap\text{-}S}$ and $G_{Overlap\text{-}D}$, and their work function is called $GWF_{Overlap\text{-}S}$ and $GWF_{Overlap\text{-}D}$, respectively. The un-overlapped gate section and its work function are defined as $G_{Un\text{-}overlap}$ and $GWF_{Un\text{-}overlap}$. The bottom gate is divided into three parts. The change of gate work function between different parts, even between $G_{Overlap\text{-}S}$ and $G_{Overlap\text{-}D}$ is expected to have great effect on the movement of electrons, affecting the distribution of energy bands and thus improving the performance and reducing leakage of the device. With the help of TCAD, the impact of these parameters on the off-state current (I_{off}) and on-state current (I_{on}) of the TFTs are systematically investigated in the following sections.

In addition, in order to achieve the integration process feasibility of the general dual segmented bottom gate and further optimize the device performance, a novel PIDWF gate IGZO TFT is proposed, as shown in Fig. 1(d). $G_{Overlap-S}$ and $G_{Un-overlap}$ employ the same metal composition to streamline the fabrication process. In contrast, $G_{Overlap-D}$ selectively adjusts the metal work function to effectively minimize leakage. And the new structure introduces dielectric isolation between the different metal work function gate parts just near the drain regions. Compared to a TFT without a drain-overlapped gate, the PIDWF gate IGZO TFT can significantly reduce leakage while minimizing the loss of drive current. In contrast, simply reducing the drain overlap region results in a decrease in Ion without offering additional benefits [25]. The PIDWF gate IGZO TFT is expected to have less effect on the gate control ability to the channel and create ahorizontal MOS-like capacitive structure in the gate electrode, which may affect the energy band distribution and further reduce the device leakage. The length and dielectric constant of the dielectric isolation are denoted as L_D and k_D, respectively. Additionally, the key parameters in the new structure are thoroughly investigated and optimized using simulation techniques.

B. FABRICATION PROCESS

In general, the segmented gate with three parts, the $G_{Un\text{-}overlap}$, the $G_{Overlap\text{-}S}$, and the $G_{Overlap\text{-}D}$ is difficult for practical fabrication. The integration flow of the proposed PIDWF gate IGZO TFT for sequential 3-D integration is shown in Fig. 2. In practical applications, advanced techniques such as DUV or EUV lithography can be utilized to prevent significant alignment deviations. After obtaining a flat inter-layer dielectric (ILD) on bottom-tier devices, molybdenum (Mo) is deposited and expected to forms $G_{Overlap\text{-}S}$ and $G_{Un\text{-}overlap}$. Another silicon oxide is deposited on the patterned gate and then, etched to form a sidewall for later different work functional metal gate isolation. Next, the aluminum (Al) with a smaller work function is deposited on the structure and etched to form a sidewall metal gate with a different work functions for $G_{Overlap\text{-}D}$. Next, the left sidewall metal gate and isolation dielectric near the source region are removed by selective photolithography and etching process, which results in the formation of a partially isolated dual metal work function gate. In the following steps,

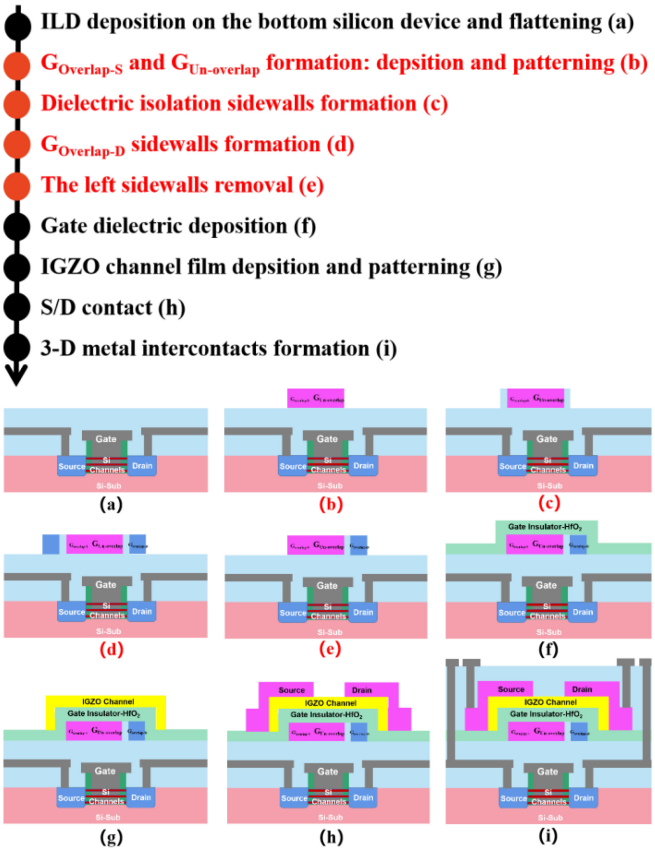

FIGURE 2. Designed process flow of partially isolated dual work function gate IGZO TFT (a) ILD deposition on the bottom silicon device and flattening, (b) $G_{Overlap-S}$ and $G_{Un-overlap}$ formation: gate deposition and patterning, (c) Dielectric isolation sidewalls formation, (d) $G_{Overlap-D}$ sidewalls formation, (e) The left sidewalls removal, (f) Gate dielectric deposition, (g) IGZO channel film deposition and patterning, (h) S/D contact formation, (i) 3-D metal intercontact formation.

the high-k gate dielectric like HfO_2 by atomic layer etching (ALD) and the IGZO channel film by sputter or ALD as well as the source and drain contact metal by sputter are sequentially deposited and patterned for the fabrication of the transistor, following by the BEOL and multi-tier 3D interconnection process. While the designed integration flow demonstrates strong process compatibility with the sequential 3D process and it also makes the fabrication of PIDWF gate IGZO TFT feasible.

C. SIMULATION ENVIRONMENT

To explore the variations of electrical characteristics between the conventional back gate IGZO TFT with the GDWF gate IGZO TFT and the proposed PIDWFgate IGZO TFT and the proposed PIDWF gate IGZO TFT, the detailed simulation investigations are performed using Silvaco TCAD. For accurate device simulations, the calibrations to the model of IGZO material are extensively implemented. The IGZO material contains a large number of defect states within the bandgap and is usually thought of as a combination of exponentially decayed states and Gaussian states. Also, internal defect statements are used to describe the defect state density in the energy

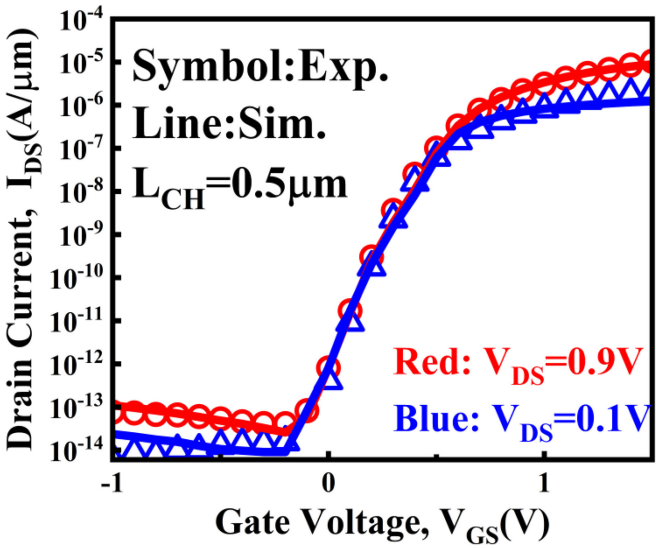

FIGURE 3. TCAD calibration results (line) and the experimental data (symbols) for the 500 nm channel-length back-gated IGZO TFTs. Red and bule represent $|V_{Ds,sat}| = 0.9$ V and $|V_{Ds,lin}| = 0.1$V, respectively.

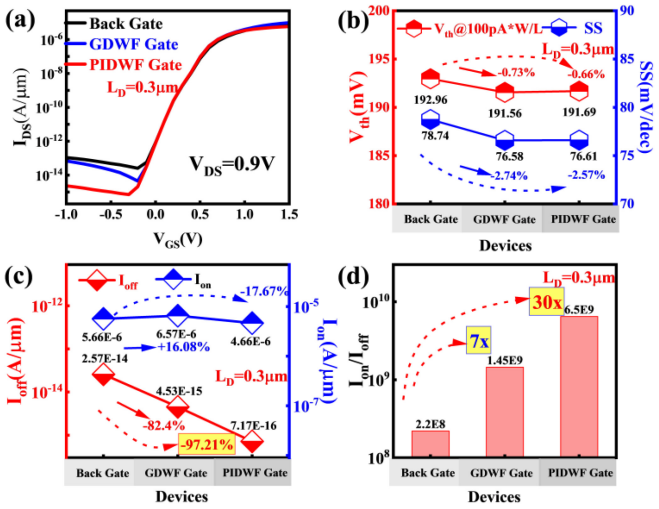

FIGURE 4. (a) Comparisons of transfer characteristic curves for three devices structures. (b) Comparisons of on-state and off-state current in different structures. (c) Comparisons of V_{th} and SS in different structures. (d) Comparisons of I_{on}/I_{off} ratio in different structures. The PIDWF gate IGZO TFT is simulated by TCAD under L_D = 0.3 μm.

TABLE 1. Device parameters.

Parameters	Definitions	Values
W_{CH}	Channel width	10μm
L_{CH}	Channel length	0.5μm
$L_{Overlap}$	Overlap length	1μm
T_{GI}	The thickness of Gate Insulator	10nm
T_{CH}	The thickness of channel	15nm
$GWF_{Un\text{-}overlap}$	The work function of un-overlapped gate section	4.37eV
$GWF_{Overlap\text{-}D}$	The work function of Gate-drain overlapped section	variable
$GWF_{Overlap\text{-}S}$	The work function of Gate-source overlapped section	variable /4.37eV
L_D	Dielectric isolation length in gate	variable
k_D	The dielectric constant of dielectric isolation in gate	variable

band gap of the semiconductor near the interface between the IGZO and the oxide. Impact ionization effects, band-to-band tunneling effects, carrier production, and recombination are also considered in the physical model for carriers' conductance in the IGZO TFT channel. Under high electric field conditions, electron tunneling from the IGZO valence band to the conduction band through trap or defect states can have a significant effect on the conductance. Therefore, the trap-assisted tunneling effect is used in the model to simulate the trap-to-band phonon-assisted tunneling effect for Dirac wells. Through extensive modifications on the transistor structure and the physical model parameters as well as the calibration of the IGZO material parameters, the simulated current-voltage electrical curves are successfully calibrated with the experimented back gate IGZO TFTs fabricated in our lab in Fig. 1(a) with very small deviations, as shown in Fig. 3. The calibrated material and physical models provide effective simulation basis for later new structure transistor investigations.

III. RESULTS AND DISCUSSION

A. ELECTRICAL PROPERTIES COMPARISON OF DIFFERENT STRUCTURES

The adopted device parameters for transistor simulations are shown in Table 1, which are the same as the implemented parameters in the fabricated devices in our lab. In GDWF gate IGZO TFT, the $GWF_{Overlap\text{-}S}$ and $GWF_{Overlap\text{-}D}$ are varied, while $GWF_{Un\text{-}overlap}$ is kept constant at 4.37 eV during the simulation. In the case of the PIDWF gate IGZO TFT, $GWF_{Un\text{-}overlap}$ and $GWF_{Overlap\text{-}S}$ are set to 4.37 eV without any modifications to simplify the process. Fig. 4(a) shows the I_{DS}-V_{GS} characteristics of back gate IGZO TFT, GDWF gate IGZO TFT and PIDWF gate IGZO TFT at V_{DS}=0.9V. In comparison to the conventional structure, both GDWF gate IGZO TFT and PIDWF gate IGZO TFT exhibit minimal threshold voltage drifts of less than 2 mV. Additionally, these structures yield decreased subthreshold swing (SS) compared to conventional back gate IGZO TFT in Fig. 4(b). In Fig. 4(c) and Fig. 4(d), compared to the back gate structure, the on-state enhancement of the GDWF gate structure has increased by 16%, while leakage has decreased by 87%. The new PIDWF gate structure exhibits a slight decrease in I_{on}, while leakage current is significantly reduced by 97.21%, resulting in a 30x enhancement in the I_{on}/I_{off} ratio.

The 2T0C DRAM leverages the gate capacitance of IGZO transistors for charge storage, with the storage node voltage denoted as V_{SN}. Accordingly, the retention time and write latency of DRAM circuits are intricately linked to the gate capacitance. Illustrated in Figure 5(a), compared to the back gate structure, the PIDWF gate structure demonstrates

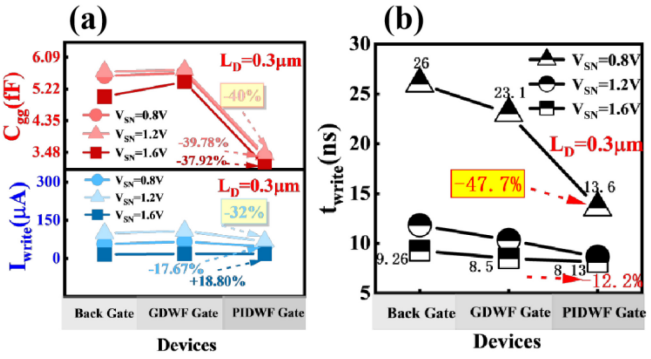

FIGURE 5. (a) Comparisons of C_{gg} and I_{write} for three devices structures in the DRAM. (b) Comparisons of t_{write} for three devices structures in the DRAM. Three curves are extracted under V_{SN} = 0.8 V, V_{SN} = 1.2 V and V_{SN} = 1.6 V. The PIDWF gate IGZO TFT is simulated by TCAD under L_D = 0.3 μm.

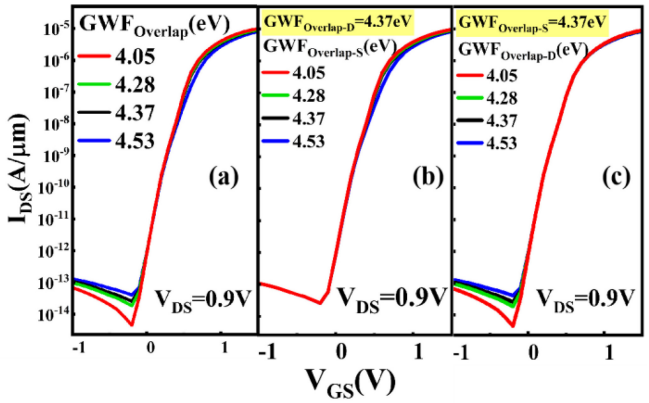

FIGURE 6. Transfer characteristics of devices as (a) the change of the $GWF_{Overlap-S}$ and the $GWF_{Overlap-D}$ simultaneously, (b) the change of $GWF_{Overlap-S}$ while fixing the $GWF_{Overlap-D}$, (c) the change of $GWF_{Overlap-D}$ while fixing the $GWF_{Overlap-S}$. All curves are obtained by TCAD under V_{DS} = 0.9 V.

a notable reduction of nearly 2 fF in gate capacitance, surpassing the decrease in write current. Firstly, the insertion of the isolation dielectric in the overlapping region leads to a reduction in the gate area relative to the channel, resulting in a partial decrease in capacitance. Additionally, the lower $GWF_{Overlap-D}$ causes the isolation dielectric between the main gate and the gate-drain overlapped section to attract a certain amount of charge. This phenomenon is equivalent to the newly generated horizontal capacitance being connected in series with the original capacitance, which significantly reduces the overall capacitance compared to the traditional back-gate structure of the device. Consequently, as depicted in Figure 5(b), integrating the PIDWF gate IGZO TFT into DRAM circuits would yield a remarkable 47.7% reduction in write latency.

Meanwhile, the device can also achieve a comparable I_{on} even while the PIDWF-gate overlapped electrode switched to the source electrode and support DRAM write operation while the signal filliping. Moreover, the retention time of DRAM is defined by

$$t_{\text{retention}} = \frac{\Delta V_{\text{SN}} \times C_{\text{gg}}}{I_{\text{off}}} \tag{1}$$

the impact of C_{gg} can be disregarded due to the significantly higher magnitude of reduction in leakage current compared to that of capacitance reduction. According to the derived formula, the adoption of the PIDWF gate IGZO TFT in DRAM can potentially elevate retention time by nearly two orders of magnitude.

B. MECHANISM ANALYSIS

For the GDWF gate IGZO TFT and PIDWF gate IGZO TFT, the capability to reduce leakage current gradually strengthens. Meanwhile, it is found that through modifying the gate metal work function in the overlapped region, the I_{off} is further reduced to some extent. Therefore, $GWF_{Overlap-S}$ and $GWF_{Overlap-D}$ are investigated in an exhaustive manner. Fig. 6(a) demonstrates that when both $GWF_{Overlap-S}$ and $GWF_{Overlap-D}$ are simultaneously decreased, there is a significant decrease in I_{off}, accompanied by a slight enhancement in I_{on}. To further understand the individual contributions of these parameters to device performance, $GWF_{Overlap-S}$ and $GWF_{Overlap-D}$ are separately investigated in the following parts. Fig. 6(b) shows that when $GWF_{Overlap-D}$ is fixed at 4.37 eV, with the decrease of $GWF_{Overlap-S}$, I_{off} remains unchanged, but it results in a similar degree of enhancement in I_{on} with Fig. 6(a). Fig. 6(c) shows that when $GWF_{Overlap-S}$ is fixed at 4.37 eV, I_{off} decreases significantly with the decrease of $GWF_{Overlap-D}$, and the degree of decrease is basically the same as that in Fig. 6(a). Based on the above results, it can be concluded that the adjustment of $GWF_{Overlap-S}$ and $GWF_{Overlap-D}$ have distinct effects on the device performance. Reducing $GWF_{Overlap-S}$ primarily enhances the on-state current of the IGZO device, although the degree of improvement is relatively modest. On the other hand, reducing $GWF_{Overlap-D}$ leads to a substantial reduction in leakage current. However, leakage reduction by the GDWF gate IGZO TFT achieved only by a smaller $GWF_{Overlap-D}$ is not very remarkable. Therefore, guided by the results from this structural analysis, a novel PIDWF gate IGZO TFT is proposed. In the new structure, the work function distinction between $G_{Overlap-D}$ and $G_{Un-overlap}$ is maintained to ensure low leakage, while the $GWF_{Overlap-S}$ and $GWF_{Un-overlap}$ are uniform to simplify the manufacturing process without significant performance changes. Furthermore, the introduction of an isolation dielectric between $G_{Overlap-D}$ and $G_{Un-overlap}$ proves to be an effective strategy for reducing leakage.

In Fig. 7(b), compared to back gate, significantly fewer electrons flow from the source to the drain within the channel of GWF gate at V_{gs}=−0.4V. Because the parameter of $G_{Overlap-D}$ had a great effect on device leakage, the physical reason behind the behavior needs careful investigation. A model called the $G_{Overlap-D}$ Induced Leakage Lowering ($G_{Overlap-D}$ILL) is proposed to explain it. As shown in Figure 7(a), the reduction of $GWF_{Overlap-D}$ results in a work function difference within the gate structure. The resulting coupling increases the barrier near the source, thereby suppressing the flow of electrons within the channel in the

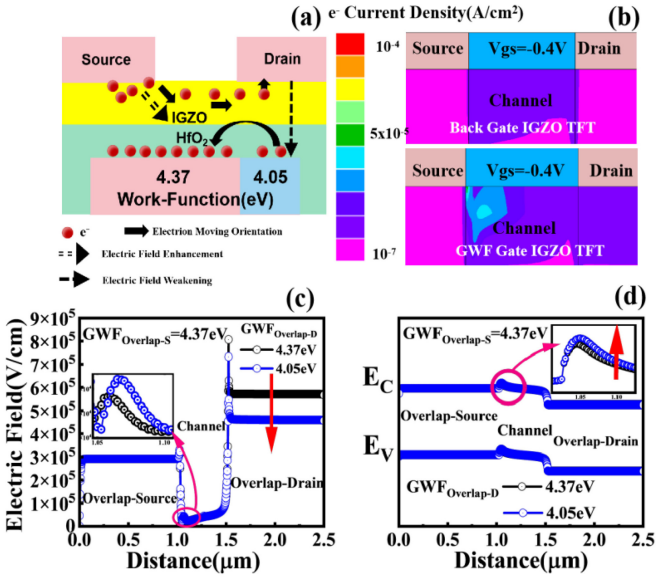

FIGURE 7. (a) Fermi energy differences before metals contact with different work functions. (b) Surface contact potential difference after metal contact with different work functions. (c) Electric field and (d) energy band distribution in the channel. All curves are simulated and extracted under $V_{GS} = -0.4$ V and $V_{DS} = 0.9$ V.

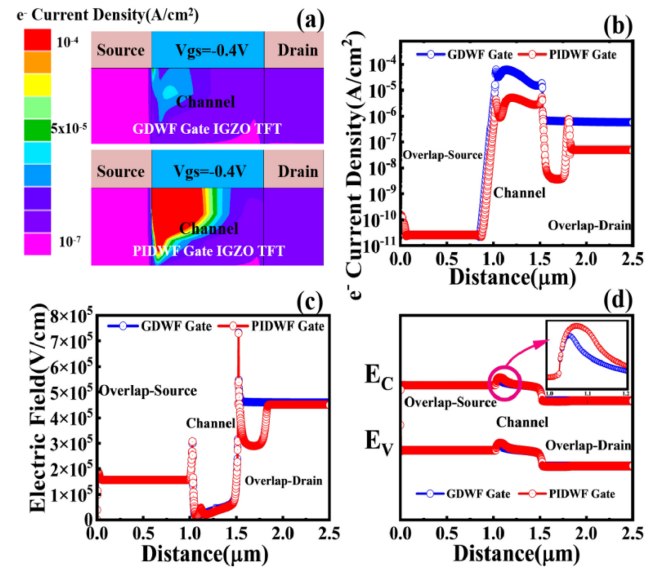

FIGURE 8. (a) Barrier in the channel and the depicted $G_{Overlap-D}$ILL model. (b) The comparisons of the electron current density, (c) electric field and (d) energy band distributions in the channel for two kinds of devices. All curves are extracted and simulated by TCAD under $V_{GS} = -0.4$ V and $V_{DS} = 0.9$ V.

off-state condition, as shown in Figure 7(d). Due to the reduced $GWF_{Overlap-D}$, the electric field between the drain and $G_{Overlap-D}$ diminishes, as shown in Figure 7(c). This alteration is unfavorable for the electron flow towards the drain, resulting in a decrease in the off-state current.

Based on compositive analysis and the proposed model, the PIDWF gate IGZO TFT demonstrates enhanced effectiveness in reducing leakage, which can be reasonably interpreted. As illustrated in Fig. 8(a) and Fig. 8(b), when

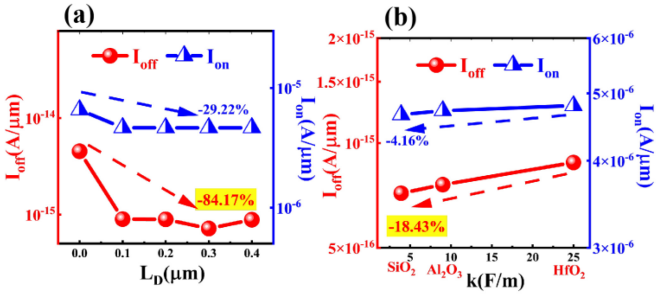

FIGURE 9. Comparison of on-state and off-state current in (a) different L_D, and (b) different isolation dielectric materials between two metals with different work functions.

compared to the dual function gate structure, the electron current density in the channel is reduced by 10x, and it is reduced by over 100x in the overlap section through the PIDWF gate structure. This reduction in leakage is attributed to the inclusion of isolation dielectrics in the overlap region. The presence of these dielectrics weakens the electric field that points vertically downward from the drain to $G_{Overlap-D}$, while simultaneously increasing the barrier in the channel. Consequently, the leakage in the I_{off} of the device is significantly reduced.

C. OPTIMIZATION AND SCALABILITY OF THE PARTIALLY ISOLATED DUAL WORK FUNCTION GATE IGZO TFT

To further optimize the new structure, the effect of different materials and the length of isolation dielectrics on the transistor leakage current is investigated. As shown in Fig. 9(a), as the dielectric length increases, the I_{off} of the device initially exhibits a sharp decrease. However, the rate of leakage reduction diminishes when L_D exceeds 0.1 μm, approaching a saturation state when L_D reaches approximately 0.3 μm. Meanwhile, the trend observed in Ion mirrors that of the leakage, albeit with a lesser magnitude. As shown in Fig. 9(b), there is a clear relationship between the dielectric constant of the dielectric material and the leakage current. As the dielectric constant decreases, the leakage current also decreases accordingly. For instance, when the dielectric constant of the isolation insulator is reduced from 25 F/m to 3.9 F/m, the transistor leakage is reduced by 22%. This observation indicates that the dielectric constant and the leakage current are inversely proportional to each other. To investigate the underlying factors contributing to the observed results, the electric field distribution and energy band distribution were extracted and analyzed. As shown in Fig. 10(a) and Fig. 10(b), The increase in dielectric length leads to a weakening of the electric field between the drain and $G_{Overlap-D}$. However, once the L_D reaches 0.3 μm, the electric field saturates and no further reduction is observed. This saturation indicates that the electric field has reached a stable state and is no longer affected by the increase in dielectric length. Fig. 10(c) and Fig. 10(d) demonstrate the impact of dielectric material changes on the electric field between the drain and $G_{Overlap-D}$, which in

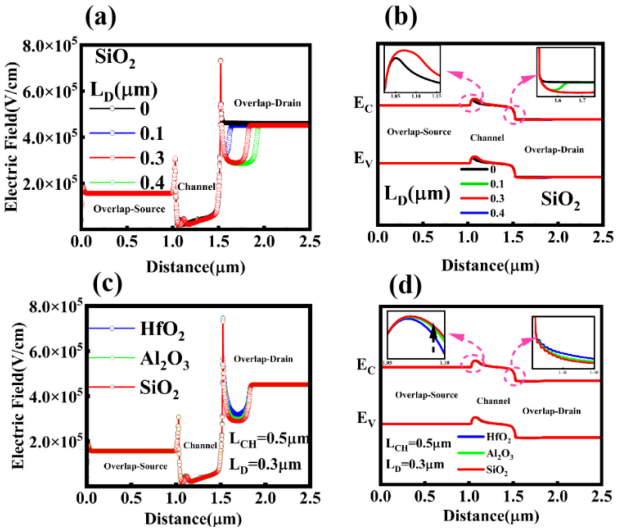

FIGURE 10. **(a) Electric field and (b) barrier in the channel with different L_D. (c) Electric field and (d) energy band distribution in the channel with different isolation dielectric materials between two metals with different work functions.**

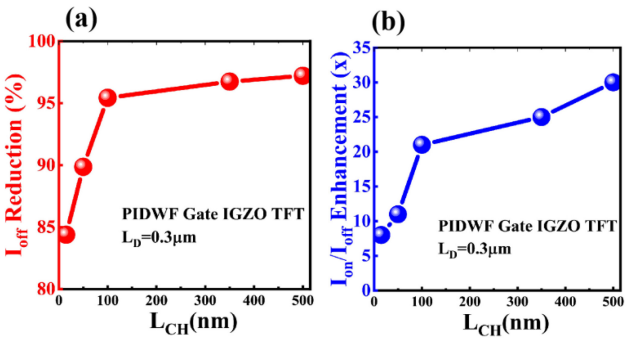

FIGURE 11. **(a) I_{off} reduction ratio and (b) I_{on}/I_{off} enhancement times for different channel lengths compared to conventional back gate IGZO TFT.**

turn affects electron flow. Decreasing the dielectric constant of the material weakens the electric field between the drain and $G_{Overlap\text{-}D}$. Indeed, as the potential barrier in the channel becomes higher, it hinders the flow of electrons and subsequently reduces the leakage current. The simulation results further support the notion that the new structure attains optimal performance when employing a dielectric material with a smaller dielectric constant. Common silicon oxide is chosen as an example, and the dielectric length is set to 0.3 μm. This specific configuration leads to an impressive 97% reduction in the leakage current of the device.

To investigate the size scalability of the PIDWF gate structure in IGZO TFTs, simulations are conducted and compared across various channel lengths. As shown in Fig. 11, the ability of the new structure to reduce leakage diminishes slightly at smaller sizes. This phenomenon is attributed to the sharp increase in the electric field within the channel at smaller sizes. At the ultra-short channel size of 15 nm, the leakage of the PIDWF gate structure is still reduced by 84.6%, and the Ion/Ioff ratio is increased by 8 times compared to the conventional structure. This demonstrates that the new structure remains advantageous even at ultra-short sizes, which makes the new structure still promising for applications at small sizes.

IV. CONCLUSION

In summary, to obtain extremely low transistor leakage in back gate IGZO TFT for 3D eDRAM application, a partially isolated dual work function gate IGZO TFT is proposed by the introduction of dielectric isolation between dual work function gate to form asymmetric and lateral MOS-like gate electrode structures. With TCAD simulations, the leakage current is obviously reduced from 2.57×10^{-14}A/μm to 7.57×10^{-16} A/μm, resulting in almost two orders of magnetite lowering than conventional structure. This breakthrough has the potential to increase the retention time of DRAM applications by nearly 100 times. The changed distribution of the electrical field and energy band in the channel is investigated to explain the reduction of leakage as the change of $G_{Overlap\text{-}D}$. The decrease in the gate capacitance reduces the write latency of the DRAM by 47.7%. Furthermore, while to optimize the key structural parameters of dielectric isolation between dual work function gate, a final 97% reduction in leakage with threshold voltage drifts of less than 2 mV for the new device structure is achieved. Simultaneously, the integration process for the new transistor is compatible with the 3D-sequential stacking process and does not impose an additional thermal budget. This feature makes the PIDWF gate IGZO TFT more amenable to multilayer stacking, thus facilitating an augmentation in device density. Additionally, the PIDWF gate IGZO TFT is scalable and can still achieve an 84.6% reduction in leakage even with ultra-short channel lengths. Consequently, it helps alleviate the challenge of aligning the density of IGZO TFTs with that of GAA FETs. These results pave the way for sequential integration of 3D eDRAM for better AI calculation power and efficiency in the future.

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