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Comprehensive Evaluation of Junctionless and Inversion-Mode Nanowire MOSFETs Performance at High Temperatures

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ABSTRACT This work aims to perform a comprehensive comparison of the electrical properties of junctionless and inversion-mode nanowires MOSFETS, fabricated with similar gate stack and state-of-art process, in the temperature range from 300 K to 580 K. The comparative analysis is performed through the main electrical parameters of the devices, such as the threshold voltage, subthreshold current and slope, DIBL, conduction current, mobility, and maximum transconductance extracted from experimental data. Devices with different fin widths are compared. It is demonstrated that the inversion-mode nanowire transistors present higher performance with three times higher maximum transconductance and conduction current and twice higher low field mobility than the junctionless' with a fin width of 10 nm at a fixed temperature. On the other hand, the junctionless nanowire transistors presented higher thermal stability of their electrical parameters with a 75% lower variation of maximum transconductance with temperature, 77% lower maximum transconductance variation with temperature, and 22% lower temperature coefficient of mobility.

INDEX TERMS Electrical characterization, high temperature, inversion-mode, junctionless.

I. INTRODUCTION

In order to sustain the scaling process of the MOS technology predicted by Moore's law, which demonstrates that the number of transistors in a chip doubles every two years, the semiconductor industry searches for ways to reduce the transistor dimensions to enhance the circuits' performance and to reduce the cost per executed function [1]. The reduction of the device's dimensions is not always followed by the decrease of the applied potentials, which can cause an increase in the internal electric fields in the structure and in the power density, mainly in integrated circuits where a considerable number of devices operate simultaneously [2]. It intensifies the self-heating effect, where the current flowing through the transistor causes an increase in its operating temperature due to the Joule effect. In an integrated circuit, each device acts as a source of heat that spreads out to its vicinity and causes a global temperature increase [2].

However, there are some applications in which the source of heat is provenient from the environment where the circuit is inserted. These applications include the automotive industry, where sensors coupled to the engines can reach up to 200° C; the aerospatial industry, where sensors connected to probes can reach up to 175° C; the oil and gas industry, where circuits coupled to the extraction probes reach up to 175° C [3].

The MOSFET operation at high temperatures is detrimental to the transistors' electrical characteristics, which are degraded due to the dependence of the fundamental parameters of the semiconductor on temperature. One of the most affected parameters at high temperatures is the subthreshold current, which is elevated at many orders of

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magnitude, leading to a higher static power consumption [4]. Therefore, it is crucial to understand how temperature affects the operation of state-of-the-art devices, such as nanowire transistors, to design devices with higher thermal stability for specific applications at high temperatures.

Along with the scaling process, some problems, especially the short channel effects, appeared. These effects occur when the source and drain potentials electrically influence an important part of the charge controlled by the gate metal. They are intensified when the gate length is reduced due to higher proximity between the drain and source regions. Then, the drain region starts to control proportionally more charges in the channel region [5]. The multigate architecture, where the gate electrode surrounds the silicon layer [5], was proposed to keep the scaling process.

In this scenario, nanowire transistors were proposed to replace FinFET in the downscaling process of MOSFET transistors and reached maturity for mass production [6], [7]. These devices have demonstrated a suitable operation for short-channel devices due to their excellent control of channel charges, which leads to necessary electrical properties for both digital and analog applications in a wide temperature range [8]. Nanowires have a multigate architecture with both the fin width (W_{FIN}) and fin height (H_{FIN}) with similar dimensions, around 10-15 nm [5].

Among the different types of nanowire transistor structures are the triple-gate SOI junctionless (JNT) and the inversion-mode (IM) nanowire transistors based on the fin-like architecture. Their structures are illustrated in Fig. 1. The IM nanowire transistor has opposite dopant types in the channel and the source/ drain, while the JNT has the same dopant type in the channel, source, and drain, as shown in Fig. 1. The absence of PN junctions is an essential characteristic of JNT nanowires since the fabrication of the source/drain region of short-channel devices (channels with a few nanometers of length) became complex due to the need for an ultrasharp dopant concentration gradient. This complexity paved the way for the JNT to avoid this process step [9]. The JNTs also have a high doping concentration in the channel region, unlike IM ones that have not intentionally doped semiconductor in the channel. Although both JNT and IM devices have different semiconductor types and doping concentrations in the channel region, they operate under a full depletion regime in the subthreshold region [9].

An n-type IM nanowire's operation regime changes from depletion to inversion in the channel-oxide interfaces as the gate voltage increases until the threshold voltage. Unlike the IM, the JNT has two conduction mechanisms: the bulk and the accumulation conduction. An n-type JNT nanowire's operation regime changes from total depletion to partial depletion as the gate voltage increases. When the gate voltage reaches the threshold voltage, there are no more depleted atoms in the center of the silicon layer, and, in place, there is a neutral path for current flow. Then, the transistor is turned on, since the free carriers can flow from source to drain through the neutral path in the center of the silicon layer. For higher gate voltage, when the flat-band voltage is achieved, the silicon layer is almost entirely neutral, and an accumulation layer is formed near the interfaces. At this gate bias, the current is composed of a bulk current at the center and an accumulation current at the interfaces [8].

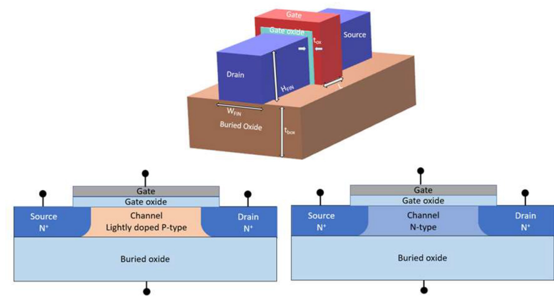

FIGURE 1. Illustration of the tridimensional structure (top) of both transistors and the transversal view along the channel length of the inversion-mode (left bottom) and junctionless (right bottom) nanowire transistors.

Several works have evaluated the electrical properties of junctionless nanowire transistors at high temperatures [4], [10]. Moreover, some works compare the operation of inversion-mode and junctionless nanowire transistors [11], [12], [13], but there is no comparative study concerning thermal variation. This work intends to experimentally compare the electrical behavior of both devices, with similar dimensions and gate stacks, at temperatures from 300 K to 580 K. By comparing devices with similar gate stacks, dimensions, and state-of-art processes, this work intends to provide quantitative results for the studied electrical parameters, complementing the previous analysis of [4], [10], [11], [12], [13], [14]. In [14], the authors compared the electric characteristics extracted at low drain bias, such as the threshold voltage, the subthreshold current, the subthreshold slope, the subthreshold current, the conduction current, and the low-field mobility from experimental data. In the present extended version, some curves were completed, such as the curve of subthreshold current in the function of the temperature and further experimental parameters were presented as the transconductance and the parameters at high drain bias of both devices at high temperatures, such as the DIBL and the saturation transconductance. In the previous paper, part of the data from different fin widths was not presented, such as the threshold voltage and mobility for all fin widths and is now presented. Also, new analyses are discussed as the occurrence of the volume inversion in the mobility of narrow devices.

II. DEVICE CHARACTERISTICS

Both IM and JNT nanowire transistors studied in this work were fabricated in CEA-Leti, in Silicon-On-Insulator (SOI) substrates with 145 nm-thick buried oxide, according to the fabrication process described in [15], [16]. Both devices' gate stack comprises an interfacial SiO_2 layer, followed by a 2.3 nm HfSiON high-k dielectrics, 5 nm TiN gate metal.

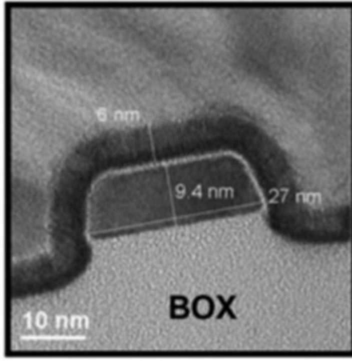

FIGURE 2. TEM image of the device.

Also, both devices have ten parallel fins, fin height (H_{FIN}) of 9 nm, and channel length (L) of 100 nm. Devices with different fin widths (W_{FIN}) of 10 nm, 15 nm, 20 nm, and 40 nm were measured. The JNTs channel region is heavily doped n-type silicon with a doping concentration (N_D) of $5{\cdot}10^{18}$ cm^{-3}. This doping concentration was determined by the method described in [17]. Other works study junctionless nanowire transistors at high temperatures with different doping concentrations. In [10], [18] and [19] the JNT studied presented N_D of 10^{19} cm^{-3} and in [11] they presented N_D of $2{\cdot}10^{19}$ cm^{-3}. The channel region is lightly-doped (or not intentionally doped) p-type silicon with a concentration (N_A) of 10^{15} cm^{-3} for the IM nanowire transistors. The source and drain regions of both transistors are heavily doped with n-type dopants with a concentration of $5{\cdot}10^{20}$ cm^{-3}. Figure 2 shows a TEM image of the device [16].

III. RESULTS AND DISCUSSION

The measurements of the drain current (I_{DS}) in the function of the gate voltage (V_{GS}) curves were directly on the wafer, with the chuck temperature adjusted with 100 mK accuracy, using a B1500A Semiconductor Analyzer. $I_{DS} \times V_{GS}$ curves were measured from 300 K to 580 K with drain voltage (V_{DS}) of 25 mV and 900 mV. Fig. 3 and Fig. 4 show the measured drain current in the function of the gate voltage of one of the total of three sets of electrical measurements in linear and logarithmic scales for IM and JNT nanowires biased with a drain voltage of 25 mV and 900 mV, respectively, in different temperatures and for different fin widths.

From the $I_{DS} \times V_{GS}$ curves at V_{DS} of 25 mV and 900 mV, the devices' main electrical parameters were extracted to make a comparative analysis between the transistors at high temperatures. In the following sections, each parameter is quantitatively analyzed.

A. THRESHOLD VOLTAGE

The threshold voltage of both devices was extracted through the g_M/I_{DS} method, where g_M is the transconductance. In this method, the threshold voltage is defined as the gate voltage in which the diffusion current (dominant at the subthreshold regime) equals the drift current (dominant at the conduction regime), which occurs at half of the maximum g_M/I_{DS} [16]. The threshold voltage in the function of the temperature of both devices with different W_{FIN} is shown in Fig. 5. For the following curves, the symbols are the mean values of V_{TH} and the bars represent the standard deviation associated with the sets of measured devices.

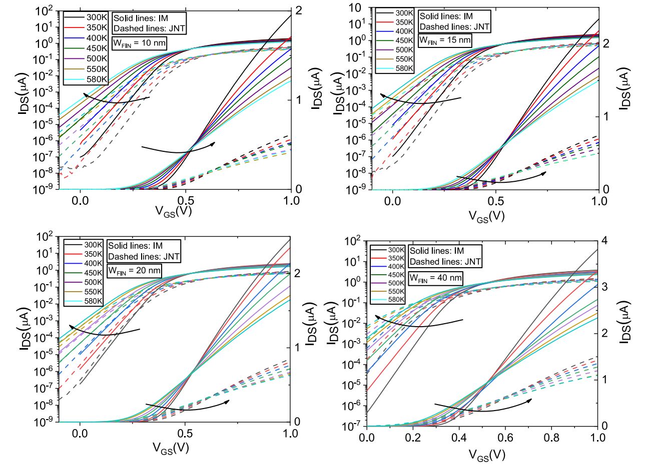

FIGURE 3. Measured I_{DS} x V_{GS} curves with V_{DS} of 25 mV in function of temperature for both devices with W_{FIN} of 10 nm (left top), 15 nm (right top), 20 nm (left bottom) and 40 nm (right bottom).

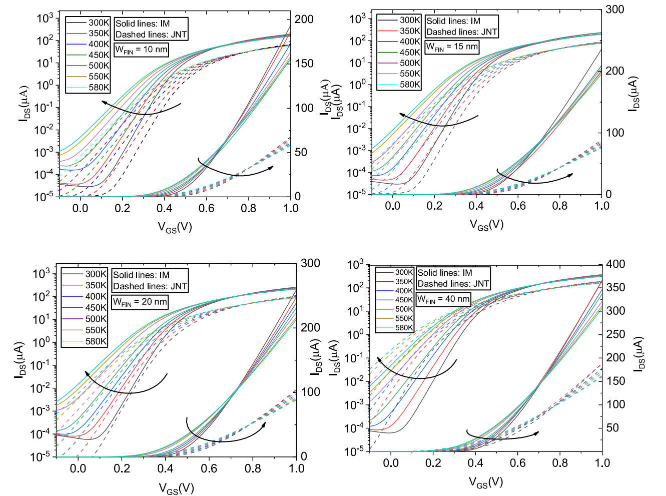

FIGURE 4. Measured I_{DS} x V_{GS} curves with V_{DS} of 900 mV in the function of temperature for both devices with W_{FIN} of 10 nm (left top), 15 nm (right top), 20 nm (left bottom), and 40 nm (right bottom).

As shown in Fig. 5, as the temperature rises, the V_{TH} decreases for both transistors. To understand how the V_{TH} of both devices varies with temperature, the models below [20], [21] were used:

$$V_{TH_{IM}}(\mathrm{T}) = \phi_M - \chi_{si}(\mathrm{T}) - \frac{E_G(\mathrm{T})}{2} + \phi_{FP} + \mathrm{f(T)} \quad (1)$$

where f(T) is:

$$\mathrm{f(T)} = -\frac{Q_d(T)}{C_g} - V_t \ln\left[\frac{C_{ch}}{C_g}\left(1 - e^{\frac{Q_d(T)}{V_t C_{ch}}}\right)\right] \quad (2)$$

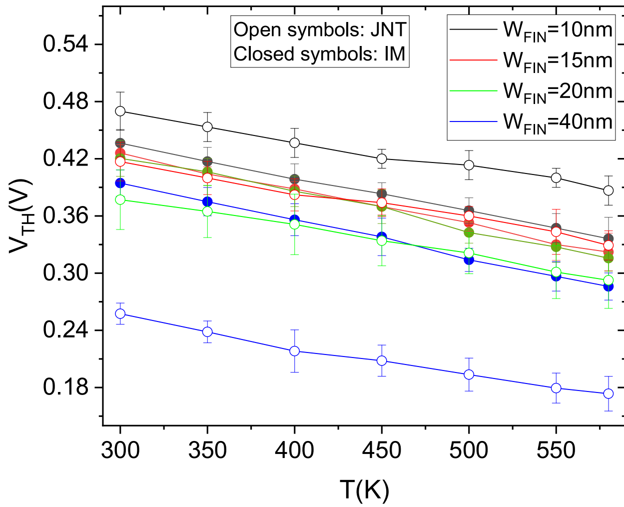

FIGURE 5. Extracted threshold voltage in the function of temperature for different W_{FIN} for both IM and JNT devices.

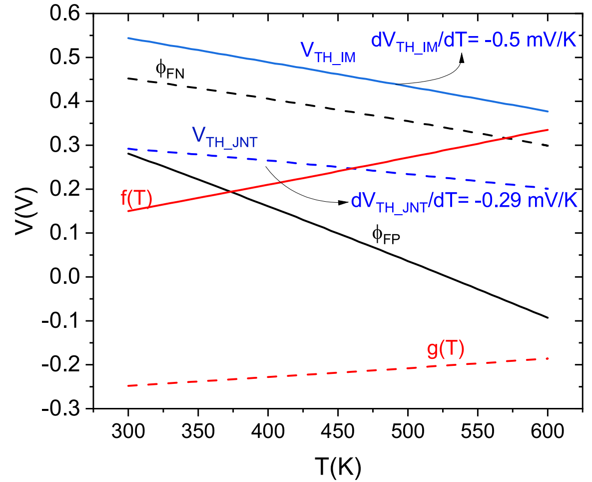

FIGURE 6. Terms of the threshold voltage of both devices in function of the temperature.

TABLE 1. Threshold voltage variation with temperature of both devices.

	Junctionless	Inversion-mode
W_{FIN}(nm)	dV_{TH}/dT (mV/K)	dV_{TH}/dT (mV/K)
10	-0.29	-0.35
15	-0.30	-0.37
20	-0.31	-0.38
40	-0.29	-0.39

$$V_{TH_JNT}(\mathrm{T}) = \phi_M - \chi_{si}(\mathrm{T}) - \frac{E_G(\mathrm{T})}{2} + \phi_{FN} + \mathrm{g(T)} \quad (3)$$

where g(T) is:

$$\mathrm{g(T)} = \frac{\alpha(\mathrm{T})}{2C_{ox}{}^2} - \frac{Q_t(\mathrm{T})^2}{8\alpha} - \frac{Q_t(\mathrm{T})}{2C_{ox}} - \frac{\beta(\mathrm{T})}{8\alpha(\mathrm{T})}\sqrt{\beta^2 - 16\alpha(\mathrm{T})V_t} + V_t \quad (4)$$

Figure 6 shows the variation of the Fermi potential ϕ_{FP} and ϕ_{FN} in the channel of IM and JNT transistors respectively and the terms related to the total charge of the channel f(T) and g(T) for devices with W_{FIN} of 20 nm. As the figures show, the term with the highest dependence on temperature is the Fermi potential, which is associated with the silicon intrinsic carriers concentration (n_i) [22]. The variation of the Fermi potential of the IM nanowire transistor with temperature is higher than the JNT's, which explains the higher dependence of V_{TH} for IM devices.

Due to its higher doping concentration at the channel, the junctionless transistors have a more intense bandgap narrowing than the inversion-mode devices, according to equation (1) [23], [24]. The term E_{bgn} accounts for bandgap narrowing due to doping concentration in the channel.

$$\mathrm{E_G} = 1,08 + 4,73 \cdot 10^{-4}\left[\frac{300^2}{300+636} - \frac{T^2}{\mathrm{T}+636}\right] - \mathrm{E_{bgn}} \quad (5)$$

Because of that, the intrinsic carriers concentration of IM nanowire transistors increases by higher orders of magnitude with temperature, since it depends on the bandgap level, as expressed in equation (2):

$$n_i = \sqrt{BT^3 e^{-\frac{E_G}{kT}}} \quad (6)$$

where B is a constant and K is the Boltzmann constant [22]. This results in a higher variation of the Fermi level of IM transistors than the JNT one, since the Fermi level variation with temperature depends on the variation of the logarithm of n_i with temperature, according to equation (3) [22]. The other two terms in equation (3) have less relevant variation with temperature in the range studied.

$$\left|\frac{\partial \phi_F}{\partial T}\right| = k\ln\left(\frac{N_{si}}{n_i}\right) + kT\frac{\partial \ln(N_{si})}{\partial T} - kT\frac{\partial \ln(n_i)}{\partial T} \quad (7)$$

Consequently, the JNT with W_{FIN} of 10 nm presents a threshold variation of −0,29 mV/K while the IM with W_{FIN} of 10 nm presents a variation of −0,35 mV/K as shown in Table 1. This difference in V_{TH} slope is smaller than the difference in the ϕ_F slope because the f(T) component of IM transistor has a higher dependence on temperature than the g(T) component of JNT transistor. The variation of f(T) and g(T) with temperature is opposite to the variation of the Fermi potential, hence, the total variation of V_{TH} is smaller than the variation of ϕ_F.

The fin width also influences the slope of V_{TH} with the temperature, since f(T) and g(T) are related to the total charge in the channel, which is dependent on the fin width as $Q_t = \mathrm{q}\ N_{Si}\mathrm{HW}_{FIN}$. The fin width is more relevant for g(T) than for f(T), since the JNT's charge is bigger due to higher concentration in the channel. That is the reason why, for a fixed temperature, the JNT transistor presented a variation of 0.21 V in V_{TH} with W_{FIN} of 10 nm and 40 nm.

However, the fin width has more impact on the slope of f(T) with temperature than g(T), which explains why the JNT threshold voltage variation with temperature presented low variation with W_{FIN}, whereas the V_{TH} variation with

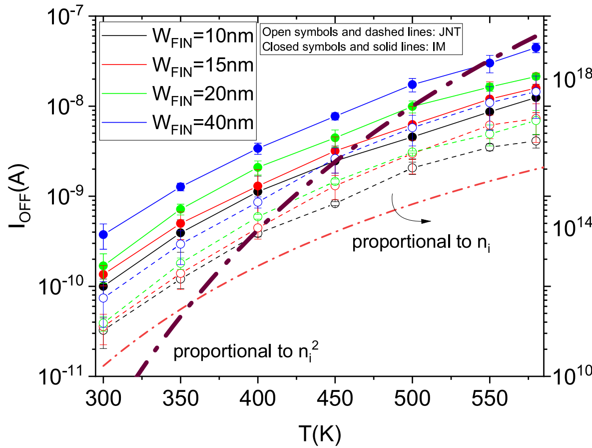

FIGURE 7. Subthreshold current in the function of temperature for both devices with different W_{FIN}.

temperature of the IM with W_{FIN} of 40 nm is 11% higher than the one with W_{FIN} of 10 nm.

B. SUBTHRESHOLD CURRENT

In order to compare the subthreshold current of both devices in the same operation conditions, the subthreshold current was extracted at a gate overdrive voltage (V_{GS}-V_{TH}) of −0.3V and V_{DS} of 0.9V. Fig. 7 shows the subthreshold current in the function of the temperature for both devices with different W_{FIN}.

Fig. 7 shows that the subthreshold current is highly dependent on temperature, varying up to 2 orders of magnitude in the studied range. There are some factors that impact the temperature dependence of the subthreshold current such as the intrinsic carrier concentration, the diffusion coefficient of the silicon, and the effective channel length in the subthreshold regime.

Among these factors, the intrinsic carrier concentration is the most relevant with respect to thermal variation. The subthreshold current is a diffusion current of minority carriers, thus, the intrinsic carriers' concentration plays an important role in this operation regime [9]. As mentioned previously, the thermal generation of electrons in silicon structure is intensified as the temperature rises and these electrons join the current and, therefore, cause the increase of the current at the same gate voltage.

The IM nanowire transistors presented approximately 3 times higher subthreshold current than the JNT at all temperatures for W_{FIN} of 10 nm. One factor that explains this difference is the effective channel length of the transistors when biased in the subthreshold regime. As discussed in [25], the JNTs have a larger channel than the mask channel length projected for the device due to the lateral depletion region towards the source/drain regions induced by the gate bias. In addition, the IM nanowire transistors present a shorter channel than the mask channel length projected in the design process due to the diffusion of dopants from the source/drain regions toward the channel. Thus, the effective channel length of IM transistors is shorter than the JNT's in the subthreshold regime, which contributes to a higher current to these devices. Moreover, the diffusion coefficient of inversion-mode nanowire transistors is higher than the JNT's due to the higher mobility in the channel, which facilitates the minority carriers' flow.

Figure 7 also shows the curves proportional to n_i and n_i^2 in function of the temperature. The junction leakage current has a diffusion component, proportional to n_i^2, and a generation component, proportional to n_i. In [26], the junction leakage in SOI transistors varied as n_i for temperatures up to 400 K – 450 K and as n_i^2 for higher temperatures and $V_{GS} = -1$ V. For the gate voltage bias applied in this work, the subthreshold current varied as n_i^2 in the entire range of temperature, which means that I_{OFF} is dominated by the junction leakage current, as can be seen in Fig. 7.

C. INVERSE SUBTHRESHOLD SLOPE

The inverse subthreshold slope (SS) is the inverse of the slope of the linear region in the subthreshold region (low gate voltage) in the semilogarithmic scale of the $I_{DS} \times V_{GS}$ curve. It can be calculated by (4):

$$S(T) = n\left(\frac{kT}{q}\right)\ln(10), \tag{8}$$

where n is the body factor of the transistor [22].

The body factor of both IM and JNT depends on the doping concentration and the depletion charge, whose variation with the temperature in the measured range can be neglected, mainly for fully-depleted SOI transistors. For this reason, the inverse subthreshold slope of both devices increases linearly with the temperature at approximately the same rate for all W_{FIN} as shown in Fig. 8. The figure show the inverse SS of JNT and IM nanowire transistors with different W_{FIN} in the function of the temperature and the line of the theoretical limit for the inverse SS, which considers the body factor equal to 1.

Both devices presented a variation of the inverse SS with a temperature of 0,197 mV/decK, which is very close to the theoretical limit of 0,199 mV/decK. This shows the high electrostatic control that the triple gate nanowire transistors provide and its immunity against short-channel effects.

D. DIBL

One of the most important short-channel effect is the drain induced barrier lowering (DIBL). For the device to conduct, the gate electrode is responsible for reducing the barrier between the source and drain regions, allowing the carriers' drift. However, as the drain voltage increase, its electrostatical influence on the channel region becomes important and can cause the lowering of the barrier without gate control, which degrades the behavior of the transistor causing the reduction of the threshold voltage [5]. In order to evaluate the influence of the high drain bias on the threshold voltage of the nanowire transistors, the DIBL was extracted

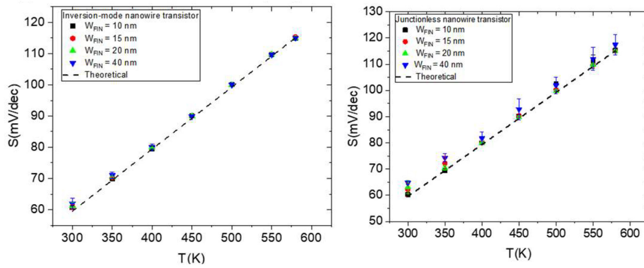

FIGURE 8. Extracted Inverse subthreshold slope in the function of temperature for inversion-mode and junctionless transistors with different W_{FIN}.

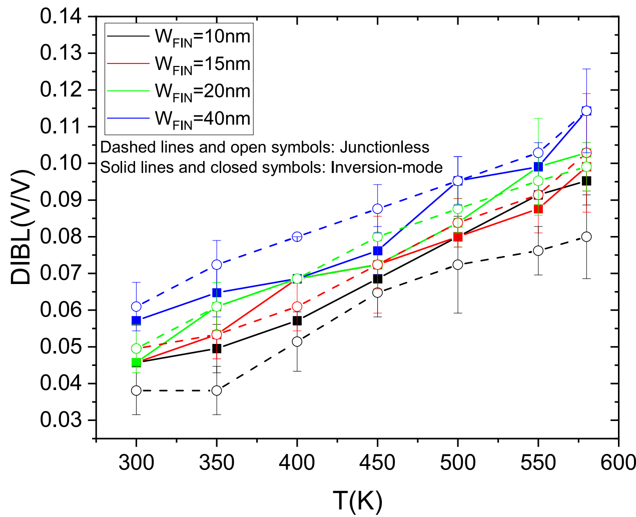

FIGURE 9. DIBL in the function of temperature for both transistors with different W_{FIN}.

comparing the values of V_{TH} at V_{DS} of 25 mV and 900 mV. The result is shown in Fig. 9.

The DIBL values of narrower devices of both types are smaller than the wider ones. This difference is due to the higher proximity between the lateral gate electrodes, which intensifies the electric field related to the gate bias in the channel region, minimizing the influence of the lateral electric field related to the drain bias in the channel.

The DIBL of both transistors has similar values at all temperatures. For the wider devices, the junctionless nanowire transistors presented a slightly higher DIBL, between 5% and 15% higher than the DIBL of the inversion-mode transistor. However, for the narrower devices, the JNT presented between 6% and 18% lower DIBL than the IM transistor. As the JNTs have no p-n junctions, the narrower devices provide better electrostatic control of the channel charges by the gate and, hence, lower values of DIBL.

The values of DIBL increase with temperature, with a rate of 0,19 K-1 and 0,17 K-1 for IM and JNT transistors, respectively for W_{FIN} of 10 nm, which means that the drain bias has more influence on the channel electrostatic at high temperatures. The height of a potential barrier in semiconductors is dependent on temperature and is

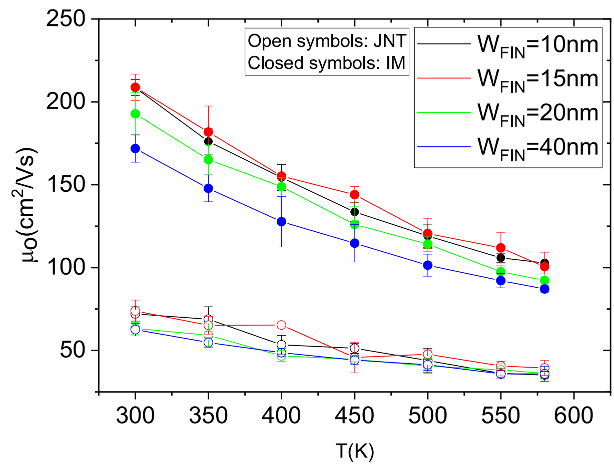

FIGURE 10. Low field mobility in the function of temperature for both devices with different W_{FIN}.

related to the increase of minority carriers through thermal generation [22]. The increase of these carriers in the channel region contributes to the reduction of the barrier due to higher thermal energy. Then, at high temperatures, the drain bias is more influential on channel electrostatic because the barrier is also reduced by thermal effects.

Moreover, the DIBL values are higher for the wider devices, which reflects a better electrostatic control of the charges by the gate contact in narrower devices due to the smaller distance between the lateral gate faces, which reduces the influence of the drain bias in the channel. The junctionless transistor provides smaller DIBL for the narrower device due to the absence of p-n junction between the drain/source and the channel. A depletion region is formed in the junction, which is controlled by the drain. At high drain voltages, this depletion region extends along the channel and damage the electrostical control of the gate increasing the DIBL. For the narrower devices, the percentage of the volume of the charges in the channel region controlled by the drain is higher, and this effect becomes more relevant [18].

E. LOW-FIELD MOBILITY

The low-field mobility of both transistors was extracted through the Y-function method [27]. Fig. 10 shows the low-field mobility of the transistors in the function of temperature for different W_{FIN} with the mean values and the standard deviation bars.

From the analysis of the graphic, one can conclude that the mobility of both devices is degraded with temperature. It occurs because the mobility degradation mechanisms are intensified at high temperatures. The main mechanisms that degrade the mobility are the phonon and ionized impurity scattering (μ_{psii}), the neutral impurity scattering (μ_{ni}), and the carrier-to-carrier scattering (μ_{cc}) [28]. They are

TABLE 2. Temperature coefficient for both devices with different WFIN.

Temperature coefficient α		
W_{FIN}(nm)	Junctionless	Inversion-mode
10	-1.088	-1.093
15	-0.952	-1.174
20	-0.853	-1.118
40	-0.845	-1.030

combined through the Matthiessen's rule expressed in (5):

$$\mu_o = \frac{1}{\left[\left(\frac{1}{\mu_{psii}}\right) + \left(\frac{1}{\mu_{cc}}\right) + \left(\frac{1}{\mu_{ni}}\right)\right]} \quad (9)$$

As the temperature rises, the amount of phonons that interact with the charge carriers increases, which changes the carrier direction of propagation and reduces their velocity and, hence, the mobility of the carrier in the material. Additionally, the amount of ionized impurity in the material increases with temperature, interacting electrically with the carriers and reducing their mobility [28]. As the JNT nanowire transistor has a higher dopant level, its mobility is more degraded by ionized impurity scattering for all temperatures and W_{FIN} than the IM nanowire transistors', as shown in Figure 10. These two components of mobility contribute to the degradation of the mobility of both devices at high temperatures.

At low temperatures, there is a gain of mobility since there is less vibration of the lattice. However, a fraction of the impurities do not have enough thermal energy to ionize, so the neutral impurity scattering mechanism becomes relevant. Hence, part of the gain due to less phonon scattering is compensated with a higher neutral impurity scattering mechanism. For low doped semiconductors, the neutral impurity scattering mechanism is less relevant since there is fewer impurity atoms in their structure, hence, there is a gain of mobility at low temperatures, unlike for heavily doped semiconductors. This results in a higher variation of the mobility for low doped semiconductors as observed in Fig. 10.

The relation between mobility and temperature can be expressed through the temperature coefficient α, according to (6).

$$\mu \propto T^{\alpha} \quad (10)$$

Table 2 shows the extracted coefficients α for both transistors with different W_{FIN}.

The mobility degraded purely by the phonon scattering mechanism presents a coefficient α of -1.5, whereas, the mobility degraded purely by the impurity scattering mechanism presents a coefficient α of $+1.5$ [4]. For the heavily doped junctionless transistors in [10], the phonon and the impurity scattering mechanisms counterbalanced each other, and, hence, the mobility of the devices presented low variation with temperature. In [4], the temperature coefficient for the n-type devices was around -1, which indicates the predominance of the phonon scattering mechanism in mobility degradation with temperature in the range studied (from 300 K to 500 K).

In the present work, the JNT nanowire transistors exhibited a temperature coefficient between -0.845 and -1.088, whereas the IM nanowire transistor presented a temperature coefficient between -1.093 and -1.174, which shows that the JNT transistors' mobility is less dependent on temperature. The values of α indicate that phonon scattering mechanisms predominantly degrade the mobility of both devices because the values are closer to $-1{,}5$ than from $+1{,}5$, which is coherent since in the temperature range studied, the concentration of ionized and neutral impurity has low variation with temperature.

Moreover, as the values of the temperature coefficient of the JNT nanowire transistor are closer to $+1{,}5$ than the IM nanowire transistors', the impact of the variation of the impurity scattering with temperature is higher in the JNT mobility. It is also coherent since the JNT has a proportionally higher amount of neutral impurity at 300 K that becomes ionized at higher temperatures. There is a compensation mechanism in the variation of the JNT mobility with the temperature where part of the variation of the phonon scattering mechanism is compensated by the variation of the impurity scattering mechanism, which explains the higher thermal stability of the JNT mobility.

The triple-gate nanowire transistors have three planes of current conduction, two in the laterals and one at the top of the silicon layer. The top plane has a crystallographic orientation more favorable to the current conduction than the lateral planes. Hence, it was expected that wider devices have higher mobility, since a higher fraction of the carriers travel through the top plane than in the narrower devices, as is observed in. However, Fig. 10 shows that the mobility of the wider devices is lower than the narrower devices'. This result is also observed in other works [29], [30], [31]. In [32] and [33], this result is attributed to the volume inversion effect, which affects devices with $_{FIN}$ width in the order of a few nanometers. The inversion volume occurs when the carriers no longer accumulate in the silicon-oxide interfaces, as predicted by classical physics and start to accumulate in the center of the silicon layer due to the quantum confinement effect in narrow devices [33]. As the surface scattering is not relevant in the center of the silicon layer as in the interfaces with the oxide, the mobility in the center of the silicon layer is higher, which explains the result obtained.

F. TRANSCONDUCTANCE

The transconductance is the variation rate of the drain current in relation to the gate voltage. It was extracted from the derivative of the $I_{DS} \times V_{GS}$ curves, the maximum value of the transconductance g_{Mmax}, and it was normalized by the effective channel width $W = 2H_{FIN}+W_{FIN}$, as shown in Fig. 11.

The curves were approximated by straight lines and the slopes of the curves for both transistors are shown in Table 3.

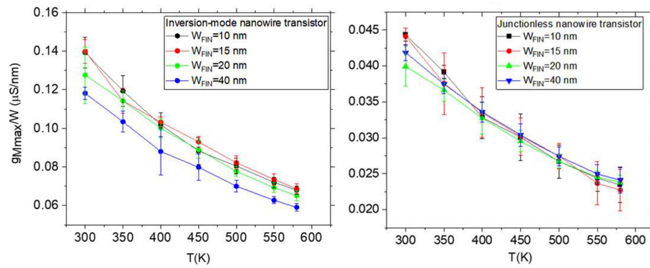

FIGURE 11. Maximum transconductance in function of temperature for IM and JNT transistors with different W_{FIN}.

TABLE 3. Variation of the maximum transconductance normalized by its value at 300 K with temperature for both devices with different WFIN.

	Junctionless	Inversion-mode
W_{FIN}(nm)	$d(g_{M_MAX} / g_{M_MAX_300K})/dT$ (K^{-1})	$d(g_{M_MAX} / g_{M_MAX_300K})/dT$ (K^{-1})
10	-1.523	-1.928
15	-1.568	-1.757
20	-1.529	-1.850
40	-1.512	-1.771

Similarly to mobility, the maximum transconductance of IM transistors has higher values at all temperatures and for all W_{FIN}. On the other hand, the variation of the normalized g_{M_max} of the JNT transistor with temperature is approximately 79% of the IM one for W_{FIN} of 10 nm. For other values of W_{FIN}, this relation remained around 82% and 89%.

As the geometric properties and the drain bias are equivalent for both devices, the difference between the variation of g_{Mmax} with temperature is limited to the mobility variation with temperature. As discussed previously, the mobility of the JNT transistor has a higher thermal stability than the IM transistor's, which explains the higher thermal stability of the maximum transconductance of these devices as observed.

Moreover, the transconductance in the saturation regime was extracted from the $I_{DS} \times V_{GS}$ curves at a drain bias of 0.9 V. The values of transconductance were extracted at the same gate overdrive voltage of 0.5 V, considering the threshold voltage at V_{DS} of 0.9 V used in the DIBL calculation. Fig. 12 shows the saturation transconductance normalized by the effective channel width (g_{M_SAT}/W) in the function of the temperature for both devices with different W_{FIN}, with the mean values and the standard deviation bars.

This result is important to evaluate the behavior of both devices at the saturation regime. As observed in the maximum transconductance at low drain bias, the IM devices also presented higher values of saturation transconductance and higher dependence on the fin width and temperature. However, the devices presented similar values of the saturation transconductance normalized by their value at 300 K, as seen in Table 4. This occurs because, at high drain bias, the ratio between the transconductance at 300 K of the IM and the JNT transistors increases while the ratio between the variation of the mobility of the IM and the JNT transistors decreases compared to the low drain bias case.

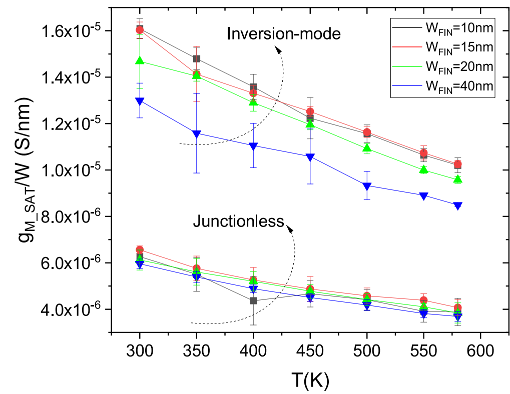

FIGURE 12. Saturation transconductance in function of temperature for both devices with different W_{FIN}.

TABLE 4. Variation of the saturation transconductance normalized by its value at 300 K with temperature for both devices with different W_{FIN}.

	Junctionless	Inversion-mode
W_{FIN}(nm)	$d(g_{M_SAT} / g_{M_SAT_300K})/dT$ $(mK)^{-1}$	$d(g_{M_SAT} / g_{M_SAT_300K})/dT$ $(mK)^{-1}$
10	-1.24	-1.30
15	-1.27	-1.20
20	-1.30	-1.29
40	-1.34	-1.22

This result indicates that the inversion-mode nanowire transistor is better for operating at the saturation regime at a fixed temperature. In contrast, the junctionless nanowire transistor is better for temperature-dependent applications at the saturation regime.

G. CONDUCTION CURRENT

As done for the subthreshold current, the conduction current was extracted at a gate overdrive voltage of 0.4 V and V_{DS} of 0.9 V to compare the current of both devices in the same operating conditions. Fig. 13 shows the conduction current normalized by the effective channel width in the function of the temperature for both devices with different W_{FIN}, with the mean values and the standard deviation bars.

Following the tendencies of the maximum transconductance, the conduction current of both devices decreases with the temperature as shown in Table 5. The conduction current variation with temperature depends on the threshold voltage variation and on the mobility variation with temperature as the equation (7):

$$\frac{\partial I_{ON}}{\partial T} = \left(C_{ox}\frac{W}{L}V_{DS}\right)\left[(V_{GS} - V_{TH})\frac{\partial \mu_n}{\partial T} - \mu_n\frac{\partial V_{GT}}{\partial T}\right] \quad (11)$$

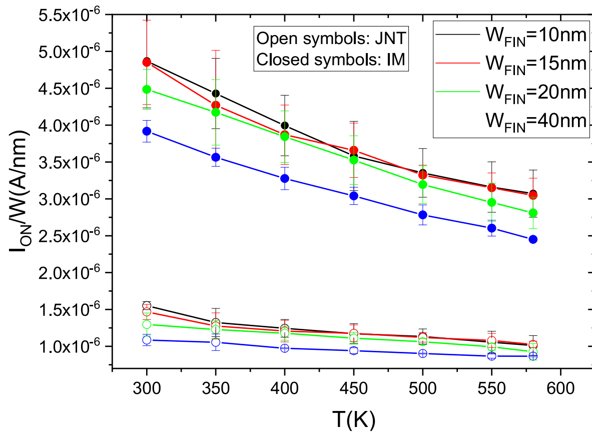

FIGURE 13. Conduction current normalized by the effective fin width in the function of temperature for both devices with different W_{FIN}.

TABLE 5. Conduction current normalized by its value at 300 K variation with temperature for both devices with different W_{FIN}.

	Junctionless	Inversion-mode
W_{FIN}(nm)	$d(I_{ON}/I_{300K})/dT$ (K^{-1})	$d(I_{ON}/I_{300K})/dT$ (K^{-1})
10	-0.97	-1.37
15	-0.90	-1.32
20	-0.99	-1.36
40	-0.83	-1.35

As the extraction was done at the same gate overdrive voltage, the threshold variation was compensated by the gate voltage variation. Hence, the conduction current variation with temperature follows the mobility variation with temperature. This explains why the conduction current of the inversion-mode transistors has a higher dependence on temperature than the current of the junctionless nanowire transistors since the mobility of the IM nanowire transistors is more dependent on temperature. The JNT nanowire transistor presented 77% lower variation of the I_{ON} than the IM nanowire transistor with W_{FIN} of 10 nm. For other values of W_{FIN}, the variation was approximately 80% lower for the JNT transistors.

IV. CONCLUSION

This work compared experimental results for the electrical characteristics of Junctionless and Inversion-Mode Nanowire MOSFETs in the high temperature range. The operation of both structures is degraded with the rise in temperature as the devices presented reduced threshold voltage, mobility, maximum transconductance, conduction current, and higher subthreshold current and subthreshold slope. The subthreshold slope of both devices was close to the theoretical limit, and both devices presented low DIBL, which shows the excellent electrostatic control that these structures provide. At room temperature, the inversion mode nanowire transistors presented three times higher mobility, maximum transconductance, and twice higher conduction current than the junctionless nanowire transistors with a fin width of 10 nm. However, they presented a three times higher subthreshold current than the junctionless nanowire transistor. Thus, except for the subthreshold current, the inversion mode devices presented better electrical properties at room temperature for all fin width values. They exhibited better electrical performance at any fixed temperature in the range studied.

On the other hand, the junctionless nanowire transistor presented a 17% lower variation of threshold voltage, a 22% lower temperature coefficient for mobility, a 75% lower variation of the maximum transconductance, and a 77% lower variation of conduction current with temperature than the inversion mode nanowire transistors for fin width of 10 nm. Hence, one can conclude that the junctionless nanowire transistors have higher thermal stability, as their parameters have lower variation with temperature than the inversion-mode nanowire transistors.

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