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Investigation on the Dynamic Characteristics of Hydrogen Plasma Treated p-GaN HEMTs Circuit Using ASM-GaN Model

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ABSTRACT This study demonstrates the first work that achieves accurate modeling of Hydrogen plasma-treated (H-treated) p-GaN gate devices with the ASM-GaN model, facilitating simulations for applications in monolithic integrated circuit (IC) design. The workflow for ASM-GaN model parameter extraction and optimization using IC-CAP is proposed. The I-V characteristics of both Enhancement / Depletion (E/D) mode devices are modeled and fitted. The impact of device capacitance on the dynamic properties of monolithic IC is investigated through the ASM model. The results demonstrate that C_{ds}, C_{gd}, and C_{gs} have different effects on the monolithic logic circuit performances. The high-level fitting of experimental data and circuit simulation of Inverter, NAND, and Comparator circuits proves the credibility of the modeling workflow and device capacitance modulation. This work provides a method to speed up the GaN monolithic IC design by accurate modeling with fast parameter extraction workflow regardless of the fabrication process. The reliable prediction of the circuit's dynamic performance will lay the foundation for designing and scaling up the GaN monolithic IC application.

INDEX TERMS GaN HEMTs, ASM model, hydrogen plasma treatment, DCFL circuit, capacitance, dynamic performance.

I. INTRODUCTION

In recent years, gallium nitride (GaN) has captured the attention of industry due to its superior properties, such as high operating temperature, high breakdown voltage, and fast switching speed [1]. Accurate device modeling is essential in integrated circuit design to mitigate errors arising from the fabrication process [2], [3], [4]. In GaN device simulation models, the Advanced Spice Model (ASM) has exhibited exceptional performance and has caught the interest of industries [5], [6], [7], [8]. By leveraging various physical effect formulas [9], the ASM can represent the physical phenomena in GaN devices, including the trapping effect, velocity saturation effect, temperature-dependent effect etc. Moreover, researchers have expanded the ASM applicability in various scenarios [7], [9], [10].

In the realm of GaN power electronics, the p-GaN gate structure is a commercially available Enhancement-mode (E-mode) approach. However, during fabrication, the inductively coupled plasma (ICP) dry etching of the p-GaN layer leads to etching damage, which reduces the devices' uniformity and stability. To address these reliability issues arising from surface states in p-GaN HEMT, Hydrogen plasma treatment (H-treated) presents a promising solution [12], [13].

For the GaN monolithic integration, early work on circuit simulation uses the Advanced Curtice GaAs model to characterize the HEMT devices [14], [15], where the device

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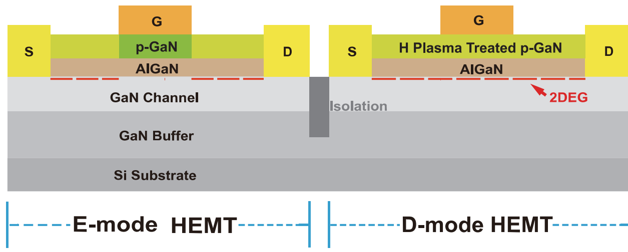


FIGURE 1. H-treated p-GaN E/D-mode HEMT structures.

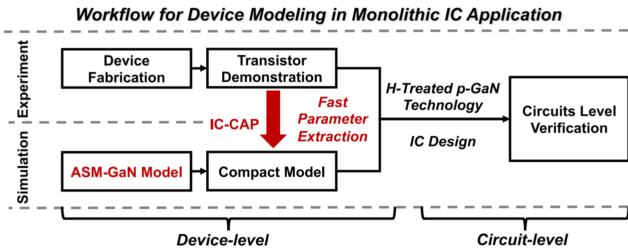


FIGURE 2. Workflow of the device modeling for the Monolithic IC Application.

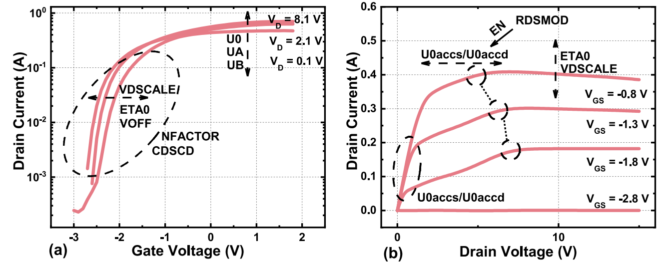


FIGURE 3. Illustration of ASM-GaN parameter extraction from (a) transfer curves, (b) output curves.

performance is not accurately fitted. Hence, the circuit performance is unpredictable. Instead, the ASM model is preferred to provide more accurate device characteristic fittings for GaN devices. Although much ASM model-based progress has been made in the radio frequency (RF) field, the application for monolithic ICs for power electronics has not been reported, especially for the circuit modules such as drivers and protection blocks in power electronics.

This paper presents a workflow using the ASM-GaN model for the verification of H-treated GaN monolithic ICs. It presents an approach for extracting key GaN device parameters for matching device characteristics. In addition, this research extends capacitance modulation for accurate circuit-level dynamic performance estimation to improve the scalability of circuit-level applications to accommodate novel process GaN device implementations in monolithic IC design, highlighting its broad applicability and potential impact.

II. THE MODELING WORKFLOW OF THE H-TREATED P-GAN HEMTS DEVICE

The structure of the H-treated p-GaN E/D-mode HEMTs in this paper is shown in Figure 1. The ICP-induced Hydrogen plasma can form the Mg-H bond to passivate the p-GaN layer to restore the two-dimensional electron gas (2DEG) channel. The high-resistance H-treated p-GaN also serves as the dielectric layer for the D-mode HEMT. Figure 2 provides an overview of device modeling and its relevance to monolithic IC applications. Utilizing a compact model is instrumental in facilitating IC design during the experimental phase of device fabrication. Incorporating the device model enables the co-optimization of monolithic IC fabrication with IC design, thereby potentially enhancing the scalability of IC modules.

After importing the ASM-GaN model, the experimental data are used to extract the device model parameters, including VOFF, NFACTOR, CDSCD, ETA0, U0, NS0ACCS, VSATACCS, and RTH0 etc., through the output and transfer characteristics. The key parameters affecting the trend of the transfer and output curves are shown in Figure 3. The data used are in the IC-CAP ASM Model manual [11], [16]. Ahsan et al. demonstrate that these parameters significantly determine the performance and intrinsic capacitances of HEMT devices [17]. Tuning the parameters would greatly improve the accuracy of the device model.

The workflow outlined in Figure 4 provides a comprehensive ASM parameter extraction process overview. This process involves fitting the device's transfer and output characteristic parameters using IC-CAP. As shown in Figure 5 (a), the modified blocks within the IC-CAP model have been specifically tailored for this purpose, with customized instructions and codes detailed within these blocks. The parallelepiped blocks in Figure 5 (a) indicate that multiple files can be included without causing interference. In addition, the red dashed box in Figure 5 (b) represents the optimizer algorithm, as documented in [11] manual, which offers the potential for further optimization of the model fit. Finally, the extracted device parameters critical to transmission and output performance are presented in detail in Table 1, including their values and definitions.

The fitted simulation results shown in Figure 6 demonstrate the transfer and output characteristics of D-mode and E-mode HEMTs. Figure 6 (a) presents the transfer curve of the D-mode HEMT, where the gate voltage was swept from -6 V to 4 V with the drain voltage at 10 V. Figure 6 (b) demonstrates the transfer curve of the E-mode HEMT with the gate voltage swept from 0 V to 5 V. The output curves of both HEMTs were displayed in Figure 6 (c) and Figure 6 (d).

Once parameters in DC sweep analysis have captured the intrinsic capacitances of the device, it becomes imperative to determine the parasitic capacitance, which significantly impacts the dynamic performance [17]. Dynamic performance is paramount in GaN monolithic ICs, as evidenced by the circuit performance demonstrated in this article. Careful selection of device capacitance values is essential to reproduce the circuit waveforms accurately, facilitating IC design. Parasitic capacitance includes access

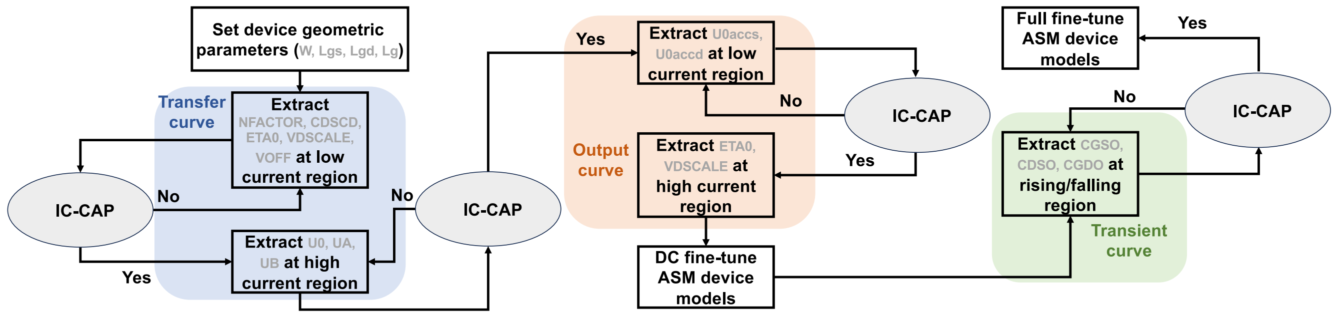
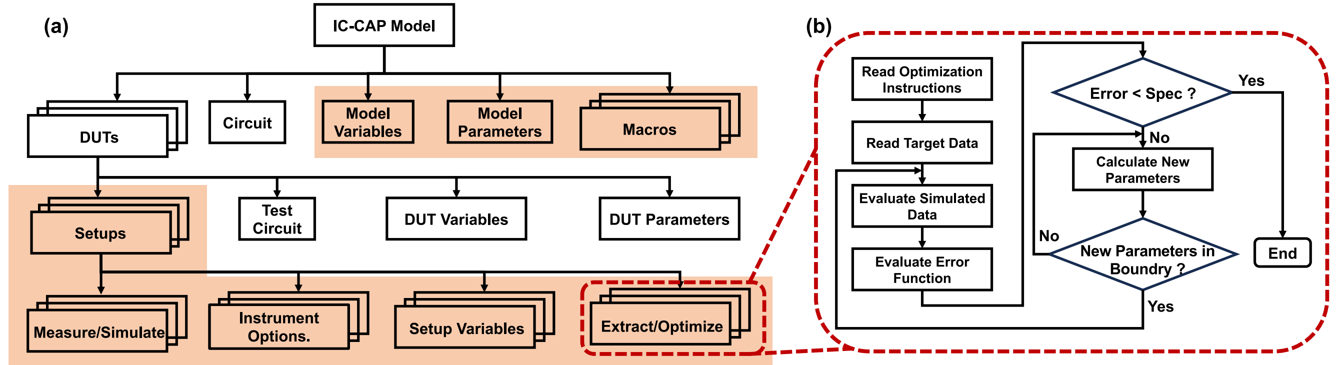


FIGURE 4. Fast parameter extraction workflow of the ASM Model with the aid of IC-CAP.



Macros - *Combination of the available menu functions used to create complex operations.*

DUTs - *Representation of different physical devices configurations.*

Instrument Options - *Instrument options control the state of the hardware for a setup.*

FIGURE 5. IC-CAP function blocks and the parameter extraction/optimization workflow: (a) PathWave Device Modeling (IC-CAP) model components. (b) Optimization flow diagram in IC-CAP [11].

TABLE 1. The key extracted device ASM model parameters for H-treated E/D mode device.

	Parameter	Description	E-mode Device	D-mode Device
Transfer Function	Voff (V)	Cut-off Voltage	1.5	-2.3
	NFACTOR	Sub-VOFF Slope parameters	0.5	0.5
	CDSCD	Sub-VOFF Slope Change due to Drain Voltage	1e-3	3.8e-1
	U0 ($\frac{m^2}{V \cdot S}$)	Low field mobility	4.3e-2	3.1e-2
	UA ($\frac{1}{V}$)	Mobility Degradation Coefficient	3.3	1.2
	UB ($\frac{1}{V}$)	Second Order Mobility Degradation Coefficient	1e-18	2.9e-18
Output Function	Rdsmod	Selects Access region Resistance Model; 0-simplified, 1-more accurate	1	1
	U0accs ($\frac{m^2}{V \cdot S}$)	Source Side Access Region Mobility	6.8e-3	1.7e-3
	U0accd ($\frac{m^2}{V \cdot S}$)	Drain Side Access Region Mobility	6.8e-3	1.7e-3
	ETA0	DIBL Parameter	1e-4	0.2
	VDSCALE (V)	DIBL Scaling VDS	1	5

region capacitance, overlap capacitance and fringing capacitance [21]. Following the guidelines of the ASM manual, the overlap capacitances (C_{dso}, C_{gso}, C_{gdo}) are used as a

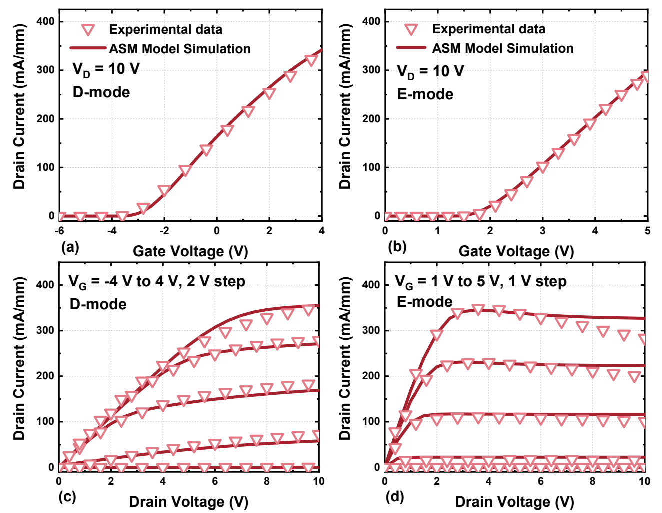


FIGURE 6. Measured (dotted line) and simulated (solid line) device characteristics using ASM structure: transfer curves of (a) D-mode and (b) E-mode, output curves (c) and (d), $L_g/L_{gs}/L_{gd}/W_g$= 2 μ m / 3 μm / 3 μm / 100 μm.

method to emulate realistic device capacitances (C_{ds}, C_{gd}, C_{gs}) in subsequent simulations.

$$Input\ Capacitance : C_{iss} = C_{gd} + C_{gs}$$

TABLE 2. The device capacitances range of p-GaN HEMTs.

References	C_{ds} (pF)	C_{gd} (pF)	C_{gs} (pF)
[18]	6.7	0.3	25.7
[19]	100	20	80
[20]	300	30	100
In this work	(30, 300)	(0.1, 30)	(25, 100)

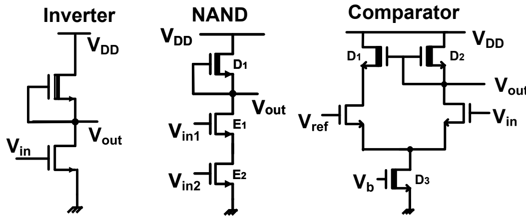


FIGURE 7. Schematic of Direct-Coupled FET Logic (DCFL) inverter, NAND gate, and bootstrapped comparator circuit.

$$\begin{aligned} &Output\ Capacitance : C_{oss} = C_{gd} + C_{ds} \\ &Reverse\ Capacitance : C_{rss} = C_{gd} \end{aligned} \quad (1)$$

The industrial-level capacitance values were selected as the guidance for simulating the circuits, as illustrated in Table 2. The values were chosen based on [18], [19] for C_{ds},[20] for C_{ds}, and [10], [18], [19], [20] for C_{gd}. Consequently, the simulated device capacitance values are within the data range measured in the reference. The definitions between the input, output, and reverse capacitance and the device capacitance are illustrated in 1.

The circuit diagrams in Figure 7 illustrate the Direct-Coupled FET Logic(DCFL) inverter, NAND gate, and bootstrapped comparator circuit in this study. For the following dynamic simulation of the DCFL inverter, a D-mode to E-mode gate width ratio of 30:100 was used; for the NAND circuits, a D-mode to E-mode gate width ratio of 10:200 was employed to match the fabricated circuit results.

III. THE EXPLORATION OF DEVICE CAPACITANCES C_{DS}, C_{GD}, C_{GS} IN INVERTER CIRCUITS

This section demonstrates the impact of device capacitances on the dynamic performance of the inverter circuit. Equations 2-4 present the correlation of rise time τ_{rise}, fall time τ_{fall} with device parameters [22]. The voltage V_{DD} and $V_{T,D}$ ($V_{T,E}$) corresponds to the supply voltage and threshold voltage of D-mode HEMT (E-mode HEMT). In contrast, the $f(V_{DD}, V_{T,D})$ and $g(V_{DD}, V_{T,E})$ are independent to device capacitances variations. The μ_D and μ_E, $C_{ob,D}$ and $C_{ob,E}$ are mobility and gate barrier capacitances for D/E-HEMTs respectively. The load capacitance C_L is expanded in Equation (4) to link with device capacitances investigated in this section.

$$\tau_{rise} = \frac{C_L}{\mu_D C_{ob,D}} \left(\frac{L}{W}\right)_D f(V_{DD}, V_{T,D}) \quad (2)$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ob,E}} \left(\frac{L}{W}\right)_E g(V_{DD}, V_{T,E}) \quad (3)$$

$$C_L = C_{gd,D} + C_{gd,E} + C_{ds,D} + C_{ds,E} + C_{int} \quad (4)$$

As depicted in Figure 8 (a), the performance of the inverter circuit in terms of C_{ds} has been investigated, revealing a degradation in the charging and discharging abilities as the C_{ds} of either the E-mode or D-mode HEMT increases. In the circuit, the D-mode HEMT could pull up the output voltage while the E-mode HEMT would pull down the output voltage. So, the significant difference between τ_{fall} and τ_{rise} can be attributed to the device gate width scale of D-mode: E-mode = 30:100. The gate width difference means a much stronger discharging current than the charging current. This explains why the τ_{fall} is much smaller than τ_{rise}. However, there is a difference in the impact of C_{ds} on the charging and discharging abilities. Specifically, if the capacitance C_{ds} is increased to the same extent for both HEMTs. The charging performance will be more severely affected compared with the discharging performance. In the inverter circuit, an increase in the C_{ds} value of either HEMT will weaken the charging and discharging capacities, as evidenced by the output voltage curve of the circuit.

In Figure 8 (b), it is demonstrated that C_{gd} has negligible impact on the charging and discharging capability of the inverter circuit. C_{gd} is known to have a relatively low value in GaN HEMTs [23]. C_{gd} has unnoticeable connections with the charging and discharging capability of the inverter circuit. In Figure 8 (c), the effect of C_{gs} on the charging and discharging ability of the inverter circuit is investigated. The simulation results indicate that increasing C_{gs} minimally impacts the performance of the inverter. The low capacitance value of C_{gs} has been reported by previous researchers [1], [9], [24].

IV. THE EXPLORATION OF DEVICE CAPACITANCES C_{DS}, C_{GD}, C_{GS} IN NAND CIRCUITS

Figure 9 (a) depicts the input signals for the NAND circuits. The four phases result in four operating states, illustrated in Figure 9 (b). Notably, each phase of input signals and operating conditions are depicted with the same color.

As illustrated in Figure 10 (a), increasing the C_{ds} of the D-mode HEMT in the NAND circuit from 30 pF to 300 pF noticeably amplifies the problem of unexpected voltage drops in the NAND output signal when it should remain logic high. Increasing the C_{ds} of the E-mode HEMT results in a higher voltage drop during the transition of the input signal (V_{in1} V_{in2}) from "00" to "01". This is because the E-mode HEMT has a path to the ground that can pull down the voltage level more effectively, causing the output voltage to drop significantly when a single E-mode HEMT is turned on. From the related work [8], [19], [20], three (C_{ds}) values have been reported. Therefore, based on the referenced data, these three C_{ds} values are selected for simulation. Firstly, the first two kinds of used simulated value $C_{ds} = 30$ pF, and $C_{ds} = 90$ pF are chosen to match the reported value in [8] and [19] separately. The last simulated value $C_{ds} = 300$ pF

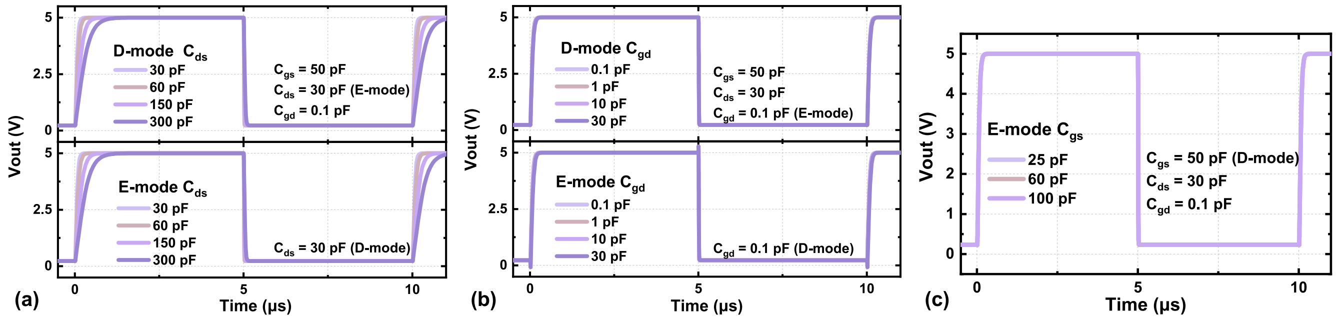


FIGURE 8. **The simulated switching waveform at the frequency of 100 kHz), setting (a) C_{ds}, (b) C_{gd} and (c) C_{gs} of E-mode and D-mode HEMTs as variables in inverter circuits.**

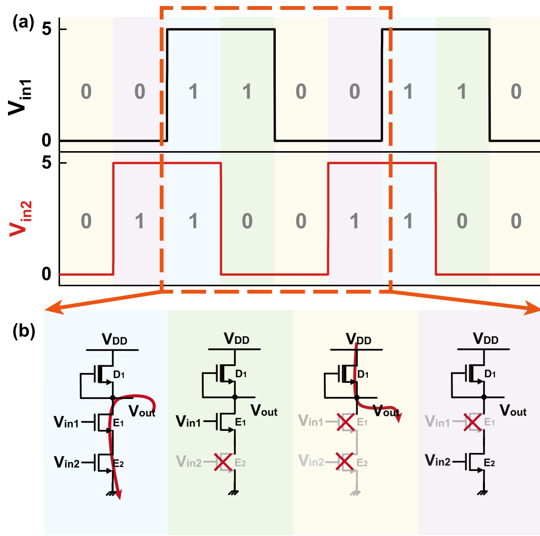


FIGURE 9. **The NAND setup (a) input signal (b) working stations of NAND circuits in 4 different phases.**

(150 pF for E-mode) capacitance is chosen to account for potential variations due to the fabrication process [20]. The values of C_{gd} and C_{gs} selected in Figure 10 (b) and (c) are similar to the selection of C_{ds} in Figure 10 (a).

The investigation of C_{gd} in the NAND circuit has revealed two unique phenomena, as depicted in Figure 10 (b). Increasing the C_{gd} of the D-mode HEMT in the NAND circuit reduces the voltage drop of the output voltage when the input signal changes from "10" to "00". This is due to the increased ability of the D-mode HEMT to store charge, thereby enhancing the output voltage to maintain a high potential. Meanwhile, the voltage drop increases when the input voltage changes from "10" to "00", which is similar to the reason for increasing the E-mode C_{ds}. The voltage drop issue is considerably exacerbated by increasing the C_{gd} of the E-mode HEMT in the NAND circuit from 0.1 pF to 30 pF.

It has been observed that the C_{gs} of the E-mode HEMT affects the output of the NAND circuit, inferred from the data presented in Figure 10 (c). Increasing the C_{gs} of the E-mode from 25 pF to 100 pF leads to an increase in the voltage drop when "10" becomes "00". Simultaneously, an increase in voltage summits is observed when the input signal changes from "01" to "11". This can be attributed to the increased charge stored in the E-mode HEMT due to the increase in C_{gs}, which releases more charge at the stage "11" input signal.

V. THE FITTING BETWEEN THE ASM MODEL SIMULATED DATA AND EXPERIMENTAL RESULT

After establishing the correlations between device capacitance and circuit performances in Sections III and IV, it would be easier to exploit these conclusions to match the switching waveform of the three circuits in Figure 7. All the GaN H-treated devices are also based on the platform proposed in that work [25]. Because all the experiments and simulations focus on the monolithic GaN HEMTs, the devices' capacitance in this section is meaningful for exploring the All-GaN HEMTs circuits.

The Figure 11 and Figure 12 correspond to the Inverter circuit. Specifically, Figure 11 depicts the inverter circuits' precise voltage transfer curve fitting, which captures the input voltage range of 0 V to 5 V. The Inverter dynamic circuits are featured in Figure 12, with the upper figure representing the output at 100 kHz frequency and the lower figure corresponding to a frequency of 500 kHz. However, there are some voltage swings at the low output voltage. These ringing voltages are mainly caused by the parasitic inductive effect when V_{out} directly connecting to the ground. Figure 13 compares simulation and experimental results of NAND gate at a frequency of 100 kHz. The upper and lower figures correspond to different input phases. In Figure 14, the output response of the comparator circuit is fitted at different reference voltages from 2 V to 4 V, with a step voltage of 0.5 V. Although the simulation data still shows small deviations compared to the experimental data due to the non-ideality of the real test environment setup, the results demonstrate the ASM-GaN workflow's feasibility in modeling the monolithic IC's dynamic characteristics.

VI. CONCLUSION

This research marks a significant milestone as it accurately models H-treated p-GaN gate devices using the ASM-GaN

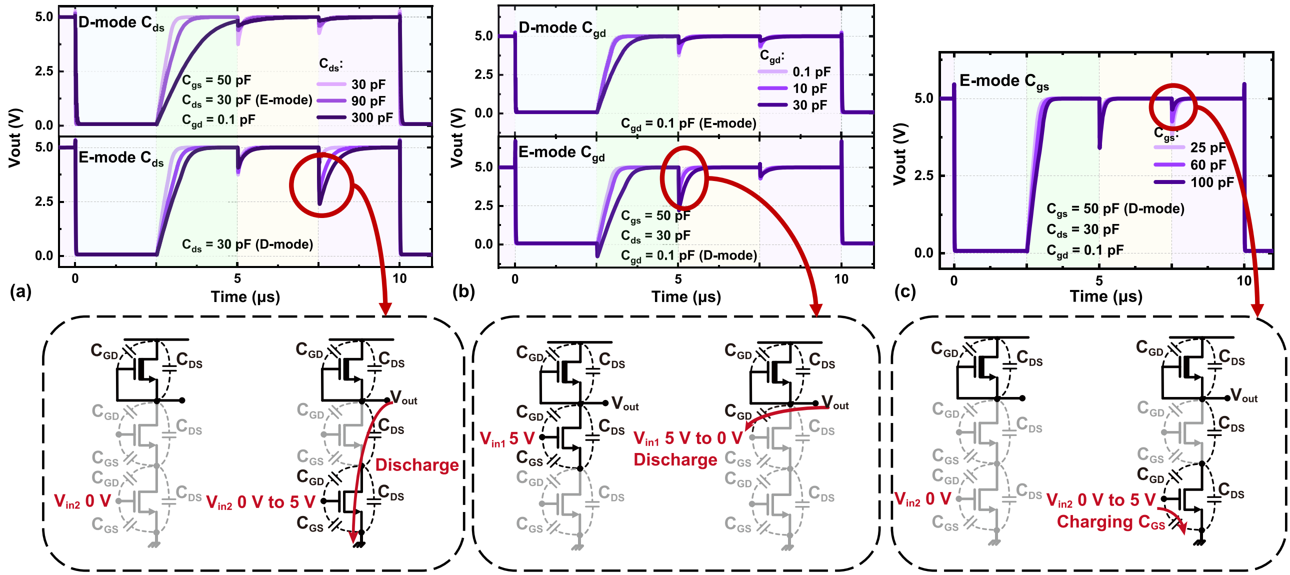


FIGURE 10. (a) The simulated switching waveform at the frequency of 100 kHz, setting (a) C_{ds}, (b) C_{gd} and (c) C_{gs} of E-mode and D-mode HEMTs as variables in NAND circuits.

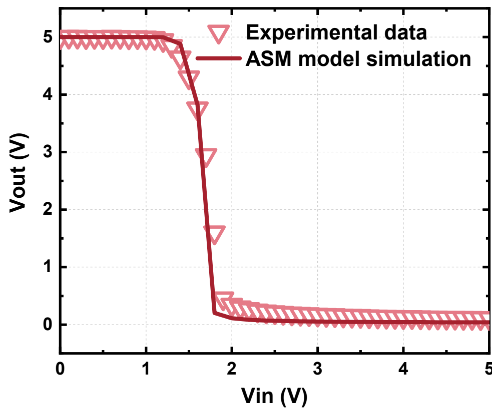


FIGURE 11. The fitting of inverter circuit's voltage transfer curve between experiment data (dotted line) and ASM model simulation data (solid line).

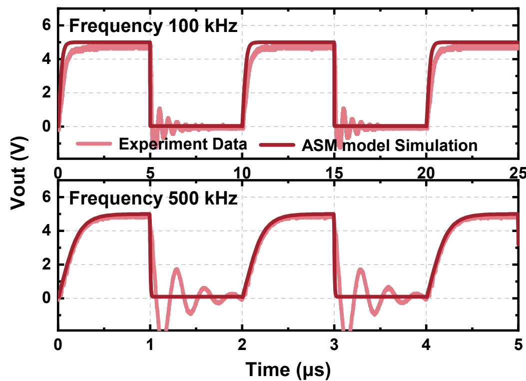


FIGURE 12. The fittings of inverter's switching waveform between experiment data (light colored line) and ASM model simulation data (dark colored line) at 100 kHz and 500 kHz.

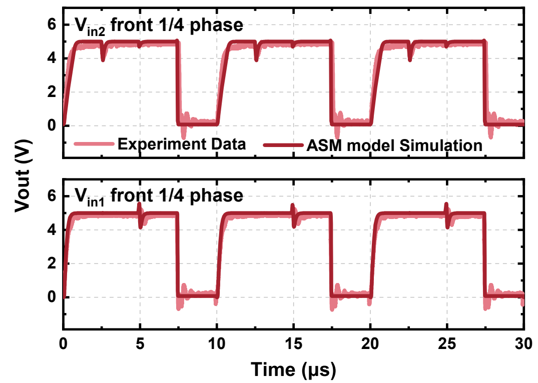


FIGURE 13. The fitting of the NAND circuit's switching waveform between experiment data (light colored line) and ASM model simulation data (dark colored line) at 100 kHz, with two different phases.

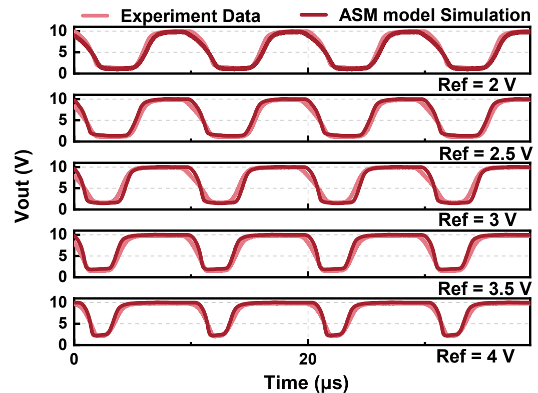


FIGURE 14. The fitting of comparator circuit's switching waveform between experiment data (light colored line) and ASM model simulation data (dark colored line), within reference voltages equal to 2 V, 2.5 V, 3 V, 3.5 V, and 4 V.

model, a novel workflow for ASM-GaN model parameter extraction and optimization using IC-CAP is proposed. The I-V characteristics of both E/D mode devices are modeled and fitted. Through ASM model analysis, the effect of device capacitance on the dynamic characteristics of monolithic

ICs is thoroughly investigated. The results reveal distinct effects of parasitic capacitance C_{ds}, C_{gd} and C_{gs}. This study presents an efficient method for accelerating GaN monolithic IC design through accurate modeling and rapid parameter extraction for advancing GaN monolithic IC applications, enabling scalable and robust designs, independent of fabrication processes.

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