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A 4H-SiC CMOS SPICE Level 3 Model for Circuit Simulations

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***Abstract*— In this paper, a compact DC SPICE model for 4H-SiC lateral metal oxide semiconductor field effect transistors is shown both for PMOSFET and NMOSFET. It is validated through experimental comparisons by varying channel sizes, temperature in the range between 298K and 573K, and body voltage conditions. A new model of the threshold voltage is introduced in order to take into account the effects of the high interface defects density. Finally, an inverter logic gate is simulated at different temperatures and compared with experimental data and with BSIM4SiC simulation outcomes, where a maximum logic threshold voltage error of 0.85% to the experimental data is shown compared to 6.78% of BSIM4SiC.**

***Index Terms*— 4H-SiC CMOS technology, circuit simulation, interface state density, SPICE modeling.**

I. Introduction

4H-SILICON CARBIDE, 4H-SiC, semiconductor devices are suitable for high temperature applications thanks to its intrinsic physical properties [1] and the operation of integrated circuits above $473K$ has been frequently shown. For example, 4H-SiC Bipolar Junction Transistor ICs operate up to $773K$ [2], but they need a multi-epitaxial layer stack [3], which limits the complexity of the circuits and makes the fabrication process expensive. Recently, a 4H-SiC Complementary Metal Oxide Semiconductor, CMOS, technology has been made available [4] and digital and analog ICs have been demonstrated up to $873K$ [5]. Moreover, the possibility to integrate circuits with other devices, like UV sensors [6], opens to new application fields.

To design ICs, the device models have to accurately predict the electrical behaviors, but, up to now, only a few of 4H-SiC lateral MOSFETs models are available both due to the recent technology development and due to the high density of $SiO_2/4H-SiC$ interface defects. Indeed, the threshold voltage, V_{TH}, and the channel mobility, μ_{CH}, have a different dependency on the electrical parameters as well as on the temperature compared to the Silicon ones. In [7] a modified version of BSIM4 model, BSIM4SiC, has been proposed, instead [8] shows a surface-potential based model, named PSP, which takes into account the interface state defects. In this scenario, SPICE Level 3-based model can be a good trade-off between complexity and accuracy, but only a few of them are available in literature. For example, [9] reports the SPICE parameters only at room temperature and extracts V_{TH}-values by using the linear extrapolation method, which is unreliable when the interface defects density is high [10]; instead, [11] shows a DC SPICE Level 3 model, but it is only for NMOSFETs for a fixed geometry of the channel and without temperature effects.

In this paper we propose a SPICE Level 3 Compact DC model for 4H-SiC lateral NMOSFETs and PMOSFETs operating under different bias conditions and temperatures. The geometry dependencies are taken into account as well as body effects through a semi-empirical model of V_{TH} and experimental comparisons are shown with single devices and with an integrated CMOS logic circuit. The model is suited for analog and digital circuits and it is focused on strong inversion conditions and long channel devices.

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II. Proposed SPICE Model

In Fig.1 our DC SPICE model for a 4H-SiC lateral MOSFETs has a Level 3 MOSFET, M_1, a voltage controlled voltage source, E_1, a current controlled current source, F_1, and two switches. The total current, I_{DS}, is as follows:

$$I_{DS} = I_{DS,1} + I_{DS,2} \tag{1}$$

where $I_{DS,1}$ is imposed by M_1 [12], whose parameters are in Tab.I, instead $I_{DS,2}$ by F_1 and has the following expression:

$$I_{DS,2} = I_{DS,1}(1 + \zeta V_{SB})^{-1} - I_{DS,1} \tag{2}$$

In (2) ζ is a fitting parameter, which allows to introduce the reduction of I_{DS} due to the channel mobility decrease when positive V_{SB} are applied in the case of NMOSFETs [13]. For $V_{GS} > V^*_{TH}$, the gate-source voltage, V^*_{GS}, of $M1$ is imposed by E_1, (SW_1 ON and SW_2 OFF) and is equal to:

$$V^*_{TH} = \alpha_2(T)V^2_{GS} + \alpha_1(T)V_{GS} + \alpha_0(T) \tag{3}$$

instead, V^*_{GS} is null when $V_{GS} \leq V^*_{TH}$ (SW_1 OFF and SW_2 ON). Eq.(3) improves the basic Level 3 SPICE model, because it describes the effects of the defects at the $SiO_2/4H-SiC$ interface on the overall electrical behaviours. Indeed, the V_{TH}-dependency on the bias gate voltage, due to the trap charge density at the interface, either is a complex function, like Gauss hypergeometric function [14], or needs iterative

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approaches [15], making unreliable any V_{TH}-extraction techniques as well as unfeasible any SPICE models. Instead, (3) considerably simplifies the complex dependency of V_{TH} on the bias gate voltage and permits its easy implementation in SPICE. In Tab.I all the parameters of the model are reported and also valid for PMOSFET, where V_{GS}, V_{DS}, V_{SB} and I_{DS} are changed with V_{SG}, V_{SD}, V_{BS} and I_{SD}, respectively. It is worth to note that, although the model is the same for both transistors, the different effects of interface traps on devices characteristics are described through the different coefficients of Tab.I, where, for example, a linear dependency on V_{SG} is found for PMOSFET whereas a quadratic one for NMOSFET.

III. Results

Measured and modeled output characteristics of the MOSFETs with different channel lengths, $L \in [6;10]\mu m$, and widths, $W \in [10, 100]\mu m$, at room temperature and $V_{BS} = 0V$ are shown in Fig.2.a)-c) and Fig.2.g)-i), where the maximum errors of the model from experiments are of 9.7% for NMOSFETs and of 8.9% for PMOSFETs. The only discrepancy between experimental and model results is in the transition from linear to saturation regions, where there is an overestimation of the current of $+9.7\%$ for the 20/6 NMOSFET at $V_{GS} = 20V$. This soft-transition is still unclear, but it could be ascribed to the reduction of the channel mobility due to the high longitudinal electric field, which induces the saturation of the carrier velocity, and, simultaneously, to the surface roughness scattering when high transversal electric field is applied [16].

TABLE I
SPICE parameters of the Proposed Model.

Parameter		Unit	Value NMOS	PMOS
.LEVEL=3				
GAMMA	γ	$[V^{0.5}]$	γ_0	
DELTA	δ	$-$	δ_0	
ETA	η	$-$	η_0	
THETA	θ	$[V^{-1}]$	θ_0	
UO	μ_0	$[cm^2V^{-1}s^{-1}]$	μ_{00}	
PHI	$2\varphi_F$	$[V]$	φ_0	
KAPPA	K	$-$	1	
NSUB	N_{SUB}	$[cm^{-3}]$	10^{17}	10^{16}
TOX	t_{ox}	$[m]$	$55 \cdot 10^{-9}$	
VMAX	v_{max}	$[m\,s^{-1}]$	v_{max00}	
VTO	V_{T0}	$[V]$	0	
.PARAM				
ALPHA0	α_0	$[V]$	$\alpha_{01}[1+\alpha_{02}(T-T_0)^{\alpha_{03}}]$	
ALPHA1	α_1	$-$	$\alpha_{11}[1+\alpha_{12}(T-T_0)^{\alpha_{13}}]$	
ALPHA2	α_2	$[V^{-1}]$	$\alpha_{21}[1+\alpha_{22}(T-T_0)^{\alpha_{23}}]$	
ZETA	ζ	$[V^{-1}]$	$\zeta_{00}[1+\zeta_{01}(T-T_0)]$	
ETA0	η_0	$-$	$\eta_{00}+\eta_{01}L+\eta_{02}L^2$	
THETA0	θ_0	$[V^{-1}]$	$\theta_{01}[1+\theta_{02}(T-T_0)^{\theta_{03}}]$	
PHI0	φ_0	$[V]$	$\varphi_{01}[1+\varphi_{02}(T-T_0)]$	
U00	μ_{00}	$[cm^2V^{-1}s^{-1}]$	$\mu_{01}\,(1+\mu_{02}/W)\,(T/T_0)^{\mu_{03}}$	
VMAX00	v_{max00}	$[m\,s^{-1}]$	$v_{max01}[1+v_{max02}(T-T_0)^{v_{max03}}]$	
GAMMA0	γ_0	$[V^{0.5}]$	1.25	10^{-3}
DELTA0	δ_0	$-$	$5.79 \cdot 10^5 W$	$1.75 \cdot 10^5 W$
ZETA00	ζ_{00}	$[V^{-1}]$	$1.8 \cdot 10^{-1}$	$3.05 \cdot 10^{-13}/L^2$
ETA00	η_{00}	$-$	$-5 \cdot 10^{-1}$	-22.5
THETA01	θ_{01}	$-$	$1.1 \cdot 10^{-2}$	$8.52 \cdot 10^{-7}/L^{0.865}$
U01	μ_{01}	$[cm^2V^{-1}s^{-1}]$	22	$32 \cdot 10^{-3}/L^{0.436}$
VMAX01	v_{max01}	$[m\,s^{-1}]$	$0.03/L$	$15.39/L^{0.52}$
ALPHA01	α_{01}	$[V]$	$1.9 \cdot 10^{-2}$	-11
ALPHA02	α_{02}	$[K^{-\alpha_{03}}]$	$9.6 \cdot 10^{-3}$	$-2.9 \cdot 10^{-2}$
ALPHA03	α_{03}	$-$	1	$4.3 \cdot 10^{-1}$
ALPHA11	α_{11}	$-$	$7 \cdot 10^{-2}$	1.23
ALPHA12	α_{12}	$[K^{-\alpha_{13}}]$	$9.6 \cdot 10^{-2}$	$-4.7 \cdot 10^{-4}$
ALPHA13	α_{13}	$-$	$7.4 \cdot 10^{-1}$	1
ALPHA21	α_{21}	$[V^{-1}]$	$3.1 \cdot 10^{-2}$	0
ALPHA22	α_{22}	$[K^{-\alpha_{23}}]$	$-1.4 \cdot 10^{-3}$	$-$
ALPHA23	α_{23}	$-$	1	$-$
ZETA01	ζ_{01}	$[K^{-1}]$	$-2 \cdot 10^{-3}$	$6 \cdot 10^{-3}$
ETA01	η_{01}	$[m^{-1}]$	$-5 \cdot 10^4$	$4.75 \cdot 10^6$
ETA02	η_{02}	$[m^{-2}]$	$5 \cdot 10^{10}$	0
THETA02	θ_{02}	$[K^{-\theta_{03}}]$	$3.4 \cdot 10^{-3}$	$-4.54 \cdot 10^{-1}$
THETA03	θ_{03}	$-$	1.14	$1.3 \cdot 10^{-1}$
U02	μ_{02}	$[m]$	$1.4 \cdot 10^{-6}$	$9.1 \cdot 10^{-7}$
U03	μ_{03}	$-$	$6 \cdot 10^{-1}$	$8.4 \cdot 10^{-1}$
PHI01	φ_{01}	$[V]$	2.97	2.85
PHI02	φ_{02}	$[K^{-1}]$	$-5.9 \cdot 10^{-4}$	$-7.5 \cdot 10^{-4}$
VMAX02	v_{max02}	$[K^{-v_{max03}}]$	$8.8 \cdot 10^{-3}$	$2 \cdot 10^{-3}$
VMAX03	v_{max03}	$-$	$8.8 \cdot 10^{-1}$	$4 \cdot 10^{-1}$
T0	T_0	$[K]$	298.15	298.15

L is expressed in $[m]$

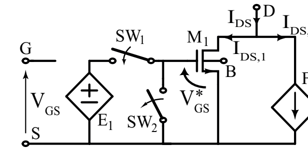

Fig. 1. Circuit of the proposed SPICE model.

In Fig.2.d)-f), .j)-l), temperature and body effects on NMOSFETs and PMOSFETs characteristics are reported as well as the trans-characteristics of Fig.3.a)-b) also highlights the temperature effects. Indeed, the model describes the increase of the current with the temperature both in linear region (see Fig.3.a)-b) at $V_{DS} = V_{SD} = 1V$) and in saturation region (see Fig.3.a)-b) at $V_{DS} = V_{SD} = 20V$) and also the reduction with the increase of the body bias. The temperature dependency can be ascribed to the combined effects of V_{TH} reduction and channel mobility increase due to the decrease of the occupied interface trap density and the prevalence of Coulomb scattering mechanism [16], [17]. Such behaviour is completely opposite to Silicon one and makes inadequate the classical SPICE parameters temperature dependence [12] for 4H-SiC MOSFETs. For this reason, our model introduces new temperature dependencies, as reported in Tab.I: *i*) the channel mobility depends on $(T/T_0)^{\mu_{03}}$, where μ_{03} has positive values for both MOSFETs; *ii*) the reduction of V_{TH} with the temperature has been described through a temperature dependence of α_0, α_1, and α_2 parameters of (3); *iii*) v_{max}, ζ and θ also depends on the temperature.

In Fig.2.d)-f) the body effect is evident for NMOSFET, also at different temperatures, where I_{DS} reduces with positive V_{SB} as expected [1], instead PMOSFET shows a weak dependence on V_{BS}, as reported in Fig.2.j)-l). Comparing our model with experimental curves in $T \in [298;573]K$ and $V_{SB} = [0;12]V$, I_{DS} of NMOSFET shows an error of 6.6% respect to the 10% of PMOSFET at $T = 573K$ and $V_{BS} = 12V$ (see Fig.2.l), which is acceptable considering the low complexity of the model and the wide temperature range for the comparison. Moreover, it is worth to note that 4H-SiC PMOSFETs are generally biased at $V_{BS} = 0V$ because their series connections are avoided due to the low $\mu_{CH,p}$ and the high $V_{TH,p}$ values. In literature there are studies about the effects of the body bias on the PMOSFETs parameters, but further analysis are required because they are unable to fully describe the phenomenon: for example [16] shows that the surface roughness scattering mechanism reduces the

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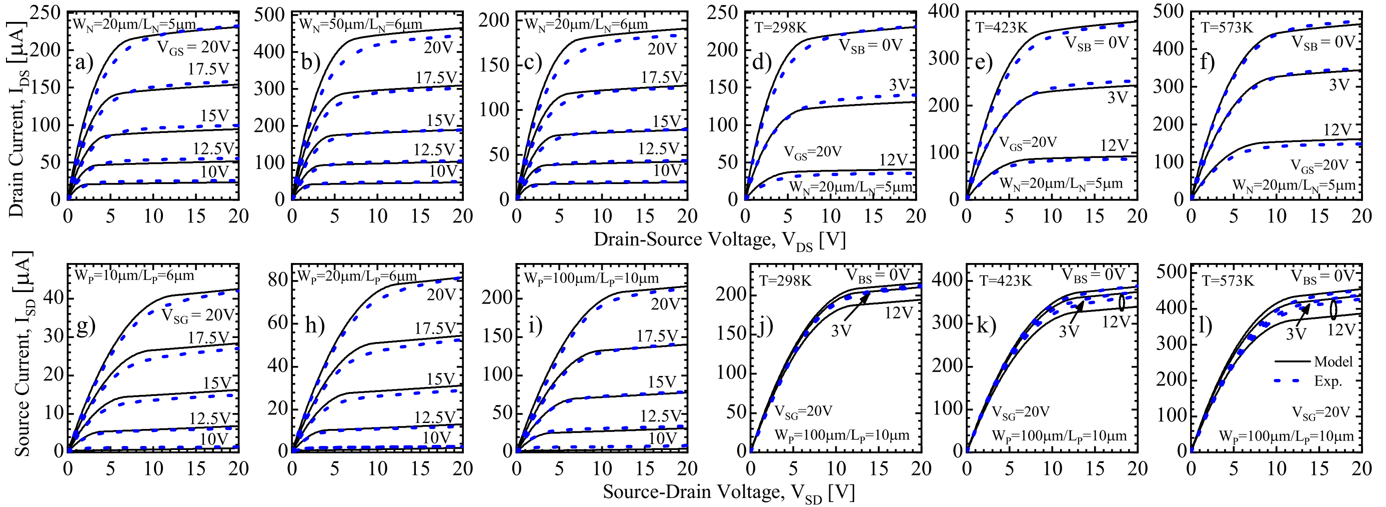

Fig. 2. Comparisons between SPICE model and experimental characteristics. Geometry dependencies of NMOSFETs (a)-c)) and of PMOSFETs (g)-i)) at various gate voltages and at T=298K. Body and temperature effects for NMOSFET (d)-f)) and of PMOSFET (j)-l)) at $\boldsymbol{V_{GS} = V_{SG} = 20V}$.

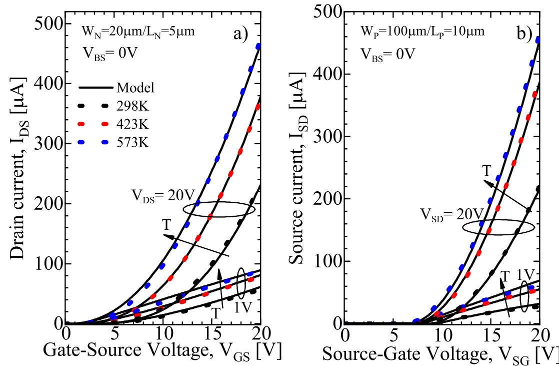

Fig. 3. Comparisons between SPICE Model and experimental trans-characteristics for a)NMOSFET and b) PMOSFET.

$\mu_{CH,p}$ by -50% under body bias conditions, which is too high in comparison to the -1.02% of I_{SD} observed in our measurements, and, therefore, an enhancement phenomena is expected to counterbalance $\mu_{CH,p}$ reduction.

To further validate our model, in Fig.4 we compare the experimental results of [18] for a 4H-SiC CMOS inverter

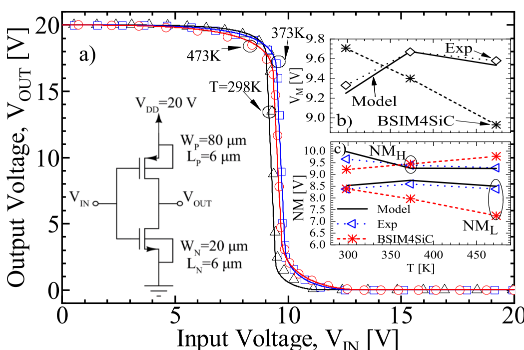

Fig. 4. a) Comparison between SPICE model and [18] of 4H-SiC CMOS NOT trans-characteristic. In the insets, comparisons of b) $\boldsymbol{V_M}$ and of c) $\boldsymbol{NM_{L,H}}$ between SPICE, BSIM4SiC and measurements.

gate ($W_P/L_P = 80/6$ and $W_N/L_N = 20/6$) characterized along the temperature range $T \in [298; 473]K$, together with numerical simulations performed through a BSIM4SiC model [19]. It is worth to note that we decided to choose experimental data from literature in order to generalize and to extend the applicability of the model. Beyond the good description of the characteristics in the whole voltage range, our model correctly predicts them for each temperature value. In particular, it is interesting to note that our model describes the temperature behaviour of the threshold logic voltage, V_M, starting from $9.33V$ at room temperature, increasing to $9.67V$ at $T = 373K$ and, then, reducing to $9.58V$ at $T = 473K$, (see the inset b) of Fig.4). Contrarily, BSIM4SiC model shows an incorrect monotonic temperature behaviour of V_M as well as a minimum error of 2.79% at $T = 373K$, which is much higher than the maximum error of our model, equal to 0.85% at $T = 298.15K$. Furthermore, the high, NM_H, and low, NM_L, noise margin errors of the inset c) of Fig.4 are, respectively, 3.26% and 1.79% at $T = 298K$ for our model and, respectively, 13.62% and 5.23% at $T = 473K$ for BSIM4SiC ones.

IV. CONCLUSIONS

A compact DC 4H-SiC MOSFET SPICE Level 3 model is proposed for strong inversion conditions, taking into account temperature, geometrical and body bias dependencies. Comparisons with experimental single devices and circuit, combined with simulation outcomes when higher order models are used, highlight a good trade-off between complexity and accuracy of the model. Indeed, due to the high density of traps at the interface, our model describes the unusual V_{TH}-behavior with a quadratic equation easily implementable in a SPICE simulator. Moreover, although simulations of digital circuits are shown, the good description of the electrical characteristics in the saturation region and the absence of discontinuity of the curves permit a small-signal AC analysis at a low frequency range used in analogue circuit simulations.

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