4H-SiC Radiation Hardened Static Random Access Memory

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***Abstract*— 4H-SiC static random-access memory (SRAM) was suggested and demonstrated for extreme-environment applications. The 4H-SiC SRAMs show the proper memory states with high static noise margins (SNMs). After exposure to a significant gamma-ray radiation of 810 kGy, the SRAMs continued to function effectively, maintaining positive SNM values necessary for proper memory operation. After the gamma-ray radiation, the SRAM operation was tested at high temperature, and it continued to function normally even at temperatures as high as 500°C.**

***Index Terms*— 4H-SiC, SRAM, CMOS, total ionization dose effect, high temperature.**

I. Introduction

SILICON Carbide (SiC) is an increasingly promising wide bandgap semiconductor for power electronics, now being integrated into electric vehicles (EV) and bullet trains. This trend is driven by SiC's superior material properties, such as its high breakdown electric field and exceptional thermal conductivity, making it ideal for power electronics applications. Beyond these attributes, the SiC has high electron-hole pair creation energy and high atomic displacement energy. These properties allow us to enhance our application area of electronics in extreme environments with high temperatures and high radiation, such as space exploration, nuclear power stations, and nuclear fusion reactors. In Japan, we are facing the decommissioning of the Fukushima Daiichi Nuclear Power Station, which was damaged by a heavy earthquake and tsunami in 2011. For that, radiation-hardened electronics have been strongly requested.

The SiC electronics for extreme environments are mainly requested such as, radiation-hardened image sensors, amplifier circuits, and logic processors. The SiC image sensors for extreme environments have been suggested and demonstrated. UV imaging with 4H-SiC has been demonstrated with image sensors based on 4H-SiC bipolar transistors [1]. Similarly, 4H-SiC active pixel sensors (APS) for CMOS image sensors, utilizing 4H-SiC MOSFETs, have been suggested and successfully demonstrated [2]. These 4H-SiC APSs remained operational after 2 MGy(H_2O) gamma-ray irradiation, and real-time operation of 4H-SiC 64 pixels CMOS image sensors has been demonstrated [3]. For visible light detection, a hybrid-type CMOS image sensor with 4H-SiC MOSFETs and Si photodiode has been suggested [4]. For the logic circuits for the high temperature at around 500°C, 4H-SiC bipolar junction transistors (BJTs), 4H-SiC junction field effect transistors (JFETs), and 4H-SiC metal-oxide-semiconductor transistors (MOSFETs) have been demonstrated [5], [6], [7], [8], [9], [10], and high radiation-hardness of the SiC devices have been reported [11], [12], [13], [14]. 4H-SiC BJT and MOSFETs were demonstrated at up to 3.4 MGy(SiO_2) [12] and 1.13 MGy(SiO_2) [13], respectively. The device operation of 4H-SiC JFETs after 17 MGy(H_2O) was also reported [14].

SiC CMOS circuits have been reported for the extreme environment applications [15]. With SiC NMOS and PMOS, CMOS operation has been demonstrated at a high temperature of 200°C [16]. 4H-SiC CMOS gate buffer circuits combined with SiC power devices are also suggested for reducing parasitic inductance [17]. On the other hand, the modern microprocessor consists of logic circuits for arithmetic logical unit (ALU) and memory circuits for registering data as its fundamental circuits. In the microprocessor, for the computation, reading and writing operations are executed at the register memory circuits, and then memory devices are used. Static random-access memory (SRAM) is the most common volatile memory for the register in silicon microprocessors. For developing the 4H-SiC CMOS large-scale integrated circuits, the SiC SRAM will be indispensable. The SiC SRAM has been reported as a component of SiC digital circuits [18], and its operation of up to 200°C with a source voltage of 20 V was demonstrated. For deriving more performance of SiC integrated circuits for harsh environment applications, the radiation hardness and the high temperature operations of the SRAM are strongly required. Recently, the radiation hardness of fully depleted Silicon-on-Insulator (FD-SOI) SRAM has been reported [19], [20]. The experimental total ionization dose (TID) results show that the FD-SOI SRAM cells are robust to doses around 200 krad(Si)(=2 kGy(Si)) [19],

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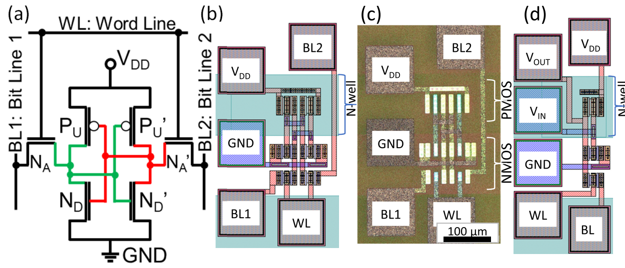

Fig. 1. 4H-SiC SRAMs: (a) circuit, (b) device layout, (c) microphotograph of the fabricated SRAM circuit, (d) layout of the SRAM half-cell invertor.

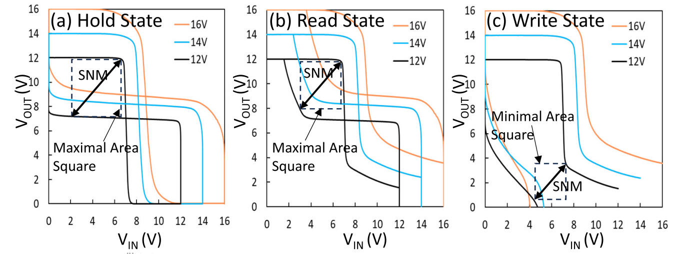

Fig. 2. Output characteristics of the 4H-SiC SRAM half-cell invertor: (a) hold state, (b) read state, (c) write state.

and static noise margin (SNM) of the read state became zero at 500 krad(Si) (=5 kGy(Si)) [20]. While FD-SOI SRAMs are suitable for radiation levels in the kGy range, achieving radiation hardness beyond 10 kGy requires the use of other semiconductor materials for SRAMs.

In this study, we designed and fabricated 4H-SiC SRAM with 4H-SiC CMOS and demonstrated its operation successfully with a source voltage of 12 V. We also investigated the SRAM operations after high gamma-ray radiation of 810 kGy.

II. Experiment

4H-SiC 6T(transistor)-SRAMs with 4 NMOS and 2 PMOS were designed and fabricated. The circuit and layout of the SRAM are shown in Fig.1 (a) and (b). The half-cell invertors with word line and bit line were also fabricated for noise margin characterization. The channel length of NMOS and PMOS was 2 μm. The channel widths were designed with SPICE simulation. The fabrication process closely followed our previous works [2], [8], [9], except for the n-well formation. The 4H-SiC n-well region was formed by n-type 4H-SiC epitaxial deposition after forming deep trench structures. A 4H-SiC P-type epitaxial layer was formed on a 4H-SiC (0001) 4° off-axis substrate. The thickness was 5 μm and the impurity density was 5×10^{16} cm^{-3}. For the n-well structure formation, after a lithography for the well region, Bosch etching on the SiC layer was carried out with gases of SF_6 and C_4F_8, and the SiC etching depth was 6 μm. After the deep etching, n- epitaxial layer was grown up by high-temperature CVD. The impurity concentration was 8×10^{15} cm^{-3}. Chemical mechanical planarization (CMP) was then performed to isolate n-well regions. For source/drain formation, SiO_2 was formed for the hard mask of high-temperature ion implantation. The SiO_2 hard mask was formed by APCVD at a thickness of 400 nm. After lithography for the n+ region, ion implantation was carried out at 500°C. The impurity was arsenic, and the ions were implanted at the depth of 70 nm for forming uniform impurity concentration in the SiC substrate. The impurity concentration was 5×10^{19} cm^{-3}. After removing the SiO_2 hard mask layer, an APCVD SiO_2 layer was deposited again for p+ region formation. This p+ region contained source and drain regions of the PMOSs and body contacts of the NMOSs. After lithography for the p+ region, the ion implantation with the impurity concentration of 4×10^{20} cm^{-3} was carried out, and the implanted impurity was aluminum. After the two ion-implantations, a carbon layer was formed on the SiC substrate, and activation annealing was applied at a temperature of 1700°C. After the impurity activation, thick SiO_2 of 500 nm was deposited by LPCVD. After a lithography for gate regions, the SiO_2 region was patterned by a wet etching with buffered hydrofluoric acid (BHF) treatment. After that, thermal oxidation was carried out at 1150°C. The thickness was 15 nm. The gate oxide was treated with a post-oxidation annealing (POA) [21]. In this process, the wet-POA with H_2O and O_2 was carried out to reduce PMOS's threshold voltage. After the gate oxide formation, contact vias were formed on the source and drain regions. For the via formation, SiO_2 was removed at this region, and Ni and Nb were deposited by a sputtering method and were annealed for forming silicide contacts [22]. Al gate electrodes and the first metal wiring layer were formed simultaneously, followed by the formation of three additional Al metal wiring layers and dielectrics [2]. After that, the samples were treated with H_2 annealing at 400°C. The microphotograph of the fabricated SRAM is shown in Fig.1 (c).

III. Results and Discussion

A. 4H-SiC SRAM Operations

The output characteristics of the 4H-SiC SRAM was measured using the half-cell invertors at the "hold", "read" and "write" states. Figure 2 shows the output characteristics of the three states. The measurements were carried out at the power supply voltage of V_{DD} = 12, 14, and 16 V. The butterfly curves of the "hold" states showed proper SRAM characteristics with the wide SNMs. The SNMs are defined by the length of the diagonal of the maximal area square as shown in Fig.2. And at $V_{IN} = 0$ and $V_{IN} = V_{DD}$, in which NMOS and PMOS in the SRAM were turned off, the output voltage kept the values at $V_{OUT} = V_{DD}$ and $V_{OUT} = 0$, respectively, in other word voltage drops were not observed, then any leakage currents were ignorable. As the V_{DD} value increased, the ON regions of both NMOS and PMOS transistors expanded, and the logical switching points stabilized at approximately half of the V_{DD} value. Figure 3 shows the SRAM memory operations. In the writing operation, at first, the bit lines 1 and 2 were set to be V_{DD} and 0 V respectively, and the word line was turned on to be V_{DD}, and the SRAM cell became a "1" state. In the read operation, the bit lines were initially pre-charged to V_{DD} and then left floating, after which the word line was activated. At this state, a voltage drop was observed at the bit line 2, indicating that the SRAM cell retained the "1" state, thus confirming a successful read operation. The writing-and-reading "0" state in the 4H-SiC SRAM were also successfully performed.

B. Total Ionization Dose Effects

The radiation experiments were carried out in the Co-60 radiation facility, in QST, Takasaki, Japan. The gamma-ray dose rate was 9 kGy(H_2O)/h and irradiated up to 810 kGy(H_2O). Figure 4 shows the transfer characteristics of the 4H-SiC MOSFETs and output characteristics

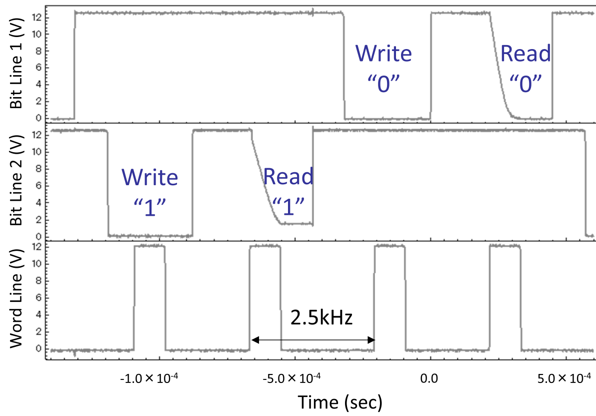

Fig. 3. Writing-reading operation characteristics of the 4H-SiC SRAM cell.

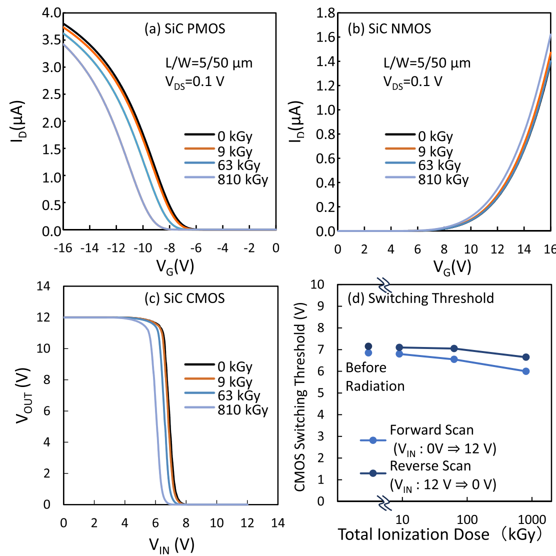

Fig. 4. Transfer characteristics of the 4H-SiC MOSFETs and output characteristics of the 4H-SiC CMOS invertor after gamma-ray radiation: (a) PMOS, (b) NMOS, (c) CMOS, and (d) switching threshold.

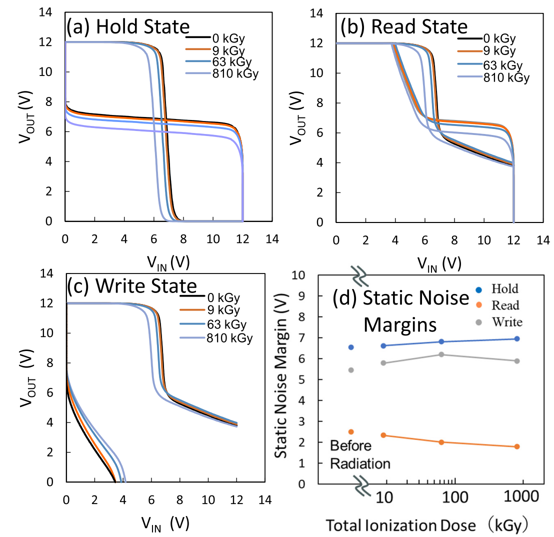

Fig. 5. Output characteristics of the 4H-SiC SRAM half-cell invertor after gamma-ray radiation: (a) hold state, (b) read state, (c) write state, and (d) static noise margins (SNMs).

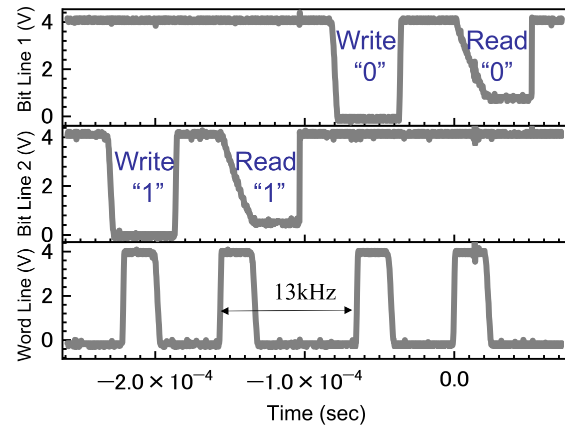

Fig. 6. Writing-reading operation at 500°C of the 4H-SiC SRAM cell after high gamma-ray radiation of 810 kGy.

of the 4H-SiC CMOS invertor after gamma-ray radiation. The NMOS was relatively stable to the radiation, however, the PMOS threshold voltage was decreased slightly by the 810 kGy radiation. This threshold voltage reduction in the PMOS induced a reduction of the CMOS switching threshold shown in Fig. 4 (d). Figure 4 (d) also shows the difference of the switching threshold between forward and reverse scans slightly increased after the gamma-ray exposure. Figures 5 (a), (b), and (c) show the output characteristics at the "hold", "read" and "write" states of the SRAM half-cell invertor. After exposure to the high radiation dose of 810 kGy, the half-cell inverter maintained its output characteristics, with the SNMs remaining sufficient for reliable memory operation. Figure 5 (d) shows the SNMs as the function of total ionization dose. As the radiation increased, the "write" states' SNM slightly increased, on the other hand, the "read" states' SNM decreased. This is because positive charges remained in the gate oxide after the radiation, and threshold voltage was shifted to the negative side at both NMOS and PMOS and then the NMOS current increased, however, the PMOS current decreased, as shown in Figs. 4 (a) and (b). The increased current in the pass-gate NMOSs along the word line enhanced the stability of the "write" state but reduced stability in the "read" state. For more radiation hardness, it is necessary to combine the device design for reducing positive charges in the gate oxide and circuits designs for keeping the memory stable. Following the 810 kGy radiation dose, the SRAM operation was further tested at a high temperature of 500°C. Figure 6 shows the operation characteristics at 500°C. The operation frequency was 13 kHz. The writing-and-reading operations on the 4H-SiC SRAM were successfully observed.

IV. Conclusion

A 4H-SiC SRAM was successfully designed and fabricated with 4H-SiC CMOS technologies. With the SRAM half-cell invertor, the "hold", "write" and "read" states were investigated, and these states showed enough static noise margins for the SRAM operation. At the 4H-SiC SRAM cell, the writing-and reading operations of "1" and "0" states were successfully performed. The effects of high gamma-ray irradiation were also evaluated, with the SRAM maintaining functionality even after exposure to a total dose of 810 kGy, and all SNMs remaining positive Additionally, the SRAM demonstrated operational capability at elevated temperatures of up to 500°C. These results indicate that 4H-SiC SRAM holds significant potential as volatile memory for extreme-environment applications.

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