# Thermionic Field Emission in the Lifetime Estimation of p-GaN Gate HEMTs

G. Greco, P. Fiorenza, F. Giannazzo, M. Vivona, C. Venuto, F. Iucolano, and F. Roccaforte

***Abstract*— The current transport mechanism at metal gate/p-GaN interface in p-GaN HETMs has been investigated. Space Charge Limited Current (SCLC) well describes the behaviour of current density ($J_G$) at lower applied bias ($V_G$ < 6 V), while Thermionic Field Emission (TFE) represents the dominant current mechanism at higher $V_G$. Then, p-GaN gate reliability was investigated by time-to-failure (TTF) analysis carried out at constant positive $V_G$. In particular, the devices' lifetime as function of the applied $V_G$ was described considering the $J_G$-$V_G$ dependence according the TFE model. In this way, a maximum $V_G$ for 10-year lifetime ($V_{Gmax}^{10\ years}$) of 8.5 V has been estimated, significantly higher than that extracted by conventional E-model (7 V).**

***Index Terms*— Gallium nitride, normally-off HEMT, p-GaN.**

## I. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are considered key devices for next generation of high-frequency and high-power electronics [1]. The spontaneous presence of the two-dimensional electron gas (2DEG) in AlGaN/GaN heterostructures makes HEMTs inherently normally-on devices. However, in power electronics, normally-off operation is highly required [2]. In this context, the use of a p-GaN gate represent a consolidated pproach to deplete the 2DEG and obtain normally-off operation [3]. Here, the metal/p-GaN Schottky contact plays a crucial role in controlling the gate-leakage current ($I_G$). Indeed, an excess of the $I_G$ can lead to degradation of the electrical characteristics and compromise the device reliability. Consequently, understanding the current transport mechanisms at the p-GaN gate region under forward gate bias is very important to control the device behaviour and to properly address the reliability optimization [4], [5], [6]. The degradation of the p-GaN gate under forward bias was discussed in literature invoking different mechanisms. As an example, Tallarico et al. [7] attributed the device failure to a percolation path created by holes injection into the p-GaN through the metal/p-GaN interface. In fact, He et al. [8] highlighted the importance of a robust metal/p-GaN barrier to limit device degradation induced by hole injection. Hua et al. [9] introduced a thin n-GaN layer between the metal and the p-GaN to limit the hole injection through the metal/p-GaN barrier as well as the possible lateral leakage current. On the other hand, Tapajina et al. [10] justified the device failure by the generation of donor-like traps close to the p-GaN/AlGaN interface, which create localized leakage paths. Rossetto et al. [11] considered the device degradation originating from the high electric field within the SiN passivation and the p-GaN layer. In this context, Stockman et al. [12] emphasized the impact of the gate manufacturing processes on the leakage current transport mechanisms, especially at high forward bias. Indeed, for a correct prediction of the device lifetime and a full comprehension of its failure mechanisms, it is extremely important to establish the dominant gate current transport mechanism. In this letter, the gate current of p-GaN HEMTs has been studied and time-to-failure analysis has been performed at $V_G$ in the range of 9-10 V. At this gate bias level, the TFE model has been identified as the dominant current transport mechanism. Then, considering the $I_G$-$V_G$ correlation exhibited in the TFE model, it was possible correctly estimating the maximum gate bias for a ten years device lifetime.

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## II. Device Design and Fabrication

Normally-off p-GaN HEMTs have been investigated in this work. The p-GaN/AlGaN/GaN heterostructures grown on Si substrate, consisted of 18-nm-thick AlGaN barrier layer with a 20% Al content, and 90 nm thick p-GaN gate with a Mg concentration of $3 \times 10^{19}$ cm$^{-3}$. Ohmic contacts based on Ta were used to fabricate the source and drain electrodes, while the Schottky gate contact was a Ti-based metallization [13]. Small unit cell with dual finger gate HEMTs for 650V/200-mΩ application and with a threshold voltage ($V_{TH}$) of 1.2 V, has been investigated in our study. The access regions have been obtained by selectively removing the p-GaN layer using an Atomic Layer Etching in chlorine-based chemistry. The device electrical characterization has been carried out in a Karl–Suss MicroTec probe station equipped with a parameter analyser.

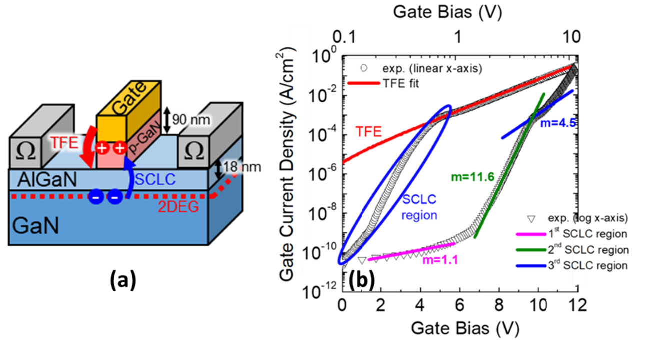


Fig. 1. Schematic cross section of the p-GaN HEMTs. Electrons (SCLC model) and holes injection (TFE model) involved in the current transport mechanism are indicated in the schematic (a). $J_G$-$V_G$ curves of the p-GaN HEMTs displayed in log-log (bottom) and semi-log (top) scale. The fits of the experimental data with the SCLC model and with TFE model are also reported (b).

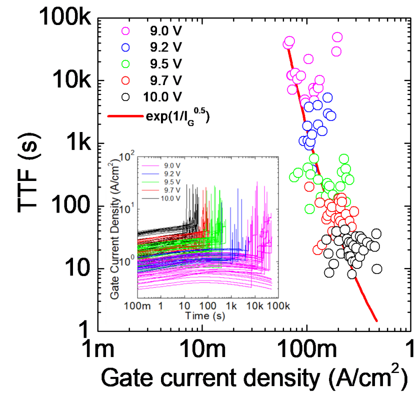


Fig. 2. Time-to-failure (TTF) as function of the gate current value before breakdown occurs. The continuous line depicts the TTF dependence on the $J_G$ according Eq. 2. In the inset the gate current as function of stress time.

## III. Results and Discussion

Fig. 1 reports the experimental $J_G$-$V_G$ characteristics of the device, acquired at room temperature in semi-logarithmic and Log-Log scale. As can be seen, the dependence of the gate current on the gate bias exhibits various slopes, indicating the occurrence of different transport mechanisms. Indeed, at lower $V_G$ (< 6 V), the gate current density $J_G$ can be described by a power law equation $J_G \propto V_G^m$. This behaviour is well evident in the Log-Log scale, where the exponent *m* assumes different values depending on the bias range. In particular, in OFF state for $V_G<V_{TH}$ the slope is quite low (m = 1.3), while by increasing the $V_G$ above the $V_{TH}$, once the 2DEG appears below the gate (ON state), the slope significantly increases up to m = 11.3. The change of the slope occurs at $V_G$ = 1.2 V, which corresponds to the $V_{TH}$ value estimated from the transfer characteristics of the p-GaN HEMTs. Such a behaviour can be explained considering a space-charge-limited current (SCLC) model in the presence of traps distribution in the semiconductor [14], [15]. In our specific case, the presence of traps in the AlGaN layer plays a key role in the current transport mechanism [16], [17]. Indeed, by increasing the gate bias ($V_G>V_{TH}$), the electrons injected into the AlGaN start filling up the traps in the semiconductor, resulting in a space charge region formation. A further increase in the applied bias induces the complete filling of these traps, limiting the additional injection of charges [18]. Indeed, by further increasing the gate bias the channel conductivity slightly decreases, generating a reduction in the slope of the J-V curve (m = 4.5). With

With a further increase of the bias ($V_G$ > 6 V), the $J_G$ displays an exponential behaviour on the gate bias, which depends on the properties of the metal/p-GaN interface and can be described by the TFE model [19]:

$$J_{G-TFE} \propto exp\left(-\frac{q\Phi_B}{E_0}\right)\cdot exp\left(\frac{qV_G}{kT}-\frac{qV_G}{E_0}\right) \quad (1)$$

with $q$ the elementary charge, $k$ is the Boltzmann constant, $\Phi_B$ the Schottky barrier height of the metal/p-GaN interface and $T$ the temperature. $E_0$ and $E_{00}$ are the tunneling parameter and the characteristic energy, respectively $E_0 = E_{00}\ coth\left(\frac{E_{00}}{kT}\right)$ and $E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_A}{m^*\epsilon}}$ with $\varepsilon$ and $m^*$ and $N_A$ the dielectric constant, the effective mass for holes in GaN and the doping concentration of the p-GaN. From the fit of the $J_G$-$V_G$ characteristics at high voltage, the $\Phi_B$ and $N_A$ of the metal/p-GaN interface have been determined, resulting 0.84eV and $1.1\times10^{18}$ cm$^{-3}$, respectively. The change from SCLC to TFE model occurring at about $V_G$ = 6 V is in agreement with the distribution of the potential drop across the metal/p-GaN/AlGaN/GaN heterostructure, considering the heterostructure properties as well as the metal/p-GaN barrier properties estimated by TFE fit [20].

Clearly, such parameters together with the involved transport mechanism (TFE) identified at high gate bias, have an influence on the expected device lifetime and reliability. This aspect has been carefully considered by a time-dependent-breakdown (TDB) analysis. To reach the device breakdown in a reasonable time (less than 12 hours), a gate bias stress $V_{Gstress}$ between 9 and 10 V was used. The time needed to reach the breakdown, defined as Time-To-Failure (TTF) was estimated for each $V_{Gstress}$. In Fig. 2 the measured values of TTF at the different gate bias stress has been correlated with the gate current density acquired before device breakdown ($J_{G-break}$). The inset of Fig.2 shows the gate current density as function of the stress time.

As can be seen, the gate current level increases with the bias stress value. This behaviour has been extensively investigated in Ref. 21. Such a continuous increase of the gate current was attributed to hole trapping effect. However, for a constant gate bias stress, the gate current density only weakly increases with the stress time, before undergoing a rapid increase that sets the device breakdown. As reported in [21], this effect could be correlated with the generation of new defects in the p-GaN gate region, which enhance the holes injection and cause the device failure. Interestingly, the observed TTF shows a significantly changes with gate bias condition, from hundred thousand of seconds (at lower $V_G$) to tens of seconds (at higher $V_G$). From the plot displayed in Fig.2, it was possible to establish a correlation between the TTF to the $J_{G-break,}$ (see

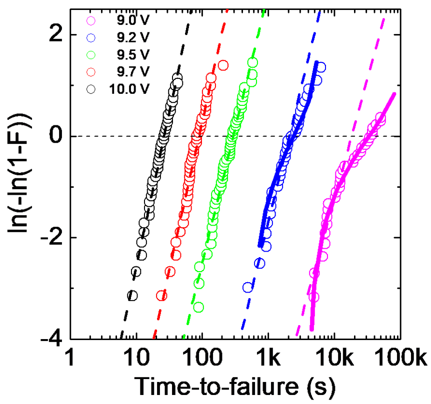


Fig. 3. The failure statistics analysed as ln(-ln(1-F)) as function of the time-to-failure for VG gate bias stress between 9 and 10 V. The dashed lines represent the failure behaviour predicted by Weibull distribution, while lognormal distribution is displayed by continues lines.

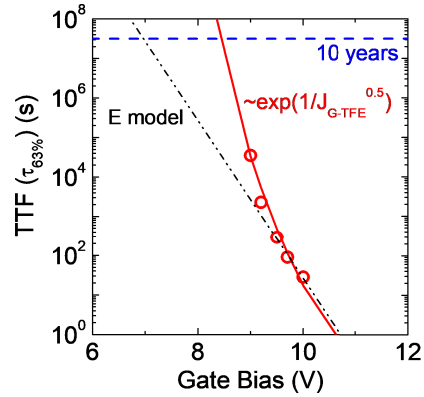


Fig. 4. Time to failure (TTF) versus gate bias stress. The black dot-dashed line represents the lifetime prediction by E-model. The red continuous line displays the calculation of the TTF taking into account the dependence of the $J_G$ on $V_G$ according the TFE model.

the continuous line in Fig.2b):

$$TTF \sim exp\left(\frac{1}{\sqrt{J_G}}\right) \quad (2)$$

Correlating the gate leakage current with the device time-failure is a debated topic. Tapajna et al. [10] extrapolated a power law behaviour with $TTF \sim \frac{1}{I_G}$. Other authors reported an exponential behaviour, e.g. $TTF \sim exp\left(\frac{1}{J_G}\right)$ [7] or $TTF \sim exp\left(\frac{1}{J_G}\right)^{1/4}$ [12]. However, a clear correlation with the physics involved in the gate current was not reported. In Fig.3 the failure statistics is displayed according the Weibull distribution, showing the ln(ln(1/(1-F))) versus the time-to-failure, with F the cumulative failure probability, defined as $F = 1 - exp\left(-\frac{TTF}{\eta}\right)^{\beta}$, and $\eta$ the scale factor of 63.2% value of the distribution and $\beta$ the shape factor. The failure distribution shows a different behaviour depending on the gate bias range. Indeed, for $V_G > 9.5$ V a linear behaviour can be observed, with a $\beta$ value close to 2.5, typically associated with "wear-out" failure mechanism [22], extrapolated from the linear fit of the Weibull distribution (dashed lines). Instead, in case of $V_G < 9.5$ V, the failure statistics do not follow a linear behaviour as predicted by the Weibull distribution. Rather, a lognormal distribution (continues lines displayed for $V_G = 9.0$ V and $V_G = 9.2$ V), where the ln(-(1-F)) is proportional to ln(TTF), is more suitable to describe this behaviour. This deviation has been correlated with the presence of electron trapping phenomena that compensate the device degradation due to holes injection, increasing the expected lifetime predicted by the Weibull distribution. These effects can be deduced by the clear decrease of the $J_G$ occurred at $V_G$ of 9.0 V and 9.2 V, after about 300 s. Such a reduction is correlated to the electron trapping effects and it has been discussed in [21].

In Fig.3, the intersections of the failure distribution with ln(-ln(1-F)) = 0 represent the time when 63% of the distribution has failed, $\tau_{63\%}$. The lifetime $\tau_{63\%}$ is displayed as function of the corresponding gate bias in Fig. 4. Here, with a correct prediction it is possible to estimate the maximum gate bias value ensuring a 10 years lifetime, $V_{Gmax}^{10years}$. Typically, according to the E-model, the TTF is expected to exponentially increase with the decreasing $V_G$, i.e. $TTF(\tau_{63\%}) \sim \frac{1}{exp(V_G)}$ [22]. Applying this model for the lifetime $\tau_{63\%}$ a $V_{Gmax}^{10years} \approx$ 7 V can be extrapolated. However, the E-model well describes only the statistics acquired at higher $V_G$ (> 9.5 V). To estimate a realistic dependence of the TTF on the $V_G$, it is necessary to take in consideration the mechanisms of the current transport for the gate current extrapolated at higher $V_G$, i.e. the TFE model. Indeed, by combining the expression of $I_G$ of the TFE model (Eq.1) with the dependence of the TTF on the $I_G$ (Eq.2), it is possible to obtain a more suitable description of the TTF dependence on the applied $V_G$:

$$TTF(\tau_{63\%}) \sim exp\left(\frac{1}{\sqrt{exp(V_G)}}\right) \quad (3)$$

Following Eq.3, it is possible to estimate the $V_{Gmax}^{10years}$ of about 8.5 V, which is much more optimistic of that extrapolated by the simply E-model (around 7 V) and very well above the standard working gate bias of these devices, i.e. around 6 V.

## IV. Conclusion

In conclusion, the gate current mechanisms has been investigated, distinguishing between lower gate bias condition ($V_G <$ 6 V), where the Space Charge Limited Current (SCLC) is the dominant transport mechanism, and higher gate bias condition ($V_G >$ 6 V), in which the dominant current mechanism is represented by the Thermionic Field Emission (TFE) model. Then, the reliability of p-GaN HEMTs has been discussed, correlating the time-to-failure (TTF) to the applied gate bias. Indeed, by taking into account the gate current transport mechanism at high $V_G$ and the relationship between the TFF and gate current density, it was possible to estimate the maximum $V_G$ for 10-year lifetime ($V_{Gmax}^{10-years}$), resulting about 8.5 V, above the value of 7 V extrapolated by the E-model.

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