Fabrication and Characterization of Kilovolt p-Type SiC JBS Diodes With Enhanced Current Capability and Electroluminescence Phenomenon

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***Abstract*— Junction Barrier Schottky (JBS) Diodes are fabricated for the first time on p-type Silicon Carbide (SiC) substrates with the avalanche breakdown voltage (BV) of 1200 V. The SiC p^+ substrates are grown by the top seeded solution growth (TSSG) method, with the average resistivity of 50 mΩ·cm and the hole carrier concentration above 1 × 10^{20} cm^{-3}. The conductivity modulation is investigated based on the p-type SiC epitaxy, exhibiting enhanced current capability at elevated temperatures. This study demonstrates the application of p-type SiC substrates in power devices through kilovolt JBS diodes and paves the way towards ultra-high-voltage/current applications of bipolar SiC transistors. Remarkably, we observe an obvious electroluminescence (EL) of the p-type SiC JBS diodes. The luminescence intensity under the carrier recombination mechanism between the conduction band and the Al acceptor energy level has an obvious linear relationship with the conduction current. This finding serves as compelling evidence of the potential of p-type SiC materials in a wide range of applications.**

***Index Terms*— p-type silicon carbide, junction barrier Schottky, top seeded solution growth, conductivity modulation, electroluminescence.**

I. Introduction

SILICON carbide power devices based on N-type substrates have achieved remarkable performance. The bipolar SiC transistors, such as Insulated Gate Bipolar Transistor (IGBT) and Gate-Turn-Off Thyristor (GTO), are desirable for the ultra-high-voltage/current application. Since electrons have higher mobility than holes in SiC, the N-IGBT has a faster switching speed than the P-IGBT. However N-IGBT is limited by the quality and resistivity of p-type SiC substrate [1], [2].

High-efficiency doping and defect control of n-type SiC single crystals have been achieved using the physical vapor transport (PVT). However, the PVT growth of p-type SiC single crystals faces the challenges of quick depletion of Al doping sources, limited Al doping concentrations, nonuniform distribution of Al dopants, and high concentration of compensation centers in PVT-grown p-type SiC [3], [4]. The top seeded solution growth (TSSG) method enables continuous and stable p-type doping of the crystal by introducing Al into the high-temperature solution, which would increase the doping concentration of Al to the order to magnitude of 10^{20} cm^{-3}. The lower growth temperature efficiently decreases the concentration of compensation centers, and the lower growth rate facilitates defect engineering that is capable of decreasing dislocation densities [5]. Therefore, p-type SiC substrates grown by the TSSG approach is attractive in the application of n-channel transistor.

In this letter, we successfully develop the p-type SiC junction barrier Schottky diodes with the avalanche breakdown voltage of 1200 V. Moreover, the conductivity modulation was also investigated based on the p-type SiC epitaxy, exhibiting the enhanced current capability at elevated temperatures. Remarkably, we observed an obvious EL phenomenon when the device was in forward conduction, and analyzed it combined with the carrier recombination luminescence mechanism. This work demonstrates a clear linear relationship between luminescence intensity and diode current, which paves the way for a new and promising sensing method.

II. Design and Fabrication

P-type SiC single crystals were grown by the TSSG method. Commercial semi-insulating 4H-SiC (000-1) wafers with a diameter of 2 inches were employed as seed crystals. During the growth, the temperature of the SiC seed crystals was set at ∼1800 °C within the Ar atmosphere. The seed crystal was rotated at 30 rpm and lifted up at a lifting rate of 60 $\mu m \cdot h^{-1}$. The existing growth process conditions achieve an average resistivity of 50 mΩ·cm and a hole carrier concentration higher than 1×10^{20} cm^{-3}. The p-type SiC drift layer was grown by chemical vapor deposition (CVD) with the thickness of 10 μm

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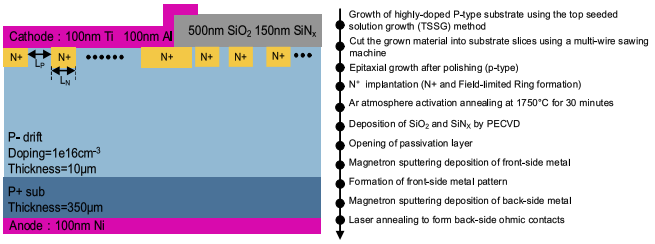

Fig. 1. (a)Schematic cross section of the SiC JBS device on the P-type substrate and P-type epitaxy. (b)Major process flow of the diode fabrication.

and the Al doping concentration of 1×10^{16} cm^{-3}. Without using the minority carrier lifetime enhancement process, the average minority carrier lifetime of p-type SiC epitaxial wafer at room temperature was tested by microwave photoconductivity method and was found to be 201ns.

The p-type JBS was demonstrated on the 2-inch p-type SiC wafer. The details of the device structure and fabrication process are shown in Fig. 1. The JBS structure was formed by the N^+ implantation following by the post implantation activation annealing at 1750 °C in Ar for 30 minutes. The spacing between N^+ region (L_P) is varied from 1 μm to 5 μm. The p-type Schottky was formed by the Titanium (Ti)-based metal stack and Nickel (Ni) was deposited and annealed to form the Ohmic contact to the backside of the p-type SiC substrate.

III. Device Characteristics

A. Electrical and Thermal Properties

Fig. 2 shows the reverse current-voltage (I-V) characteristics of the p-type JBS diodes. BV increases from 1030 V to 1200 V with L_P narrowing from 5 μm to 1 μm, indicating the effective pinch-off of the P-N junction beneath the Schottky interface. Larger spacings lead to higher leakage currents at high voltages and higher leakage current at elevated temperatures than at room temperature, which is mainly due to the reduction of the Schottky barrier height [6], [7]. Moreover, the BV increases at elevated temperatures, demonstrating avalanche characteristics that signify the high quality of the p-type SiC drift layer. Avalanche breakdown still dominates the breakdown mechanism, and the collision ionization coefficient decreases with rising temperature, which can be attributed to enhanced phonon scattering at elevated temperatures [8], leading to slightly higher blocking voltage at elevated temperatures.

Fig.3 presents a comparison of the forward I-V characteristics between different structures of p-type JBS diodes and the Schottky Barrier Diodes (SBD). Using Ti as the Schottky barrier metal, the barrier height measured by capacitance-voltage (C-V) according to formula (1) is about 1.94 eV, which is consistent with the 1.97 eV calculated theoretically according to formula (2):

$$\phi_{Bp} = V_{bi} + \phi_p + \frac{kT}{q} - \Delta\phi \tag{1}$$

$$\phi_{Bp} = \frac{E_g}{q} + \chi_s - \phi_M \tag{2}$$

As shown in Fig. 4, the build-in potential (V_{bi}) of 1.74 V was extracted from the C-V measurement. ϕ_p is the gap between the valance band and the Fermi level calculated based on the carrier concentration, and $\Delta\phi$ is the image force lowering of the Schottky barrier [9]. E_g, χ_s and ϕ_M are the bandgap width,

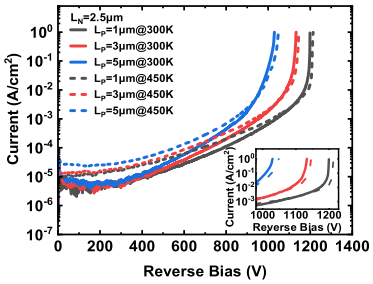

Fig. 2. Measured blocking characteristics of JBS devices. Inset: The zoomed-in scale of reverse I-V characteristics near the breakdown region.

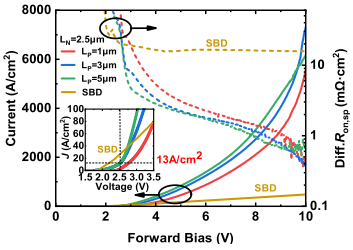

Fig. 3. Measured forward I-V characteristics of SBD and JBS devices.

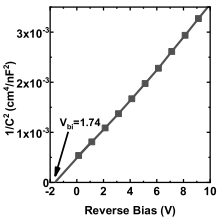

Fig. 4. 1/C^2-V characteristic measured at 100kHz.

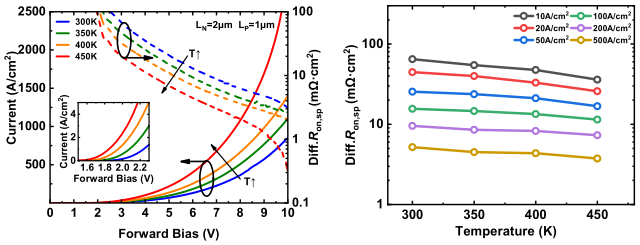

Fig. 5. (a)Measured forward I-V characteristics of JBS devices. (b) Differential specific on-resistance changes with temperature at different current densities.

electron affinity, and metal work function, respectively. The specific values can be found in reference [10]. The ideality factor for the carrier transportation of the Schottky interface is fitted to be ~2.05. The N^+ region is formed by ion implantation and annealing, which will bring interface states, residual defects, and surface roughening in JBS diodes [11]. And due to recombination in the depletion layer below the Schottky, the ideality factor will increase [12].

The high Schottky barrier and limited hole conductivity facilitate the triggering of the PN junction and enable bipolar conduction. JBS devices shows obvious conductance modulation, and the on-resistance is significantly reduced compared with SBD devices. As the L_p decreases (equivalent to the increase of N^+ region ratio), it exhibits stronger conductance modulation behavior at higher currents. The inset of Fig. 5(a) illustrates that as L_p decreases, the pinch-off effect increases, and the device turn-on voltage is close to the PN junction turn-on voltage. The PN junction triggers at a relatively-low current density of 13 A/cm^2 due to the low hole mobility in the p-type material.

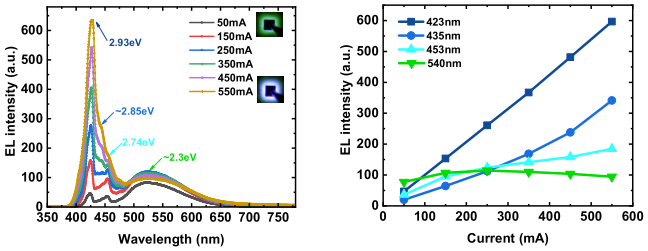

Fig. 6. (a)EL spectrum of JBS device based on P-type SiC under linear coordinates. (b) Relationship between luminescence peak intensity and current.

Fig. 5 show that the p-type JBS diodes exhibit a pronounced negative temperature coefficient. As temperature increases, in contrast to the increase of on-resistance for the n-type JBS due to the reduced mobility [13], the on-resistance of the p-type JBS decreases rapidly due to improved Al acceptor ionization [14]. In addition, in p-type JBS devices, electrons act as minority carriers, and the conductivity of electrons is much greater than that of holes. Thus, as the temperature rises, the minority carrier lifetime increases [15], leading to more noticeable conductivity modulation. This work shows that the increase of Al acceptor ionization rate and the improvement of minority carrier lifetime for p-type SiC shows a greater impact on the conductivity than the decrease in carrier mobility at high temperature.

B. Electroluminescence of p-Type SiC JBS Diodes

A clear EL phenomenon has been found for p-type SiC JBS diodes, which is difficult to be observed for n-type SiC JBS because of the high current density (larger than 1000A/cm^{-2}) required for n-type SiC JBS to achieve bipolar conduction [16], [17], [18]. As shown in Fig. 6(a), there're four luminescence peaks locating at 423 nm (2.93 eV), 435 nm (2.85 eV), 453 nm (2.74 eV) and 540 nm (2.30 eV) for the p-type SiC JBS diodes under forward current. When the input current is below 150mA, the intensity of the luminescence peak locating at 540 nm is the highest, resulting in the green emission of the p-type SiC JBS diodes. As the input current increases in the range from 150 mA to 550 mA, the luminescence peaks locating at 423 nm and 453 nm prevail over the peak at 540 nm, which gives rise to the blue-violet emission of the p-type SiC JBS diodes.

As shown in Fig.7, the peak wavelengths at 423nm (2.93 eV) and 453nm (2.74 eV) are in good agreement with the radiative recombination of electron-hole pairs between conduction band-aluminum defect level and the nitrogen-aluminum defect levels [19], respectively. The blue emission peak at approximately 435 nm (~2.85 eV) is commonly caused by stacking faults (SFs) in the epitaxial film. At the location of a SF, electron conduction displays a quantum well structure, resulting in the conversion of the indirect bandgap to a quasi-direct bandgap [20], [21]. Consequently, this alteration in the energy band significantly enhances the radiative recombination [22]. The emission peak in the green spectrum at around 540 nm (~2.30 eV) is attributed to recombination processes involving deep level traps. This is also the main radiative recombination mechanism in n-type SiC, commonly observed in the SiC MOSFET body diode [23], [24]. Compared with the EL spectrum of n-type SiC, p-type SiC has two more peaks caused by Al acceptor energy level.

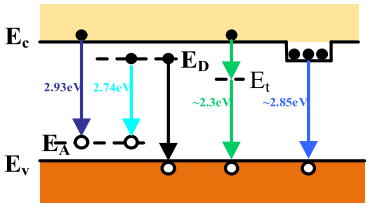

Fig. 7. Carrier recombination luminescence mechanism.

The light intensity at these two wavelengths is higher than that of the other wavelengths, indicating that the Al acceptor energy level may provide effective radiative recombination centers.

In p-type SiC, the recombination of carriers between the conduction band and acceptor energy levels serves as a potent mechanism for light emission, particularly with increasing current. As shown in Fig. 6(b), the intensity of the spectral peak at wavelength 423nm increases linearly with the increase of current, that is, the number of photons generated by the recombination of the conduction band and the acceptor energy level is proportional to the conduction current. In essence, the EL intensity (I_{EL}) is linked to the current density via the external quantum efficiency (EQE) of the LED, as [25]:

$$I_{EL} = \sum EQE \frac{j(\lambda)}{q} \tag{3}$$

EQE is mainly affected by the environment and the characteristics of the material itself [26], [27], [28]. Under the same external conditions, EQE can be considered a constant value within a certain current level range. And the $j(\lambda)$ can be understood as the radiation recombination current that releases photons of a certain energy. Therefore, within a specific wavelength and a certain current range, there is a linear relationship between luminance intensity and current. This is consistent with the phenomenon at 423nm wavelengths. At low current levels, minority carriers undergo recombination and emit light through adjacent deep-level defects. As the current increases, the limited number of deep-level defects results in the dominance of recombination luminescence from other mechanisms. And the slope of the EL intensity and current at the 435nm wavelength gradually becomes larger, because the direct band gap structure significantly improves the carrier radiation recombination efficiency. Therefore, when the current increases, the radiative recombination that occurs at the dislocation defect increases.

IV. Conclusion

The resistivity of p-type SiC substrate with a resistivity of 50 mΩ·cm grown by the TSSG method is far lower than the resistivity of the substrate grown by the PVT method, and is very close to the resistivity of the N-type substrate. This highly doped and low resistivity p-type SiC substrate was also successfully verified on 1200V JBS devices. We also analyzed the EL phenomenon. The luminescence of SiC power devices can be leveraged to acquire spectral information, enabling the extraction of details about the device's conduction current and operational state. By analyzing parameters such as photon wavelength and luminous intensity within the spectrum, the real-time working status and conduction current level of the device can be monitored, which is expected to bring about innovation in power electronics applications. The linear relationship between current and EL intensity will play a role in more application scenarios.

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