High-k Metal–Insulator–Metal Capacitors for RF and Mixed-Signal VLSI Circuits: Challenges and Opportunities

This article presents a detailed review of the progress in metal–insulator–metal capacitor technology and provides insight into challenges and opportunities for future research.

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ABSTRACT | Metal–insulator–metal (MIM) capacitors are inevitable and critical passive components in analog, mixed-signal, and memory applications. These capacitors occupy nearly 40% of circuit area among other passive and active components of the integrated circuit (IC). Considering this fact, the International Roadmap for Devices and Systems (IRDS) recognized and recommended the miniaturization of MIM capacitors with high permittivity dielectric materials. For future analog and radio frequency (RF) applications, the IRDS has predicted that MIM capacitors should hold a high capacitance density of >10 fF/μm^2, a low voltage linearity of <100 ppm/V^2, and a low leakage current density of <10 nA/cm^2. In this regard, many research works have been carried out over the last few decades with various high-k dielectrics to achieve "low voltage linearity." However, many of them are facing problems with structural defects, interface traps, and poor polarization process due to limitations of fabrication processes. This article attempts to review the challenges and opportunities involved in the reduction of voltage linearity and leakage of MIM capacitors. Also, this article presents the physical limits and challenges involved in MIM capacitor integration with back end of line (BEOL) process of recent complementary metal–oxide–semiconductor (CMOS) technologies. Using physical modeling, the design formula for low voltage linearity coefficient was derived, which helps IC developers in the design and implementation of highly linear RF-analog and mixed-signal (AMS) systems.

KEYWORDS | Back end of line (BEOL); high-k dielectrics; leakage; metal–insulator–metal (MIM) capacitors; radio frequency (RF)/mixed-signal integrated circuits (ICs); voltage linearity.

I. MOTIVATION

Wireless communication and advanced computational technologies are integrated into a single chip for smartphones and wireless personal area network applications, which are collectively called system-on-chip (SoC). Alternatively, the applications of SoC are extended in various domains, such as the Internet of Things (IoT), biomedical, and radio astronomy. SoC technology needs denser integrated circuit (IC) chips with many independent functionalities, such as digital signal processor (DSP), image processor, memory, analog/radio frequency (RF) systems, and networking. Considering these requirements, a new trend, called "More than Moore" (MTM), was

initiated by the International Technology Roadmap for Semiconductors (ITRS) in 2005, beyond the "Moore's law" [1], [2]. In recent times, the MTM trend has been reviewed by the International Roadmap for Devices and Systems (IRDS) to incorporate analog/RF/microwave, sensors, and energy harvesting circuit integration and miniaturization [3].

In transceiver SoCs, a few fundamental blocks/circuits are essential, such as modulator systems, analog circuits, analog-to-digital (AD) circuits, or mixed-signal circuits, commonly referred to as analog and mixed-signal (AMS) circuits. These subsystems need high-precision elements to drive and process the high-frequency signals. On the other hand, the linearity and mismatch are challenging in high-precision low-power biomedical and communication ICs. To quantify the performances of such subsystems, a few driving figures of merit (FOMs) of IC technologies were attributed, namely, frequency of operation, bias/drive voltage, power consumption, semiconductor and insulating materials, die size, and fabrication cost. While considering these FOMs and standard specifications, scaling of transistor alone cannot improve the performance-to-cost ratio. Therefore, the miniaturization of various passive elements, such as inductors and capacitors, is required according to the MTM of IRDS.

"Capacitor" is an essential and significant passive element in various AMS applications. Capacitors are often used for dc isolation, coupling, decoupling, and bypass in AMS circuits. In these circuits, various sizes of capacitors or capacitor banks take a large portion of IC area. Therefore, the miniaturization of capacitors has become a challenge for IC fabrication. Metal–oxide–semiconductor (MOS) capacitors were employed for many years due to the advantages of native complementary metal–oxide–semiconductor (CMOS) technology. Also, MOS capacitors can be integrated with other active elements easily. However, they suffer from undesirable variations in capacitance due to charge accumulation at oxide–semiconductor and depletion effects at polysilicon electrodes. This results in nonlinearity, poor quality factor, and large sheet resistance. These factors in MOS capacitor are not acceptable for high-precision processing techniques [4]. Due to this, nanostructured parallel-plate capacitors with metal electrodes became popular, and later, they were called "metal–insulator–metal (MIM) capacitors."

Reports of ITRS and IRDS, published from 2000 to 2021, recognized the advantages of MIM capacitor and recommended it for AMS and dynamic random access memory (DRAM) applications. Those reports list the technology requirements and challenges for MIM capacitor through various performance parameters, such as high capacitance density of >10 fF/μm^2 and voltage linearity of <100 ppm/V^2 [3]. Many articles were published earlier on the fabrication of high-k dielectric MIM capacitors using various dielectric deposition techniques to meet these challenges. Among them, many are successful in achieving high capacitance density. However, many capacitors show high voltage linearity, high leakage current density, and low
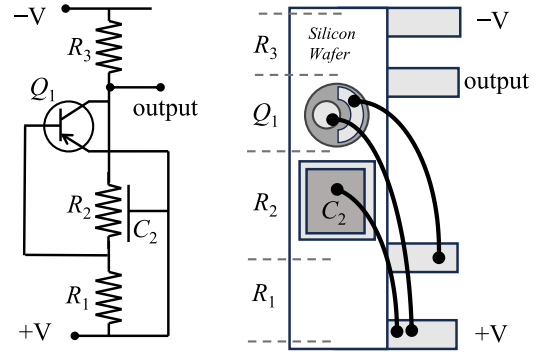
Fig. 1. *Kilby's first IC [5] was an RC phase shift oscillator with a planar p-n junction capacitor, which is the first analog IC capacitor.*

quality factor. This is due to the structural defects during deposition and defects due to long electrical stress. In view of these facts, several attempts on hybrid or multilayer MIM capacitors have been demonstrated over the past two decades.

In many RF/AMS ICs, MIM capacitors are fabricated, along with transistors, using back end of line (BEOL) and front end of line (FEOL) technologies. Therefore, the compatibility of the desired dielectric layers with BEOL/FEOL process is essential. In this article, we presented the detailed review of the progress in MIM capacitor technology. It starts with evaluation of MIM capacitors, from first to recent ICs. Then, the performance parameters of MIM capacitors are described with short notes. Based on these parameters, the progress in experimental and theoretical works on MIM capacitors is reviewed in multiple categories, namely, single, hybrid, and multiple dielectric layers. From these observations, the limiting issues are addressed using analytical modeling. This article also lists the challenges and opportunities for the development of high-performance MIM capacitors for next-generation AMS/RF ICs.

II. EVOLUTION OF MIM CAPACITORS

Kilby's first IC was an RC phase shift oscillator that was constructed with one transistor, three resistors, and one capacitor, as shown in Fig. 1 [5]. This first analog IC capacitor was a planar p-n junction capacitor, made of diffusing n-type layer in p-type substrate with single top electrode plate [5]. Later, MOS capacitors were also proposed with a stack of SiO$_2$/Si between two metal plates [5]. However, it was claimed that the SiO$_2$/Si MOS capacitors showed a better stable capacitance than p-n junction capacitance. From 1960 to 1990, many researchers developed various planar capacitors for wireless radio circuits. MOS capacitor fabrication methods were optimized and became the most successful technology. High-k materials, such as Si$_3$N$_4$, Al$_2$O$_3$, TiO$_2$, and Ta$_2$O$_5$, were predominately used in capacitors as insulators to increase the capacitance density. In the 1990s, nanostructured thin-film technologies evolved in the fabrication of single-chip radio-frequency integrated circuits (RFICs) [6].

MOS capacitor was largely preferred for AMS IC technologies. However, it showed undesirable variations in capacitance with voltage and poor interface quality with high-k materials. These variations are tolerable in some applications, such as DRAM and few analog applications. However, it cannot be acceptable in high-precision circuits, such as DSPs, and AD and digital-to-analog (DA) converters [7], [8]. The precision is not about the value of capacitance, but it is a measure of sensitivity of capacitance with voltage and temperature, often measured using the voltage coefficient of capacitance (VCC). The VCC depends on the quality of dielectric material, thickness of dielectric layer, and interface property of metal/insulator or polysilicon/insulator. Those three properties are largely affected by the fabrication method.

Polysilicon–insulator–polysilicon (PIP) capacitors replaced MOS capacitors in 1999 [7], [8], [11]. PIP capacitors were realized using liquid-phase chemical vapor deposition (LPCVD) grown polysilicon layers and with high-temperature deposition of dielectric, such as thermal oxidation [7], [8]. However, PIP capacitors also suffered variations of capacitance with voltage due to the depletion effect at the polysilicon/substrate interface and associated parasitic capacitance. With careful reduction of depletion effect, PIP capacitors had shown lower voltage linearity than MOS capacitors [7]. However, the in situ doping of polysilicon and additional mask for etching had increased the manufacturing cost compared to the CMOS technology. Though PIP capacitor technology was well established, poor RF compatibility at very high frequency, poor quality factor ($<$50) due to resistive losses at polysilicon plates, intraelement parasitic capacitance, and lossy silicon substrate were the dominant weaknesses [4], [7].

Metal electrodes were used to replace the polysilicon top and bottom contacts, particularly Pt or TiN [4], so they were called "MIM capacitors." It was constructed over top of metal lines to avoid series resistance and crosstalk between silicon substrates. PIP and MIM capacitors are shown in Fig. 2(a) and (b), respectively. The inset of Fig. 2(a) shows the cross-sectional view of PIP capacitor, which had been placed over a field oxide. The voltage linearity of this capacitor is shown in Fig. 2(a). It can be observed that the increase in doping of polysilicon improved the VCC. This is due to the reduction of depletion at polysilicon/insulator interfaces. On the other hand, MIM capacitors with Al_2O_3 and $AlTiO_x$ dielectric layer are shown in the inset of Fig. 2(b), which exhibits a very low dependence with voltage and frequency. This is due to an improved metal/insulator interface, and the field distribution of MIM capacitors lies within two metal electrodes.

III. PERFORMANCE MEASURES OF MIM CAPACITORS

The performance of the MIM capacitor can be evaluated by many parameters, such as capacitance density, leakage current density, voltage nonlinearity, breakdown field, dielectric relaxation, dependence of capacitance with frequency,


(a)

(b)
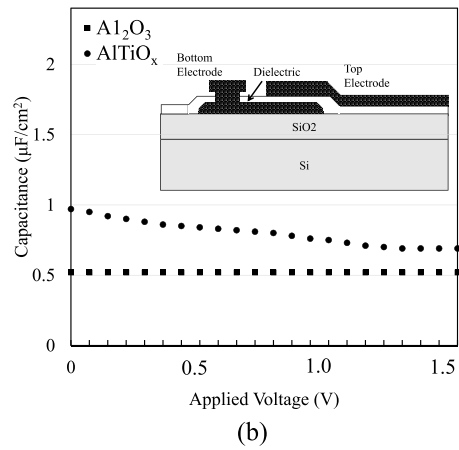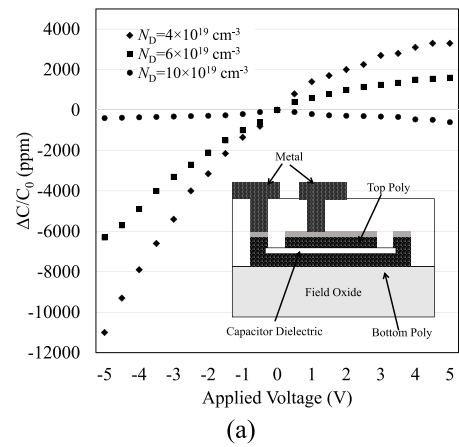
Fig. 2. *In the evolution of capacitors for ICs, two important structures were significant. (a) PIP capacitor [7], shown in inset, whose variation of capacitance for applied voltage is high about $>$2000 ppm/V^2. (b) MIM capacitor, in the inset, has almost stable capacitance with applied voltage for dielectric layer of Al_2O_3 and $AlTiO_x$ [4].*

and reliability. The minimum and maximum values of these parameters are limited based on the applications. For example, the dependence of capacitance with voltage in an MIM capacitor is acceptable in a DRAM circuit, but this is severely constrained in analog or mixed-signal applications. On the other hand, the leakage current density is limited to almost the same as 10 nA/cm^2 for both applications. The leakage current density should be extremely low for blocking capacitors, but decoupling capacitors can be leaky. In this section, the performance parameters of MIM capacitors are reviewed with short notes.

A. Capacitance Density

Integrated MIM capacitors are almost similar to planar parallel-plate capacitors. Its capacitance density can be expressed using the well known equation

$$\frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{1}$$
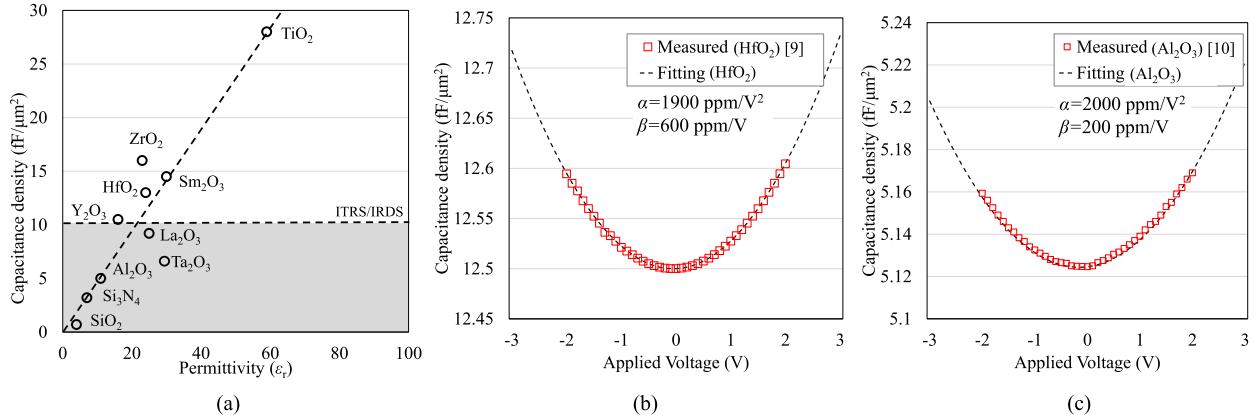
Fig. 3. *(a) Relationship between the capacitance density of MIM capacitors with various dielectrics and the relative permittivity (ε_r) shows a linear fit. This indicates the need of high-k dielectrics to achieve the ITRS/IRDS challenge of >10 fF/μ m^2 (above the shaded region). Voltage linearity characteristics of MIM capacitors with (b) HfO$_2$ and (c) Al$_2$O$_3$ indicate the dependency of capacitance with applied potential with a parabolic fit C(V) = C$_0$(αV^2 + βV + 1). The fitting coefficients α and β are presented in insets (measured data: [9], [10]).*

where C and A are the capacitance and electrode area, respectively; and ε_0, ε_r, and d are the free-space permittivity, relative permittivity of dielectric material, and thickness of dielectric layer, respectively. Since all IC designs have scaled to micrometer level, the capacitance density is preferred with unit of "fF/μm^2." ε_r is also represented as k elsewhere, referring to "kappa." It is clear that the capacitance density is directly proportional to the dielectric constant and inversely proportional to dielectric thickness. In this regard, many high-k materials have been introduced in MIM capacitors, whose dielectric constant is higher than that of SiO$_2$ ($k = 3.9$). On the other hand, the thickness of dielectric layer d should be as low as possible, which depends on the dielectric deposition method and acceptable leakage current density.

Fig. 3(a) shows the capacitance density as a function of relative dielectric permittivity. The shaded region distinguishes the capacitance density above and below the ITRS/IRDS recommendation of >10 fF/μm^2. A linear relationship of capacitance density with permittivity is observed. It is clear that most of the oxide thin-film quality and technologies show relatively similar performance. Among these oxides, high-k dielectric materials, such as Al$_2$O$_3$, HfO$_2$, and Ta$_2$O$_5$, have been often used in MIM capacitors, which show high capacitance density with good reliability and low leakage current density [15], [16], [17], [18]. Yet, Al$_2$O$_3$ MIM capacitors were demonstrated with capacitance density <10 fF/μm^2. Oxides with $\varepsilon_r > 20$, such as HfO$_2$ and ZrO$_2$, show high capacitance density. Althogh Ta$_2$O$_5$ shows a high permittivity, it results in capacitance density <10 fF/μm^2. This is due to crystalline nature of Ta$_2$O$_5$. Rare-earth materials show relatively high capacitance density, and however, the process integration with existing CMOS process flow should be explored. Ferroelectric materials show several orders of dielectric constant than paraelectrics. BaTiO$_3$, Br$_x$Sr$_{1-x}$TiO$_3$, and other ferroelectric materials have also been employed recently

[14], [19]. It has been found that the crystalline properties, grain size, and processing temperature are largely affecting the quality and dielectric constant of ferroelectric materials.

B. Voltage Linearity

In AMS applications, each swing of signal (peak-to-peak) is discretized by 1000 or more levels. In such cases, a small change in capacitance due to temperature or applied voltage may lead to errors in many calculations. This sensitivity to voltage is measured using VCC [7]

$$\text{VCC} = \left[\frac{C(V) - C_0}{C_0} \right] \times 10^6 \ (\text{ppm/V}) \qquad (2)$$

where C_0 is the capacitance measured at zero voltage. In most of the cases, the relation of VCC with voltage is parabolic in nature. Such parabolic characteristics are modeled using the empirical relation

$$C(V) = C_0 \left(\alpha V^2 + \beta V + 1 \right) \qquad (3)$$

where α and β are the quadratic and linear coefficients of capacitance with units of ppm/V^2 and ppm/V, respectively. For example, Fig. 3(b) and (c) shows the measured capacitance–voltage (CV) characteristics of the MIM capacitors with HfO$_2$ and Al$_2$O$_3$ dielectrics, reported by Ding et al. [9] and Hourdakis and Nassiopoulou [10], respectively. We show the fitting of empirical equation (3) with measured CV data. Both MIM capacitors exhibit a high quadratic VCC of >1000 ppm/V^2. For AMS applications, the challenge lies in reducing the quadratic VCC value to less than 100 ppm/V^2 [3]. It has been found in many reports that the VCC largely depends on polarization, thickness of dielectric layer, atomic arrangement, defect density, temperature, and signal frequency
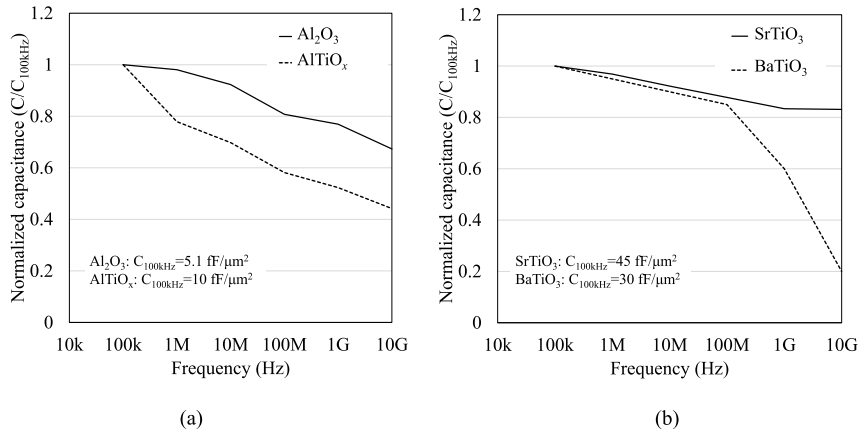
Fig. 4. *Signaling frequency influences the capacitance significantly which is evident from frequency-dependent capacitance characteristics of (a) Al$_2$O$_3$ and AlTiO$_x$ and (b) SrTiO$_3$ and BaTiO$_3$ MIM capacitors (measured data: [12], [13], [14]). The rate of reduction of capacitance for higher signaling frequency is attributed to the limited dielectric polarization process and the defects in the fabricated dielectric layer.*

[20], [21]. Most of the MIM capacitors with high-k dielectrics show positive quadratic VCC, which are reviewed in Section IV. Interestingly, few ferroelectrics and SiO$_2$ show negative α [20], [22]. The sign of α depends on the density of induced and permanent dipoles in dielectrics [20]. Modeling of positive and negative quadratic VCCs is presented in the following sections.

C. Frequency Dependence

Signaling frequency influences the capacitance significantly. When a time-varying signal is applied to an MIM capacitor, the dipolar molecules of dielectric material orient according to the positive and negative cycles. This mechanical rotation or polarization with electric field direction cannot follow the high-frequency electrical signal. Thus, the polarization of material reduces, which causes a reduction in polarizability or dielectric constant for higher frequencies, and such an effect is referred to as dielectric relaxation or frequency dependence of capacitance. Various polarization mechanisms, such as space charge polarization, orientation polarization, ionic polarization, and electronic polarization, are involved in the polarizability at various frequency ranges. The time lag between the external electric field and polarization decides the frequency range, often referred to as Curie–von Schweidler law. From the Deybe approximation, the decay of ε_r was derived, which shows a flat response between the frequency transitions [24]. Jonscher [24], [25] found that the frequency dependence of polarization is a fractional power law due to a many-body mechanism. This is referred to as the universal dielectric response. McPherson [26] simplified the expression as

$$\varepsilon_r = \varepsilon_{r0} \left(\frac{f_0}{f} \right)^n \qquad (4)$$

where ε_{r0} is the dielectric constant at signaling frequency $f = f_0$. This physical model was verified for SiO$_2$ nanoparticle successfully. The fitting factor n typically ranges from 0.04 to 0.05.

The atomic arrangement and defect profile of dielectric material also influence the polarization mechanism according to excitation signal frequency. Therefore, the material and quality of fabrication technology decide the rate of reduction of capacitance with frequency. For example, the thermally oxidized Al$_2$O$_3$ and AlTiO$_x$ MIM capacitors exhibit different rates of reduction in capacitance for increase in frequency [12], as shown in Fig. 4(a). It is clear that the capacitance density of AlTiO$_x$ MIM capacitor shows a fast reduction of capacitance as frequency increases. This is the result of high density of defects/traps and low time constant of traps available at the metal-to-oxide interface [12]. Ferroelectric materials, such as SrTiO$_2$ and BaTiO$_2$, show high permitivity. However, they exhibit faster degradation of capacitance with frequency compared to paraelectric materials. This is due to the large trap density and grain size of ferroelectrics. Fig. 4(b) shows the frequency-dependent capacitance of SrTiO$_2$ and BaTiO$_2$ MIM capacitors. We can observe that the BaTiO$_2$ MIM capacitor shows a fast reduction of capacitance compared to SrTiO$_2$ MIM capacitors. This is due to the Ni electrode that helps in the reduction of defects [13].

Quadratic-VCC of MIM capacitors is also influenced by signaling frequency. Gonon and Vallae [21] reported the modeling of VCC as a function of frequency and trap density based on the electrode polarization mechanism. It was observed that the dependence of capacitance in the MIM capacitor is due to field-activated mobility or hopping of charges with polarization. The model specifies the VCC as

$$\text{VCC} = \frac{\triangle C}{C_0} \approx \rho \frac{\sigma_0^{2n}}{\omega^{2n}} \qquad (5)$$
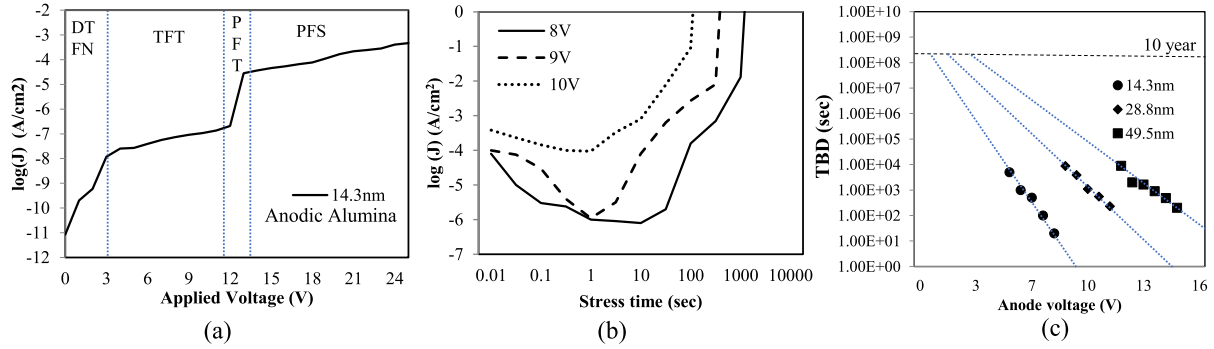
Fig. 5. *Leakage current density is an FOM of MIM capacitor. (a) Various leakage mechanisms involved in the charge transport of an anodic Al$_2$O$_3$ MIM capacitors for the applied voltage are presented. (b) Induced leakage current and breakdown characteristics for a constant potential over a stress time, which showcases the aging performance of the MIM capacitor. (c) TBD for various constant stress voltages. This is useful to predict the reliability, failure, and lifetime characteristics of an MIM capacitor (measured data: [23]).*

where $\triangle C$ is the change in capacitance with voltage; C_0 is the capacitance at zero bias; and ρ is the proportionality constant, which depends on Debye length and permittivity of dielectric material. It shows that the VCC decreases with frequency, which was confirmed with measured data [21]. It also indicates that the dielectric materials with high conductivity may exhibit high VCC due to the influence of high defect density.

D. Leakage Current and Reliability

Leakage mechanisms in MIM capacitors degrade the performance of RF and analog circuits. This intern attributes the power leakage of the circuit, which significantly affects the linearity and efficiency of the subsystem. Because of this, the reduction of leakage current in MIM capacitors has become one of the most important requirements. It was proved experimentally and mathematically that the leakage current density is higher for high-k materials. It is well known that bandgap and relative permittivity of the metal oxides show a linear fit and inverse proportionality [27]. Due to this, the Schottky barrier (SB) height and effective barrier thickness at the metal/dielectric interface degrade and help the carriers to leak from one metal to another [28].

Five leakage mechanisms in dielectrics have been reported so far, namely, direct tunneling (DT), Fowler–Nordheim tunneling (FNT), Schottky emission (SE), Poole–Frenkel (PF) emission, and trap-assisted tunneling (TAT). Each mechanism dominates other at various ranges of applied voltage and trap distribution in dielectrics. Fig. 5(a) shows the measured leakage current density of an anodic alumina MIM capacitor [23], along with various leakage/conduction mechanisms involved. A higher slope at very low voltage indicates the Schottky thermionic emission of electrons to the unoccupied defect or trap states near metal–insulator interface. Low field current density is dominated by TAT, which depends on temperature, defect density, and trap well depth. PF

emission occurs at high fields due to the excitation of trapped electrons in the defect states to conduction states, in bulk dielectrics. Poole–Frankel emission/saturation is observed after the second knee point. The trap barrier height is reduced to zero for voltages above the second knee point, and thus, the charged (coulombic) traps have no effect on the carrier transport [29].

The reliability of an MIM capacitor is statistical information about the device's performance under certain real-time conditions, such as continuous electrical, temperature, and mechanical stresses. It specifies the lifetime of an MIM capacitor under continuous time electrical stress. To measure this parameter, the leakage current density of test device is measured at a constant voltage for a period of time, say 10^5 s at 20 V. This applied electrical stress creates new traps in the dielectric layer, which changes the leakage current, and this is called stress-induced leakage current (SILC). These newly created traps form a leaky path for the charge flow and result in a breakdown, which is recorded as time to breakdown (TBD). TBD can be measured at various high constant stress voltages. Fig. 5(b) and (c) shows the measured TBD characteristics of an anodic Al$_2$O$_3$ MIM capacitors [23]. This capacitor shows a high reliability, which shall break down after ten years if 1 V is applied continuously.

Time-dependent dielectric breakdown (TDDB) is often studied to understand the stress and failure mechanisms of MIM capacitors. One of the reliability specifications in MIM capacitors is that the TDDB should satisfy at least ten-year lifetime and the accumulated failure rate of <10 ppm. SiO$_2$, Ta$_2$O$_5$, and HfO$_2$ are often preferred for MIM capacitors as these materials show excellent thermodynamical stability. Many dielectric stacks were proposed for MIM capacitors to achieve high reliability. However, there is a need for dielectric reliability assessment through physics-based model to predict lifetime at a few operating conditions. These models were classified in to two categories [26]: 1) field-based (E-models) and 2) current-based ($1/E$-models) TDDB models. For instance, the E-models
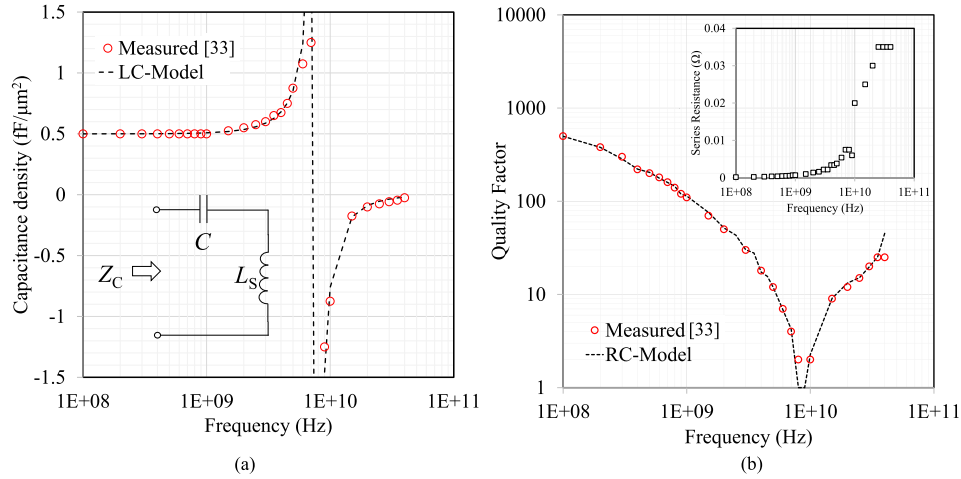
Fig. 6. *(a) Fitting of the simple LC equivalent circuit model, shown in the inset, with measured effective capacitance of an MIM capacitor. This indicates the transition of capacitive to inductive nature at a very high frequency, known as series resonant frequency f_S. The relationship between the energy lost and stored by a capacitor is measured by the quality (Q) factor. (b) Measured Q factor of an MIM capacitor with the computed Q factor of an equivalent series RC model. It reveals that the loss or series resistance increases with frequency, as presented in the inset. (Measured data: [33].)*

have been reported using the exponential law [30]

$$t_{\text{TDDB}} = t_0 e^{-\varsigma V}.$$

Alternative to these models, semi-empirical models were reported with power law [31]

$$t_{\text{TDDB}} = \eta V^{-n}$$

which was found suitable to compute the TDDB even for positive/negative electrical stress conditions. However, these models are semi-empirical, which shall not be used to design or optimize the MIM capacitors. McPherson [26] presented a detailed physical model for frequency-dependent TDDB lifetime of MOS capacitors through extensive computation and analysis of local field at the molecular level. In this model, first the local field E_{loc} was computed as a function of ε_r as

$$E_{\text{loc}} = [1 + L(\varepsilon_r - 1)] E_{di} = \left[\frac{(2 + \varepsilon_r)}{3}\right] E_{di} \quad (6)$$

where $L = 1/3$ is the Lorentz factor for field correction [26]. Equation (6) is used to compute the recovery rate from the metastable bonded state to the stable bonded state of dielectric molecules. This relationship is used to compute the frequency-dependent TDDB lifetime by placing (18) and presented in [26], named as McPherson TDDB model

$$t_{\text{TDDB}}(f) = \tau_{\text{pulse}} \exp\left(\varepsilon_r(T, f) \cdot \frac{\mu_0 E_{di}}{3kT}\right) \times t_{\text{TDDB,dc}} \quad (7)$$

where the ratio of total time and ON-time of square pulse is given as $\tau_{\text{pulse}} = (t_{\text{ON}} + t_{\text{OFF}}/t_{\text{ON}})$. μ_0 is the effective dipole moment of the dielectric molecule, which is significantly affected by the local field. This model successfully predicts the TDDB lifetime of SiO_2 MOS capacitors in comparison with measured data at operational temperature $T = 125$ °C. From the literature survey, it was found that frequency-dependent TDDB lifetime was seldom reported for MIM capacitors, neither experimentally nor theoretically.

The intrinsic traps during oxidation and extrinsic traps due to electrical stress lead to dielectric relaxation in MIM capacitors, which are some of the error sources for mixed-signal ICs. It, particularly, attacks the A/D converters [32]. Dielectric relaxation refers to the time-dependent trapping and releasing of charges/carriers in defect sites of dielectrics. Polarization of the trapped charges occurs during relaxation for the applied voltage leads to time-dependent current variations in the MIM capacitor. Such a mechanism is also referred to as memory effect [32]. This time-dependent charge transfer also affects the VCC of capacitors and disturbs the AMS system.

E. RF Parameters of MIM Capacitors

In RFICs or monolithic microwave ICs (MMICs), capacitors are preferred to reduce the size and cost. They also exhibit wideband characteristics, which is useful for broadband systems. Chip and integrated capacitors for RF applications should be characterized using Z- or S-parameters for higher signaling frequencies, up to 10 GHz. This practice is essential for accurate characterization, device modeling, and circuit design. Integrated MIM capacitors are often modeled as capacitor (C) with a series inductor (L_S) as shown in the inset of Fig. 6(a), considering that

Table 1 ITRS/IRDS Summarizes the Technology, Design, and Reliability Requirements of MIM Capacitors for Future Analog/Mixed-Signal ICs. This Table Lists the Key Challenges and Requirements in MIM Capacitor Technology for AMS Applications [3]

Year of Production →	2018	2019	2020	2021	2023
Capacitance density ($fF/\mu m^2$)	10	10	10	10	12
Voltage linearity (ppm/V^2)	< 100	< 100	< 100	< 100	< 100
Leakage (A/cm^2)	$< 10^{-8}$	$< 10^{-8}$	$< 10^{-8}$	$< 10^{-8}$	$< 10^{-8}$
σ Matching (%·μm)	0.3	0.2	0.2	0.2	0.2
Q factor	> 50	> 50	> 50	> 50	> 50

the effect of series resistance is negligible. Therefore, the impedance of the capacitor is

$$Z_C = -\frac{j\left(1 - \omega^2 L_S C\right)}{\omega C}.$$

From this, the effective capacitance can be written as

$$C_{\text{eff}} = C\left[1 - \omega^2 L_S C\right]^{-1} = C\left[1 - (\omega/\omega_S)^2\right]^{-1}$$

where $\omega = 2\pi f$ is the operating angular frequency and $\omega_S = 2\pi f_S$ is the series resonant frequency. After f_S, the total reactance of the capacitor becomes inductive. Parthasarathy et al. [33] reported the characterization of integrated MIM capacitors, fabricated in IBM 0.18-mm SOI technology. Using the vector network analyzer, the effective capacitance was measured using a ground-signal-ground (GSG) padset up to 40 GHz. Fitting the equivalent circuit model from measured data is presented in Fig. 6(a). We can observe a best fit of effective capacitance occurs for the nominal capacitance $C = 2.1$ pF and series inductance $L_S = 1.9$ nH. One shall observe the transition from positive to negative value of capacitance at series resonant frequency $f_S = 9.2$ GHz. Therefore, the designers of RF circuits should consider this feature of MIM capacitors. For instance, the decoupling capacitors are often used as dc blocking inductance at higher frequencies above the series resonant frequencies. Also, decoupling capacitors are used to block unwanted high-frequency signals and EMI in high-speed mixed-signal circuits. Therefore, the study of series resonant frequency, quality factor, and impedance through RF analysis is important.

Quality factor is one of the important parameters of MIM capacitors. It measures the ability of capacitor to store energy, while some amount of energy is lost. If the storage and dissipated energies are represented in terms of capacitance (C) and resistance (R_S), we can write the quality factor as

$$Q = \frac{1}{2\pi f R_S C}. \tag{8}$$

Fig. 6(b) shows the fitting of measured quality factor with model in (8). This fitting was achieved by piecewise selected values of R_S, which is plotted in the inset of Fig. 6(b). As evident, the series resistance is gradually increasing and saturates after 25 GHz. After the

series resonant frequency (9.2 GHz), the series resistance rapidly increases from 0.01 to 0.035 W due to fast roll-off of negative capacitance density (or equivalent inductance). This dependence becomes weak after 25 GHz, and hence, the quality factor and the series resistance saturate. This is due to the losses in the dielectric and insulator/metal interface. Such behavior was reported in monolithic and integrated capacitors [34]. MIM capacitors should hold low dielectric loss and low series resistance. In most fabrication technologies, the metal ions of electrode are migrating into the dielectric layer during very high-temperature metalization or oxidation. This intern reduces the quality and reliability of dielectric material. This needs a low contact resistance interconnects, desirably short. In recent works, many researchers have shown interests in copper/low-k dielectric contacts, which offers a low series resistance and provides good integration with silicon/GaAs technologies [35], [36]. These electrodes stop the migration of metal ions into the dielectric layer, which further improves the reliability [36]. These low-k contacts also reduce parasitic capacitance with nearby metal contacts.

IV. HIGH-k DIELECTRIC MIM CAPACITORS

Three decades before, a high-precision capacitor was proposed to achieve a low VCC [7]. Conventional SiO$_2$ ($k = 3.9$) and SiO$_3$N$_4$ ($k = 7$) dielectric PIP capacitors showed the capacitance density of ~ 2 fF/μm^2 with the VCC of >100 ppm and the very low leakage current density of <1 nA/cm^2. These capacitors occupy a large area to get a high capacitance since they possess low capacitance density. At the same time, for DRAM requirement, this area increases about five times. This leads to an increase in noise, IC size, and high fabrication cost. On the other hand, ITRS restricts the maximum temperature of dielectric processing up to 400 °C to make compatibility with BEOL fabrication processes [3].

ITRS and IRDS recommend the technology requirement for MIM capacitors, in terms of various performance parameters. Table 1 shows the future requirements of MIM capacitor according to IRDS [3]. It is expected to achieve more than 10 fF/μm^2 for the year 2021 with a low leakage of 10 nA/cm^2 and a low VCC of less than 100 ppm/V^2. In this regard, many high-k materials were introduced as dielectrics in MIM capacitors in the last two decades. Along with high capacitance density, many studies were dedicated to achieve low voltage linearity,

low leakage current density, and improved reliability. This section covers a detailed review of various high-k materials and their processing techniques for MIM capacitors.

DRAM and AMS ICs need simple, low fabrication temperature, and low-cost dielectric deposition method. MIM capacitors are usually fabricated, as reported in many articles, as follows. First, the wafer or substrate will be cleaned using the Radio Corporation of America (RCA) cleaning technique. A thick insulating layer of field oxide (usually SiO_2) is deposited/grown using thermal oxidation. A bottom electrode of metal or metal-alloy thin film will be deposited using physical vapor deposition (PVD) or thermal evaporation. A nanostructured dielectric thin film will be deposited by a unique deposition tool. High-temperature annealing with O_2 ambient, or plasma treatment, will be applied to crystallize and reduce the oxygen vacancies in bulk dielectrics. After cleaning thoroughly using deionized water, the top metal electrode will be deposited similar to the bottom electrode. Lithography and etching process will be carried out to reach the ground or excite the bottom electrode. The selection of electrode metal, metal deposition technology, dielectric material, dielectric deposition technology, and thickness of each layer are considered based on the availability and applications. Various fabrication methods have been proposed in MIM capacitor technology to meet such requirements, such as atomic layer deposition (ALD), sol–gel, sputtering, thermal oxidation, anodic oxidation, and PVD/chemical vapor deposition (CVD). Using these technologies, various dielectric structures, such as single layer, bilayer, and multilayer, have been developed for MIM capacitors for the past ten years. Most popular oxides, such as Al_2O_3, HfO_2, and Ta_2O_5, were extensively investigated. However, some of the rare-earth and ferroelectric dielectric materials are also receiving attention for high-density MIM capacitors.

Al_2O_3 is an attractive high-k dielectric material with an energy bandgap of 8.3 eV, a dielectric constant of 9–10, and a heat of formation of 399 kcal/mol [37]. The intrinsic dielectric properties of Al_2O_3, i.e., dielectric relaxation and reliability, were extensively investigated in [37] and [38]. It was concluded that Al_2O_3 MIM capacitors exhibit high reliability and low leakage current density [38]. Chen et al. [12] reported the fabrication of Al_2O_3 MIM capacitor using thermal oxidation and subsequent annealing at 400 °C. This 12-nm-thick Al_2O_3 MIM capacitor with TaN as bottom electrode shows a capacitance density of ~5 fF/μm^2 and a leakage current density of 10 nA/cm^2 [12]. The capacitor shows a high VCC of >2000 ppm/V^2 with low sensitivity or variation of capacitance with frequency. In the same work, it was reported that doping Ti with Al_2O_3 results in AlTiO$_x$ (an alloy of Al_2O_3 and TiO_2). The AlTiO$_x$ MIM capacitor showed a high capacitance density of 10 fF/μm^2 [12]. However, it has a strong dependence on capacitance with temperature and frequency. This is due to weak Ti–Al–O bond, defect sites at bulk and metal/insulator interface, and poor oxidation due to doping of Ti ions. Later, Ding et al. [39] also fabricated Al_2O_3 MIM capacitor

of almost same thickness with TaN electrodes. It shows a high capacitance density of 6.05 fF/μm^2 and a low leakage current density of 48 nA/cm^2 with a high breakdown field of 8.61 MV/cm. This capacitor shows an acceptable VCC of less than 795 ppm/V^2 [39]. The post-deposition oxidation of Al thin film is not complete overall sites. This should form Al-rich nonstoichiometric Al_2O_3 film. This may affect the polarization phenomena and leads to a reduction of effective permittivity of the Al_2O_3 thin film. This incomplete oxidation also increases the leakage current density, at least by an order. From the modeling of leakage currents, it was identified that the conduction mechanism is dominated by TAT and FP hopping mechanisms in both capacitors. It is worth noting that the TaN electrodes have good thermal stability and improved interface quality with high-k oxides.

The 15-nm ALD Al_2O_3 MIM capacitor with TiN as electrode was reported by Be'cu et al. [17]. The capacitor showed a capacitance density of 4.5 fF/μm^2. In this work, the modeling of capacitance variation with temperature was reported. It was observed that the capacitance increased linearly with temperature, which is due to an increase in permanent dipole moment at higher temperatures. It was also observed that VCC has a quadratic relation with applied electric field due to displacement of metal cation from equilibrium [17]. Preparation of nanostructured Al_2O_3 thin film using anodic oxidation for MIM capacitors has been carried out by few authors in recent years [10], [40], [41]. Hourdakis and Nassiopoulou [10] reported the performance of MIM capacitors with porous anodic Al_2O_3 using anodization electrolytes as citric acid aqueous solutions. A high capacitance density of ~5 fF/μm^2 was achieved with an effective dielectric thickness of ~15 nm. A high quadradic VCC of 1907 ppm/V^2 was observed, which may be due to high defect density on porous alumina. Later, Kannadassan et al. [41] demonstrated the fabrication of barrier-type anodic Al_2O_3 MIM capacitor with a dielectric thickness of 14.3 nm. The anodization was performed using an electrolyte solution of ammonium pentaborate dissolved in ethylene glycol, which offers barrier anodic thin films. A capacitance density of ~6 fF/μ m^2 with low leakage current density of <10 nA/cm^2 was observed. A low quadratic VCC of ~500 and 120 ppm/V^2 was achieved for dielectric thicknesses of 14.3 and 49.5 nm, respectively [41]. Barrier-type anodic alumina exhibit low defect density (<10^{15}/cm^3) with large ionic polarization [42], [43]. Barrier-type anodic alumina-based MIM capacitor was fabricated using sulfuric acid and was reported later [40]. It is observed that a high capacitance density of 7 fF/μm^2 with a low VCC of less than 500 ppm/V^2. In comparison of Al_2O_3 MIM capacitors fabricated using various deposition/growth schemes, considering ITRS/IRDS recommendation, anodization exhibits an excellent performance close to the ALD scheme. However, anodization has a few limitations considering the CMOS/BEOL process flow. Selective oxidation of MIM capacitor site is difficult. Also, the choice of anodic
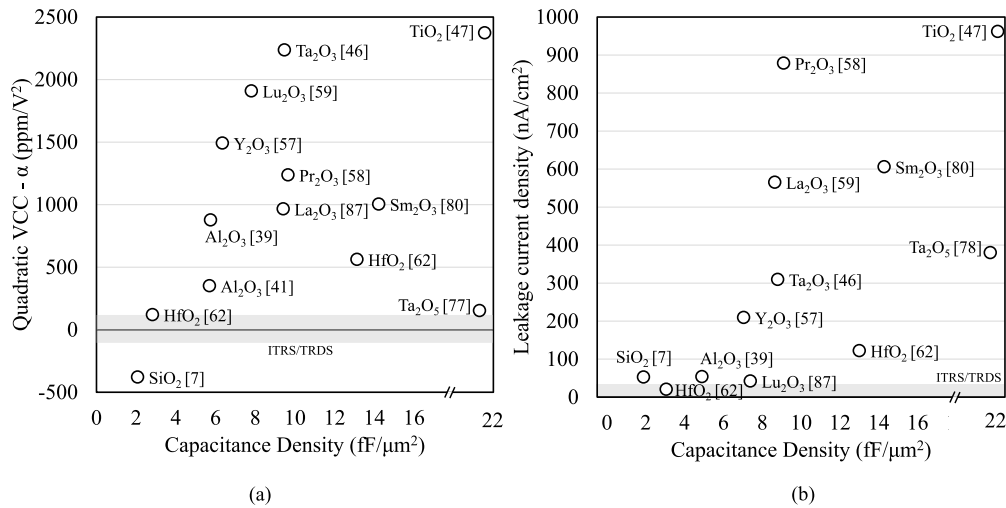
Fig. 7. *In literature, we often find MIM capacitors with undoped single-layer dielectrics, which include SiO_2, Al_2O_3, HfO_2, Ta_2O_5, and TiO_2. (a) and (b) Quadratic-VCC (α) and leakage current density of MIM capacitors as a function of capacitance density for various undoped single-layer dielectrics, respectively, found in the literature. The gray region shows the requirement of ITRS/ITDS. Most of the oxides exhibit a high VCC and high leakage characteristics, except HfO_2.*

potential/current to achieve a dielectric thickness is critical, which may result in physical breakdown.

HfO_2 is one of the attractive materials for dielectrics in nanoscale devices, which has been extensively studied by many researchers during the last decade. With a dielectric cosntant of ~25 and a bandgap of 5.7 eV, replacing SiO_2 by HfO_2 reduces the short-channel effects in MOSFET. Mise et al. [28] reported that HfO_2 is a promising and optimum dielectric material for DRAM technologies. Using PVD technology, 50-nm HfO_2 MIM capacitor achieved a capacitance density of 3.3 $fF/\mu m^2$ with a leakage current of 90 nA/cm^2 at 5 V [44]. A high-density MIM capacitor with HfO_2 was fabricated by Yu et al. [45]. It shows a capacitance density of 13 $fF/\mu m^2$ for the 10-nm-thick film using ALD [45]. Hu et al. [46] demonstrated the fabrication of 56-nm-thick HfO_2 MIM capacitor using pulsed-laser deposition (PLD). This capacitor shows a high capacitance density of >18 $fF/\mu m^2$ and a leakage current density of less than 2 nA/cm^2 for 3 V. No annealing or sintering was performed during fabrication since the deposition was carried out at temperature of 200 °C [46]. The VCC reduces from 134 to 44 ppm/V^2 as the frequency increases due to the reduction in polarizability of dipole molecules.

Tantula or Ta_2O_5 is one of the stable dielectric materials, such as Al_2O_3, whose dielectric constant varies from 25 to 30. Tu et al. [47] and Jeong et al. [48] demonstrated the compatibility of Ta_2O_5 MIM capacitors using MOCVD for Cu BEOL technology. These capacitors showed a capacitance density of less than 5 $fF/\mu m^2$ with a very low VCC of 9.9 ppm/V^2, and this is due to higher thickness of Ta_2O_5 [47], [48]. However, the leakage current density was predicated as 100 times greater than that of Al_2O_3 and SiO_2 [47], [48]. Sedghi et al. [102] reported the fabrication of

Ta_2O_5 MIM capacitor using wet anodization. The reliability and temperature-dependent leakage characteristics were also reported in this investigation. It was observed that the trap barrier height of Ta_2O_5 is 1.3 V, which is close to that of Al_2O_3. Titanium dioxide or titania (TiO_2) is an attractive material that has evolved with considerable interest in a variety of applications such as gas sensors, photovoltaic devices, and capacitors [49], [50], [51]. TiO_2 naturally exists in three crystalline phases, namely, rutile, anatase, and brookite, with a dielectric constant of 40–100 and an energy bandgap of ~3.0 eV [52]. However, its dielectric constant can be improved by various treatments, particularly annealing until 800 °C [53]. A decade ago, TiO_2 MIM capacitors have been fabricated using thermal oxidation [51] and dc magnetron sputtering [54]. Thermal oxidation and dc magnetron sputtering yield MIM capacitor with high leakage current density ($>10^{-4}$ A/cm^2) and capacitance variation $\Delta C/C_0$ of more than 10^4 ppm [51], [54]. Also, the polarization and high defect density in bulk/metal–insulator interface are leading to high dependency of capacitance with frequency [54]. The high leakage current density of Ta_2O_5 and TiO_2 MIM capacitors is due to their low bandgap of 4.2 eV and 3 eV, respectively.

Few rare-earth dielectrics were also employed in MIM capacitors in the last decade. Yang et al. [55] and Yang et al. [56] reported MIM capacitors with Sm_2O_3 and La_2O_3, respectively. These capacitors were fabricated with optimization on PVD, which showed a high capacity of more than 7.5 $fF/\mu m^2$. It was observed that the VCC reduces from 1000 to 100 ppm/V^2 when the dielectric thickness was increased [55], [56]. Y_2O_3 and Pr_2O_3 were also used in MIM capacitors, which yield more than 8 $fF/\mu m^2$ with a VCC of $>10^4$ ppm/V^2 and $>10^3$ ppm/V^2, respectively [57], [58]. Lu_2O_3 MIM capacitors with Ni
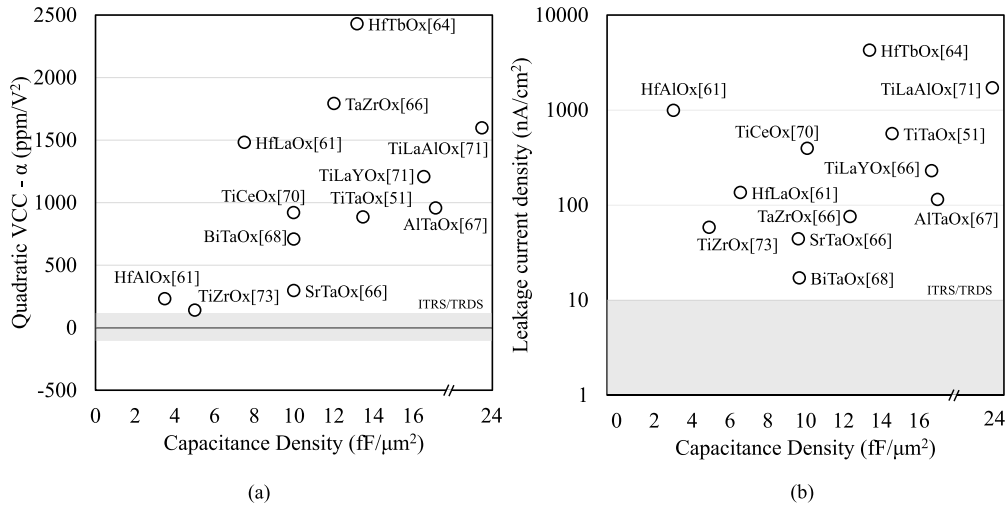
Fig. 8. *Doping of Al, Ti, and Ta with high-k oxides for MIM capacitors is reported many times in literature to improve the performance. (a) and (b) Quadratic-VCC (α) and leakage current density of MIM capacitors with various doped (binary and ternary) single-layer dielectrics, respectively, found in the literature. In comparison with the gray region, the ITRS/ITDS recommendation, the VCC, and the leakage characteristics are improved from MIM capacitors compared to undoped dielectric cases, yet they could not reach the demand.*

top electrode show a capacitance density of 7.5 fF/μm^2 and a leakage current density of 50 nA/cm^2 at 1 V [59]. It shows a good reliability of 0.51% of $\Delta C/C_0$ at 3 V for the continuous stress of ten years. Fig. 7(a) and (b) shows the comparison of quadratic VCC and leakage current density (at 1 V) of MIM capacitors with various undoped single-layer dielectrics. It is observed that the capacitance density is high as the dielectric constant of the material increases. However, the quadratic VCC (here after: α−VCC) and leakage current density are higher for MIM capacitors with high capacitance density compared to ITRS/IRDS requirements (gray region). This is due to the inverse relationship of bandgap and permittivity of the dielectric oxides. Among these undoped oxides, HfO$_2$ and Al$_2$O$_3$ MIM capacitors show high performance for RF/mixed-signal applications. This may be due to improved crystalline and defect properties, which show low dependence of polarization with applied voltage and high breakdown field. While Ta$_2$O$_5$ is potentially good material, its amorphous nature results in low capacitance density and high VCC. Triyoso et al. [60] demonstrated BEOL-compatible Ta$_2$O$_5$ MIM capacitor with a high density of >20 fF/μm^2 and an α−VCC of <200 ppm/V^2. From material characterization, it was observed that most of the deposition methods of Ta$_2$O$_5$ results amorphous, which reduces the capacitance and enhances the quadratic VCC.

Single-layer dielectric MIM capacitors with conventional oxides show high capacitance density by reducing the thickness and good quality of oxide growth. However, reduction of α−VCC and leakage current density is challenging against high capacitance density. In this regard, many attempts were reported on ternary oxide-based dielectrics for MIM capacitors. In most of the cases, ternary oxides were achieved by co-doping of metal oxides or oxidation of metal alloys. It is popular that high

permittivity oxide is mixed with high bandgap oxides to achieve high capacitance density (>10 fF/μm^2) and low leakage current density (<1 nA/cm^2). Few reports on fabrication and characterization of HfAlO$_x$ MIM capacitors presented high capacitance densities with attractive α−VCC of <200 ppm/V^2 [61], [62]. High mole fraction of Al$_2$O$_3$ shows low α−VCC and low leakage current density, and however, the capacitance density reduces as the permittivity reduces. Also, the inclusion of Al$_2$O$_3$ shows less dependent of leakage current on device temperature than HfO$_2$ [62].

Alternatively, the doping of Al, Ti, and Ta with high-k oxides for MIM capacitors is reported many times [61], [62], [63], [64], [65], [66]. TiTaO, TiCeO, TiZrO, TiLaAlO, TiLaYO, and a few combinations are worth mentioning [51], [67], [68], [69], [70], [71]. A very high density greater than 20 fF/μm^2 was demonstated using TiTaO$_x$ MIM capacitors [51]. With the advantage of high breakdown field strength of Ta$_2$O$_5$, the MIM capacitor shows significant reduction of leakage current density in comparison with TiO$_2$. Cheng et al. [18] reported the fabrication and characterization of TiZrO MIM capacitor using a sputtering process. A high capacitance density of 5.5 fF/μm^2 with a VCC of 105 ppm/V^2 was reported. It was observed that the improvement in VCC and low leakage is due to a higher band offset ($\triangle E_C$) of 1.42 eV, which is higher than HfO$_2$ and Ta$_2$O$_5$. Fig. 8 shows a comparison of quadratic VCC and leakage current density (at 1 V) of MIM capacitors with various single-layer ternary oxide dielectrics. Except for the HfAlO$_x$ case, many of the dielectrics show high capacitance density for MIM capacitors. However, most of them show high α−VCC and leakage current density. This shall be due to the high density of trap and large grain size as a result of TiO$_2$ doping. This makes the fast reduction of capacitance for high frequency, which is undesirable

for AMS ICs. Yet, the fabrication of MIM capacitors with doped dielectrics in BEOL-compatible fabrication processes is seldom reported.

V. STACKED HIGH-k DIELECTRIC MIM CAPACITORS

Mise et al. [28] have shown that the effective barrier height of high-k MIM structure decreases with increment in permittivity. If the DT of charges from metal to metal alone is being considered, the effective barrier thickness drastically reduces for the increase in dielectric constant. This shall further lead to high leakage and poor reliability of oxide. On the other hand, $\alpha-$VCC is largely influenced by the polarization process of dielectric material. This effect can be reduced by adding thin layers of oxides with low $\alpha-$VCC. Fabrication of high-k dielectric stack engineering has emerged in MIM capacitors to solve these issues. Usually, a thin barrier layer of large bandgap dielectric material (Al_2O_3 and SiO_2) is stacked with very high dielectric constant material (ZrO_2, TiO_2, and HfO_2). Recently, many authors have reported on various bilayer stack MIM capacitors such as HfO_2/SiO_2, $HfTiO/Y_2O_3$, TiO_2/SiO_2, and $SrTa_2O_7/SrTiO_3$ [19], [22], [72], [73]. Two motivations are often visible in various reports of dielectric stack MIM capacitors for analog/mixed-signal applications:

1) reduction of $\alpha-$VCC with a low-k dielectrics or polar dielectrics;
2) reduction of leakage current density by introducing large bandgap materials.

Laminated HfO_2/Al_2O_3 stack MIM capacitors were reported by Ding et al. [74] for RF applications. These capacitors exhibit a capacitance density of more than 4 fF/μm^2 with an acceptable VCC of 200 ppm/V^2 at 1 MHz. It was found that the thickness of Al_2O_3 significantly reduces the VCC and sensitivity of capacitance with frequency. Along with HfO_2, many high-k oxides, such as $HfO_xC_yN_z$ [75] and $LaAlO_3$ [63], were stacked and proposed in recent years. MIM capacitor with laminated $Ta_2O_5/HfO_2/Ta_2O_5$ stack was developed in [48]. The capacitor shows a capacitance density of 4 fF/μm^2 and a low VCC of 16.9 ppm/V^2 with a high leakage of 10^{-7}A/cm^2 at 3.3V [48]. MIM capacitor with a dielectric stack of 3 nm Al_2O_3 on 40-nm Ta_2O_5 was reported by Ishikawa et al. [76], which showed a capacitance density of 4.4 fF/μm^2 and a VCC of 400 ppm/V^2. However, the capacitance density increased to 9.2 fF/μm^2 with a VCC of 3580 ppm/V^2, while the Ta_2O_5 thickness was reduced to 16 nm [76]. Here, Al_2O_3 acts like a barrier layer, which reduces the leakage current density. The Al_2O_3/Ta_2O_5 stack showed a low leakage current density of 10^{-8} A/cm^2, which is lower compared to HfO_2/Ta_2O_5. This is due to large bandgap of Al_2O_3 compared to HfO_2. Kannadassan et al. reported the fabrication of TiO_2/Al_2O_3 MIM capacitor using anodic oxidation. They observed that the capacitor exhibits a high capacitance density of 7.6 fF/μm^2

and a low leakage current density of <10 nA/cm^2 and a low VCC of <200 ppm/V^2 [77].

Negative $\alpha-$VCC of SiO_2 was investigated by many researchers for the last two decades; however, it was modeled accurately by Kannadassan et al. [78] and Phung et al. [20]. This behavior is helpful in canceling the positive VCC of many high-k dielectric materials. Kim et al. [22] proposed such a possible stack and achieved a very low VCC of 14 ppm/V^2. Stack of 12-nm ALD HfO_2 and 4-nm PVD SiO_2 with TaN electrodes results in a capacitance density of 6 fF/μm^2 with a low leakage of 10 nA/cm^2 at 4 V [22]. Using similar canceling idea, Yang et al. [79] reported the fabrication of MIM capacitors with rare-earth Sm_2O_3 stacked on SiO_2, which showed a low VCC of less than 100 ppm/V^2 with a capacitance density of 7 fF/μm^2. However, it shows high leakage compared to HfO_2/SiO_2, as 10^3 nA/cm^2 at 4 V. This is due to low bandgap of Sm_2O_3 and dominant PF emission at low voltages [79]. TiO_2/SiO_2 stack MIM capacitor has been demonstrated recently by Wu et al. [72]. The capacitor exhibits a high capacitance density up to 11.2 fF/μm^2 and a very low VCC of 30 ppm/V^2. Here, 14-nm TiO_2 film was deposited using e-beam evaporation at room temperature, followed by furnace annealing in O_2 ambient at 380 $^\circ$C. The resulting TiO_2 is amorphous with a dielectric constant of 31. Later, polycrystalline TiO_2 with a dielectric constant of 111 was achieved by rapid thermal annealing in the presence of N_2 at 500 $^\circ$C [72]. $Pr_2Ti_2O_7$ on SiO_2 stacked MIM capacitor was reported by Wenger et al. [71], which results in 3.2 fF/μm^2 with a VCC of less than 100 ppm/V^2. Due to a low dielectric constant of SiO_2, the total capacitance of MIM capacitor was decreased in these works. Fig. 9 shows the performance of MIM capacitor with various dielectric stacks. Many stacks of high-k dielectrics show high capacitance density with low leakage current density. On the other hand, the stacks of high-k/SiO_2 exhibit a low VCC of less than 100 ppm/V^2 due to negative VCC attribute of SiO_2.

VI. CHALLENGES IN MIM CAPACITORS OF AMS ICs

In Sections IV and V, a detailed review on the fabrication and performance of high-k MIM capacitors was presented. Many capacitors exhibit a high capacitance density of >10 fF/μm^2 because of dielectric materials with high dielectric constant. However, many of the capacitors with single dielectric layer exhibit high VCC and high leakage current density. Therefore, we need to understand the basic physics of VCC and leakage current of MIM capacitor. This understanding, through physical equations, can help us to design low VCC and low leakage MIM capacitors with optimal thickness for the dielectric constant.

A. Physical Limits of Voltage Linearity in MIM Capacitors

The origin of nonlinear behavior of capacitance with voltage was understood through physics and modeling
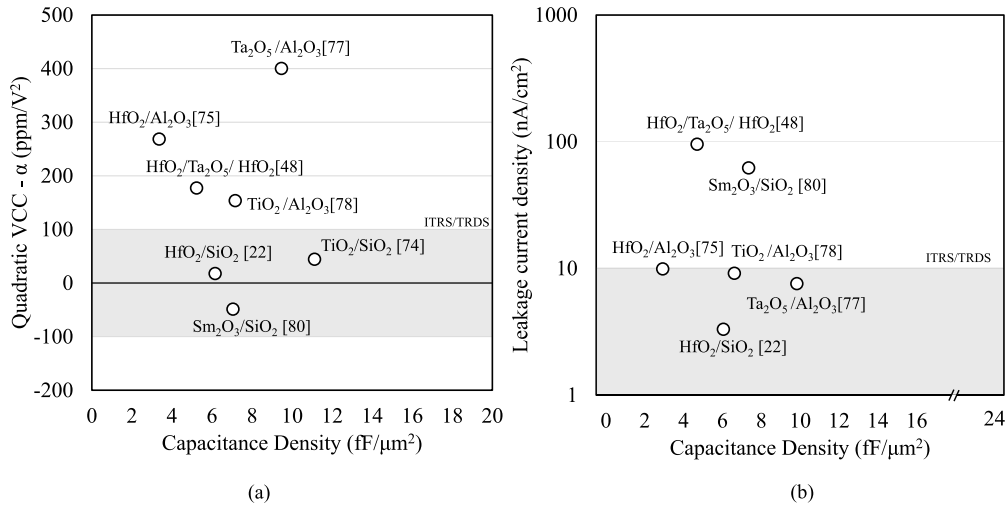
Fig. 9. *Many reports on MIM capacitors with multilayer stacked dielectrics, often a combination of SiO_2, Al_2O_3, HfO_2, Ta_2O_5, TiO_2, and few rare-earth materials. (a) and (b) Quadratic-VCC (α) and leakage current density of MIM capacitors with bilayer and multilayer dielectrics, respectively, found in the literature. While the performance of MIM capacitors is significantly improved to reach the ITRS/ITDS recommendation (gray region), only a few stacked dielectric layers with SiO_2 show excellent performance. It was found that these improvements are due to the negative VCC nature and large bandgap of SiO_2 MIM capacitors.*

by many researchers around the world. Few derived the physical model of VCC based on polarization mechanisms, such as orientation polarization [20], electrode polarization [21], electrostriction [80], and ionic polarization [17]. Phung et al. [20] demonstrated the physical model of negative VCC for SiO_2 MIM capacitors using orientation polarization. This model shall be suitable for dielectrics with strong permanent dipole moments. However, many high-k dielectrics show dominant induced dipole moments, such as Al_2O_3 and HfO_2. Recently, our group demonstrated the analytical model using microscopic and macroscopic modeling for voltage linearity, which can be used for all high-k dielectrics [78] and other polar dielectrics [81]. In this section, the review of physical models of positive and negative VCC of MIM capacitors is presented.

Dielectric materials are attributed to the polarization of dipole molecules for the applied external electric field. Inside MIM capacitors, the capacitance has involvement of various polarization mechanisms, namely, electronic polarization (P_e), ionic polarization (P_i), orientation polarization (P_o), and space charge polarization (P_{sc}). Thus, the total effective polarization of dielectric layer is $P = P_e + P_i + P_o + P_{sc}$. Here, the ionic and electronic polarization are almost independent of applied field. The electronic polarization shows the induced dipole moment of polarized molecules due to the shift of metal ions of molecule with respect to oxygen for the applied external field. This polarization of induced dipoles is called ionic polarization, which is largely dominant in ionically bonded materials (such as Al_2O_3). P_i causes increase in permittivity for the applied external field; therefore, it results in positive quadratic VCC. The negative VCC is dominated by the polarization of induced/permanent dipoles in a few

dielectric materials. In the SiO_2 system, the Si atom and four oxygen atoms are grouped by local tetrahedral bonding, even in the amorphous state. When the field is applied, the lattice distortion occurs and leads to the formation of induced dipole.

In the macroscopic scale, the polarizations of dielectrics are modeled in different ways. The average dipole moment of induced dipoles is derived as $\overline{M_i} = \alpha_d \overline{\cos^2\theta} E_{loc}$ [82]. However, few dielectrics with permanent/active dipoles takes $\overline{M_o} = \alpha_d \overline{\cos\theta} E_{loc}$. Here, the local electric field (within the unit molecule) $E_{loc} = \lambda E$ and the internal electronic polarizability α_{ie}, and the dipoles are distributed at an angle of θ with respect to the external field (E) attributes the polarization. The mean value of $\cos^2\theta$ and $\cos\theta$ can be computed using the Boltzmann statistics [78]. They can be, further, expressed as

$$\overline{\cos^2\theta} = L_2(\beta) = 1 - \frac{2}{\beta}L(\beta) \approx \frac{\beta^2}{15} \qquad (9)$$

and
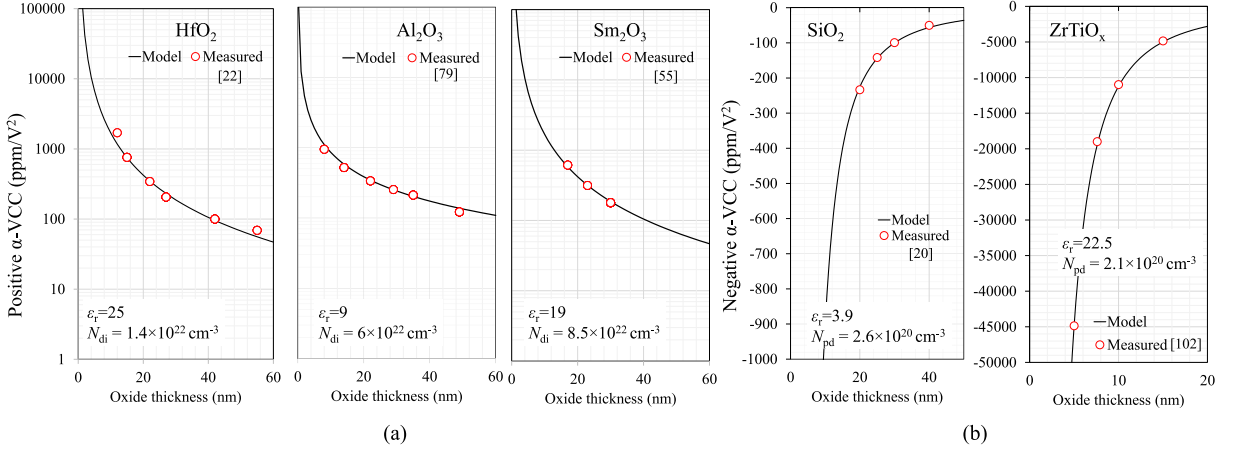
$$\overline{\cos\theta} = L(\beta) = \tanh(\beta) \approx -\frac{\beta^3}{3} + \beta \qquad (10)$$

where $\beta = (\alpha_{ie} E_{loc}/kT)$. These approximations are valid within the statistics [83]. This results in the macroscopic polarizations as

$$\alpha_i = N_{di}\alpha_{ie}L_2(\beta) \qquad (11)$$

$$\alpha_{op} = \lambda N_{pd}\alpha_{ie}\frac{L(\beta)}{\beta}. \qquad (12)$$

Fig. 10. *To achieve low VCC ($<$100 ppm/V^2), one should understand the physical nature of various dielectric materials, in view of dielectric polarization. By analytical modeling of the permittivity of the dielectric layer for the applied external E-field, the quadratic VCC is modeled as a function of oxide thickness [see (16) and (17)]. This model is mapped along with measured VCC of MIM capacitors with a few selected dielectrics, which exhibit (a) positive VCC and (b) negative VCC. The fitting indicates the agreement of the analytical model with experiment and offers a gateway to solve the IRTS/IRDS challenge.*

At the microscopic level, the internal/induced electronic polarizability of charges within the dipole sphere α_{ie} can be arrived through the Clausius–Mossotti equation [84]

$$\alpha_{ie} = \frac{3\varepsilon_0}{N_{pd}}\left(\frac{\varepsilon_r - 1}{\varepsilon_r + 2}\right). \tag{13}$$

Finally, we can derive the field-dependent permittivity of dielectrics with induced and permanent dipoles, $\varepsilon_{r,id}$ and $\varepsilon_{r,pd}$, respectively, as

$$\varepsilon_{r,id}\left(E\right) = \varepsilon_0\varepsilon_r + N_{di}\left[\frac{3\lambda\varepsilon_0}{N_{di}}\left(\frac{\varepsilon_r - 1}{\varepsilon_r + 2}\right)\right]^3 \frac{E^2}{15\left(k_BT\right)^2} \tag{14}$$

$$\varepsilon_{r,pd}\left(E\right) = \varepsilon_0\varepsilon_r + N_{pd}\left[\left[-\frac{3\varepsilon_0}{N_{pd}}\left(\frac{\varepsilon_r - 1}{\varepsilon_r + 2}\right)\right]^3 \frac{\left(\lambda E\right)^2}{3\left(kT\right)} + 1\right]. \tag{15}$$

These equations are compared to the empirical relation, $C(V) = C_0(\alpha V^2 + \beta V + 1)$, where C_0 is the capacitance at zero bias. The resulting positive and negative quadratic VCCs (α) of MIM capacitors are

$$\alpha_{+\text{VCC}} \approx 1.8\left(\frac{\varepsilon_0}{N_{di}k_BT}\right)^2\left[\lambda\left(\frac{\varepsilon_r - 1}{\varepsilon_r + 2}\right)\right]^3 \frac{1}{d^2} \tag{16}$$

$$\alpha_{-\text{VCC}} \approx -9\left(\frac{\lambda\varepsilon_0}{N_{pd}kT}\right)^2\left[\left(\frac{\varepsilon_r - 1}{\varepsilon_r + 2}\right)\right]^3 \frac{1}{d^2}. \tag{17}$$

Readers are suggested to refer to the literature [78], [81] for detailed derivations. Fig. 10(a) and (b) shows the fitting of positive and negative VCC of various dielectric materials, respectively. Fitting parameters are listed as

insets. It is evident that the proposed models of $\alpha_{+\text{VCC}}$ and $\alpha_{-\text{VCC}}$ are accurate and valid, at room temperature. Yet, these model equations should be validated with frequency and temperatrue. McPherson [26] reported the frequency and temperature dependence of dielectric constant for paraelectric dielectrics with a physical model. We adopted the similar model and modified as

$$\varepsilon_r\left(T, f\right) = 1 + \left(\frac{T_0}{T}\right)^n\left(\frac{f_0}{f}\right)^m\chi_e \simeq \varepsilon_{r0}\left(\frac{f_0}{f}\right)^m \tag{18}$$

where T_0 and f_0 are the reference temperature and frequency, respectively, at which ε_r is initially measured. ε_{r0} is the measured dielectric constant at reference operating frequency (f_0) and temperature (T_0). The temperature and frequency dependence factors n and m are typically nonzero values, respectively; however, they are small. This model is used in (16) and (17) to validate the frequency and temperature dependence of $\alpha_{+\text{VCC}}$ and $\alpha_{-\text{VCC}}$. Fig. 11(a) and (b) shows the calculated $\alpha_{+\text{VCC}}$ and $\alpha_{-\text{VCC}}$ of various MIM capacitors in comparison with measured results reported elsewhere [22], [85], assuming that $f_0 = 1$ kHz and $T_0 = 300$ K. Both positive and negative VCCs show a linear dependence with temperature and frequency. The fitting factors n and m are listed as insets of Fig. 11(a) and (b), respectively. It is clear that the temperature and frequency dependence of dielectric constant has a huge impact on VCC. These phenomena should be studied by microelectronic engineers to design the high-performance and reliable mixed-signal ICs.

Using these models, one can find the thickness of dielectric layer of MIM capacitor to achieve the ITRS/IRDS requirement. Equation (16) is rearraged to compute the physical thickness required to arrive
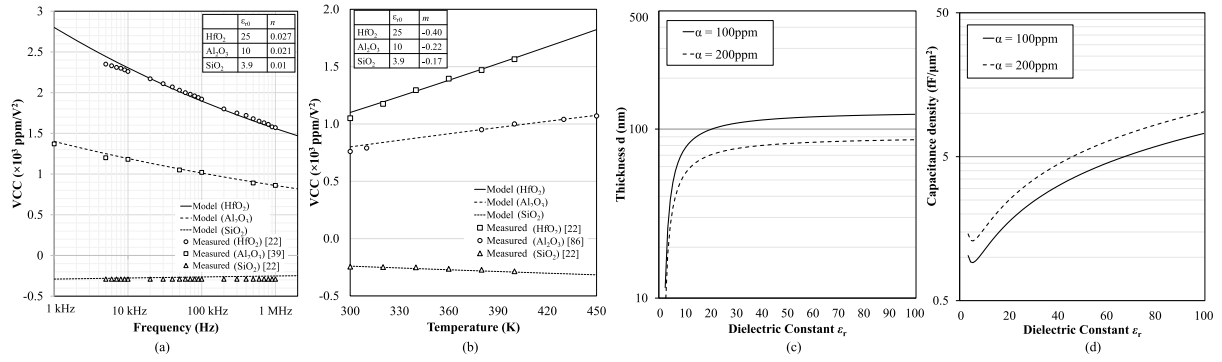
Fig. 11. *Presented analytical model of α_{+VCC} and α_{-VCC} is also validated for the measured data against (a) frequency and (b) temperature. This model can predict the nature of MIM capacitors for analog applications at high frequencies and high temperatures. By rearranging (16), one shall find the suitable thickness of the dielectric layer to achieve $\alpha = 100$ ppm/V^2 and 200 ppm/V^2, plotted in (c). Furthermore, (d) plots the achievable capacitance density for the calculated dielectric thickness to meet $\alpha = 100$ ppm/V^2 and 200 ppm/V^2. These plots inquire the critical technology requirements for future analog/mixed-signal ICs.*

$\alpha = 100$ and 200 ppm/V^2 as a function of permittivity, as shown in Fig. 11(c) (assuming that $N_{di} = 10^{22}$/cm^3 and $T = 300$ K). For the same dielectric constant, the optimal thickness increases to achieve lower VCCs, which results in lower capacitance density. Fig. 11(d) shows the achievable capacitance density of single dielectric layer MIM capacitors with $\alpha = 100$ ppm/V^2 and 200 ppm/V^2. From both plots, one shall understand the critical technology requirement for MIM capacitors. They suggest to use high-k dielectric material with $\varepsilon_r < 60$ to achieve low quadratic VCC. However, the electrode area should be large enough to achieve desirable capacitance. This may increase the overall IC area. Al$_2$O$_3$, HfO$_2$, and ZrO$_2$ MIM capacitors are good choice with in $\varepsilon_r < 60$. For $\varepsilon_r > 60$ dielectrics, such as TiO$_2$, the thickness requirement exceeds 100 nm, which significantly increases the design complexity and fabrication cost to manage the interconnect/via implementation.

B. Physical Limits of Leakage Current of MIM Capacitors

To meet the ITRS/IRDS recommendations of capacitance density and leakage current density, listed in Table 1, the MIM capacitor should hold an ultrathin film of high-k dielectrics. However, the reliability and leakage of MIM capacitors are inversionally proportional to the dielectric thickness. For instance, Schuegraf and Hu [86] derived the maximum operating voltage of MOSFET for the thickness high-k oxides to achieve an intrinsic lifetime of ten years. It was observed that, even without traps/defects, the oxide dielectrics experience leakage by DT and FNT mechanisms. Considering these facts, we took two tunneling phenomena, DT and FNT, to compute the material-dependent leakage current density of MIM capacitors. This framework shall help us to quantify the optimal thickness with respect to the choice of permittivity (ε_r). Also, the limitations of high-k dielectric MIM capacitors to achieve ITRS/IRDS recommendations can be understood.

DT and FNT mechanisms are largely depending on the SB at the metal–insulator interface. Robertson [27] computed the band offsets and SB heights of high-k oxides [28]. Using a dimensionless pinning factor (S), the bandgap and permittivity of the oxides are related to simple empirical relations. This work was performed for the MOS structure, and therefore, the SB height shall be calculated relative to the conduction band edge of silicon. Using metal work function ϕ_m and conduction band edge of silicon ϕ_{Si}, we can calculate the band offset with

$$\phi_{\text{BO}} = \phi_{\text{BR}} + \phi_m - \phi_{\text{Si}}. \tag{19}$$

Using this relationship, the relative barrier height ϕ_{BR} is computed as a function of permittivity (ε_r) and presented in Fig. 12(a). It is worth noting that $\phi_{\text{BO}} < 0$ after $\varepsilon_r > 60$, which indicates that the DT is dominant in that regime of ε_r. To relate ε_r and ϕ_{BO}, we proposed a simple empirical model

$$\phi_{\text{BO}} \approx 5.28 - 1.25 ln\left(\varepsilon_r\right). \tag{20}$$

This model shows good comparibility with ϕ_{BO} data from [27]. Using this equation, the current density due to DT and FNT in thin dielectric MIM capacitors, respectively, can be caculated for the applied potential [86]

$$J_F\left(V\right) = \zeta \frac{\left(2\phi_{\text{BO}}^2 - \phi_{\text{BO}}V\right)}{d^2} \exp\left[-\xi T_F\right] \tag{21}$$

$$J_D\left(V\right) = \zeta \frac{V^2}{d^2} \exp\left[-\xi T_D\right] \tag{22}$$

where d is the physical thickness of dielectric layer. The FNT and DT mechanisms are dominant for $\phi_{\text{BO}} < V$ and $\phi_{\text{BO}} \geq V$, respectively. Here, ζ and ξ are proportionality
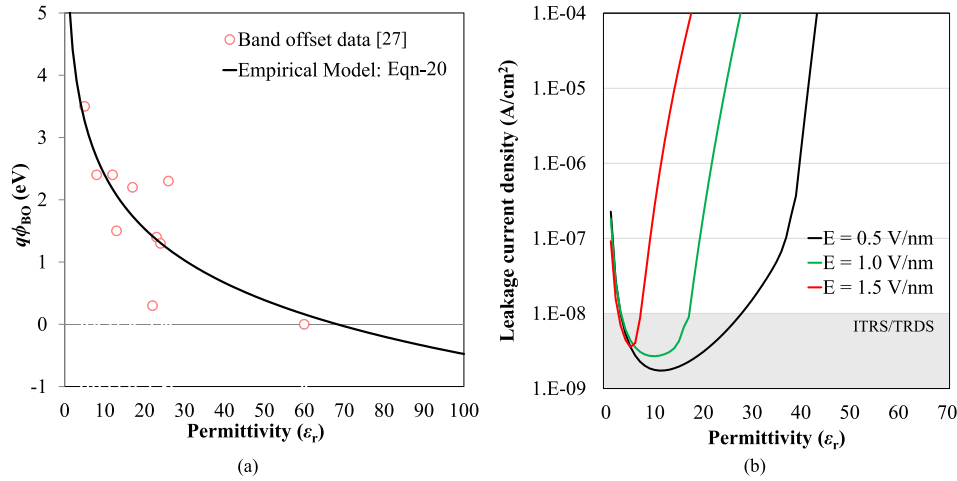
Fig. 12. *Unlike VCC, the physical model of leakage characteristics of MIM capacitors depends on bandgap relative to metal work function. (a) Simple empirical model is proposed to fit the computed band offset (ϕ_{BO}) and empirical model as a function of relative permittivity (ε_r) (measured data: [27], [28]). (b) This model is further used to map the total current density as a function of permittivity (ε_r) for the applied electric field (E), against the ITRS/IRDS challenge of <10 nA/cm² (gray region).*

constants

$$\zeta = \frac{q^2}{8\pi h \phi_{BO}}$$

$$\xi = \frac{8\pi}{3h}\sqrt{2m_{\text{eff}}q}$$

and the tunneling probability coefficients T_F and T_D are

$$T_F = d.\frac{\left[\phi_{BO}^{3/2} - (\phi_{BO} - V)^{3/2}\right]}{V} \tag{23}$$

$$T_D = d.\frac{\phi_{BO}^{3/2}}{V}. \tag{24}$$

Using the calculated the band offset ϕ_{BO} from (20), for the applied field of $E = V/d = 0.5$, 1 and 1.5 V/nm, the total current density $J_{\text{eff}} = J_F + J_D$ is computed for various permittivity (ε_r) and presented in Fig. 12(b). It is clear that materials with $\varepsilon_r < 30$ exhibit low leakage current density of <10 nA/cm² for the operating field of 0.5 V/nm. As the field strength increases, the DT mechanism dominates the current density, which reduces the window of permittivity (ε_r) for ITRS/IDRS requirements. Within this limited window, few successful oxides exhibit excellent performance, such as Al$_2$O$_3$ and HfO$_2$. Similar observation is observed in Fig. 7(b).

C. Challenges in BEOL Process

BEOL technology successfully implements complicated CMOS circuits with metal interconnects, via, and metal layers. After the era of aluminum (Al), copper (Cu) has been employed in present day IC fabrication, nearly for 20 years. This is due to low resistitivty (<10 $\mu\Omega\cdot$cm) and better electromigration endurance [87]. Reports on the study of MIM capacitor's performance in Cu interconnect for BEOL process found in early 2000 [35], [36].

Armacost et al. [35] reported the first demonstration of integrated MIM capacitors in 180-nm CMOS technology. They fabricated a silicon nitride MIM capacitor with six wiring levels and a dual damascene interconnect scheme. A good capacitance density of >0.5 fF/μm² was achieved with low leakage current density of <10 nA/cm² for the bias voltage up to 10 V. To avoid Cu contamination, Al/TiN electrodes were grown with ALD. Yet, these complex structures need additional lithography and cleaning processes.

Ng et al. [36] reported the fabrication of MIM capacitors with Ta electrodes, which reduced overall fabrication cost significantly. This results a high capacitance density of >1 fF/μm² and a high quality factor of >100, which are largely preferred for RF/analog applications. For the past 20 years, few reports have been found on the fabrication of MIM capacitors, which are compatible with BEOL process integration. Al$_2$O$_3$ [47], [88], Ta$_2$O$_5$ [60], HfO$_x$ [89], and ZrO$_2$ [90] MIM capacitors were reported by few industries and academia. Recently, a multilayer stack of high-k/Al$_2$O$_3$/high-k dielectrics for MIM capacitor in a three-level BEOL process was demonstrated by Cheng et al. [91]. They could achieve a high capacitance density of >20 fF/μm² and a low leakage current density of <10 nA/cm² for decoupling capacitor applications. They also achieved high reliability with TBD of >10 years for the constant bias voltage ~ 3.5 V.

A few challenges on the fabrication of MIM capacitors in the BEOL process were listed in the literature, which should be considered to reduce the fabrication cost and device failure. During the etching/polishing of low-k dielectrics to reach the MIM structure, few topographic complexities result in failure of capacitor fabrication [92]. One of the common topography issues is shorterning of top and bottom electrodes by Cu via due to over polish. This short circuits the MIM capacitor, resulting poor parasitic effects and instable oscillation/noise within RF/analog

circuits. On the other hand, poor polish may result from remaining layers of low-k oxide above the MIM capacitor, which results in open-circuit conditions.

Alternatively, Cu contamination during or post-fabrication of MIM capacitor in the BEOL process results in degradation of dielectric quality. These phenomena significantly affect the effective thickness, which increases the leakage and reduces the lifetime of the capacitors and low-k dielectrics. This in turn available as noise/inteference source within RFICs. Annealing or post-treatment temperature shall allow the diffusion of Cu or electrode material inside high-k and low-k dielectrics. Cu interconnect/via are often the source of parasitic and electrostatic discharge (ESD) effects in MIM capacitor banks of analog or RF circuits. To reduce this effect, low-k or ultralow-k dielectrics were introduced between interconnects [93], [94]. However, the electrodes of MIM capacitors shall couple with nearby interconnect or ground line based on the thickness of low-k dielectrics. Recently, the line-edge roughness in interconnect/low-k interface was studied by Chu et al. [95]. As the technology nodes are scaled down, this roughness becomes relatively larger than in earlier days. It is worth noting that these challenges multiply to several orders for 3-D integrations. The analytical/simulation studies predict that this roughness will reduce the TBD significantly. It was suggested to develop a fault-tolerant design with relaxed roughness. Novel experimental and design schemes are required to address these complexities and reliability issues.

VII. OPPORTUNITIES ON FUTURE MIM CAPACITORS OF AMS ICs

From the earlier discussions, it is clear that quadratic VCC is low for MIM capacitors with thicker dielectric layer. However, it reduces the capacitance density lower than the minimum ITRS/IRDS requirements. On the other hand, as the bandgap of dielectric material is inversely proportional to the dielectric constant, the leakage current may be high if we choose dielectric material with higher dielectric constant. This challenge was understood by many researchers. They demonstrated the fabrication and characterization of MIM capacitors with multiple dielectric layers which are discussed in section V. Yet, achieving high capacitance density, low quadratic VCC, and low leakage current density beyond the physical limits is challenging. Also, the IC fabrication process in view of BEOL/FEOL technology adds a few limitations in realizing high-performance MIM capacitors for RF and AMS applications. In this section, we presented the possible solutions for the realization of high-performance MIM capacitors for future RF/AMS IC technology.

To reduce the voltage linearity coefficient, a few techniques can be adopted, while dielectrics that provide positive and negative quadratic VCC can be stacked to reduce the effective quadratic VCC of MIM capacitor. It also helps to achieve a low leakage current below the ITRS/IRDS requirement. However, the series capacitance

of stacked dielectrics may reduce the capacitance density in overall. Fortunately, using the models of positive and negative quadratic VCC, we can develop design equations to achieve zero VCC in MIM capacitors. For stacked or multilayer dielectric MIM capacitors, the CV relation can be expressed as

$$
\begin{aligned}
C_{\text{tot}}(V) &= C_{\text{tot},0}\left(\alpha_{\text{tot}}V^2 + \beta_{\text{tot}}V + 1\right) \\
&= \frac{C_1(V_1)\cdot C_2(V_2)}{C_1(V_1) + C_2(V_2)}
\end{aligned} \tag{25}
$$

where V_1 and V_2 are electric potential across the first and second layers, respectively. Each layer can be modeled into a lumped capacitance whose individual capacitance can be expressed as a function of voltage as

$$
C_1(V_1) = C_{1,0}\left(\alpha_1 V^2 + \beta_1 V + 1\right) \tag{26}
$$

and

$$
C_2(V) = C_{2,0}\left(\alpha_2 V^2 + \beta_2 V + 1\right) \tag{27}
$$

where $C_{1,0}$ and $C_2,0$ are capacitance at zero bias for the first and second layers, respectively. By the way, α_1, α_2, β_1, and β_2 are quadratic and linear coefficients of individual dielectric layers. For the applied voltage across the dielectric stack V, the potential across each layer can be expressed as $V_1 = \delta_1 V$ and $V_2 = \delta_2 V$. The constants were derived as

$$
\delta_1 = \left(\frac{k_2 d_1}{k_1 d_2 + k_2 d_1}\right) = \frac{C_{\text{tot},0}}{C_{1,0}} \tag{28}
$$

and

$$
\delta_2 = \left(\frac{k_1 d_2}{k_1 d_2 + k_2 d_1}\right) = \frac{C_{\text{tot},0}}{C_{2,0}} \tag{29}
$$

where k_1 and k_2 are relative dielectric constants of each layer with thickness of d_1 and d_2, respectively. Therefore, one shall write the total quadratic and linear coefficients of stack as
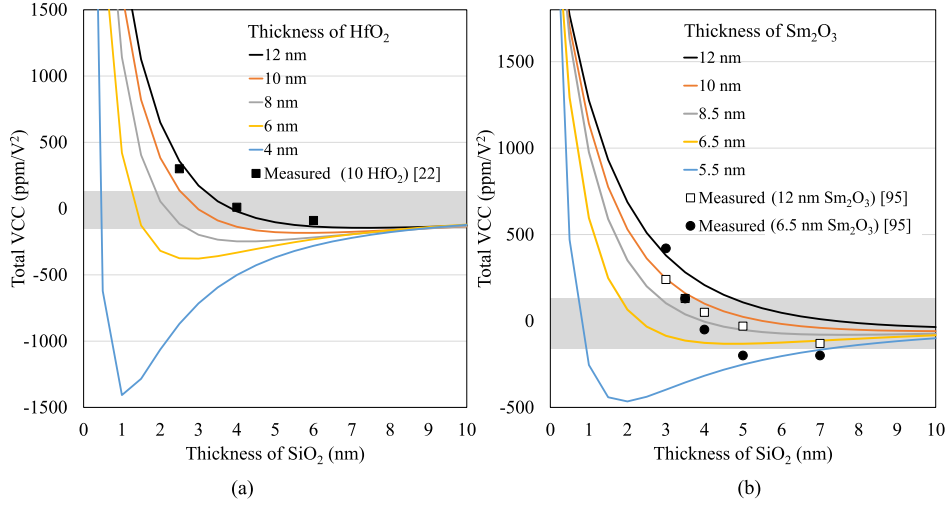
$$
\alpha_{\text{tot}} = \delta_1^3 \alpha_1 + \delta_2^3 \alpha_2 \tag{30}
$$

and

$$
\beta_{\text{tot}} = \delta_1^2 \beta_1 + \delta_2^2 \beta_2. \tag{31}
$$

The total capacitance density at zero bias is

$$
C_{\text{tot},0} = \frac{k_1 k_2}{(k_1 d_2 + k_2 d_1)}. \tag{32}
$$

Fig. 13. *Stacking a high-k dielectric layer with SiO$_2$ layer, which offers negative VCC, is a good approach, reported by few in literature. Using simple circuit theory, the total VCC of stacked dielectric MIM capacitors is computed as a function of SiO$_2$ thickness using (30). This total VCC is plotted for (a) HfO$_2$/SiO$_2$ and (b) Sm$_2$O$_3$/SiO$_2$ MIM capacitors (measured data [22] and [96]). The model fits well the measured data and indicates the achievement of ITRS/IRDS challenge (gray region) with a possibility to achieve less than an ultralow VCC of 10 ppm/V^2.*

Using 30, the total VCC α_{tot} of various high-k/SiO$_2$ stacked MIM capacitors can be calculated. Fig. 13(a) and (b) shows the calculated α_{tot} for HfO$_2$/SiO$_2$ and Sm$_2$O$_3$/SiO$_2$ MIM capacitors as a function of SiO$_2$ thickness, with respective physical parameters in the insets of Fig. 10. Along with calculated α_{tot}, the measured data are also plotted from the experimental works of Kim et al. [22] and Chen et al. [96] and found that the fitting is reasonable. In both MIM capacitors, the reduction of α_{tot} was observed for thinner high-k layer (d_1) against the thickness of SiO$_2$ (d_2). This is due to the influence of δ_1 and δ_2. α_{tot} can be further reduced by reducing the thickness of SiO$_2$. The region of expectation for the IRDS requirement falls within ± 100 ppm/V^2, which is highlighted in the plots. It is evident that the model can be used to optimize or design the low voltage linearity MIM capacitors.

To achieve $\alpha_{\text{tot}} = 0$ ppm/V^2, we need according to (30)

$$\delta_1^3 \alpha_1 = -\delta_2^3 \alpha_2. \tag{33}$$

If we assume that the first and second layers have dielectric materials with positive and negative VCCs, respectively, we can rewrite the coefficients as $\alpha_{+\text{VCC}} = \alpha_1$ and $\alpha_{-\text{VCC}} = \alpha_2$. Equation 33 can be, now, rearranged as

$$(k_2 d_1)^3 \alpha_{+VCC} = - (k_1 d_2)^3 \alpha_{-VCC}. \tag{34}$$

These quadratic coefficients $\alpha_{+\text{VCC}}$ and $\alpha_{-\text{VCC}}$ can be substituted from (16) and (17)

$$(k_2 d_1)^3 \left(1.8 \left(\frac{\lambda_1 \varepsilon_0}{N_{di} kT} \right)^2 \left[\left(\frac{k_1 - 1}{k_1 + 2} \right) \right]^3 \frac{1}{d_1^2} \right)$$

$$\approx (k_1 d_2)^3 \left(9 \left(\frac{\lambda_2 \varepsilon_0}{N_{pd} kT} \right)^2 \left[\left(\frac{k_2 - 1}{k_2 + 2} \right) \right]^3 \frac{1}{d_2^2} \right). \tag{35}$$

This can be rearranged to

$$\frac{d_1}{d_2} \approx 5 \frac{\left[k_1 \left(\frac{k_2 - 1}{k_2 + 2} \right) \right]^3}{\left[k_2 \left(\frac{k_1 - 1}{k_1 + 2} \right) \right]^3} \left(\frac{\lambda_2 N_{id}}{\lambda_1 N_{pd}} \right)^2 \tag{36}$$

where $\lambda_i = 3k_i / [2k_i + 1]$ for $i = 1$ and 2 are field correction factors. Equation (36) formulates the design condition of MIM capacitors with zero quadratic VCC. It describes that the zero VCC can be achieved by proper choice of thickness of d_1 and d_2 for positive VCC (k_1) and negative VCC (k_2) dielectric materials, respectively. Largely, this design method is limited by the choice of negative VCC materials. For instance, SiO$_2$ $(k_2 = 3.9)$ and ZrTiO$_x$ $(k_2 = 22.5)$ show clear negative VCC nature, which is presented in Section VI-A. Alternatively, SiN $(k_2 = 3.4)$ [32] and bariam titanate $(k_2 = 90)$ [100] are also exhibit negative VCC property. Using (36), the calculated (d_1/d_2) is computed as a function of k_1, for various k_2 such as SiO$_2$ and ZrTiO$_x$, and presented in Fig. 14. The solid lines indicate the recommended (d_1/d_2) for the choice of dielectric materials with selected negative VCC materials.

Few MIM capacitors of low VCC close to zero whose (d_1/d_2) are computed and placed in Fig. 14(a). MIM capacitors of HfO$_2$/SiO$_2$ [22], Al$_2$O$_3$/SiO$_2$ [98], and Er$_2$O$_3$/SiO$_2$ [97] with $(d_1/d_2) \approx 3.00$, 1.743, and 2.121 exhibit a low VCC of -14, 20, and -73 ppm/V^2, respectively. Similarly, ZrLaO$_x$/ZrTiO$_x$ MIM capacitors show a low VCC of 14 ppm/V^2. These attempts show that low VCC of <10 ppm/V^2 should be possible with present day or
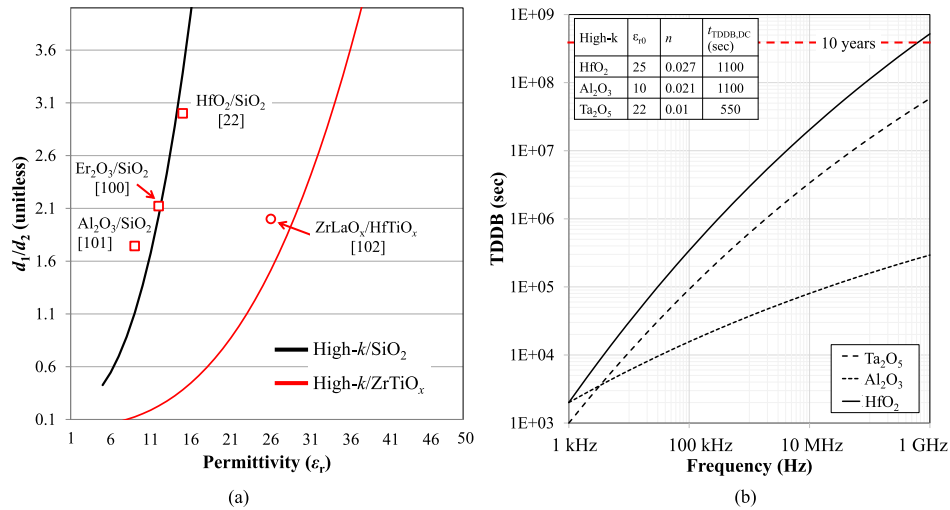
Fig. 14. *Zero VCC is possible by carefully solving the (30). (a) Solution is presented in (36) shows the ratio of the thicknesses of the high-k dielectrics (with α_{+VCC} and $\varepsilon_r = k_1$) and dielectrics (with α_{-VCC} and $\varepsilon_r = k_2$), as a function of k_1, for various k_2 (measured data: [20], [22], [98], [99]). This solution is a design equation for MIM capacitors to achieve ultralow VCC for future analog/mixed-signal ICs. Alternatively, the lifetime of high-k MIM capacitors is assessed for the operating frequency to study the reliability of future ICs. (b) Predicted TDDB lifetime of high-k MIM capacitors for the operating frequency up to 1 GHz using the McPherson TDDB model in (7). It indicates that the higher signaling frequency offers excellent reliability.*

near-future technology. It is possible using (36) which gives a design formula to achieve an MIM capacitor with low VCC. Among two polar dielectrics, SiO_2 shows low ε_r, which limits the maximum achievable capacitance density ($\sim$5 fF/μm^2). Alternatively, $ZrLaO_x/ZrTiO_x$ MIM capacitors show a high capacitance density of $\sim$13 fF/μm^2, which accomplish the requirement of ITRS/IRDS. This stacking of dielectric materials with negative and positive VCC opens new opportunities for high-precision MIM capacitors. Such capacitors help in the reduction of design complexity due to error compensation circuits within RF/AMS ICs. This study should be extended to calculate leakage current density, which helps designers to optimize the circuit design and fabrication cost.

Scaling the dielectric thickness and stacking of dielectric layers for the MIM capacitors progress to achieve high capacitance density and low VCC. However, the leakage and dielectric reliability limit them. Many mechanisms are involved in the leakage current of MIM capacitors. As mentioned in Section VI-B, MIM capacitors with insulating layer of $\varepsilon_r < 30$ exhibit low leakage current density, such as Al_2O_3 and HfO_2. These observations were arrived from the simple empirical model for the relationship between conduction band offset with ε_r. One can further develop a detailed semi-empirical model with an account of work function of metal contacts. Such a model and detailed analysis shall help to identify suitable material for the contacts of high-k MIM capacitors ($\varepsilon_r > 30$) to achieve ITRS/IDRS requirement. The dielectric reliability includes voltage-dependent dielectric breakdown and TDDB that are already discussed in section III-D. Frequency-dependent TDDB lifetime studies were reported

in recent times [101]. It was observed that the increase in frequency exhibited high TDDB lifetime compared to dc operation. In the model proposed by Arabi et al. [101], the defect generation during the electrical stress was significantly reduced while operating with ac signals of high frequency. This is due to the small or negligible recovery time.

Using the McPherson TDDB model (7), one can compute the typical TDDB lifetime of high-k MIM capacitors. From the measured data of $t_{TDDB,dc}$ for various high-k oxide MIM capacitors [15], [23], [102], we predicted the frequency-dependent TDDB lifetime, for the $E_{di} = 2$ MV/cm, keeping $t_{ON} = t_{OFF}$, $T = 300$ K. Fig. 14(b) shows the predicted TDDB lifetime for the operating frequency up to 1 GHz. The calculation parameters, such as ε_r and frequency dependency factor n, are listed in the inset table. One can observe that the high ε_r offers a longer TDDB lifetime, which is further increased for higher signaling frequencies. In close view, a high TDDB of ten years ($\sim$3.1 $\times$ 10^8 s) shall be achieved by HfO_2 MIM capacitors when it is operated with 1-GHz unipolar clock cycles. Kwak et al. [103] demonstrated the unipolar and bipolar voltage stress conditions for stacked dielectrics MIM capacitors. From the extrapolated data of experimentally calculated normalized voltage linearity coefficient, one can observe that unipolar signaling offers a low variation in capacitance over the years compared to continuous voltage stress. On the other hand, the normalized VCC over the stress time for bipolar stress conditions increased by about 70% compared to unipolar voltage stress. For future AMS applications, a detailed reliability analysis of MIM capacitors as a function of operating voltage, frequency, stress conditions, and

temperature is needed. Other important features of dielectric reliability are capacitor area, intrinsic defects, and process variability. Studies related to design strategies, production calibration, and compensation circuit design are needed to achieve low variability against voltage and frequency for high-performance RF/AMS ICs.

VIII. CONCLUSION

In this review, we presented the key challenges and opportunities involved in the fabrication, modeling, and design of high-k MIM capacitors for RF/analog ICs. From the evaluation and literature survey on various research work and attempts in theoretical and experimental to achieve high-precision MIM capacitors, the technological challenges are addressed through analytical modeling to achieve low quadratic VCC and low leakage current. These models show the limits of existing technology and solution for future demands. A detailed summary of challenges involved in the BEOL integration process of recent CMOS technologies is also presented.

Several novel schemes for the fabrication and design of high-precision and high-performance capacitors are needed to advance the present status as demanded by technology roadmaps, such as ITRS and IRDS. New materials, both bulk and nanomaterials, their deposition schemes, and compatibility with existing Cu-low-k BEOL technology should be addressed by industry and academia for low fabrication cost and high reliability. New layout design methods should be invented to achieve low parasitic, high TBD, and low failure in simulation/optimization tools that promise high-performance RF/AMC IC.

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