Ultra-compact 1×4 optical power splitter based on variable-length segment optimized inverse design

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***Abstract*—Fixed-length segment (FLS) optimization method offers a way to realize the high-efficiency analog inverse design of nanophotonic devices. However, due to the limitation of the variable dimensions and restricted search space, this method can hard to simultaneously achieve large bandwidth, compact size, and efficient performance when dealing with high-dimension design. Here, we propose a highly efficient variable-length segment (VLS) based inverse design method, aiming to solve complex analog inverse design and fully demonstrate the targeted performance. It divides the optimized region into several tapered segments of unequal length and inserts a subwavelength transition waveguide between each tapered segment, which can expand the search space of the algorithm, thus making it easier to obtain a better locally optimal solution. As typical complex proof-of-concept examples, a 1×4 power splitter on a silicon-on-insulator (SOI) platform is chosen to demonstrate the validity of our design paradigm. The simulation results show that, compared with the conventional FLS, VLS has about 4-5 times higher efficiency and obtains better optimization performance. In our experiment, the fabricated device has a compact footprint of 9.8μm×4.9μm and is complementary metal oxide semiconductor (CMOS) compatible. The measured insertion loss and the uniformity are less than 0.58dB and 0.8dB, respectively. In addition, the tolerances to fabrication errors are also investigated. Our work may find important applications in the advanced design of future nanoscale high-quality optical devices.**

***Index Terms*—Optical power splitter, inverse design, silicon photonics, integrated optics devices.**

I. Introduction

Due to the explosive increase in the number of mobile terminals and the rapid development of cloud computing services, the use of optics to realize ultra-broadband communication has raised considerable interest [1-3]. As a fundamental and indispensable building element serving the purpose of power distribution, the on-chip optical power splitter is not only the critical link of photonic integrated circuits (PICs) but also a significant part of integrated devices such as Mach Zehnder interferometer (MZI) [4,5], wavelength multiplexing/demultiplexing [6], logic gates [7] and microcavity [8]. In many applications, such as optical phased array (OPA) [9-12], 1×N (N>2) power splitters are strongly required.

In recent years, various types of structures have been reported to realize 1×N (N>2) power splitters. The most common method is to cascade 1×2 power splitters [13-16]. However, this cascading method amplifies the insertion loss and non-uniformity of the individual power splitters, and cascaded devices tend to have larger footprints. The work in [17] proposes 1×4 inverse tapered power splitters based on a 340nm SOI platform, it can provide a low insertion loss (IL) and large bandwidth (BW), nevertheless, the structure is hard to fabricate. Already, 1×4 power splitters based on fan-out bending subwavelength grating (FBSWG) and multimode interferometer (MMI) have been reported in [18,19]. Unfortunately, the experiment results point out that those structures can not ensure good performance in a large BW. On the other hand, numerous inverse design methods are being used to realize nanophotonic devices, driven by the need for high-density PIC. The mainstream inverse design methods can be broadly classified into digital subwavelength structure inverse design represented by direct binary search (DBS) and analog subwavelength structure inverse design represented by topology optimization, shape optimization, and fixed-length segment method combined with particle swarm optimization algorithm (FLS-PSO). The DBS algorithm is a violent search algorithm, which is simple and convenient, and only one-pixel unit can be optimized by one iteration simulation, so the algorithm converges relatively slowly. However, its minimum feature size is rule-uniform, so the process manufacturability is strong [16,20-22]. Shape optimization [23] and topology optimization[24-26] algorithms usually use the adjoint electric field method based on gradient descent, and the algorithms converge quickly. Unfortunately, the shape of the topology optimization and shape optimization designed device is often random and complex, and the process manufacturability of the device is poor. Those defects always lead to a large discrepancy between the experimental and simulation results. Additionally, shape optimization is not suitable for photonic devices with small footprints [27]. It's worth noting that FLS-PSO has played an important role in the design methods of nanophotonic

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devices, including direction coupler [28], Y branch [29], and polarization splitter [30]. Particularly, a 1×4 MMI power splitter optimized by FLS-PSO is proposed and fabricated [31], which has a total length of 36μm and an IL of 0.89dB within a BW ranging from 1520 to 1624nm. Nevertheless, one primary problem with FLS-PSO is that the structure usually has sharp angles, which is hard to fabricate by realistic nanofabrication techniques. Moreover, the foremost problem is the fact that FLS-PSO invariably has poor performance when faced with complicated high-dimension design. So there are still many problems with the method that need to be improved. Therefore, it is necessary to introduce an inverse design methodology that can simultaneously take into account the convergence speed of the algorithm and satisfy the manufacturability of the device, and use it to design a 1×4 optical power splitter with compact size, large bandwidth, and superior performance.

In this article, we have proposed the variable-length segment method combined with particle swarm optimization algorithm (VLS-PSO) for analog inverse design. The method increases the dimensionality of the variables and the search space of the algorithm from the conventional FLS-PSO, which improves the convergence speed of the algorithm, and the method can effectively avoid smaller feature sizes and sharp angles, so the process is highly manufacturable. In addition, we design a 1×4 optical power splitter , and the structure is fully compatible with the standard silicon photonic fabrication process without fine features beyond the lithography resolution limit. Calculation results show that an IL <0.55dB, a uniformity (U) <0.3dB and a BW from 1500nm to 1600nm are obtained for the optical power splitter. In addition, the method tends to have more compact footprints than traditional methods due to a more flexible design paradigm. Meanwhile, our device can maintain high performance with width variations of ±20nm, and such a large fabrication tolerance can be easily guaranteed by modern fabrication technology [32,33]. We also design three different 1×4 optical power splitters under the same conditions using the FLS-PSO algorithm, DBS algorithm and VLS-PSO without subwavelength transition waveguides, respectively. The final results show the advantages of our proposed VLS-PSO in terms of convergence speed and convergence results compared to the remaining several inverse design methods. We are convinced that VLS-PSO will provide a powerful tool for the inverse design of novel analog nanophotonic devices. The proposed 1×4 optical power splitter is experimentally demonstrated on a 220nm SOI platform. The experimental results reveal that the IL and U are lower than 0.58dB and 0.8dB from 1530nm to 1570nm, respectively. The device has an ultra-compact footprint of only 9.8μm×4.9μm, which is expected to be a crucial building block for constructing broadband and compact PICs in the SOI platform in the future. In addition, since this optimization paradigm is also applicable to the design of numerous on-chip devices such as mode multiplexers, crossed waveguides, polarization splitters and filters, etc, consequently, we are fully convinced that VLS-PSO holds significant potential in the inverse design of large-scale subwavelength patterns, such as mode conversion devices and WDM devices. As a result, it enables the exploration of nanophotonic devices with previously unattainable functionality or enhanced performance.

This paper is organized as follows. Section II gives the theory of VLS-PSO and proposes the operation principle. In Section III, simulation results of the proposed optical power splitter are discussed to verify the effectiveness of the device. In Section IV, an experiment is performed, and the performances of the proposed device are analyzed. Finally, conclusions are drawn in Section V.

II. Principle of Operation

FLS-PSO is a common method for analog inverse design [28-31,34], the schematic diagram of FLS is shown in Fig. 1(a). It slices the region to be optimized into several tapered segments of equal length h, afterward, regards the base of each tapered segment w_i as variables, and the PSO algorithm is utilized to optimize those variables.In this context, optimizing the device is akin to performing a finite element analysis, where the width of each segment acts similarly to the differential element ‘dx’ in calculus. Unfortunately, when w_{i-1} and w_{i+1} are both larger than w_i, the structure will have a tapered slot beyond the lithography resolution limit (the position circled in Fig. 1(a)). Although it is possible to avoid sharp angles by adding numerical constraints to the y coordinates of the adjacent points [35], nevertheless, the reduction of the search space is likely to fail to yield the desired optimization results. Additionally, FLS-PSO always fails to achieve the desired results when dealing with complicated inverse designs, which will be demonstrated by our subsequent comparison simulation. VLS, as opposed to FLS, slices the region to be optimized into several tapered segments of unequal length h_i. Moreover, we insert a subwavelength transition rectangular waveguide of unequal length l_i between every two tapered segments, last but not least, w, l, and h will be regarded as variables for subsequent algorithm optimization, which means that the differential element ‘dx’ in the traditional method no longer has a fixed value, but is completely determined by the algorithm, consequently, it is a completely new method of optimizing away from FLS-PSO. It should be added that although the method has a larger number of segments, the final device footprint can be even compact than that of the FLS-PSO due to the controllable length range of each segment. Typically, when dealing with multivariate and multi-objective optimization problems, we subconsciously assume that the more variables there are, the more difficult it tends to be to find the optimal

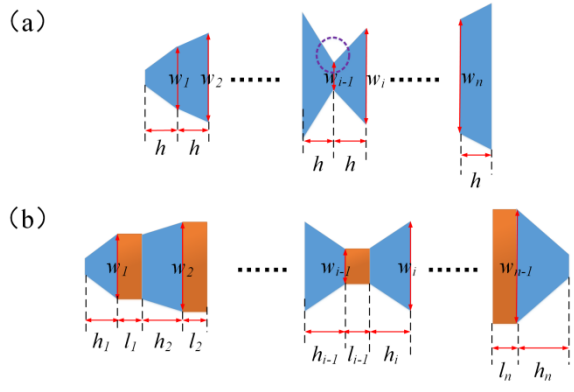

Fig. 1. (a) schematic diagram of the conventional FLS, and (b) schematic diagram of our proposed VLS.

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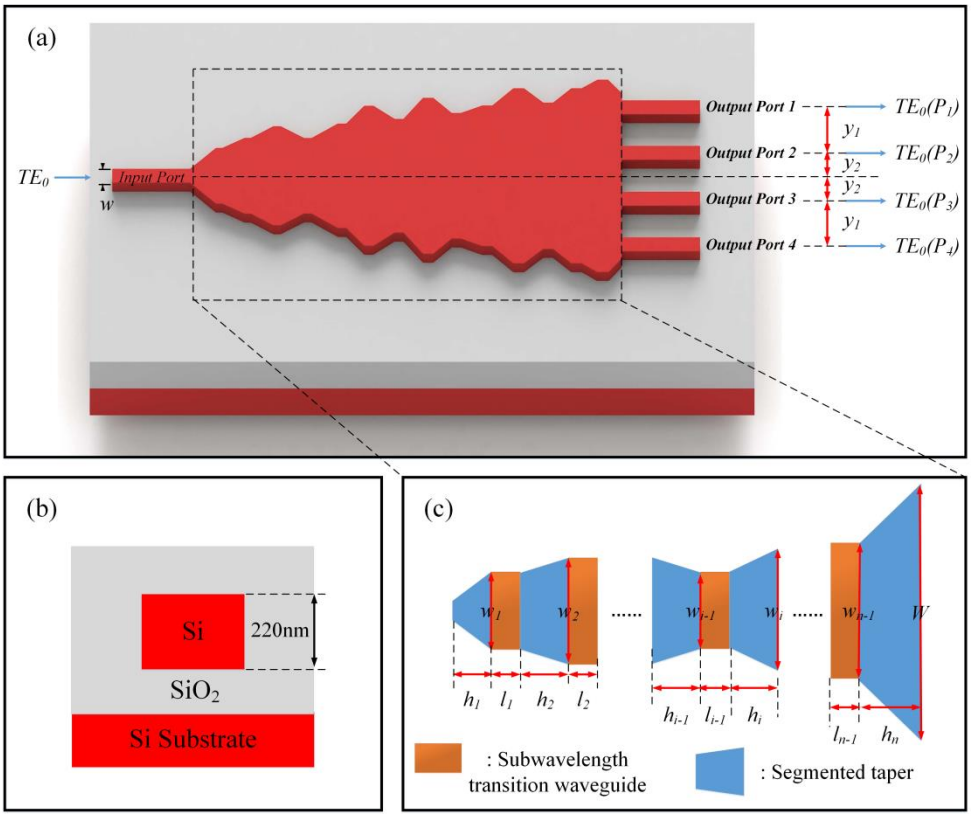

Fig. 2. (a) schematic diagram of the proposed 1×4 power splitter based on VLS. (b) Schematic of the cross-section. (c) Detailed drawing of the optimized region.

solution. Because more variables means a more complex structure, a larger sample space, and more locally optimal solutions. Therefore, rationally reducing the sample space is a common way to improve the efficiency of inverse design [36]. Nevertheless, VLS does the opposite, we try to increase the dimensionality of the variables. There are two apparent advantages of VLS over FLS, firstly, the introduction of the subwavelength transition waveguide avoids sharp angles, and secondly, the increase in the dimension of the variables expands the search space of the algorithm, and surprisingly, it's counter-intuitive to think that this approach can increase the optimization efficiency of the algorithm by a significant amount.

In order to prove the concept of VLS-PSO, we have designed a 1×4 power splitter, and the schematic diagram is shown in Fig. 2. The width of the input port and four output ports w are set as 0.5μm, and the bottom of the tapered segment which is connected to the output waveguides W is set as 4μm. The region to be optimized is divided into 15 tapered segments and 14 subwavelength transition waveguides by VLS, whose shapes are determined by the variables h_1,...,h_{15}, l_1,...,l_{14}, and w_1,...,w_{14}. Since the position of the four output ports also affects the performance of the power splitter, it is necessary to introduce the variables y to control the position of the output ports. The power splitter has symmetry in structure, consequently, the positions of the four output ports can be determined by variables y_1 and y_2. y_1 refers to the distance from port 1 (4) to port 2 (3), and y_2 refers to the distance from port 2 (3) to the symmetry axis of the device. As a result, the structure of the 1×4 power splitter is controlled by these 45 variables. Before optimization, it is necessary to limit the range of each variable. To ensure that our device is compact enough, we limit the size of the region to be optimized to 10μm×5μm, so the upper limit of w_1,...,w_{14} are set to 5μm. Also to ensure that the width of each

TABLE I
STRUCTURE PARAMETERS OPTIMIZED BY VLS-PSO(MICROMETER)

Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
w_1	0.74	w_{10}	4.32	h_5	0.38	h_{14}	0.55	l_8	0.02
w_2	1.02	w_{11}	4.07	h_6	0.43	h_{15}	0.3	l_9	0.02
w_3	1.79	w_{12}	3.98	h_7	0.8	l_1	0.02	l_{10}	0.17
w_4	2.9	w_{13}	3.91	h_8	0.79	l_2	0.2	l_{11}	0.2
w_5	2.83	w_{14}	3.69	h_9	0.32	l_3	0.2	l_{12}	0.2
w_6	3.81	h_1	0.47	h_{10}	0.8	l_4	0.03	l_{13}	0.04
w_7	4.4	h_2	0.75	h_{11}	0.5	l_5	0.03	l_{14}	0.2
w_8	4.84	h_3	0.31	h_{12}	0.34	l_6	0.2	y_1	0.89
w_9	4.59	h_4	0.8	h_{13}	0.41	l_7	0.02	y_2	0.46

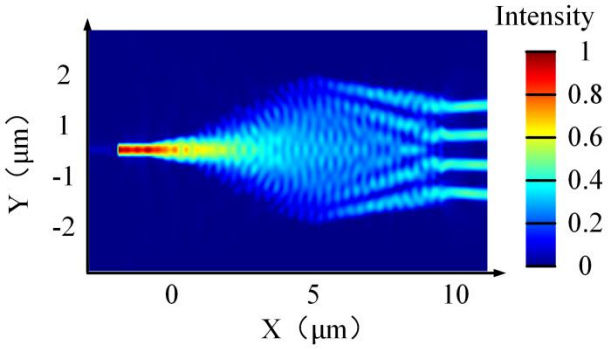

Fig. 3. Simulated light propagation in the VLS-PSO optimized power splitter at 1550nm.

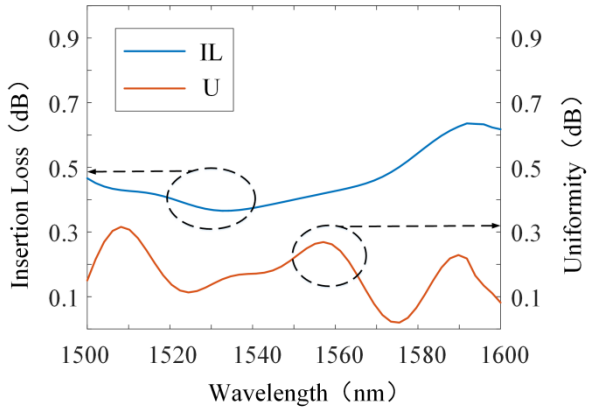

Fig. 4. Simulated insertion loss (IL) and uniformity (U) of the 1×4 power splitter.

segment is larger than the width of the input waveguide w, the lower limit of $w_1,...,w_{14}$ are set to 0.7μm. On this basis, to ensure that the side edges of each segment are not too steep, the ranges of $h_1,...,h_{15}$ and $l_1,...,l_{14}$ are set to [0.3μm,0.8μm] and [0.02μm,0.2μm], respectively. To reduce the IL and U, expand the BW, and obtain the ultra-compact property, the 3D finite-difference time-domain (FDTD) simulations combined with the PSO algorithm are applied to design the structure. We take five wavelengths at equal intervals from 1500nm to 1600nm. Besides, FDTD is used to measure the power of output port 1 and output port 2. To take into account the IL and U of the 1×4 power splitter, the figure of merit (FOM) function is defined as:

$$FOM = \sum_{m=1}^{2}\sum_{t=1}^{5}((P_m(\lambda_t) - 1/4)^2), \quad (1)$$

where $P_m(\lambda_t)$ (t = 1, 2,…,5. m= 1, 2) represents the optical power obtained from the output port m when the fundamental transverse-electric (TE_0) mode is launched into the input port at the wavelength λ_t. The importance of noting is that, in general, an excessively small value of y1 and y2 results in the occurrence of crosstalk between different output waveguides (in this context, crosstalk refers to the transfer of energy from output port 1 to output port 2 through directional coupling, rather than intermodal crosstalk). However, when we use the power of individual output ports at different wavelengths to calculate the FOM for the device's iterative, the crosstalk between different channels has been taken into account. Therefore, there is no need to worry about crosstalk affecting

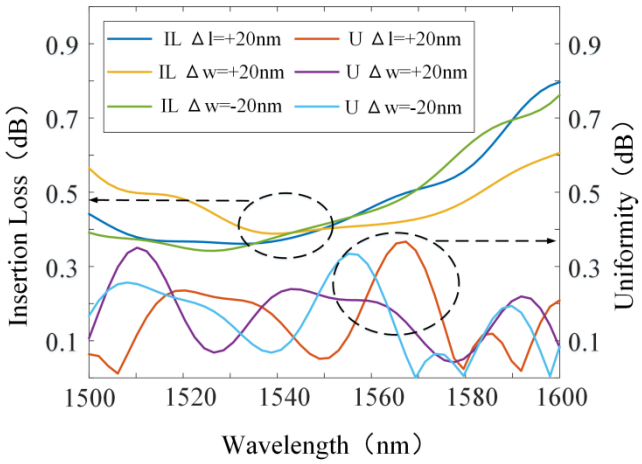

Fig. 5. Simulated insertion loss (IL) and uniformity (U) with dimensional errors of Δw = ± 20nm and Δl = +20nm.

the performance of our device. In this work, it takes approximately 16 hours of computation to obtain the optimized structural parameters on a computer with a 16-core CPU (AMD 3970X). Correspondingly, the optimized parameters are listed in Table 1.

III. Simulation Results for The Proposed Device

Figure 3 shows FDTD simulations of light propagation at the wavelength of 1550 nm. Four images with equal intensities are formed at the output facet of the power splitter, which means our device can perform well at the wavelength of 1550nm. To further demonstrate the performance of our devices over large bandwidths, Fig. 4 depicts the IL and U of our designed 1×4 power splitter as a function of the wavelength. Here, the corresponding definitions are written as:

$$IL = -10\log((P_1 + P_2 + P_3 + P_4)/P_{in}), \quad (2)$$

$$U = -10\log(\min(P_1, P_2, P_3, P_4)/\max(P_1, P_2, P_3, P_4)), \quad (3)$$

where P_{in} stands for the optical input power launched into the input port, similarly, P_n (n=1,2,3,4) stands for the optical power received from the output port n. We monitored the power at the output port of the device at a total of 50 wavelengths and connected them using a smooth curve. As shown in Fig. 4, when the wavelength increases from 1500 to 1600nm, IL and U are lower than 0.63dB and 0.31dB, respectively. The tolerance to fabrication errors is also studied, and dimensional errors of Δw=±20nm ($w_1,...,w_{14}$) are assumed in the width, which is very common in practical fabrication. In addition to this, it can be seen from Table 1 that the minimum feature size of the power splitter is determined by the length of subwavelength transition waveguide $l_1,...,l_{14}$, which is also part of the device that is most prone to fabrication errors in actual techniques. Consequently, it is necessary to further take into account the effect of the error in l on the performance of the device when simulating. To this end, we have calculated the device performance when Δl=+20 nm. All the results are presented in Fig. 5. Note that in Fig. 5, changing Δw from -20nm to +20nm, the IL and U are smaller than 0.74dB and 0.35dB within a BW from 1500nm to 1600nm, respectively. Increasing all l by 20 nm, the IL and U are smaller than 0.79dB and 0.37dB within a BW from 1500nm to 1600nm. It can be observed that only a slight degradation in device

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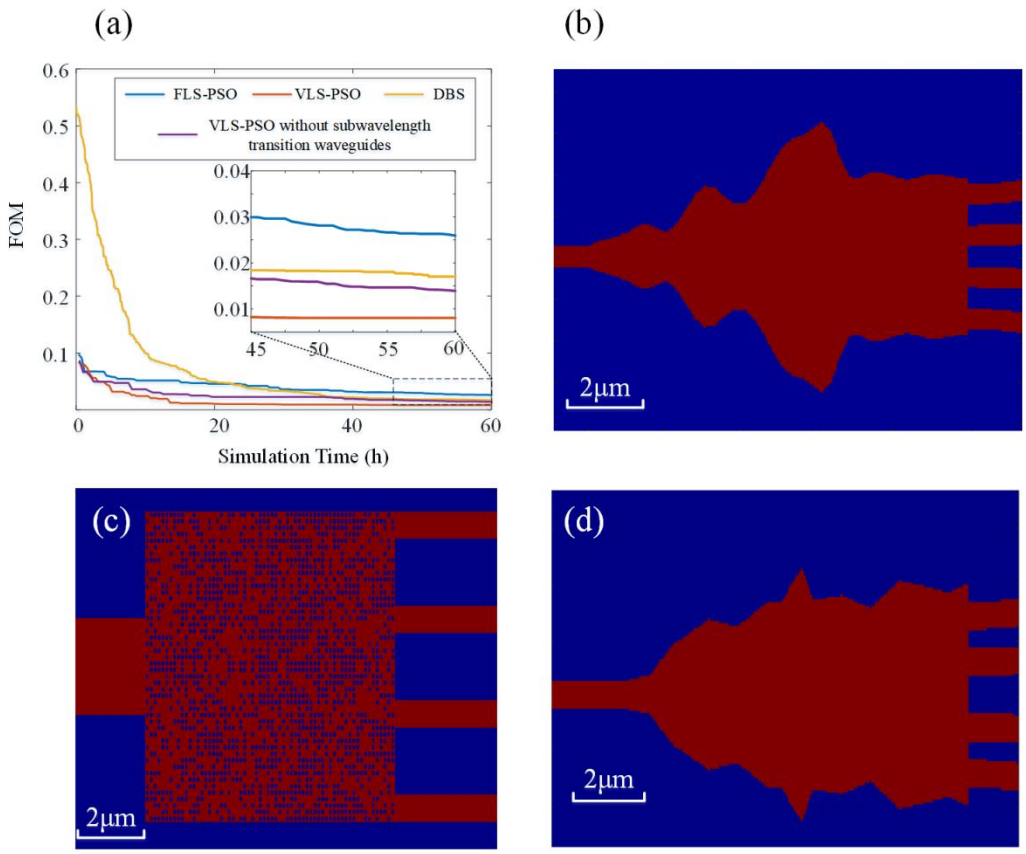

Fig. 6. (a) FOM trend of 1×4 power splitter optimized by VLS-PSO, FLS-PSO, DBS and VLS-PSO without subwavelength transition waveguides, respectively. (b) Optimized geometry of FLS-PSO. (c) Optimized geometry of DBS. (d) Optimized geometry of VLS-PSO without subwavelength transition waveguides.

performance is produced, which illustrates our device has a superior fabrication tolerance.

To further illustrate the advantages of VLS-PSO, we design three completely different 1×4 power splitters using the FLS-PSO, DBS algorithms and VLS-PSO without subwavelength transition waveguides, respectively, as a comparison. All the comparison devices are based on the 220nm SOI platform. It is worth emphasizing that since different optimization methods take different amounts of time for a single iteration, we determine the strengths and weaknesses of the methods by comparing the convergence of different optimization methods after running them for the same time on the same server. The FOM function for each of the four comparison methods is given by Eq. (1).

In FLS-PSO, we divide the optimized region into 20 segments, the length of each segment is 0.5μm, so the total length of the device is 10μm. The specific division is shown in Fig. 1(a), and the variation range for the widths of segments is [0.7μm,5μm]. It is obvious to see that the number of segments of VLS-PSO is more than that of FLS-PSO, which is to verify that VLS-PSO still has faster iteration speed and better optimization effect even when the sample space is significantly larger. Also to compare the stability of the methods, each of the FLS-PSO and VLS-PSO is optimized three times. Due to variations in convergence speeds among different methods, the VLS-PSO only requires 16 hours to approach convergence; however, each method was optimized for a duration of 60 hours to ensure accurate comparison of final convergence values. After 60h of optimization, the final FOM for VLS-PSO are 0.0089, 0.0083, and 0.008, and the final FOM for method FLS-PSO are 0.0286, 0.0335, and 0.0241. The FOM trend of the respective optimal results of the two methods is displayed in Fig. 6(a), and the structure of the optimal result obtained by FLS-PSO is shown in Fig. 6(b). VLS-PSO requires about 16 hours to approach convergence, while FLS-PSO requires more than 60 hours, and the convergence value of VLS-PSO is only 1/3 of that of FLS-PSO. On the other hand, the convergence FOM value obtained by VLS-PSO are more centralized, those results also manifest that VLS-PSO has stability when dealing with complex optimized scenarios. Those advantages can be attributed to the fact that the VLS-PSO method expands the search dimension of the algorithm. More specifically, FLS-PSO limits the length of the device, and at the specific length, there may not have an outstanding result that satisfies our optimization needs. On the contrary, VLS-PSO innovatively introduces *h* and *l* as variables in Fig. 1(b), which can better utilize the search capability of the algorithm and is more likely to achieve better convergence results despite the increased number of variables. The area of the different algorithms should be of comparable size in order to adhere to the principle of controlling variables during comparison. In the DBS algorithm, the optimized region measuring 7.68μm × 5.76μm is divided into 64×48 pixels. The shape of each pixel is a square of 120nm×120nm, with a central circular hole. The diameter of the circular holes is set to be 90nm. The logical state for the central circular hole can be “1” or “0”, standing for

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TABLE II
COMPARISON SIMULATION PERFORMANCE OF 1×4 POWER SPLITTERS DESIGNED BY DIFFERENT METHOD

Method	Final FOM value	IL(dB)	U(dB)
VLS-PSO	0.008	0.63	0.31
FLS-PSO	0.0241	1.83	1.15
DBS	0.018	1.19	1.26
VLS-PSO without subwavelength transition waveguides	0.0139	0.87	0.27

a hole filled with SiO_2 or Si. By employing the DBS algorithm and FDTD method, the logical state would be clearly defined. Similarly, after 60 hours of optimization, the final result obtained by the DBS algorithm is shown in Fig. 6(c), and the convergence curve of the DBS algorithm is likewise shown in Fig. 6(a). In order to verify the necessity of the subwavelength transition waveguide for the convergence effect of the algorithm, we do a set of comparative simulations by removing the subwavelength transition waveguide from the VLS-PSO and leaving the rest unchanged. The results obtained by this method are shown in Fig. 6(d) and Fig. 6(a). By comparison, it is obvious to see that the subwavelength transition waveguide not only reduces the difficulty of process manufacturing, but also improves the optimization efficiency of the algorithm. After a comprehensive comparison of the results of the four methods, we can conclude that VLS-PSO guarantees a large process tolerance while also ensuring good convergence speed and results. In order to visualize the difference in the performance of the devices designed by the different methods, we have added the Table 2, which shows the IL, U and the final FOM value of the devices designed by VLS-PSO, FLS-PSO, DBS and VLS-PSO without subwavelength transition waveguides for comparison, respectively.

IV. FABRICATION AND MEASUREMENT FOR THE PROPOSED DEVICE

The designed 1×4 power splitter has been fabricated on a standard SOI wafer with 220-nm-thick top silicon. 100 keV electron beam lithography (EBL, Vistec EBPG5000+ES) with AR-P 6200 photoresist is carried out to define the patterns, and an inductively coupled plasma (ICP, Oxford Plasmalab System 100) dry-etching process is employed to transfer the pattern to the silicon layer. Finally, a 1-μm-thick silica layer has been deposited as the upper cladding using a plasma-enhanced chemical vapor deposition (PECVD, Oxford Plasmalab System 100) process at 300°C.

The scanning electron microscope (SEM, GeminiSEM 300) image of the fabricated 1×4 power splitter is illustrated in Fig. 7(a). TE-type grating couplers (GC) are used to couple the optical signals in and out of the fabricated devices, and the zoom-up image of TE GC is shown in Fig. 7(c). An amplified spontaneous emission (ASE) with a 1530~1570nm wavelength range light source, a polarization controller (PC), and an optical spectrum analyzer (OSA, EXFO OSA20) are employed to

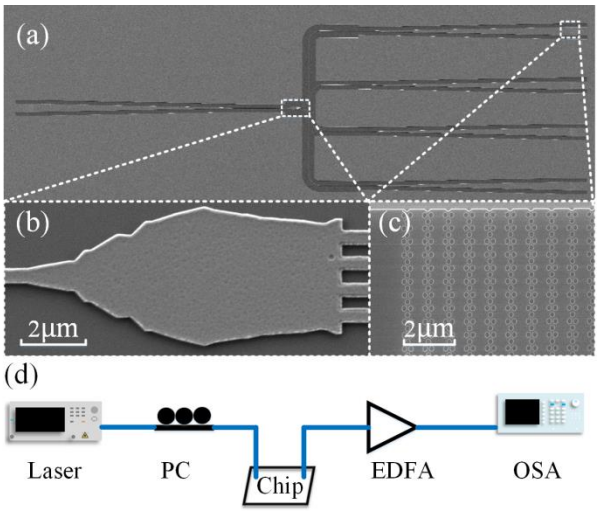

Fig. 7. (a) Microscope image of the fabricated devices. (b) SEM image of the power splitter. (c) SEM image of the grating coupler. (d) Experimental setup. PC, polarization controller; EDFA, erbium-doped fiber amplifier; OSA, optical spectrum analyzer.

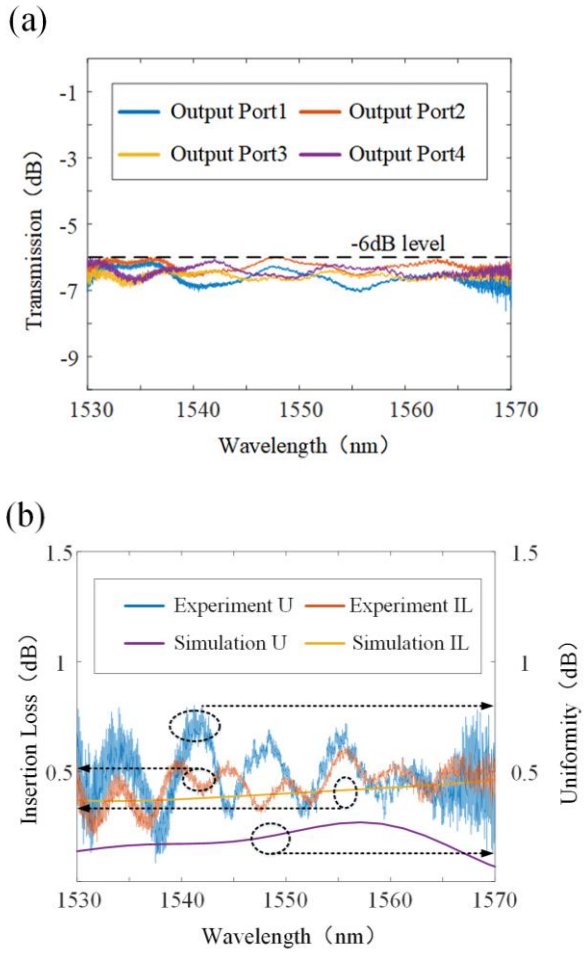

Fig. 8. (a) Measured transmission spectra of the fabricated power splitter. (b) Comparison of experimental data with simulation data.

TABLE III
COMPARISON PERFORMANCE OF 1×4 POWER SPLITTERS

Ref.	Structure	IL(dB)		U(dB)		Bandwidth(nm)		Length(μm)
		Simul.	Exper.	Simul.	Exper.	Simul.	Exper.	
[13]	Cascade Y-junction	0.26	1.2	-	2.2	100	100	4000
[17]	Inverse tapers	0.2	0.4	0.29	0.68	100	100	75
[18]	FBSWG	0.6	1.35	1	1	190	49	4.02
[31]	FLS-PSO optimized MMI	0.59	0.62	0.34	0.89	150	104	36
This work	VLS-PSO inverse design	0.63	0.58	0.31	0.8	100	40	9.8

[a]Ch: channel Simul.- the simulation results Exper.- the experiment results.

characterize the performance of the fabricated device, which is shown in Fig. 7(d). The results have been normalized according to the reference GCs fabricated on the same wafer. Thus, the measured and normalized transmission spectra wave bands are plotted in Fig. 8(a). Regarding the experimental and simulation results, the disparity in device bandwidth can be elucidated through multiple factors: (1) The light emitted from our employed amplified spontaneous emission (ASE) falls within the C+L band. (2) The erbium-doped fiber amplifier (EDFA) we utilized operates at a wavelength of 1550 nm with a bandwidth of approximately 50 nm. (3) The utilized GC has a restricted operational bandwidth. These combined factors result in power outside the 1530 to 1570 nm range being close to the lower noise level of the OSA. Therefore, the limitation of the equipment is believed to have an impact on the experimental results, and it is expected that the actual bandwidth of our chip exceeds 40nm. The transmission spectra of our 1×4 power splitters at different output ports indicate that this device can split the input optical power equally with low loss. Besides, the device's IL and U are calculated to be below 0.58dB and 0.8dB within the available wavelength range, respectively. In order to compare the difference between simulation and experiment results more intuitively, we put the IL and U data of experiment and simulation into Fig. 8(b), where the experimental IL of the 1×4 power splitter is obtained by normalizing the output power of the four ports in Fig. 8(a) and summing them up. From Fig. 8 (b), it is obvious to see that there is a large jitter in the experimental IL of the device in the measured waveband, which can be explained in two ways. Due to the limitations of our experimental equipment, the OSA exhibits significant power jitter when measuring the reflected light from the GC. Additionally, variations in performance among different GCs on the same chip arise due to process errors. Since our device's total IL is a simple superposition of optical power from four output ports, this superposition amplifies the optical power jitter by a factor of four. This could similarly explain the poorer U of the experiment than the simulation. Apart from this, the experimental data accord well with the simulation data. Our proposed device's performance is compared with other reported 1×4 power splitters with different structures, results are shown in Table 3. It can be noted that our device shows low IL, and outstanding U in an ultra-compact footprint.

V. CONCLUSION

In summary, we innovatively propose a highly efficient VLS-PSO algorithm for analog inverse design. Compared to the traditional FLS-PSO, the improved VLS-PSO avoids potential fabrication problems and provides better optimization results. Based on these, we have designed and fabricated a 1×4 power splitter on the 220-nm SOI platform as typical proof-of-concept examples, which has a total length of 9.8μm. Simulation results show that the efficiency of VLS-PSO is approximately 4 times faster than that of FLS-PSO. Moreover, the convergence FOM value of VLS-PSO is only 1/3 of that of FLS-PSO. Experimental results show that our device's IL and U are lower than 0.58dB and 0.8dB within a bandwidth from 1530 to 1570nm. Fabrication tolerance analysis further shows that VLS-PSO has better process tolerance and process manufacturability compared to the traditional analog inverse design methods. With the above characteristics, we believe our proposed 1×4 power splitter can pave the way to develop highly integrated PICs in the future. Furthermore, the proposed VLS-PSO method may provide a new perspective for designers, and it could be applied to the analog inverse design of higher-dimension and multi-objective nanophotonic devices with novel integrated functions.

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