Transmitter for Visible Light Communications Based on FPGA's Output Buffers

Stefano Ricci, *Senior Member, IEEE*, and Stefano Caputo

***Abstract*— Among the several new applications that Visible Light Communication (VLC) have made possible in recent years, board-to-board (B2B) communication represents an important field of employment for this technology. Most of the systems that would benefit from VLC-based B2B communication are digital boards that include Field Programmable Gate Arrays (FPGAs) or advanced processors. Modern FPGA output buffers have limited power, but switch at hundreds of MHz: a much higher rate compared to that of the typical single MOSFET employed in a ON-Off Key (OOK) transmitter. This letter explores the possibility of exploiting the FGPA buffers for realizing a OOK transmitter suitable for B2B communication. A transmitter circuit, driving a 70 mA LED, is proposed and characterized for 26 different electrical standards and configurations of the FPGA buffer. A 210 Mb/s link was demonstrated at a distance of 6 cm (120 Mb/s at 24 cm) with a Bit Error Rate (BER) $< 1.5 \cdot 10^{-6}$ (95% confidence).**

***Index Terms*— Visible light communication (VLC), IEEE 802.15.7, board-to-board (B2B) communication, field programmable gate array (FPGA), VLC transmitter, intra-box communication.**

I. Introduction

VISIBLE light communication (VLC) represents a new paradigm for short-range communication where the information is coded in the instantaneous luminosity of a Light Emitting Device (LED) [1].

VLC is fostering a wide range of new applications and has proven its ability to provide novel solutions to longstanding problems. For instance, in aerospace applications, cables and connectors can account for up to 8% of a satellite's mass and also present significant reliability issues [2]. VLC's technology is suitable for establish contactless Board-to-Board (B2B) communication meeting the typical requirements (distance < 20 cm, bit rate 10 Mb/s < 1 Gb/s) of the field [3]. Given the significant advantages VLC offers in addressing these issues, its use in aerospace applications is becoming strategic [4].

Most of the studies present in the literature about VLC B2B communication are finalized to meet the high requirements of data centers: in the related works, channels capable of sustaining tens of Gb/s are demonstrated [5]. These high rates are typically achieved by exploiting both linear laser transmitters (TXs) and advanced modulation methods, like Multitone Frequency Quadrature Amplitude Modulation (MFQAM).

On the other hand, the ON–OFF keying (OOK) modulation, adopted even in important standard like the IEEE 802.15.7 [6], is very simple (the '0' and '1' values of the bit are represented by 2 intensity levels of light), and it was demonstrated suitable to achieve data rates compatible with B2B applications. For example, in [7] a 262 Mb/s link is demonstrated by the use of a linear TX.

As an alternative to the linear TX [8], the OOK modulation can be implemented by a single Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) employed as a switch [9]. Although the MOSFET is able to drive large LED arrays, its switching velocity is limited. Links at relatively high distance and low rate are the main use case of this TX, like shown, for example, in [10] where a 50 m, 100 kb/s link is reported.

Going back to the B2B link in the aerospace field, it should be noted that most of the boards that would benefit from the VLC integrate Field Programmable Gate Arrays (FPGAs) or advanced processors. They are necessary, for example, to handle the communication buses employed in the field like the MIL-STD-1553 [11] or the ARINC 659 [12]. The FPGA integrates output buffers that work at hundreds of MHz. Putting everything together, a possible solution to achieve a B2B VLC that overcomes the limitation suffered by the aforementioned MOSFET TX, would be to exploit the digital output buffers of the FPGAs to drive directly a LED, modulated in OOK.

Although these apparent advantages, no study is present in the current literature that investigates such a possibility. This letter overcomes this lack by studying the performance of a VLC TX based on the FPGA output buffers. Following the flexibility of such buffers, the performances of 26 different configurations are tested with the TX circuit proposed in section II-B. The full-power bandwidth and the signal amplitude are experimentally evaluated and reported in section III. In the successive section a link is realized for measuring the Bit Error Rates (BERs) and the eye-diagrams for distances between 6-24 cm and rates between 100-320 Mb/s.

II. The Transmitter

A. The Circuit

The FPGA output level of a modern high-velocity buffer is in the range of 1.5-3.3 V, which is not enough to drive directly a LED whose junction drop is over 2V. In this letter the two different circuits reported in Fig. 1 are proposed. They address the aforementioned issue by exploiting the 'bias-tee' configuration, often employed in linear TXs [13], [14], but original for digital drivers. In bias-tee, the LED current Id is

Manuscript received 10 June 2024; revised 12 July 2024; accepted 12 July 2024. Date of publication 18 July 2024; date of current version 12 September 2024. This work was supported in part by the CAMP Project Ricerca Salute 2018 (DD n. 975, 16 January 2020), Tuscany region, Italy, under Grant CUP I58D200005200. The associate editor coordinating the review of this letter and approving it for publication was B. Shihada. *(Corresponding author: Stefano Ricci.)*

The authors are with the Department of Engineering Information (DINFO), University of Florence, 50139 Florence, Italy (e-mail: stefano.ricci@unifi.it; stefano.caputo@unifi.it).

Digital Object Identifier 10.1109/LCOMM.2024.3430393

© 2024 The Authors. This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 License.
For more information, see https://creativecommons.org/licenses/by-nc-nd/4.0/

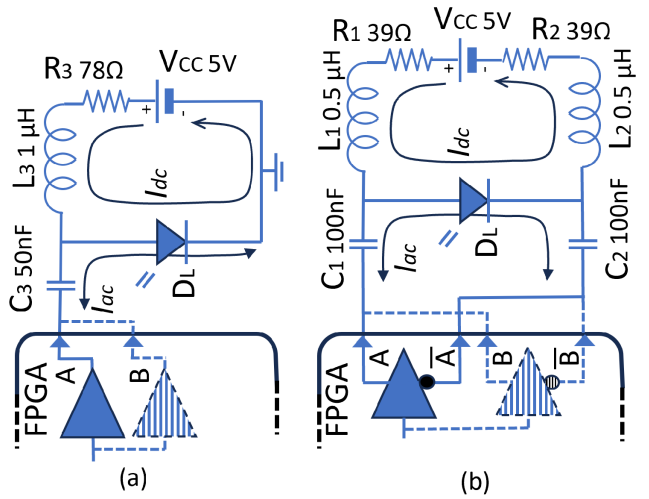

Fig. 1. FPGA transmitter. (a) Single ended transmitter; (b) Differential transmitter. The shadowed buffers are added in parallel to the main buffers to produce a higher current.

composed by the summation of the constant current Idc and the variable component Iac ($Id = Idc + Iac$). The current Idc, responsible for the mean LED luminosity, is sourced by the external supply Vcc. For the 2 circuits hold, respectively:

$$Idc = \frac{Vcc - Vd}{R_3}; Idc = \frac{Vcc - Vd}{R_1 + R_2} \quad (1)$$

where Vd is the voltage drop across the LED. The variable component Iac is produced by the FPGA drivers and coupled through the capacitors C_3 and C_1, C_2. The coils $L3$ and $L1, L2$ avoid Iac flowing through the power source. The current Iac has a zero-mean value. If Iac_m is its peak value, i.e. $-Iac_m < Iac < +Iac_m$, the current in the LED is in the range: $Idc - Iac_m < Id < Idc + Iac_m$.

Considering Ibu_m as the peak current produced by a single FPGA buffer, the following 4 configurations are investigated:

1) SEN-SOut: the single-ended (SEN) single-output (SOut) configuration is reported in the circuit shown in Fig. 1(a). The LED cathode is connected to ground, while the anode is driven by the output 'A' of a single FPGA buffer (solid blue triangle). Here we have: $Iac_m = Ibu_m/2$.

2) SEN-DOut: in the SEN double-output (DOut) configuration a second buffer (shaded triangle and connection in Fig. 1(a)) is added in parallel to the first. The buffers are driven by the same input. The resulting current is theoretically doubled with respect to SEN-SOut: $Iac_m = Ibu_m$.

3) DIF-SOut: the differential (DIF) SOut configuration is shown in Fig. 1(b). The LED cathode and anode are connected to the complementary FPGA outputs 'A' and '$\bar{A}$', driven in differential mode. Similarly to the previous case, the current in the LED is doubled: $Iac_m = Ibu_m$.

4) DIF-DOut: in the DIF-DOut configuration, a second differential buffer 'B','$\bar{B}$' (shadowed triangle and connection in the picture) is added to achieve a theoretical current of: $Iac_m = 2 \cdot Ibu_m$.

The TX was coupled to the LED 150141RS631 produced by Wurth Elektronik (Waldenburg, DE), which features a maximum current of 70 mA and an emission wavelength of 630 nm (red light). The 5V power sourced a constant current $Idc = 36$ mA, corresponding to $Vd = 2.2$ V.

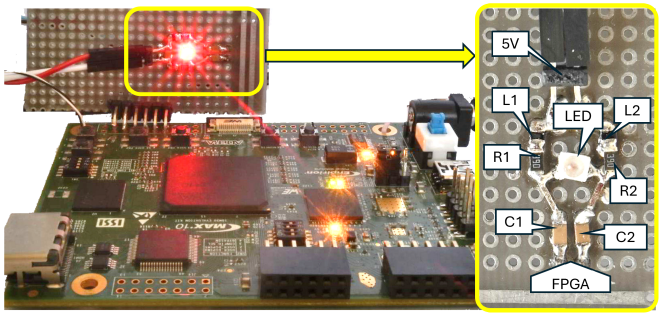

Fig. 2. The transmitter is composed by the FPGA board and the prototype breadboard, detailed on the right in the configuration of Fig 1(b).

B. FPGA Electrical Standards, Currents and Configurations

The circuit described in the previous section was connected to the output buffers of the FPGA powered at 2.5 V. Different experiments were carried out by configuring the FPGA outputs according to the following electrical standards: Low Voltage CMOS (LVC), Sub Series Terminal Logic (SSTL) class I (unterminated) and II (series terminated), and Low Voltage Digital Signaling (LVDS). In SSTL I,II and LVDS the driver current is fixed at $8, 16, 3.5$ mA, respectively. Conversely, in LVC mode, the FPGA allows to set the buffer current at $4, 8, 12, 16$ mA. Experiments were repeated for each of these current values, leading to the testing of 7 different electrical standards and current variations.

The LVC, SSTL I and II standards were applied in all of the 4 configurations reported in section II-A, resulting in a total of $6 \cdot 4 = 24$ combinations. The inherently differential LVDS, was tested in the DIF-SOut and DIF-DOut configurations, bringing the total to 26 output driver combinations.

The power consumed by the buffer is $Pb = 2.5 \cdot Iac_m$, where 2.5 V is the power voltage. It ranges from the minimum of 5 mW for LVC 4 mA SEN-SOut, to 80 mW for LVC 16 mA DIF-DOut. In addition to Pb, the total power needed by the TX includes the polarization of the LED: $Pp = 5V \cdot Idc = 180$ mW.

III. Characterization of the Transmitter

A. Experimental Set-up

A MAX10 Evaluation Kit featuring an FPGA of the 10M50XX family (Intel Corp. Santa Clara, CA) was employed for the experiments. The circuits of Fig. 1 were assembled in a prototype board, and connected to the expansion connector of the FPGA board (Fig. 2). The connections and the circuit dimensions were maintained small to limit the parasitics. The 26 buffer configurations referenced in section II-B were obtained by setting in the FPGA firmware the corresponding electrical standards and current values.

The circuit holding the LED was placed in front of the photodetector PDA10A2 manufactured by Thorlabs Inc. (Newton, NJ) at distances of 6,12,18,24 cm. This device includes a sensor with a 0.8 mm^2 area operating within the range

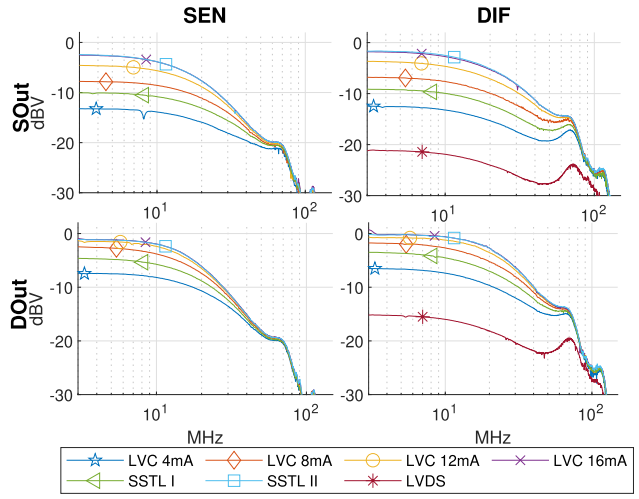

Fig. 3. Signal amplitude over frequency achieved by the 7 different electrical standards in the configurations: SIN-SOut (top-left); DIF-SOut (top-right); SEN-DOut (bottom-left); DIF-DOut (bottom-right).

200 - 1100 nm; followed by a Trans-Impedance Amplifier (TIA) with a 150 MHz bandwidth and a gain of 10k V/A. A 12 mm diameter lens was inserted before the receiver. Signal acquisition from the TIA was conducted using a RTM3004 scope (Rohde & Schwarz, Muenchen, DE).

B. Full Power Amplitude and Bandwidth

In the initial experiment we measured the signal amplitude available at the receiver and the full-power bandwidth for each of the 26 output configurations outlined in sec II-B. The LED-photodetector distance of 18 cm was used. The results are reported in Fig. 3. The figure comprises four panels arranged such that tests conducted in the SEN and DIF configurations are displayed on the left and right columns; while the top and bottom rows present results obtained in SOut and DOut configurations, respectively. Signal amplitude is expressed in dBV, with the LVDS standard contributing to the two DIF panels exclusively. It was noted that the LVC 16 mA and SSTL II electrical standards yielded identical results across all experiments, suggesting that these standards may be implemented in the FPGA using the same internal hardware.

We note that the decreasing trend of the amplitude with frequency experiences a deviation near 70 MHz. In the SEN configurations, a slight plateau is noticeable, whereas in the DIF configurations, the plateau is replaced by a peak, which becomes more pronounced with lower output current. This phenomenon can be attributed to the presence of resonance induced by parasitic elements.

The maximum amplitude of 0 dBV was recorded for the LVC 16 mA (and SSTL II) configuration set in the DIF-DOut mode (refer to Fig. 3, bottom-right panel) This outcome is expected, since $Ibu_m = 16$ mA represents the maximum output current tested among the standards, and the DIF-DOut configuration grants the maximum current gain, i.e. $Iac_m = 2 \cdot Ibu_m$ (see the analysis in sec. II-B). The amplitudes scale with the output currents in all of the configurations; however, the influence of the output current is more pronounced at lower frequencies, gradually diminishing as frequencies increase.

TABLE I
BANDWIDTH MEASURED IN DIFFERENT OUTPUT CONFIGURATIONS (−3/−6 DB IN MHZ)

Electrical Standard	SEN/SOut	SEN/DOut	DIF/SOut	DIF/DOut
LVCMOS 4 mA	21.8 / 37.9	20.0 / 33.3	21.2 / 37.2	20.0 / 33.3
LVCMOS 8 mA	19.1 / 29.6	19.1 / 29.4	20.0 / 33.5	19.1 / 29.4
LVCMOS 12 mA	17.0 / 25.0	21.1 / 30.0	19.1 / 31.0	21.1 / 30.0
LVCMOS 16 mA	15.3 / 22.4	21.1 / 30.2	18.9 / 29.3	21.1 / 30.2
SSTL I	20.1 / 32.4	18.7 / 30.3	20.3 / 33.7	18.7 / 30.3
SSTL II	15.3 / 22.4	21.1 / 29.5	18.8 / 29.1	21.1 / 29.6
LVDS			21.2 / 37.5	20.6 / 35.8

The −3 and −6 dB bandwidths are presented in Table I. The values range between 15.3 and 18.8 MHz for the −3 dB bandwidth and between 22.1 and 38.0 MHz for the −6 dB bandwidth. Notably, wider bandwidths are achieved by the electrical standards associated with lower currents, namely LVDS and LVC 4 mA (listed in the top and bottom rows of Table I). Significant decrease in bandwidth was observed with increasing currents in the SEN-SOut configuration. A similar decrease, albeit less pronounced, was also noted in the SEN-DOut configuration. Unlike the SEN configuration, the DIF configuration does not exhibit a clear relationship between bandwidth and current.

C. Performances of DIF and DOut Configurations

In section II-A it was determined that the DIF and DOut configurations would theoretically result in a 2-fold increase in the LED current compared to the SEN and SOut modes. Here, we verify this theoretical prediction by examining the expected 6 dB gain. The gain was assessed at two frequencies: 5 MHz, in the middle of the in-band region; and 30 MHz, representing the transition region. The results are reported in the panels of Fig. 4. The top-left panel illustrates that transitioning from SEN to DIF yields a modest amplitude gain (approximately 1 dB) at 5 MHz across all analyzed electrical standards. When assessed at 30 MHz (refer to the top-right panel), the gain remains consistent at about 1 dB for LVC 4 mA, but increases up to 4.3 dB for standards with higher current. Implementing parallel outputs (DOut), as depicted in the bottom panels of Fig. 4, produces the expected 6 dB amplitude increase for LVC 4 mA and LVDS. However, the gain diminishes to less than 2 dB as the current increases to 16 mA. The DIF configuration yields a noticeable gain (albeit slightly less than the theoretical prediction) at higher frequencies, but has minimal impact in the lower frequency range. Conversely, the DOut configuration produces a similar gain across both low and high frequency ranges.

Using a similar methodology, we assessed the effects of DIF and DOut configurations on the −6 dB bandwidth. The findings are presented in Fig. 5. The DIF configuration demonstrates a significant increase in bandwidth, which varies with current from 5% to 33% (as shown in the left panel). Employing parallel outputs yields a 33% bandwidth enhancement for LVDS, no discernible effect for LVC 16 mA (and SSTL II), and even a reduction ranging between the −5 and −15% for the remaining standards.

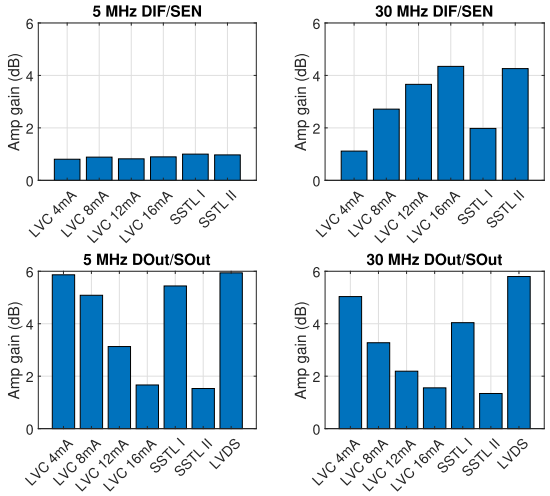

Fig. 4. Amplitude increments for the different electrical standards. Top: amplitude gain of DIF with respect to SEN at 5 MHz (left) and 30 MHz (right); Bottom: amplitude gain of DOut with respect to SOut at 5 MHz (left) and 30 MHz (right).

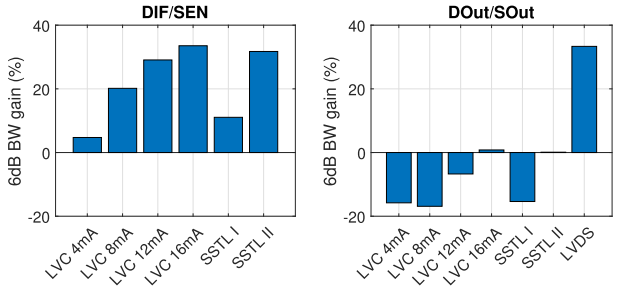

Fig. 5. Bandwidth increase for DIF with respect to SEN (left) and DOut with respect to SOut (right).

IV. Communication Tests

The next two experiments aim to evaluate the performance of the proposed TX in a VLC OOK link. A data generator, producing 8-bit packets of random bits, was integrated into the FPGA. Its output was processed through a 8/10 bit encoder, serialized and sent to the TX.

The received signal was acquired, transferred to PC and demodulated after a basic post-equalization based on the frequency responses measured in the first experiment (see section III-B). The quality of the link was assessed by estimating the open area of the eye-diagram and the BER.

A. Comparison of Transmitter Configurations

Packets of 4 Mbit of raw data were transmitted and received at a distance of 18 cm and a fixed rate of 125 Mb/s for each of the 26 combinations of electrical standards and configurations reported in section II-B. The eye diagrams were generated by overlaying 10k symbols. The area of the eye, denoted A, was normalized relative to the ideal aperture, which is calculated as the product of the symbol amplitude, denoted Amp, and the symbol time $T_b = 1/125\,Mb/s = 8\,ns$:

$$A_n = \frac{A}{Amp \cdot T_b} \tag{2}$$

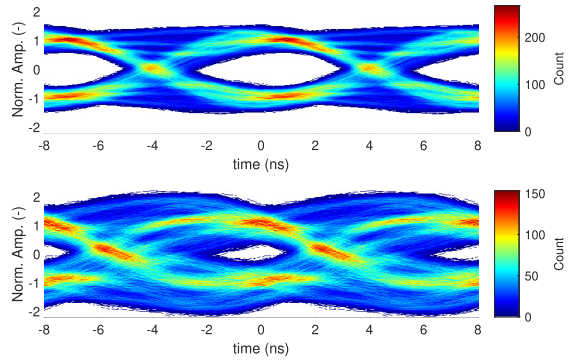

Fig. 6. Eye diagrams for LVC 4mA DIF-SOut (top) and SSTL1 SEN-SOut (bottom) obtained by superimposing 10k symbols. The symbol amplitude is normalized to $Amp = \pm 1$.

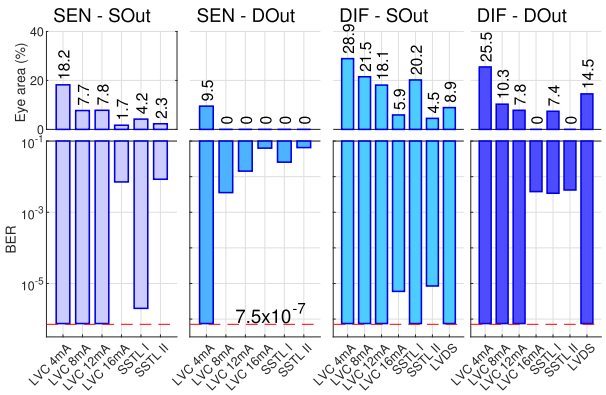

Fig. 7. Eye-areas (top) and BERs (bottom) measured at 125 Mb/s with different electrical standards and configurations. Red dashed line indicates the no-error threshold.

Fig. 6 illustrates two eye diagrams: one measured for the LVC 4 mA DIF-SOut configuration, depicted at the top, and the other representing the SSTL1 SEN-SOut configuration, shown at the bottom. The largest area was recorded in the former case with $A_n = 28.9\%$, while the latter yielded a lower value, representative of the lower range of results with $A_n = 4.2\%$.

Communication errors were assessed by comparing the received data with the ground truth. In the absence of errors a BER of $= 1/4\,M \cdot 3 = 7.5 \cdot 10^{-7}$ was estimated for the channel with a confidence of 95% [15]. The BERs and eye areas (A_n) are graphically summarized in Fig. 7 for all configurations, categorized into four groups (from right to left): SEN-SOut, SEN-DOut, DIF-SOut, and DIF-DOut.

In general, the configuration that yielded the most favorable outcomes was DIF-SOut. This was followed by SEN-SOut and DIF-DOut, while the least satisfactory results were observed with SEN-DOut where, excluding the case of LVC 4 mA, null eye-areas and quite high BERs were found. The highest BER was recorded with LVC 16 mA (and SSTL II), whereas LVC 4 mA and LVDS demonstrated error-free communication across all configurations, albeit with differing eye areas.

B. BER Versus Data Rate and Distance

For the subsequent experiment, the LVC 8 mA electrical standard in the DIF-SOut configuration was chosen. The power consumption in this case is $Pb + Pp = 10 + 180 = 190$ mW.

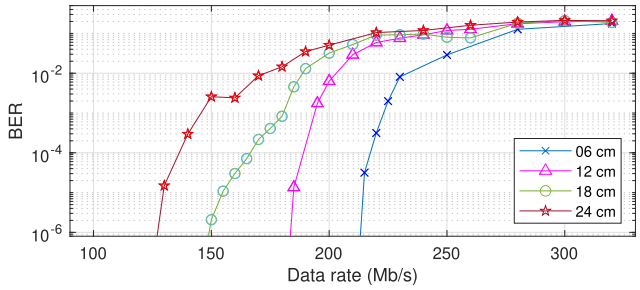

Fig. 8. BER measured by transmitting 2 Mbit of data through the LVC 8 mA standard in DIF-SOut configuration at distances 6, 12, 18, 24 cm. Marks report the measurements.

Packets containing 2 Mbit were transmitted at TX-RX distances of 6, 12, 18, 24 cm and rates from 100 to 320 Mb/s, obtained by adjusting the clock frequency of the TX logic integrated in the FPGA. The results are summarized in Fig. 8. We observed a non-smooth outline of the BER trend in some curves probably due to the resonances in the bandwidth (see Fig. 3). No error was measured for distances of 24, 18, 12, 6 cm for rates of 120, 140, 180, 210 Mb/s, respectively, corresponding to a BER $= 1.5 \cdot 10^{-6}$ (confidence of 95% [15]).

V. Discussion and Conclusion

This letter demonstrates how a simple circuit, driven by the FPGA output buffers, can serve as an effective OOK VLC TX, achieving data rates of 120 Mb/s at 24 cm or 210 Mb/s at 6 cm, with BER$< 1.5 \cdot 10^{-6}$.

The power consumption of the proposed TX is remarkably low ($<$ 200 mW). In comparison, like highlighted in review [9], only [7] and [16] support similar high rates at comparable power. However their circuit complexity is considerably higher: [7] employs a linear TX with digital pre-emphasis, while [16] employes additional circuits for carrier removal.

A mathematical model of the TX capable of analytically replicating the observed results would have been highly beneficial. Unfortunately, the lack of details about the hardware implementation of the FPGA buffers, which are proprietary industrial knowledge, presents a barrier to developing such a model. However, the result reproducibility is granted by the use of standard configurations of the FPGA buffers.

This letter provides valuable insights into selecting the optimal electrical standard and configuration of the FPGA buffer for a specific VLC application. For instance, it reveals that low-current standards, such as LVDS and LVC 4 mA, offer maximum bandwidth (and consequently higher data rates), as illustrated in Table I. Additionally, it demonstrates that utilizing the DIF-SOut configuration increases power efficiency without significantly impacting the BER, as shown in Fig. 7.

The proposed TX represents a compact and cost-effective solution for integrating B2B-VLC into applications and systems where FPGAs are already utilized, such as in many complex aerospace electronics systems.

References

[1] S. Rehman, S. Ullah, P. Chong, S. Yongchareon, and D. Komosny, "Visible light communication: A system perspective—Overview and challenges," *Sensors*, vol. 19, no. 5, p. 1153, Mar. 2019, doi: 10.3390/s19051153.

[2] R. Amini, G. Aalbers, R. Hamann, W. Jongkind, and P. G. Beethuizen, "New generations of spacecraft data handling systems: Less harness, more reliability," in *Proc. 57th Int. Astron. Congr.*, Valencia, Spain, Oct. 2006, doi: 10.2514/6.iac-06-d1.4.09.

[3] E. Ciaramella et al., "Prospects of visible light communications in satellites," in *Proc. 22nd Int. Conf. Transparent Opt. Netw. (ICTON)*, Bari, Italy, Jul. 2020, pp. 1–4.

[4] N. Karafolas, J. M. P. Armengol, and I. Mckenzie, "Introducing photonics in spacecraft engineering: ESA's strategic approach," in *Proc. IEEE Aerosp. Conf.*, Mar. 2009, pp. 1–15, doi: 10.1109/AERO.2009.4839438.

[5] C. A. Thraskias et al., "Survey of photonic and plasmonic interconnect technologies for intra-datacenter and high-performance computing communications," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 4, pp. 2758–2783, 4th Quart., 2018, doi: 10.1109/COMST.2018.2839672.

[6] *IEEE Standard for Local and Metropolitan Area Networks—Part 15.7: Short-Range Optical Wireless Communications*, IEEE Standard 802.15.7-2018, (Revision IEEE Std 802.15.7-2011), 2018, pp. 1–407.

[7] W. Xu, M. Zhang, D. Han, Z. Ghassemlooy, P. Luo, and Y. Zhang, "Real-time 262-Mb/s visible light communication with digital predistortion waveform shaping," *IEEE Photon. J.*, vol. 10, no. 3, pp. 1–10, Jun. 2018, doi: 10.1109/JPHOT.2018.2829905.

[8] S. Ricci, S. Caputo, and L. Mucchi, "FPGA-based pulse compressor for ultra low latency visible light communications," *Electronics*, vol. 12, no. 2, Jan. 2023, Art. no. 364, doi: 10.3390/electronics12020364.

[9] L. Teixeira, F. Loose, J. M. Alonso, C. H. Barriquello, V. A. Reguera, and M. A. D. Costa, "A review of visible light communication LED drivers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 919–933, Feb. 2022, doi: 10.1109/JESTPE.2021.3092284.

[10] T. Nawaz, M. Seminara, S. Caputo, L. Mucchi, F. S. Cataliotti, and J. Catani, "IEEE 802.15.7-compliant ultra-low latency relaying VLC system for safety-critical ITS," *IEEE Trans. Veh. Technol.*, vol. 68, no. 12, pp. 12040–12051, Dec. 2019, doi: 10.1109/TVT.2019.2948041.

[11] S. Jiang, S. Liu, C. Guo, X. Fan, T. Ma, and P. Tiwari, "Implementation of ARINC 659 bus controller for space-borne computers," *Electronics*, vol. 8, no. 4, Apr. 2019, Art. no. 435, doi: 10.3390/electronics8040435.

[12] P. Pendyala and V. S. R. Pasupureddi, "100-Mb/s enhanced data rate MIL-STD-1553B controller in 65-nm CMOS technology," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 52, no. 6, pp. 2917–2929, Dec. 2016, doi: 10.1109/TAES.2016.150564.

[13] X. Deng, K. Arulandu, Y. Wu, S. Mardanikorani, G. Zhou, and J.-P. M. G. Linnartz, "Modeling and analysis of transmitter performance in visible light communications," *IEEE Trans. Veh. Technol.*, vol. 68, no. 3, pp. 2316–2331, Mar. 2019, doi: 10.1109/TVT.2019.2891639.

[14] S. Ricci, S. Caputo, and L. Mucchi, "FPGA-based visible light communications instrument for implementation and testing of ultralow latency applications," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–11, 2023, doi: 10.1109/TIM.2023.3280520.

[15] Á. J. Almeida, N. A. Silva, N. J. Muga, P. S. André, and A. N. Pinto, "Calculation of the number of bits required for the estimation of the bit error ratio," in *Proc. 2nd Internat. Conf. Applic. Opt. Photon.*, Aveiro, Portugal, Aug. 2014, Art. no. 928607, doi: 10.1117/12.2063640.

[16] T. Kishi, H. Tanaka, Y. Umeda, and O. Takyu, "A high-speed LED driver that sweeps out the remaining carriers for visible light communications," *J. Lightw. Technol.*, vol. 32, no. 2, pp. 239–249, Jan. 15, 2014, doi: 10.1109/JLT.2013.2292896.

Open Access funding provided by 'Università degli Studi di Firenze' within the CRUI CARE Agreement