Silicon-Based Piezoresistive Stress Sensor Arrays for Use in Flexible Tactile Skin

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***Abstract*—Bioinspired robotics and smart prostheses have many applications in the healthcare sector. Patients can use them for rehabilitation or day-to-day assistance, allowing them to regain some agency over their movements. The most common way to make these smart artificial limbs is by adding a "human-like" electronic skin to detect force and emulate touch detection. This paper presents a fully integrated CMOS-based stress sensor design with a high dynamic range (100 kPa to 100 MPa) supported by an adaptive gain-controlled chopping amplifier. The sensor chip includes four identical sensing structures capable of measuring the chip's local stress gradient and complete readout circuitry supporting data transfer via I2C protocol. The sensor takes 10.2 ms to measure through all four structures and goes into a low-power mode when not in use. The designed chip consumes a total current of ∼300 μA for one complete operation cycle and ∼30 μA during low power mode in simulations. Moreover, the complete design is CMOS-based, making it easier for large-scale commercial fabrication and more affordable for patients in the long run. This paper further proposes the concept of a tactile smart skin by integrating a network of sensor chips with flexible polymers.**

***Index Terms*—Artificial skin, CMOS stress sensors, piezoresistive, silicon stress sensors, flexible sensors, tactile sensors.**

I. Introduction

NATURE has always inspired innovation. Numerous advancements in engineering, architecture, medicine, material technology, and agriculture have been inspired by the features of organisms that have adapted to survive even in the harshest environments. Some of the most notable examples of "biomimicry" in engineering are how Leonardo da Vinci's study of bird wings inspired the model of flying machines, which later became the current-day aeroplanes, or how Eiji Nakatsu modelled the bullet train after the beak of the kingfisher bird, the wings of an owl, and the bellies of penguins. He made the trains faster and solved the problem of sonic booms caused by air pressure accumulation when the high-speed trains exited the tunnels [1].

Another field that routinely derives inspiration from biology is robotics, especially for biomedical applications. Conventional prostheses and orthoses are designed to provide only basic functionality and support. However, if we can combine sensory interface features with soft robotics principles, we can significantly improve the rehabilitation of individuals with paraplegia and muscular disabilities. A biomechatronic system typically has four main components: biosensors that can detect the intended action through the transmitted impulses sent by the user's brain; the controller that can translate biological impulses into electrical signals; mechanical sensors that can detect and convert physical stimuli into relevant data for the controller; and the robot actuator which acts an artificial muscle to produce the desired movement corresponding to the human body function [2]. References [3], [4], [5], [6], [7], [8] show the current progress in decoding such brain-controlled impulses into actual motor movement intentions and the possible role of artificial intelligence (AI) in prosthetic and orthotic rehabilitation [9].

So far, all the papers mentioned above focus more on biosensors, controllers and actuators. However, all four components should function properly and fit seamlessly for a well-designed biomechatronic system. The mechanical sensors' design is equally essential as it ensures the robotic actuators interact with the environment correctly and the sensor feedback data is sent to the controller on time. Therefore, the overall effectiveness of a sensing system, especially for use as a tactile artificial skin, depends on a few critical factors. These include (a) sensor performance in terms of sensitivity, accuracy, robustness, etc., (b) sensor placement and conformability, (c) integration of sensing structures with robots, (d) data collection and transmission, and (e) data processing algorithms [10]. Many biomedical applications require tactile sensors, so the sensor material, transconductance medium, and structures can vary significantly based on the requirements. Sensors that need to be implanted within the body must be small, biodegradable and, most of all, comfortable. In contrast, wearable sensors are frequently affected by external forces and would benefit from being robust and flexible [11]. The advantages and disadvantages of using different materials and sensing techniques have been extensively

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discussed over the years [12], [13], [14], [15]. Furthermore, specific considerations for designing tactile sensing systems for robotic applications have also been reported in [10], [16].

The main challenge for developing artificial tactile skin has always been to design flexible and stretchable electronic sensors. Silicon is the most widely used semiconductor material for modern electronics, but its brittle nature makes it challenging for use in applications where flexibility is essential. On the other hand, organic semiconductors, elastomers, and polymers are flexible and can conform to uneven surfaces. However, due to lower mobility, electronic circuits designed using organic semiconductors often perform inferior to their silicon counterparts. Over the last decade, various techniques to make silicon wafers flexible by thinning to 20 - 50 μm have been tested with positive results [17], [18], [19], [20], [21], [22], [23]. Embedding these ultra-thin silicon chips in flexible polymer substrates can allow us to enjoy the benefits of both materials. Since the silicon fabrication process is already well established, and polymer foils can be made on a large scale using roll-to-roll manufacturing, the cost of production can be controlled effectively.

Considering all the above observations, we decided to design a silicon-based sensor. Additionally, the inherent piezoresistive property of silicon makes it an attractive material for pressure sensors. Piezoresistivity in semiconductors like silicon and germanium has been extensively studied since the early 1950s [24], [25], [26], [27]. Pressure-sensitive sensors can be made using either silicon resistors or transistors as the primary sensing element [28], [29], [30], [31], [32], [33]. Based on the comparison between the different silicon devices presented in [34], it can be concluded that silicon resistors offer the better choice for designing highly sensitive stress sensors. As a result, we will focus on silicon resistor-based stress sensor design in the following paper. This work aims to expand the available research and use it to create low-power, low-noise, directionally sensitive stress sensors with a high dynamic range. Furthermore, this paper presents a system-level concept for using the proposed sensors in a more extensive network to design an efficient and flexible tactile skin. The proposed system is based on the requirements expected from such artificial skin as presented in [16], [17] and will be discussed in detail in the upcoming sections.

This paper is organised as follows: The basic concept of our tactile skin and its construction is explained in Section II. Section III describes the implementation of the sensor unit along with the critical considerations behind certain design choices. Section IV dives into the design of the readout circuitry that supports the main sensing structure. A final top-level algorithm for the tactile network using the silicon sensor array is explained in Section V, and some simulation results are provided in Section VI. Finally, Section VII presents the conclusion to the paper with a few discussions and suggestions about the future scope of this work.

II. Flexible Tactile Skin

The target application for our stress sensors is as an artificial skin for prostheses. As mentioned earlier, such tactile systems must be flexible and conform to the mechanical device for seamless operation. Therefore, it is crucial to integrate the sensor chips with a substrate that can make them flexible without compromising their sensitivity. Since covering large areas with only silicon is impossible due to cost and bending limitations, an alternate "network" approach is used here [35]. The idea is to place multiple silicon sensor chips in an array with a fixed spacing between them. Each chip, therefore, acts as a taxel in the more extensive network. These chips are then embedded into a flexible polymer substrate that can be used to cover parts of the prosthesis as needed. Although papers with similar sensing array concepts have been summarised in [11], [12], most are capacitive or microelectromechanical systems (MEMS). Capacitive stress sensors show a high sensitivity and are more resilient to temperature variations; however, they are non-linear and more prone to stray capacitances. Since typical capacitive tactile sensors can only detect touches from electrically conducting objects, their use case can be significantly limited. Similarly, silicon-based MEMS devices are incredibly delicate and may not be capable of bearing the range of forces that are applied on a typical prosthetic device. This makes them a less-than-ideal choice for such applications where robustness is valued.

The fundamental principle behind the design of our tactile skin is based on the behaviour of thin plates under an applied load [36]. When an external force is applied to an object, it undergoes deformation, resulting in internal stresses within that object. The internal stresses depend on the magnitude of the applied force, so if one can measure the value of the generated stress, it can be used to calculate the force. We use this concept to create artificial skin by using polymer substrates to mimic the behaviour of human skin under deformation and an array of stress-sensing silicon chips to measure the stress after deformation. To maximise the efficiency of the skin, the effective distribution of chips in the array is essential.

On the one hand, large spacing within the array will prevent more chips from responding to the applied touch, increasing the chances of missing stimuli. The chips must be more sensitive to compensate for this, making the design more challenging. It will also affect the system's power consumption by increasing the current required to achieve such high sensitivity specifications. On the other hand, too little spacing will increase the cost due to a higher chip density. It will also increase the data collected from the network, lowering the system's speed. Using a higher frequency clock for data transmission could help compensate for the slow speed; however, it would increase the power consumption again. Further disadvantages of denser arrays include difficulty in wire routing and a decrease in the overall flexibility of the skin. It must be noted that the chip spacing within the array is also application-dependent. Tactile skin designed for areas with a higher contact probability (such as the tips of a robotic hand) can have a more dense array, while larger areas like the forearm can be more sparse.

A. Material and Assembly

After introducing the basic principle behind the tactile skin, we will discuss its construction before moving on to the detailed working concept. The model for our proposed system was created in COMSOL Multiphysics and optimised to obtain

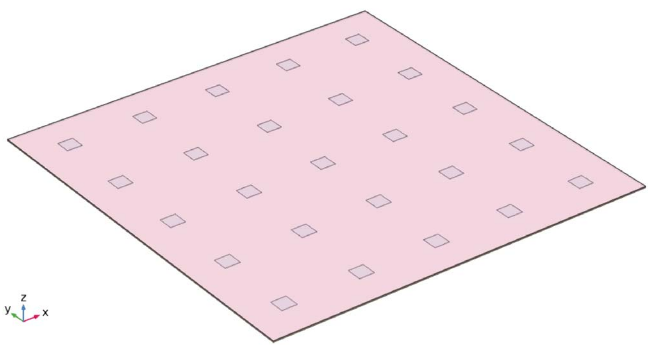

Fig. 1. Diagrammatic representation of the flexible tactile skin with a 5 × 5 chip array. The chips are 1.46 mm × 1.46 mm and are placed with an edge-to-edge spacing of 6 mm between them. This patch of skin has dimensions of 37.3 mm × 37.3 mm [35].

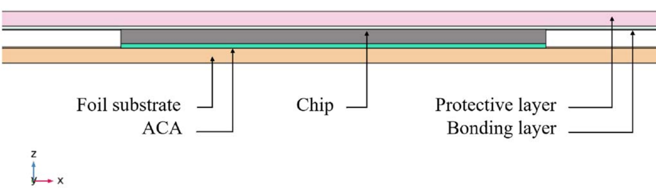

Fig. 2. A cross-sectional view of the tactile skin assembly. The chips are sandwiched between two layers of flexible PI foils. The electrical connections are provided via the conducting balls in the ACA epoxy.

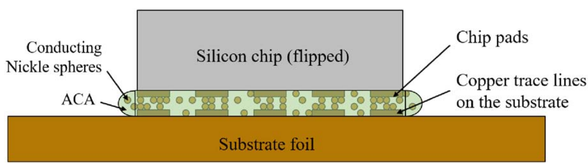

Fig. 3. Traditional flip-chip bonding process using anisotropic conducting adhesive (ACA). Since this process involves the chip being flipped, all the fabricated circuit components now lie at the chip-substrate boundary.

suitable values of the material dimensions for higher performance and sensitivity. Fig. 1 shows the pictorial representation of our proposed tactile skin, and Fig. 2 shows the different layers within the assembly. The base is constructed using a flexible Polyimide (PI) foil of 50 μm thickness as the substrate[1]. The chips are then placed on the PI foil using flip-chip bonding. All the chips in the array are supplied with the relevant power and data signals via copper trace lines deposited on the PI foil. The trace lines and chip pads are connected via an Anisotropic Conducting Adhesive (ACA) containing small conducting Nickle (Ni) spheres [37], [38]. Fig. 3 shows how the ACA epoxy establishes electrical connections in a typical flip-chip bonding process. This approach is preferred over conventional wire bonding because of its robustness during repeated bending operations. The possibility of breakage in wire-bond connections after repeated use or during assembly limits its

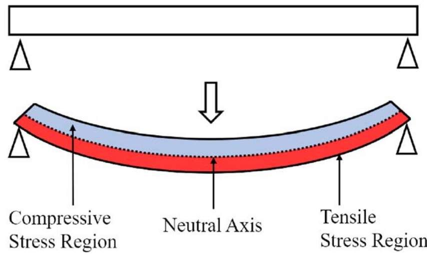

Fig. 4. Representation of the stress profile of a beam under external load.

viability for tactile applications. Finally, another 50 μm thick PI foil is adhered to the entire assembly as a protective layer. It ensures the silicon chip is protected from dust, scratches and other environmental factors. Moreover, it is evident from the literature [39] that having chips encapsulated in a protective layer or a chip-in-foil (CiF) system is more robust than a chip-on-foil (CoF) assembly.

Previous research [37] has shown that ultra-thin chips ($<$20 μm) are more flexible and can withstand higher bending cycles before failure. However, for bending-based stress sensing applications, one needs to consider the structure of the entire assembly. Fig. 4 shows a bent beam under external load. Within the cross-section of such a structure lies an area of zero strain, i.e., a line where no longitudinal compressive or tensile stress exists. The location of this neutral axis depends on the material property and thickness of all assembly layers. The closer the sensing elements lie to the neutral axis, the less stress they experience, irrespective of the applied force. If the position of the sense structures coincides with the location of the neutral axis for the tactile skin assembly, it would significantly reduce (in the worst case- completely negate) the skin's stress sensitivity, even if advanced sensor design techniques are used. Since we have chosen to use PI foils of the same thickness[2] as both our substrate and top layer, our system becomes relatively symmetric. The neutral axis, therefore, lies close to the centre of the silicon chip. Since traditional semiconductor devices are fabricated at the chip surface, the only way to distance the sensors from the neutral axis is to use thicker chips. Keeping the trade-off between stress sensitivity and flexibility in mind, we decided to keep our chips 50 μm thick. Even with these values, the overall thickness of the entire structure remains within 200 μm and should remain pretty flexible.

B. Working Concept for Array-Based Tactile skin

Fig. 6 shows the displacement of the chips in the array when an external "touch" is applied to the tactile skin (Fig. 5). COMSOL simulations were performed to verify the working concept of our proposed system. The tactile skin was designed based on the materials and specifications mentioned in Section II-A. It can be observed that the sensor chips closer to the contact area see a higher displacement and, hence, are expected to

[1]COMSOL simulations show that thinner foils are more flexible, and hence, transfer a larger stress to the surrounding chips. However, a 50 μm value was chosen as a trade-off between higher sensitivity and sturdiness to support the entire assembly.

[2]PI foils such as UPILEX S50 are preferred due to their superior mechanical, electrical and thermal properties [40]. Using a thinner protective layer would bring the neutral axis closer to the sense elements on the chip, which would lower the sensitivity of the skin.

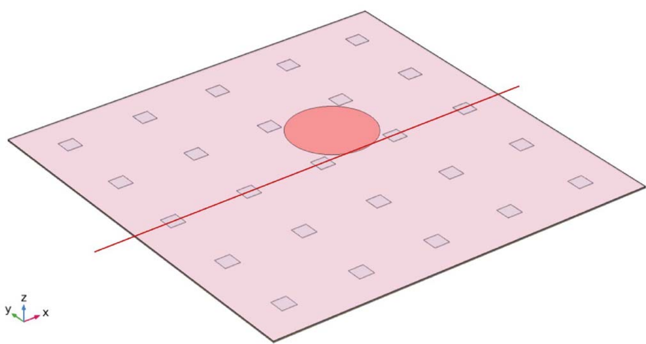

Fig. 5. Point of contact (shown in red) for an externally applied force to emulate "touch" on the tactile skin. The contact area is roughly 8 mm in diameter and lies at the centre of 4 chips of the array. The red line represents the x-axis for the stress response plots in Fig. 7.

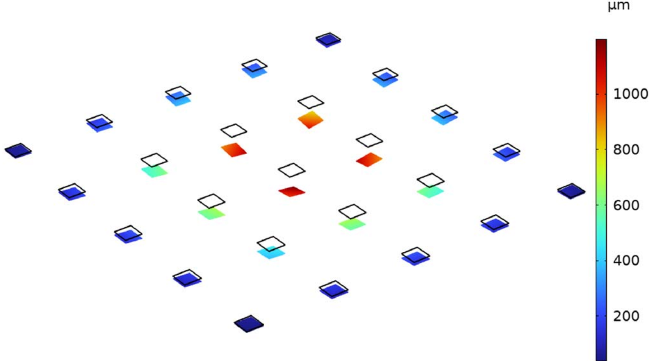

Fig. 6. The displacement of chips in the array from their "zero stress positions" due to the deformation of the tactile skin under an applied force of 5 N.

experience higher stress levels. This is confirmed by Fig. 7, which shows the response of the middle row of chips in the array (at the cut line) and the different stress components. There are a few important things that can be noticed here:

1) The stress magnitude decreases as the distance between the chips and the point of contact increases.
2) The overall magnitude of stress depends on the value of the applied force; however, the behaviour of the stress profile in all the chips of the array follows the same pattern as above.
3) The chips in our proposed assembly experience tensile stress because the components lie below the neutral axis (at the interface between the chip and the foil substrate due to the flip-chip bonding process).

Based on the observations above, we can now explain the working concept of our array-based flexible tactile skin. All the chips in the array experience different magnitudes of stress depending upon the applied force and their positions relative to the point of contact. The chips convert the sensed stress value into a corresponding digital signal, which can be transmitted to a central Microcontroller Unit (MCU) using any communication protocol. Once the stress data from all the chips in the array is collected, the point of contact can be easily interpolated based on the stress profile of the entire network (Fig. 8). Additionally, after a one-time initial calibration of the applied force and its resulting stress, we can estimate the magnitude of the contact force from the stress values. The advantage of using interpolation for post-processing is twofold: it allows us to use a sparse chip array while still detecting contacts even if they have no cross-over with any chip in the array, and secondly, it is a relatively simple algorithm to realise. There might be other sophisticated algorithms capable of giving a more precise location of contact; however, that is different from the focus of this paper. This paper aims to demonstrate the design of silicon-based stress sensors and their possible use to create highly sensitive, flexible, tactile skin. The steps to optimise the data collection and processing algorithms can be a subject of interest once the basic proposed design and its proof of concept are verified.

It may be important to mention here that the array spacing is large enough to cause a significant decrease in stress as we move farther away from the point of contact. As such, it is reasonable to expect that the chips closest to the "touch" will always see the highest stress magnitude. Therefore, the proposed system design can provide accurate contact information even if minor variations in chip sensitivity exist due to fabrication.

We can also see from Fig. 8 that the maximum stresses are located at the edges closest to the point of contact. It may, therefore, be a wise choice to place multiple sensing structures near the outer perimeter of the chip to get more information about the stress gradient. We can determine the equivalent stress direction from the magnitudes of individual chips' X and Y stress components. However, designing sensors that can detect the magnitude and the exact direction of the stress would make the analysis for the point of contact much more simple and accurate. Additionally, since the type of stress experienced by the chip depends on the position of the sensing elements with respect to the neutral axis, the chip must have the capacity to measure and differentiate between tensile and compressive stresses. Any change in the type of stress experienced by the chips can then be calibrated at the post-processing stage. This will make the tactile skin more robust against variations caused due to assembly. Therefore, the primary sensing mechanism used in the chip must be able to measure the magnitude, type and direction of the external stress. With the basic requirements of the sensor chip being established, we can now move on to the actual chip design.

III. Stress Sensor Implementation

We have briefly discussed why silicon resistors are the primary choice for our sensing element in Section I. The stress sensitivity of silicon, which is a function of its doping concentration and temperature, can be characterised in terms of its p-factor [26]. For doping densities less than 10^{18} cm^{-3}, the p-factor remains relatively constant for any variations in impurity concentration but becomes highly dependent on temperature fluctuations. However, as one moves to concentrations higher than 10^{18} cm^{-3}, the temperature dependence decreases, but at the cost of a lower p-factor, which now becomes more

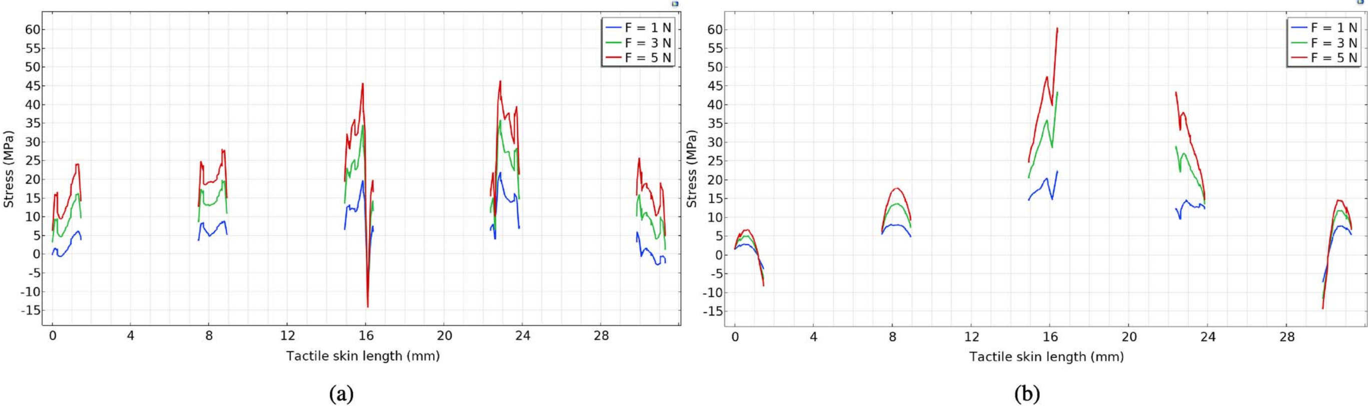

Fig. 7. COMSOL simulation results showing the (a) X component and (b) Y component of stress under an applied force of 1 N, 3 N and 5 N. The x-axis of the plots is the cut-line shown in Fig. 5. The results will vary depending on the thickness and mechanical properties of the materials used and how they are assembled.

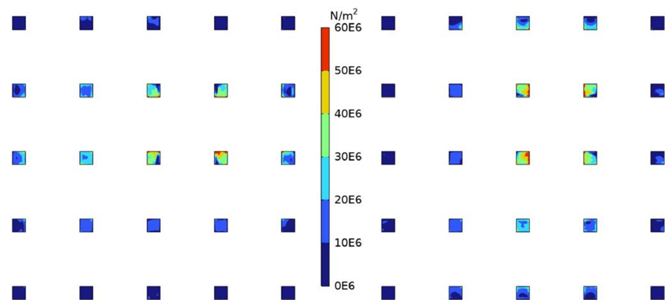

Fig. 8. The stress profile of the entire array for X component (left) and Y component (right) of stress. These surface plots are for the chip-substrate interface of the tactile skin under an applied force of 5 N (at the location shown in Fig. 5).

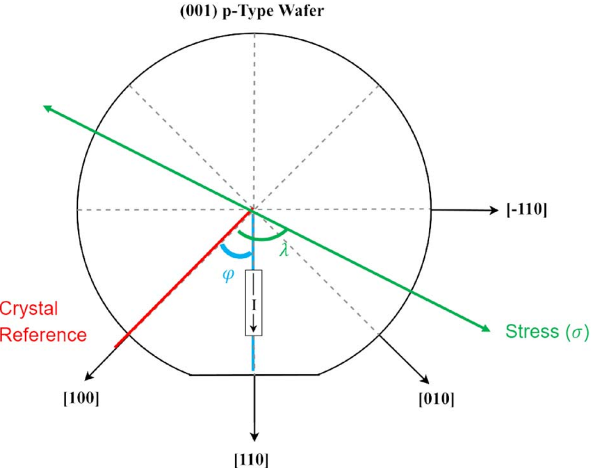

Fig. 9. Angle of resistor orientation and the stress direction with respect to the crystal reference direction [100].

sensitive to doping variations. For our application, a higher sensitivity to stress is preferred over a constant temperature response; therefore, a lower-doped N-well resistor is used as the primary sensing unit. There are techniques used in the sensor design to specifically target the temperature compensation for a more robust design. These will be discussed exclusively in Section III-A.

Since Cadence Design Environment does not have an inbuilt feature to analyse any stress behaviour, it was essential to first create a model to mimic the stress response of silicon resistors. Our VerilogA stress model is based on the relative change in silicon resistivity (ρ) as a function of the resistor orientation and the stress direction (equation (1)), as reported by Freutt in [41]. Temperature dependence of the piezoresistance coefficients is also included based on the characterisation presented in [42]. All the angles are defined with respect to the crystal reference [100] of the silicon wafer (Fig. 9). The final VerilogA model uses resistor orientation and the magnitude and direction of applied stress as input variables to simulate the stress response. The additional voltage drop across the resistor due to stress is added to the voltage drop calculated by the Process Design Kit (PDK). This also allows us to use all other PDK models for corner and mismatch simulations as usual.

$$\frac{\Delta\rho}{\rho} = \left[\pi_{11}\left(\frac{1}{2}+\frac{1}{2}\cos(2\varphi)\cos(2\lambda)\right) + \pi_{12}\left(\frac{1}{2}-\frac{1}{2}\cos(2\varphi)\cos(2\lambda)\right) + \pi_{44}\left(\frac{1}{2}\sin(2\varphi)\sin(2\lambda)\right)\right]\sigma \quad (1)$$

where,
φ = angle between the resistor orientation and [100],
λ = angle between the applied stress direction and [100],
σ = value of applied stress (+ve for tensile and $-$ve for compressive),
π_{11}, π_{12} = normal piezoresistive stress coefficients,
and π_{44} = shear piezoresistive stress coefficient.

The doping-dependent values of the piezoresistive stress coefficients were obtained experimentally using a bending setup (Fig. 10). A testing wafer with N-well resistors layouted in different directions was designed and diced to create thin silicon

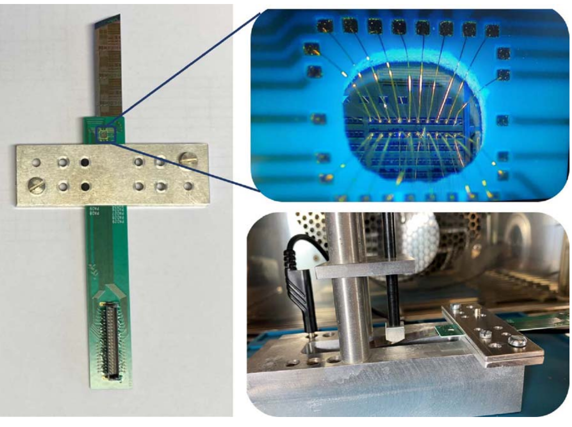

Fig. 10. Bending setup for measuring piezoresistive coefficients of N-well resistors.

TABLE I
PIEZORESISTIVE COEFFICIENTS FOR SILICON N-WELL RESISTORS

Coefficients	in 10^{-11} Pa^{-1}		
	Smith [25]	Matsuda [27]	**Measured Values**
π_{11}	-102.2	-77.3	-98.9456
π_{12}	53.4	-40.1	49.4729
π_{44}	-13.6	-14.8	-12.4675

stripes. The resistor pads on the wafer stripes were bonded to a printed circuit board for electrical connectivity, and the entire structure was clamped between two steel plates to provide a mechanically fixed end. A downward force was applied on the other edge of the stripe, which generates a surface stress given by equation (2) [43] in the direction of the stripe length. The relative change in resistance of 3 resistors with known φ, λ and σ values was used in equation (1) to solve for the piezoresistance coefficients (Table I)

$$\sigma = \frac{6F(l-x)}{wh^2} \tag{2}$$

where,
F = magnitude of applied force in Newton,
w = width of the stripe,
h = thickness of the stripe,
l = distance between the fixed edge and the point of applied force,
x = distance between the fixed edge and the resistor position.

A. Sensor Design

Fig. 11 shows our chip's basic stress sensor design. The sensing mechanism is similar to the one presented by Nurmetov in [34], [44] as this solution provides a direct first-order temperature compensation as long as the temperature coefficients of the reference (R_{ref}) and the sense (R_{sense}) resistors are identical. Moreover, as long as R_{ref} is designed to be insensitive to stress variations, the final sensed voltage V_{sense} will only respond to changes in stress and will be largely independent of temperature effects. Further trimming capability is also implemented in the design to reduce the effect of process variations and other mismatches. A 9-bit current mirror trimming is used to

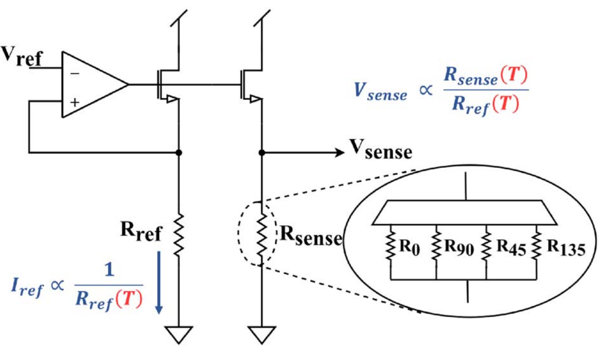

Fig. 11. Basic stress-sensing mechanism used in the chip as presented in [34], [35], [44].

target current mismatch and to ensure that V_{sense} matches V_{ref} closely for "Zero Stress" conditions. Additional 7-bit resistor trimming is used to compensate for any mismatches in the temperature coefficients of R_{ref} and R_{sense}.

The same principle is extended to introduce directional sensitivity to the design by using identical sensing resistors oriented in different directions. The sensed voltage corresponding to the desired direction can be measured at the V_{sense} node by giving the appropriate select signal to the multiplexer. This requires minimum addition to the design for its implementation and saves power and area by redirecting current to the relevant resistor when needed. The resistors can be cycled through at the desired speed based on the target application. Furthermore, the same trimming circuitry can be reused for all four resistors if the corresponding trim bits are stored in the memory correctly. The four sensing resistors are oriented in the [110], [$\bar{1}$10], [010] and [100] directions and are denoted as R_0, R_{90}, R_{45} and R_{135} respectively[3]. Fig. 12 shows the Monte Carlo results for V_{sense} after all trimming steps are over. When no stress is applied, the sensor has a nominal voltage of ~900 mV with a standard deviation of ± 295 μV. The voltage variation w.r.t temperature remains relatively constant for -40 °C to 120 °C range with a mean of 3.036 μV and a standard deviation of ± 79.39 μV.

The stress response of sense resistors R_0, R_{45} is presented in Fig. 13. The close fit between the simulation results and the experimentally measured values shows the VerilogA model's accuracy[4]. We can see from the figure that N-well resistors behave linearly within a ± 100 MPa stress range. They show a decrease in resistance when positive (or tensile) stresses are applied and an increase in resistance for negative (compressive) stress values. This behaviour proves to be very useful to detect the type of applied stress for our application. Furthermore, due to the crystalline structure of silicon, it can be observed that

[3]Resistor oriented in [110] direction is assigned R_0 as it is the direction of the wafer notch, and hence is considered the primary axis for the chip going forward.

[4]Since the experiments were performed using wafer stripes cut in 0° ([110]) only measurements corresponding for R_0 are shown. R_{45} resistors show a very low response to stress applied in purely 0° direction. Furthermore, the bending setup applied force from the top, and hence, the resistors were subjected to only tensile stress during our experiment. However, the resistors will behave similarly under compressive stress as shown in numerous prior art, including [44] and [32].

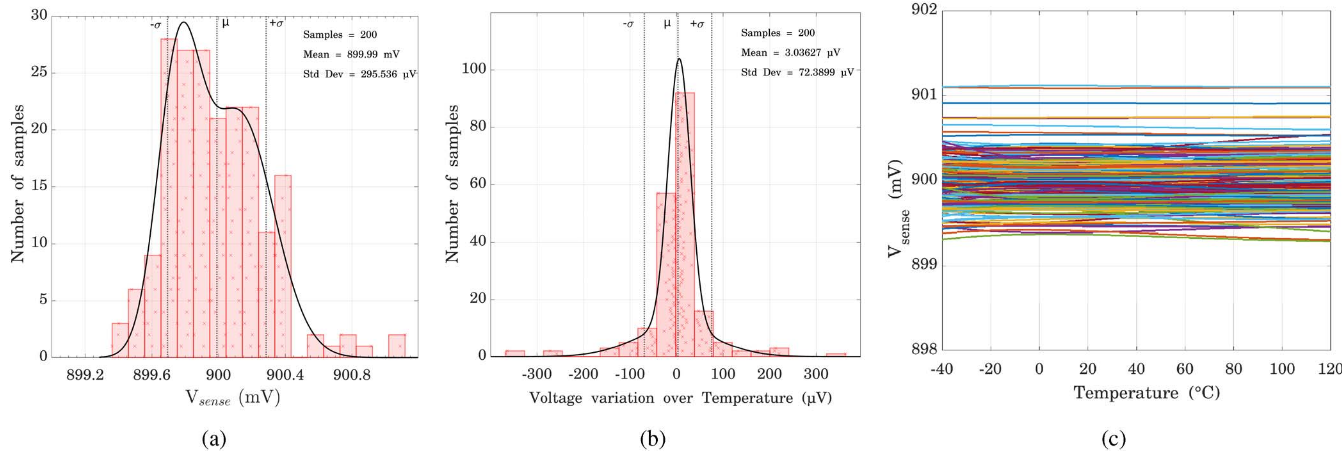

Fig. 12. Results after mismatch analysis: (a) V_{sense} after trimming for process variations, (b) the residual V_{sense} variation for a -40 °C to 120 °C temperature range, (c) the final V_{sense} w.r.t. temperature after trimming. These results are based on Monte Carlo simulations for 200 samples.

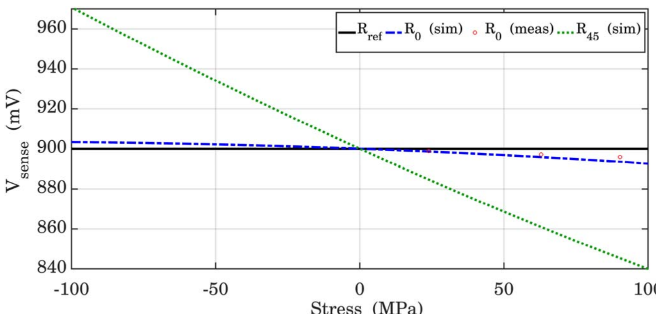

Fig. 13. The response of N-well resistors for an applied stress range from -100 MPa to +100 MPa. The stress response corresponds to the case when the applied stress is in the same direction as the sense resistor orientation [35].

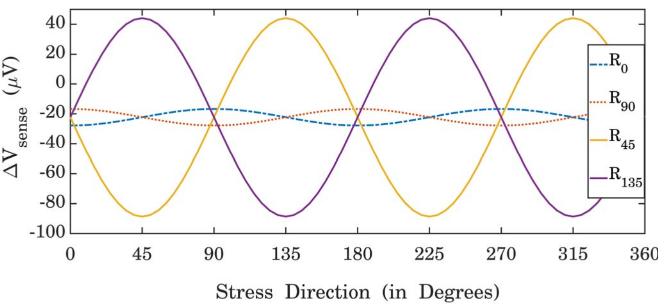

Fig. 14. Simulated stress response of N-well resistors oriented in different directions when +100 kPa tensile stress is applied in different directions [35].

R_{45} (and R_{135}) show higher stress sensitivity as compared to R_0 (and R_{90}). This can be seen more clearly from Fig. 14, which shows how each of the four sensing resistors reacts to different directions of applied stress. As expected, each resistor has the highest sensitivity to stresses in the same direction as its orientation. However, it is interesting to observe that orthogonal resistors behave symmetrically, e.g., R_{45} shows similar results for a tensile stress applied in 45° and for a compressive stress in 135°. The same issue exists in both orthogonal resistor pairs and is consistent with observations made in [44]. This problem can be solved by using the values sensed by one resistor pair to determine the type of stress and then establishing the direction through the other.

The exact direction of stress can be easily calculated from the data obtained from the sense resistors. Equation (1) can be written for each individual sense resistor by putting the values for φ based on their orientation. Care should be taken that equation (1) requires φ values with reference to [100] while we use the direction of the notch, i.e., [110] for our resistor direction nomenclature.

$$\frac{\Delta V_0}{V_0}\bigg|_{\varphi=45^\circ} = A = \left[\left(\frac{\pi_{11}}{2}+\frac{\pi_{12}}{2}\right)+\left(\frac{\pi_{44}}{2}\right)\sin(2\lambda)\right]\sigma \tag{3}$$

$$\frac{\Delta V_{45}}{V_{45}}\bigg|_{\varphi=90^\circ} = B = \left[\left(\frac{\pi_{11}}{2}+\frac{\pi_{12}}{2}\right)-\left(\frac{\pi_{11}}{2}-\frac{\pi_{12}}{2}\right)\cos(2\lambda)\right]\sigma \tag{4}$$

$$\frac{\Delta V_{90}}{V_{90}}\bigg|_{\varphi=135^\circ} = C = \left[\left(\frac{\pi_{11}}{2}+\frac{\pi_{12}}{2}\right)-\left(\frac{\pi_{44}}{2}\right)\sin(2\lambda)\right]\sigma \tag{5}$$

$$\frac{\Delta V_{135}}{V_{135}}\bigg|_{\varphi=180^\circ} = D = \left[\left(\frac{\pi_{11}}{2}+\frac{\pi_{12}}{2}\right)+\left(\frac{\pi_{11}}{2}-\frac{\pi_{12}}{2}\right)\cos(2\lambda)\right]\sigma \tag{6}$$

Adding (3) and (5), we get:

$$\frac{A+C}{2} = \left(\frac{\pi_{11}}{2}+\frac{\pi_{12}}{2}\right)\sigma \tag{7}$$

We can get the two unknown values of stress magnitude (σ) and direction (λ) by solving the above linear equations. Upon substituting equation (7) in (3) and (4) and then dividing them, we get the following solutions:

$$\lambda = \frac{1}{2}\tan^{-1}\left(\frac{A-(\frac{A+C}{2})}{(\frac{A+C}{2})-B}.\frac{(\pi_{11}-\pi_{12})}{\pi_{44}}\right)$$
$$\sigma = \frac{A-(\frac{A+C}{2})}{(\frac{\pi_{44}}{2})\sin(2\lambda)} \tag{8}$$

The stress direction (λ) can be used to obtain the stress with respect to the notch direction to better match the notation of resistor orientation.

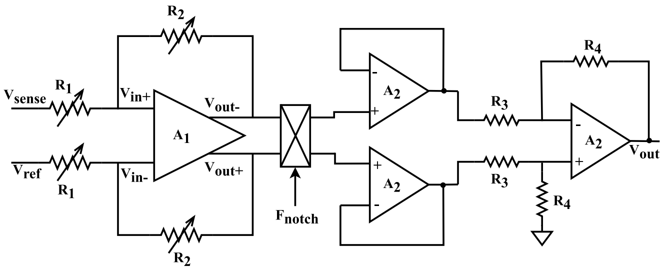

Fig. 15. A low-noise instrumentation amplifier with an adaptive gain control. The block between A_1 and A_2 represents the notch filter.

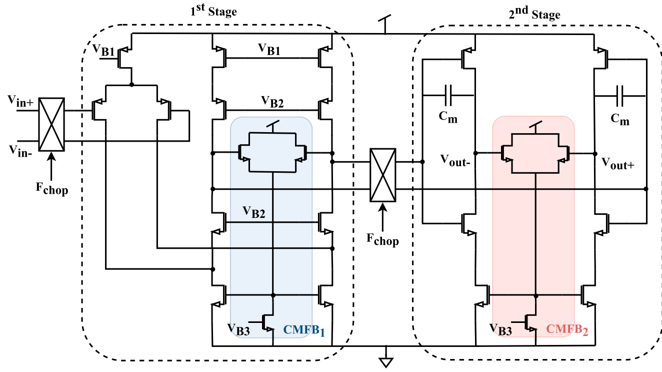

Fig. 16. Circuit diagram of the fully differential amplifier with a chopped first stage (A_1).

As shown above, four sense resistors (oriented in 45° increments) are sufficient to calculate the stress direction at all intermediate angles. In the complete tactile array, similar data can be obtained from all chips closest to the point of contact. This makes our system over-determined and more robust to sensitivity variations of the chips in the array.

IV. Read Out Electronics

We have seen from the previous section that the N-well resistors have roughly ten times lower sensitivity in 0° and 90°. This results in a very low magnitude voltage being generated in some instances. Therefore, the sensor voltage must be amplified before further processing can occur. Additionally, since there is an inherent directional dependence of sensitivity, the amplifier must have a variable gain that can be adjusted based on the target direction. This section describes the design and selection criteria for the readout circuitry that follows the sensing structure.

A. Amplifier

For low magnitudes of stresses (∼100 kPa), only a few μV of the signal is generated, especially in less-sensitive directions (Fig. 14). Combined with the fact that touch applications have low-frequency stimuli, the signal is highly susceptible to flicker noise. Our sensor chip contains a variable gain chopping amplifier to solve this issue. The amplifier gain can be set to 2, 10, 20 and 100 V/V using a 2-bit signal. These values are stored in a dedicated "gain trimming" memory and can be changed for different resistor orientations.

Fig. 15 shows the general block diagram of the amplifier. Amplifier A_1 is a two-stage, fully differential amplifier. The first stage is realised using a conventional folded cascode, followed by a current reuse amplifier as an output stage for better swing and current drive (Fig. 16). Both stages have a common drain common-mode feedback circuit. Only the first stage of Amplifier A_1 is chopped, as most of the gain is provided by that stage. Amplifier A_2 (Fig. 17) is realised using a conventional single-output two-stage amplifier with a miller compensation for stability. The chopping is performed at A_1 using a 200 kHz clock, and a switched capacitor (SC) based notch filter (presented in [45]) is used to remove ripples (Fig. 18).

The advantages of chopping in our system are twofold: firstly, it reduces the input-referred noise is to ∼80 nV/$\sqrt{Hz}$ at the input signal frequency[5] after chopping (Fig. 19), and secondly, it lowers the offset of the signal. Fig. 20 shows the Monte Carlo simulations for the amplifier output with and without chopping. The high gain of our amplifier could cause the amplified voltage to rail if the offset is too large. Therefore, chopping the first stage keeps the offset at a manageable value where it can be compensated later digitally (as explained in detail in Section V). The resistors R_1 and R_2 set the gain depending upon the signal requirement. A_2 is connected in a voltage buffer configuration to avoid loading before A_1's amplified differential output is

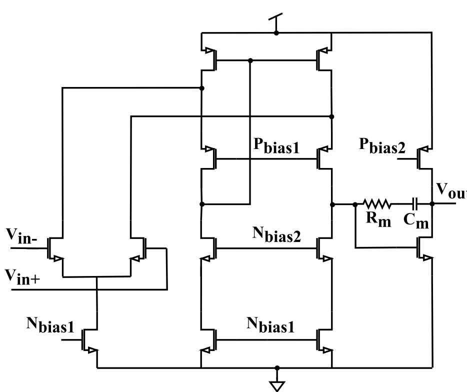

Fig. 17. Circuit diagram of a two-staged single-ended amplifier (A_2).

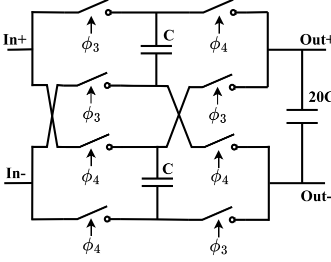

Fig. 18. A switched capacitor notch filter for ripple reduction.

[5]The input of the amplifier changes when the multiplexer switches to another resistor. Therefore, the input signal frequency for the amplifier will be the same as the multiplexer select signal, i.e., 1.5625 kHz.

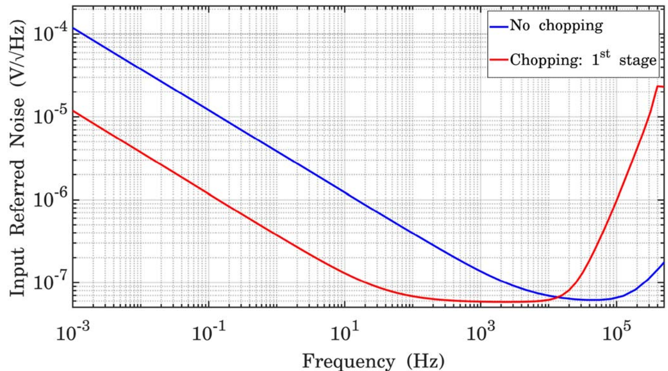

Fig. 19. The Input-referred noise plot of the instrumentation amplifier with and without chopping. Chopping is performed using a 200 kHz clock.

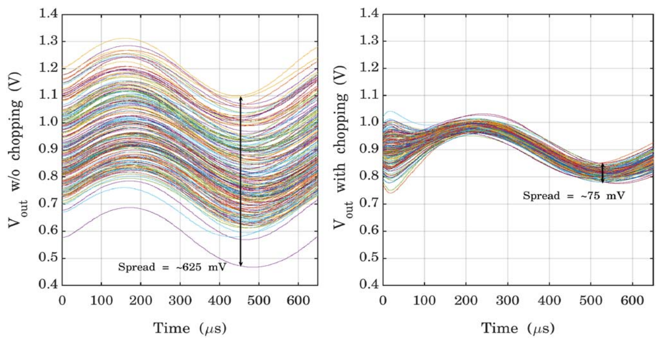

Fig. 20. Monte Carlo simulations with 200 samples for a 1 mV input signal amplified by a gain of 100.

converted into a single-ended voltage ready for digitisation. Resistors R_3 and R_4 can provide additional gain levels if needed. However, they are kept the same in our design. The final V_{out} signal is then ready to be sent to the next stage for digitisation. During normal operation, the complete amplification stage consumes an average ∼190 μA current. Power saving techniques such as a "Low Power Mode (LPM)" are used in the chip to gate the supply voltage and clocks when the chip is not in use. The amplifier only consumes a few μA of current during LPM.

B. Analog to Digital Converter (ADC)

An asynchronous 12-bit hybrid Successive-Approximation-Register (SAR) ADC converts the amplified sensor voltage into digital bits. The hybrid ADC uses a 7:5 segmentation between the capacitive and resistive components (Fig. 21) [46]. The architectural choice is based on a trade-off between conversion time, power consumption, area, and multiplexing capabilities. The unit capacitor value for the 7-bit capacitive Digital to Analog Converter (DAC) is 40 fF. Due to their lower stress sensitivity, 32 N-poly resistors, each of value 1 kΩ are used in the 5-bit resistive DAC. Care is taken during layout to keep the orientation same for the entire structure so that all resistors react similarly to any applied stress, and any stress-related variation is automatically nullified after voltage division. The complete ADC has a Signal-to-Noise (SNR) ratio of 71 dB and an Effective Number of Bits (ENOB) of 11.5 bits.

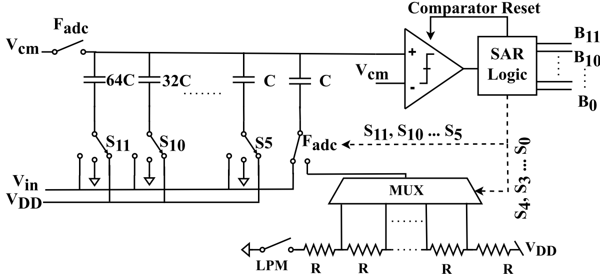

Fig. 21. A 12-bit hybrid SAR ADC with 7:5 segmentation [35].

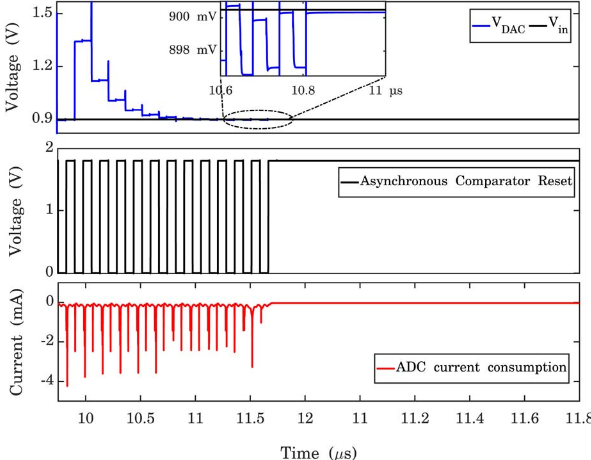

Fig. 22. The transient response of the asynchronous hybrid SAR ADC for V_{in} = 902 mV. The DAC operates at a higher internally generated frequency for faster conversion and V_{DAC} converges to the common mode voltage (V_{cm} = 900 mV).

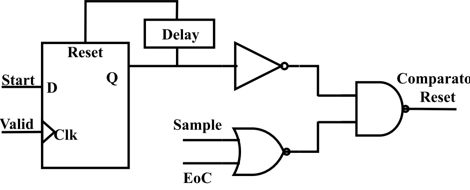

Fig. 23. Block diagram for the generation of the asynchronous comparator reset.

Fig. 22 shows the transient response of the ADC. A 50 kHz clock is used for sampling. When the sampling clock is high, the positive input of the comparator is connected to the common mode voltage (V_{cm}), while the bottom switches S_{11}-S_5 are connected to the input (V_{in}). Once the clock goes low, the bottom switches are connected one by one to the supply voltage to figure out the relevant bit value. The comparator is reset asynchronously until all bits are calculated and the node voltage at the positive input of the comparator converges back to V_{cm}. Figs. 23 and 24 show the block diagram of how the comparator reset is generated and the simplified signal waveforms. The conversion starts when the sampling clock (Sample) goes low, and the 'Comparator Reset' is pulled down, which initiates a comparison. Once the comparator reaches a stable

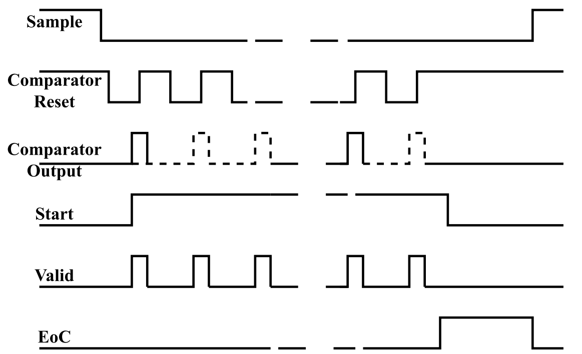

Fig. 24. Simplified waveforms to explain the working of the asynchronous SAR ADC.

output, it pulls up the 'Start' and the 'Valid' signals, and the bit cycling process begins. The 'Start' signal remains high until all digital bits are evaluated, while 'Valid' is pulled up after every successful bit resolution after comparison, which resets the comparator. The 'Delay' block ensures that all the switches are connected properly for the new bit and that the DAC has sufficient time to settle to the corresponding voltage before the comparison begins. Once all 12 bits are determined, the End-of-Conversion (EoC) signal is pulled up and remains high until the sampling clock becomes high again.

Since the asynchronous SAR ADC functions at a much faster internal clock, the conversion is finished in ~800 ns and consumes an average current of 213 μA during this time. Once the conversion is finished, only 31.7 μA current is consumed due to the resistive string for the 5-bit DAC for the remaining clock cycle. Once the 'hold' state is over, and the ADC clock becomes high again, the current path in the resistor string is cut, and the ADC only consumes 140 nA current. Therefore, the average current value for one complete conversion cycle is ~24.5 μA. Since the clock is gated during LPM, and the current path in the resistor string is opened using a switch and the ADC consumes little to no current.

C. Digital Logic and Memory

The digital logic block is one of the most important elements of the sensor chip. It generates the relevant clocks for the amplifier and the ADC blocks, along with all the other control signals used in the chip. It handles the communication and data transfer to and from the external MCU and the transition between different modes of operations (Functional Mode, Test Mode, Low Power Mode). The digital block contains several registers that act as the on-chip memory. These registers store trimming information, offset values for calibration, and the ADC output data before it is ready to be sent to the MCU via the I2C data transmission protocol. A serial protocol is preferred in our design to minimise unnecessary routing between the chips in the array. However, the disadvantage of lower data transmission throughput is handled using a creative "snapshot" methodology for our tactile skin. This will be elaborated in detail in Section V. As the digital block contains all the memory registers and state-controlling logic, it is always 'ON' even when all analog blocks are in low power mode. The entire digital block consumes ~ 30 μA current.

V. Top Level Algorithm

Fig. 25 shows the top-level block diagram for the entire chip. It can be seen that all components of our design, i.e., the piezoresistive sensors, amplifier, ADC, and the digital and I2C logic blocks, are all integrated within the same chip. All chips in the final tactile sensing array will be connected using only an I2C bus. This makes the interface between the proposed tactile skin and the MCU purely digital and more robust against noise. The complete tactile skin patch targets a 60 Hz refresh rate (16.6 ms), similar to any standard touch-based application. As mentioned in the previous section, the data communication happens via a 400 kHz I2C clock. The MCU initiates the communication, and all the chips in the array act as targets that transmit data when polled by the MCU.

Four identical sensing structures (each containing four resistors oriented in various directions) are placed at different positions within the chip. This is done to provide additional information about the local stress gradients within each chip if needed. The complete sensing unit only consumes ~50 μA current because, at any given point in time, only one sensor resistor (of any one sense structure) is connected to the supply voltage. The sensed voltage is then sequentially transmitted to the amplifier and the ADC by changing the multiplexer select signals. Once the sensed voltages from all 16 resistors are measured and digitised, they are locally stored while offset compensation and preliminary on-chip data processing are performed. Only the maximum output values for each resistor orientation type (among all sense structures) are stored in the "Final Max" memory in a 16-bit format[6]. These four highest values (for R_0, R_{90}, R_{45} and R_{135} respectively) are then sent to the MCU during polling operation. This approach of locally filtering the data to send only the maximum values for each resistor direction helps to reduce data traffic and saves time and power if multiple sense structures are placed on the chip.

Fig. 26 shows the chip's data memory overview. We can see the "Offset" memory, which stores the values of all the resistors under "zero external stress". Similar to the trimming procedure in testing mode, the offset values can be measured for all resistors of the chip array once the tactile skin is assembled. The offset values are then stored locally and subtracted from all measured values during regular operation, and the corrected values are stored in another memory register. This can compensate for any unwanted stresses that may have been introduced during the assembly of the tactile skin. The digital logic and memory are unaffected when the chip goes into low-power mode. However, copies of all trimming and offset data should be stored in the MCU to prepare for cases when fluctuations in the power supply to the tactile skin may cause the memory registers to be corrupted. A special "Reset" mode is

[6]1 sign bit to differentiate between tensile or compressive stress + 11-bit ADC output + the 4-bit multiplexer information to show the location of the corresponding sense structure and the resistor of the "maximum" value that is stored. The least significant bit of the ADC is discarded to allocate space for the sign bit, providing us with more relevant information for our application.

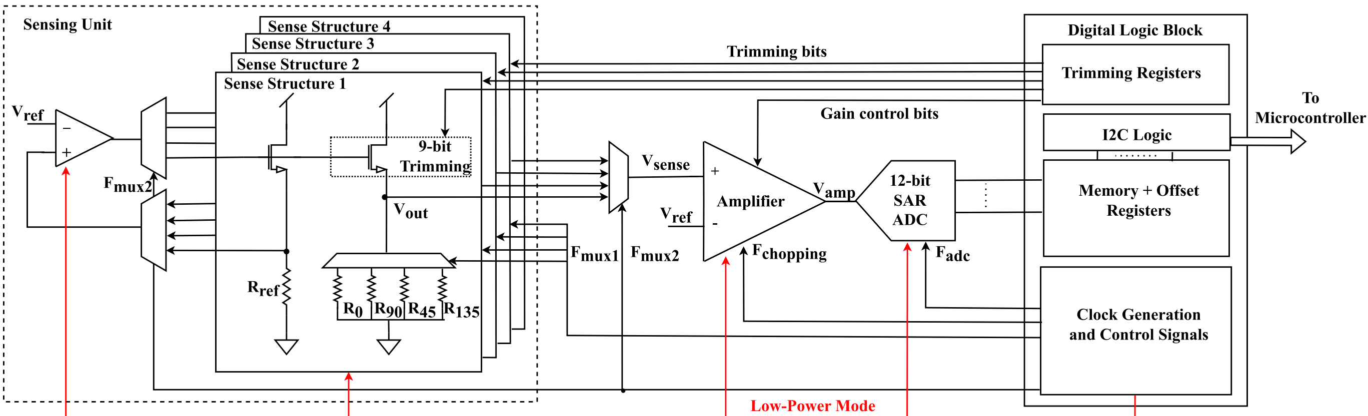

Fig. 25. Top-level block diagram of the complete stress sensor chip [35].

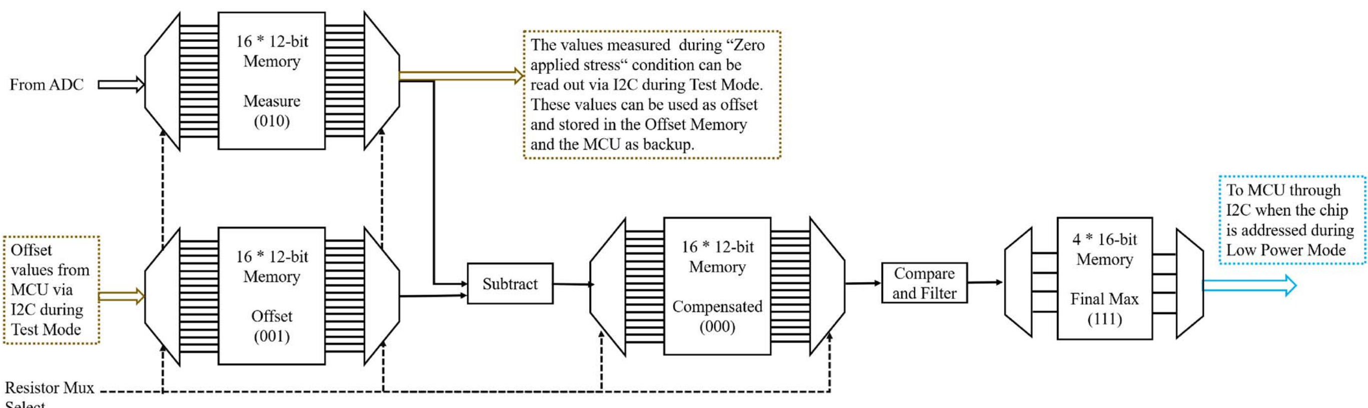

Fig. 26. Overview of the on-chip data and offset memory registers.

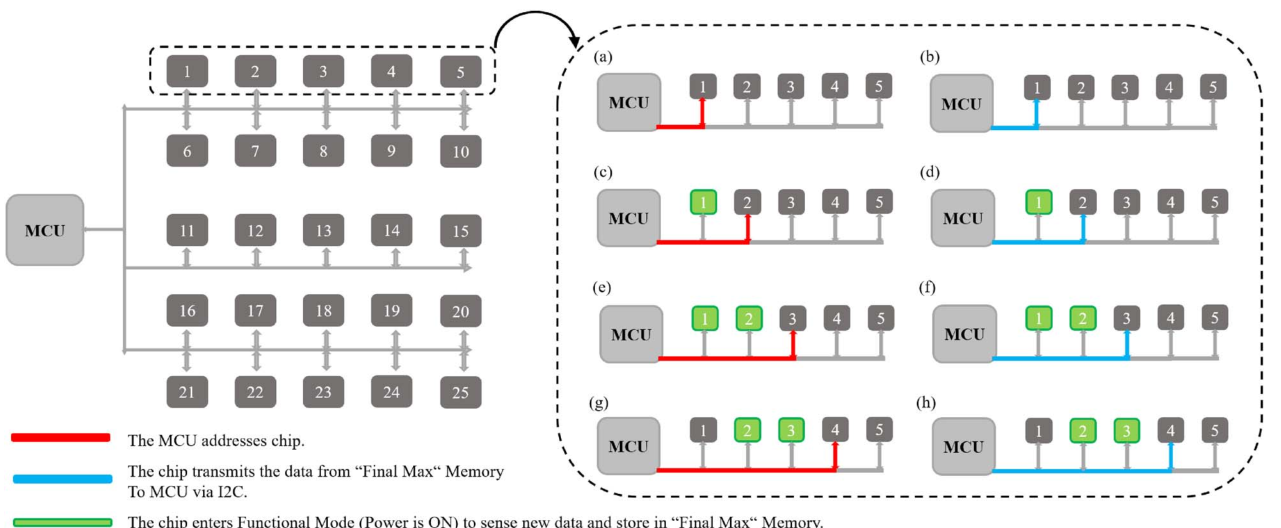

Fig. 27. Polling algorithm of the tactile array network (5 x 5). The tactile skin's refresh rate depends only on the time taken for data transmission (shown in blue) and the number of chips connected in the array.

specially designed for such a scenario, where the relevant data backup can be restored one by one in all array chips via the I2C bus.

Fig. 27 represents the polling algorithm between the MCU and the tactile sensing array. The chips of the array are in a default LPM. When the MCU addresses a chip, the chip first

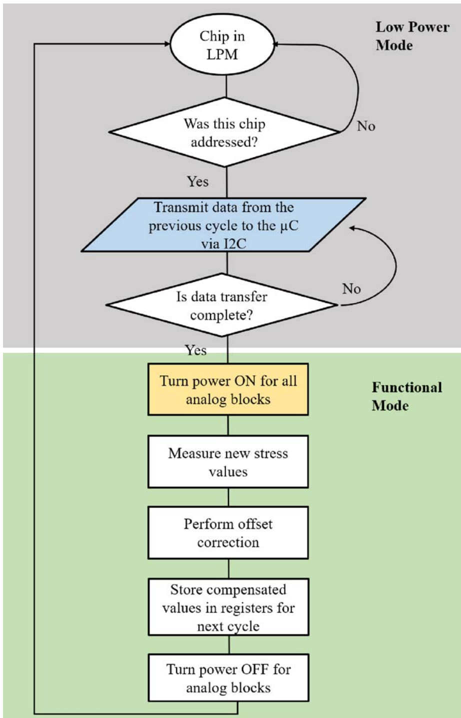

Fig. 28. The sensing and data transmission process flow for a single chip in the tactile sensing array.

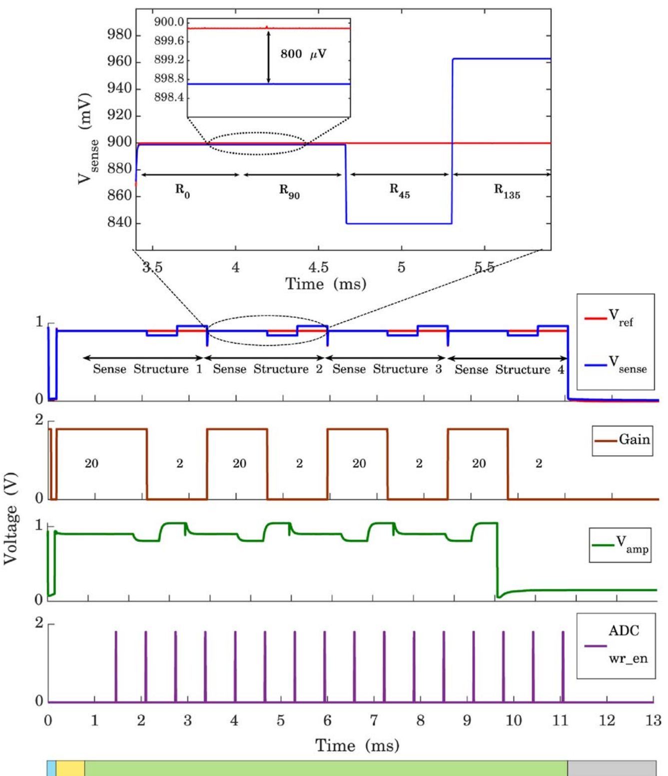

Fig. 29. Simulation waveforms for a complete sensing cycle on-chip under a 100 MPa tensile stress is applied in 45° direction. The colour legend at the bottom denotes the chip's operation state corresponding to Fig. 28.

transmits the data stored in the final max memory. After the data transmission is over, the MCU moves on to the next chip in the array while the current chip enters the functional mode to begin new sensor measurement and storage for the next polling cycle. It returns to the LPM once new sensor data overwrites the final max memory (Fig. 28). This "send-first, sense-later" approach has many advantages; firstly, the MCU can collect data from the chips successively without waiting for each one to start and finish sensing after being polled. Therefore, this significantly relaxes the performance specifications for each analog block within a chip. Secondly, this means that the speed of the tactile skin is limited by the time taken for data transmission rather than the time needed for sensing. The I2C protocol used for our design operates with a 400 kHz clock and takes ≤ 450 μs to transmit all the relevant data from one chip. That limits the network size to 36 chips for a 60 Hz refresh rate. Larger patches of tactile skin can be divided into sub-sections of 36 chips each, and the data can be collected simultaneously using MCUs that can support multiple parallel I2C protocols. Another way to increase the network size would be to use parallel data transfer protocols or serial protocols with higher data transfer rates. However, these solutions come at the cost of denser wire routing in the tactile skin or higher power consumption, respectively.

This method is called a "snapshot" approach because the data collected by the MCU corresponds to an older stress value and not the real-time measurement. The MCU, therefore, receives data with a one-cycle latency. This drawback, however, poses no challenge for low-speed applications where "touch" ordinarily lasts longer than a few milliseconds and the stress values sensed by the chips between two consecutive polling cycles of the MCU are not expected to vary.

VI. Simulation Results and Discussion

Fig. 29 shows the simulation results for one complete measurement cycle of our stress sensor chip when a tensile stress of 100 MPa was applied in a 45° direction. As stated in the previous sections, the chip is in a default LPM. Once the MCU polls the chip, it transmits the data stored in its output registers and starts the sensing operation. As seen from Fig. 29, it takes roughly 300 μs for the chip to go from LPM into functional mode. This time is allotted to ensure all the analog blocks can reach their steady-state operating points before actual sensing begins. Once the chip enters the functional mode, it cycles through all resistors in the chip at a frequency of 1.5625 kHz. The adaptive gain of the amplifier is controlled by setting the values of the gain bits to compensate for the lower stress sensitivity in some directions. The amplifier output is then digitised and stored in the on-chip register memory. The ADC output is only written into the memory when the 'ADC wr_en' signal is high. This signal is generated by the digital logic just before the multiplexer switches to the following sense resistor. This prevents unnecessary power consumption by overwriting the same memory register multiple times for a single resistor and only stores the digital data corresponding to the fully stabilised amplifier output. Finally, once all 16 resistors

TABLE II
PERFORMANCE COMPARISON WITH PRIOR ART

	This Work* **2024**	Allinger [47] 2023	Nurmetov [44] 2020	Ramirez [48] 2018	Mahsereci [32] 2016
Process	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.6 μm CMOS	0.5 μm CMOS
Sensor Type	n-doped piezoresistors	piezoFETs	n & p-type piezoresistors	piezoresistors	piezoFETs
Stress Sensors	16	32	7	8	4
Silicon area[a]	0.739 mm^2	5 mm^2	0.46 mm^2 w/o digital	-	21.16 mm^2
Sensitivity	2-bit adjustable upto 12 mV/MPa	4-bit adjustable upto 16.1 mV/Mpa	0.3 mV/MPa	-	12 nA/MPa (NMOS) 17 nA/MPa (PMOS)
Resolution	11-bit 48 kPa/LSB	12-bit 11 kPa/LSB	11-bit 175 kPa/LSB	no adc	10-bit 600 kPa/LSB
Stress Range	-100 MPa to 100 MPa	-22.53 MPa to 22.53 MPa[b]	-100 MPa to 360 MPa	5 to 65 MPa	-200MPa to 350 MPa
Stress Direction	$< 1^\circ$	in-plane & shear only	$\pm 3^\circ$	$< 5^\circ$	$\pm 2^\circ$
Offset Compensation	digital + chopping	analog	no	no	no
Thermal Compensation	analog	analog	analog + digital	analog	no
Power Consumption of complete chip	540 μW (Functional) 54 μW (LPM)	1.28 mW	357 μW (only analog)	-	1.5 mW (only analog)

* based on simulations only. The variability has been estimated using Monte Carlo simulations and may differ slightly in experimental silicon.
[a] chip core area for complete design.
[b] corresponding to the above resolution.

are sensed, the chip goes back to LPM until addressed again by the MCU.

It is pretty easy to determine the direction of the applied stress by observing the resistors with the highest V_{sense} magnitude (45° and 135°). The decision of whether the stress was tensile in 45° or compressive in 135° can be made by observing the values of the other two resistors (0° and 90°). Since the values for the 0-90 resistors are both below V_{ref} (i.e., corresponding to tensile stress), it can be safely concluded that the stress sensed by the chip is tensile, and is applied at a 45° direction. One can develop a simple algorithm for data processing that can perform similar analyses based on the 11 digital bits for magnitude and the first sign bit for the type of stress to further simplify the interpolation steps to determine the contact location. The precise stress magnitude and direction can be calculated using the formulae presented in Section III-A.

One complete measurement cycle takes roughly 10.2 ms (2.55 ms per sense structure) and consumes an average current of 300 μA during simulations. This value falls to $\sim$30 μA (corresponding to the digital logic and memory) during the LPM. The time taken for sensing is below 16.67 ms, and hence, each chip has new data stored and ready for transmission before the MCU can poll it again, thereby meeting the 60 Hz refresh rate specification set for the tactile skin. Based on the sequential polling method and the time taken by each chip for complete measurement, only 60% of the entire array network will be in high current-consuming functional mode at any given time. Hence, the average power consumed by the tactile skin patch (5 x 5) will be 4.5 mA. This range of operating current relaxes the resistance requirements for the power supply lines for the array, which, combined with the sparse placement of chips in the array, should not result in any significant heating. Furthermore, the superior thermal properties of the PI foil used as the substrate should ensure that the tactile skin can withstand these current values for prolonged and repeated measurements. It should be noted that this value does not include the power consumption during data transfer via I2C.

VII. CONCLUSION AND FUTURE SCOPE

This work presents the concept behind an array-based flexible tactile skin using fully CMOS stress sensor chips. The system-level concept for our proposed tactile skin assembly is optimised and verified using COMSOL simulations. The specifications for the sensor chip are derived from the expected top-level tactile skin specifications for our targeted application in prostheses. A simple "snapshot"-based data collection algorithm is proposed and discussed to relax the design specifications of the sensor chips and make the overall system response time faster and closer to a human-like response. Finally, we demonstrated the simulation behaviour of our designed CMOS touch sensor, which shows high-stress sensitivity and a large input dynamic range because of the designed low-noise adaptive gain amplifier.

Table II presents a comparison of our proposed sensor design with the current literature based purely on CMOS designs. The specifications mentioned in the table are for a single chip and not for the complete proposed tactile skin. Our design can achieve a resolution of up to $\sim$48 kPa/LSB (11-bit, as we discard the LSB to make space for the sign bit) and a sensitivity of up to 12 mV/MPa (using variable gain of the amplifier). Although it is less than what is reported in [47], our chip can resolve precise stress directions, which is a current limitation of their work. Our design also has a lower power consumption than the other designs. The active power is slightly higher compared to [44]; however, our design shows a higher sensitivity due to the adaptive gain amplifier and includes additional noise and offset cancellation techniques such as chopping. The overall current consumption of our proposed chip is still lower than the other mentioned literature, and the presence of a low-power mode makes our design superior for high-sensitivity and low-power applications.

The next step in this research includes experimental verification of the sensor chip and the flexible skin network under applied stress. Further work may also include sophisticated processing algorithms to locate the point of contact from the network data. Frequent data collection by the MCU during long periods of no contact can be reduced by changing the polling-based data collection to an event-driven one. However, that would involve using a different data transmission protocol that allows the target devices to initiate communication.

Another way to reach a compromise would be to use a combination of sensors in the tactile skin. One can include sparsely distributed wide-range, low-resolution proximity sensors in the tactile skin. In the default state, the MCU would only poll the proximity sensors at a lower sampling rate. This would reduce the collected data and lower the power consumption by keeping the stress sensor chips in the LPM. Once the proximity sensors detect an approaching object, the MCU resumes the regular polling-based operation with the high-sensitivity stress sensors. Such a combination of dual sensors could provide an ideal compromise between the saving power by allowing the network to go into a no-sensing state when no external object interactions are expected and keeping the tactile skin “alert” to react to any change in stimuli when needed.

The proposed design can be customised based on the target application requirements, while the general principle remains the same. The design offers a great scope of optimisation and can help to bridge the gap between artificial skin and human-like sensitivity and comfort in the coming times.

ACKNOWLEDGMENT

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REFERENCES

[1] S. Mashimo, E. Nakatsu, T. Aoki, and K. Matsuo, “Attenuation and distortion of a compression wave propagating in a high-speed railway tunnel,” *JSME Int. J. Ser. B*, vol. 40, no. 1, pp. 51–57, 1997, doi: 10.1299/jsmeb.40.51.

[2] E. Akdoğan, and M. H. Demir, “Rehabilitation technologies: Biomechatronics point of view,” in *A Roadmap of Biomedical Engineers and Milestones*. London, UK: IntechOpen, 2012.

[3] A. R. C. Donati et al., “Long-term training with a brain-machine interface-based gait protocol induces partial neurological recovery in paraplegic patients,” *Sci. Rep.*, vol. 6, no. 1, Aug. 2016, Art. no. 30383, doi: 10.1038/srep30383.

[4] T. Beyrouthy, S. K. Al Kork, J. A. Korbane, and A. Abdulmonem, “EEG mind controlled smart prosthetic arm,” in *Proc. IEEE Int. Conf. Emerg. Technol. Innovative Bus. Practices Transformation Societies (EmergiTech),* Balaclava, Mauritius, 2016, pp. 404–409, doi: 10.1109/EmergiTech.2016.7737375.

[5] M. Capogrosso et al., “A brain–spine interface alleviating gait deficits after spinal cord injury in primates,” *Nature*, vol. 539, no. 7628, pp. 284–288, Nov. 2016, doi: 10.1038/nature20118.

[6] H. Lorach et al., “Walking naturally after spinal cord injury using a brain–spine interface,” *Nature*, vol. 618, pp. 126–133, May 2023, doi: 10.1038/s41586-023-06094-5.

[7] A. Selfslagh et al., “Non-invasive, brain-controlled functional electrical stimulation for locomotion rehabilitation in individuals with paraplegia,” *Sci. Rep.*, vol. 9, no. 1, May 2019, doi: 10.1038/s41598-019-43041-9.

[8] Z. Tayeb et al., “Validating deep neural networks for online decoding of motor imagery movements from EEG signals,” *Sensors*, vol. 19, no. 1, Jan. 2019, Art. no. 210, doi: 10.3390/s19010210.

[9] S. Nayak and R. Kumar Das, “Application of artificial intelligence (AI) in prosthetic and orthotic rehabilitation”, *Service Robotics*. London, UK: IntechOpen, Nov. 26, 2020, doi: 10.5772/intechopen.93903.

[10] R. S. Dahiya, P. Mittendorfer, M. Valle, G. Cheng, and V. J. Lumelsky, “Directions toward effective utilization of tactile skin: A review,” *IEEE Sensors J.*, vol. 13, no. 11, pp. 4121–4138, Nov. 2013, doi: 10.1109/JSEN.2013.2279056.

[11] L. Li et al., “Flexible pressure sensors for biomedical applications: From ex vivo to in vivo,” *Adv. Mater. Interfaces*, vol. 7, no. 17, Jul. 2020, Art. no. 2000743, doi: 10.1002/admi.202000743.

[12] N. Yogeswaran et al., “New materials and advances in making electronic skin for interactive robots,” *Adv. Robot.*, vol. 29, no. 21, pp. 1359–1373, Nov. 2015, doi: 10.1080/01691864.2015.1095653.

[13] A. Hari M and L. Rajan, “Advanced materials and technologies for touch sensing in prosthetic limbs,” *IEEE Trans. Nanobiosci.*, vol. 20, no. 3, pp. 256–270, Jul. 2021, doi: 10.1109/TNB.2021.3072954.

[14] J. C. Costa, F. Spina, P. Lugoda, L. Garcia-Garcia, D. Roggen, and N. Münzenrieder, “Flexible sensors—From materials to applications,” *Technologies*, vol. 7, no. 2, Apr. 2019, Art. no. 35, doi: 10.3390/technologies7020035.

[15] G. Cheng, E. Dean-Leon, F. Bergner, J. Rogelio Guadarrama Olvera, Q. Leboutet, and P. Mittendorfer, “A comprehensive realisation of robot skin: Sensors, sensing, control, and applications,” *Proc. IEEE*, vol. 107, no. 10, pp. 2034–2051, Oct. 2019, doi: 10.1109/JPROC.2019.2933348.

[16] R. S. Dahiya, G. Metta, M. Valle, and G. Sandini, “Tactile sensing—From humans to humanoids,” *IEEE Trans. Robot.*, vol. 26, no. 1, pp. 1–20, Feb. 2010, doi: 10.1109/TRO.2009.2033627.

[17] H. Heidari, N. Wacker, S. Roy and R. Dahiya, “Towards bendable CMOS magnetic sensors,” in *Proc. 11th Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Glasgow, U.K., 2015, pp. 314–317, doi: 10.1109/PRIME.2015.7251398.

[18] J. N. Burghartz, C. Harendt, T. Hoang, A. Kiss and M. Zimmermann, “Ultra-thin chip fabrication for next-generation silicon processes,” in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Capri, Italy, 2009, pp. 131–137, doi: 10.1109/BIPOL.2009.5314128.

[19] R. S. Dahiya and S. Gennaro, “Bendable ultra-thin chips on flexible foils,” *IEEE Sensors J.*, vol. 13, no. 10, pp. 4030–4037, Oct. 2013, doi: 10.1109/JSEN.2013.2269028.

[20] N. Wacker et al., “Stress analysis of ultra-thin silicon chip-on-foil electronic assembly under bending,” *Semicond. Sci. Technol.*, vol. 29, no. 9, Aug. 2014, doi: 10.1088/0268-1242/29/9/095007.

[21] H. Heidari, N. Wacker, and R. Dahiya, “Bending induced electrical response variations in ultra-thin flexible chips and device modelling,” *Appl. Phys. Rev.*, vol. 4, no. 3, Sep. 2017, Art. no. 031101, doi: 10.1063/1.4991532.

[22] D. A. van den Ende et al., “Mechanical and electrical properties of ultra-thin chips and flexible electronics assemblies during bending,” *Microelectron. Rel.*, vol. 54, no. 12, pp. 2860–2870, Dec. 2014, doi: 10.1016/j.microrel.2014.07.125.

[23] C. Harendt et al., “Hybrid systems in foil (HySiF) exploiting ultra-thin flexible chips,” *Solid-State Electron.*, vol. 113, pp. 101–108, Nov. 2015, doi: 10.1016/j.sse.2015.05.023.

[24] Y. Kanda, “Piezoresistance effect of silicon,” *Sensors Actuators A Physical*, vol. 28, no. 2, pp. 83–91, Jul. 1991, doi: 10.1016/0924-4247(91)85017-i.

[25] C. S. Smith, “Piezoresistance effect in germanium and silicon,” *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954, doi: 10.1103/physrev.94.42.

[26] Y. Kanda, “A graphical representation of the piezoresistance coefficients in silicon,” *IEEE Trans. Electron. Devices*, vol. 29, no. 1, pp. 64–70, Jan. 1982, doi: 10.1109/T-ED.1982.20659.

[27] K. Matsuda, Y. Kanda, K. Yamamura, and K. Suzuki, “Nonlinearity of piezoresistance effect in p- and n-type silicon,” *Sensors Actuators A Phys.*, vol. 21, no. 1–3, pp. 45–48, Feb. 1990, doi: 10.1016/0924-4247(90)85008-r.

[28] S. Yang, D. Wu, Z. Wang, and X. Li, “A CMOS stress sensor chip with integrated signal processing circuits,” in *Proc. IEEE SENSORS*, Busan, *Korea (South)*, 2015, pp. 1–4, doi: 10.1109/ICSENS.2015.7370233.

[29] M. Kuhl, P. Gieschke, O. Paul, and Y. Manoli, “A differential difference amplifier with automatic gain selection as readout interface for CMOS stress sensors in orthodontic brackets,” in *Proc. 16th Int. Solid-State

Sensors, Actuators Microsyst. Conf., Beijing, China, 2011, pp. 819–822, doi: 10.1109/TRANSDUCERS.2011.5969177.

[30] Z. Yu, C. Scherjon, Y. Mahsereci, and J. N. Burghartz, "A new CMOS stress sensor ratiometric readout for in-plane stress magnitude and angle detection," in *Proc. IEEE SENSORS*, Glasgow, U.K., 2017, pp. 1–3, doi: 10.1109/ICSENS.2017.8234135.

[31] M. O. Kayed, A. A. Balbola, and W. A. Moussa, "A new temperature transducer for local temperature compensation for piezoresistive 3-D stress sensors," *IEEE/ASME Trans. Mechatron.*, vol. 24, no. 2, pp. 832–840, Apr. 2019, doi: 10.1109/TMECH.2019.2891069.

[32] Y. Mahsereci, S. Saller, H. Richter, and J. N. Burghartz, "An ultra-thin flexible CMOS stress sensor demonstrated on an adaptive robotic gripper," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 273–280, Jan. 2016, doi: 10.1109/JSSC.2015.2498183.

[33] P. Gieschke, Y. Nurcahyo, M. Herrmann, M. Kuhl, P. Ruther, and O. Paul, "CMOS integrated stress mapping chips with 32 N-type or P-type piezoresistive field effect transistors," in *Proc. IEEE 22nd Int. Conf. Micro Electro Mech. Syst.*, Sorrento, Italy, 2009, pp. 769–772, doi: 10.1109/MEMSYS.2009.4805496.

[34] U. Nurmetov, "Design of a fully CMOS compatible mechanical stress sensor," Ph.D. diss., Tech. Univ. Munich, Munich, Germany, 2021.

[35] V. Verma, V. Haberhauer, D. Petrić, A. N. I. Torrent, and R. Brederlow, "Silicon-based CMOS stress sensors for tactile perception based smart skin for prostheses," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Toronto, ON, Canada, 2023, pp. 1–5, doi: 10.1109/BioCAS58349.2023.10388689.

[36] S. Timoshenko and S Woinowsky-Krieger, *Theory of Plates and Shells*. Vol. 2. New York, NY, USA: McGraw-Hill, 1959.

[37] C. Landesberger et al., "Novel processing scheme for embedding and interconnection of ultra-thin IC devices in flexible chip foil packages and recurrent bending reliability analysis," in *Proc. Int. Conf. Electron. Packag. (ICEP)*, Hokkaido, Japan, 2016, pp. 473–478, doi: 10.1109/ICEP.2016.7486872.

[38] N. Palavesam, C. Landesberger and K. Bock, "Investigations of the fracture strength of thin silicon dies embedded in flexible foil substrates," in *Proc. IEEE 20th Int. Symp. Des. Technol. Electron. Packag. (SIITME)*, Bucharest, Romania, 2014, pp. 267–271, doi: 10.1109/SIITME.2014.6967042.

[39] M. H. Malik, G. Grosso, H. Zangl, A. Binder, and A. Roshanghias, "Flip chip integration of ultra-thinned dies in low-cost flexible printed electronics; The effects of die thickness, encapsulation and conductive adhesives," *Microelectron. Rel.*, vol. 123, Aug. 2021, Art. no. 114204, doi: 10.1016/j.microrel.2021.114204.

[40] "Ultra heat-resistant Polyimide Films, UPILEX-S," UBE Corporation. [Online]. Available: Available: https://www.ube.com/upilex/catalog/pdf/upilex_s_e.pdf

[41] F. Fruett and G. C. M. Meijer, *The Piezojunction Effect in Silicon Integrated Circuits and Sensors*, vol. 682. New York, NY, USA: Springer-Verlag, 2002.

[42] C.-H. Cho, R. C. Jaeger, and J. C. Suhling, "Characterisation of the temperature dependence of the piezoresistive coefficients of silicon from $-150\,°C$ to $+125\,°C$," *IEEE Sensors J.*, vol. 8, no. 8, pp. 1455–1468, Jul. 2008, doi: 10.1109/jsen.2008.923575.

[43] C. Liu, Foundations of MEMS, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2012.

[44] U. Nurmetov et al., "A CMOS temperature stabilized 2-D mechanical stress sensor with 11-bit resolution," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 846–855, Apr. 2020, doi: 10.1109/JSSC.2020.2967554.

[45] R. Burt and J. Zhang, "A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2729–2736, Dec. 2006, doi: 10.1109/JSSC.2006.884195.

[46] X. Y. Tong, Z. M. Zhu, Y. T. Yang, and L. X. Liu, "D/A conversion networks for high-resolution SAR A/D converters," *Electron. Lett.*, vol. 47, no. 3, pp. 169–169, Jan. 2011, doi: 10.1049/el.2010.3469.

[47] K. Allinger and M. Kuhl, "A closed-loop 12bit CMOS-integrated stress sensor system with 4bit adjustable sensitivity from 178 to 11 kPa/LSB at up to 22.5kS/s and 5bit dynamic range adjustment," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2023, pp. 1–3, doi: 10.1109/ISSCC42615.2023.10067788.

[48] J. L. Ramirez and F. Fruett, "Integrated octagonal mechanical stress sensor with temperature compensation," *IEEE Sensors J.*, vol. 18, no. 14, pp. 5707–5714, Jul. 2018, doi: 10.1109/JSEN.2018.2843534.

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