Multilevel Limit Cycle Oscillator for Synchronizing Grid Connected Inverters in Fault Ride-Through Applications

Erick Vázquez, Javier Roldán-Pérez, *Senior Member, IEEE*, and Milan Prodanovic, *Senior Member, IEEE*

***Abstract*—Grid synchronization algorithms are important in control systems of power electronic converters. These algorithms must ensure proper synchronization even in the case of disturbances such as voltage-sags and phase-jumps, which are common in high-voltage and low-voltage ride-through applications. Therefore, the development of robust synchronization algorithms in these situations is of interest. In this article, a nonlinear synchronization algorithm suitable for application in grid-following inverters operating under fault ride-through conditions is proposed. This algorithm is called multilevel limit cycle oscillator frequency-locked loop (MLCO-FLL), and it is used as a pre-filter for a synchronous reference frame phase-locked loop (SRF-PLL). This algorithm is robust against phase-jumps and variations in the voltage, both representing important features for fault ride-through applications. Also, it automatically detects the operation at different voltage levels without state machines or logic conditions. These features might be of interest in other research fields, where the detection of orbits is important. A comparison with other linear and nonlinear synchronization algorithms showed that MLCO-FLL features important advances. Moreover, in future, it is possible to improve its performance once its characteristics and parameters are examined in detail. Simulations and experimental results obtained from a 15 kW inverter connected to a grid-emulator were used to validate the MLCO-FLL.**

***Index Terms*—Frequency-locked loop (FLL), grid synchronization, limit cycle oscillator, multilevel limit cycle oscillator (MLCO).**

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I. Introduction

In response to the increased penetration of grid-connected distributed generators (DGs), many countries are requesting grid-support services from DGs, both in steady-state and during fault conditions. The most common services are high/low voltage ride-through (HVRT-LVRT) capability, voltage and frequency support and reactive power regulation [1], [2]. Fast variations in the amplitude of the grid voltage are common and mainly appear due to the actions of electrical protections after grid faults [3]. These variations greatly affect the synchronization of power inverters and are more severe in the case of aggressive phase jumps. Grid codes that are now being developed around the world force renewable generators to remain connected to the grid in the case of voltage disturbances [4]. For instance, in many countries, converter-interfaced generators should remain connected to the grid and work properly if the voltage fluctuates between 0.9 and 1.1 pu. Outside this range, these generators should also remain connected for a period of time that depends on the type and depth of the sag [5]. For instance, according to the Australian grid code [6], wind generators should remain connected even in the case of severe sags and swells, and the disconnection time is described as a function of the fault duration. Active and reactive power (or current) compensation curves during sags are also provided in grid codes. It is commonly requested to limit the active power injection while providing additional reactive power to rise the grid voltage. In some cases, it is also requested to inject some specific profiles of negative-sequence components [7]. The implementation of control strategies to fulfill the grid code is complex as the requirements are becoming increasingly demanding and the converters have many inherent limitations (current, voltage, etc.) [8]. In particular, current and power controllers should operate adequately under balanced and unbalanced voltage conditions. Meanwhile, synchronization algorithms must be fast and robust against unbalances, harmonics, frequency variations, and phase jumps [9].

The requirements mentioned before imply that generators should have both LVRT and HVRT capability. To guarantee these capabilities, the control system of converter-interfaced generators needs to use adequate frequency, phase, and voltage [10]. This can be achieved by using state machines and logic operations that switch between algorithms depending on the

grid voltage levels. Therefore, hybrid control systems based on decision-making blocks, together with voltage and/or frequency estimation loops are common in the literature. For example, algorithms based on a phase-locked loop (PLL) [11], [12], a second-order generalized integrator frequency-locked loop (SOGI-FLL) [13] or delayed signal cancellation (DSC) blocks [14] have already been applied to deal with LVRT and HVRT scenarios. However, the stability implications of such changes in the control system are difficult to analyze because the dynamic equations are based on piece-wise nonlinear systems [15], [16]. For this reason, the development of synchronization algorithms capable of remaining synchronised even during extreme events is of interest and limit cycle oscillators (LCOs) have favorable properties with this respect.

Symmetrical oscillators such as stable LCOs are an emerging topic in engineering applications. These oscillators can be applied to model systems that exhibit self-sustained stable oscillations [17]. These dynamic processes are intrinsically nonlinear and oscillate with a predefined amplitude, shape, and frequency. Also, if the system is disturbed by an exogenous signal, the trajectory will come back to its original stable limit cycle (SLC) [18]. Linear oscillators also have closed orbits. However, their amplitude is defined by the initial conditions and any disturbance will change its value, inevitably. This does not happen in LCOs due to their internal structure [17].

There exist different types of limit cycles and the main difference between them is the shape of the periodic waveforms. The best known LC is the van der Pol oscillator, which produces a waveform that contains fundamental and harmonic components [17]. This oscillator has been used for synchronizing power converters several times [19], [20]. However, there are other types of oscillators that can also be used for synchronization purposes. In particular, those having circular symmetry are of interest since they do not introduce harmonic distortion [21], [22], [23]. For instance, the LCO-FLL in [23] has a high degree of immunity and robustness against sags, swells, phase-frequency shifts, and harmonics. However, it needs additional calculations to detect fault conditions. This limitation could be fixed by expanding the number of stable circular limit cycles so that the trajectory switches between them, automatically, when the level of the input voltage changes.

Sustained oscillations of different amplitudes sometimes appear in dynamic processes and are commonly called multilevel limit cycles (MLCs) [24], [25], [26], [27]. Some studies have found MLCs in H-Bridges controlled with the zero-current switching control strategy [24] and in power converters with sliding-mode control [25]. However, in these cases, MLCs are considered as an undesired side-effect. In fields of applied mathematics not related to power conversion, Galias and Tucker [26] found that some specific nonlinear systems have four limit cycles. Some other works have found an even larger number of limit cycles in other mathematical models [27]. Therefore, it is clear that MLCs appear sporadically in some systems. However, as far as the authors know, there are no works related to their synthesis and application. As a consequence, the literature on this specific topic is scarce. A few works related to the synthesis of MLCs have been developed in other research fields, such as predator-pray models [28] or distributed network models of neuronal oscillators [29]. However, MLCs have not been applied for synchronizing power converters in FRT applications.

In this article, a method for synchronizing power converters in FRT applications based on synthetic MLCs is presented. Thanks to its nonlinear properties, the MLCO-FLL remains synchronized with the grid even in the case of large disturbances, such as voltage sags and phase jumps. Also, it features voltage sag detection without additional logic conditions. Even though this can be done using additional logic conditions in traditional PLLs, it is a novel feature that might be of interest for other applications. For instance, it could be used to classify FRT scenarios according to the depth of voltage sags. The main differences with the LCO-FLL are: 1) The MLCO-FLL is a generalization of the LCO-FLL and it has more degrees of freedom (since it has more than one limit cycle). 2) The MLCO-FLL has intrinsic hysteresis properties. 3) The attraction level of each LC is different. Even though the variation of the attraction level is not explored here, it is another degree of freedom that may be explored further in order to improve the algorithm performance. The MLCO-FLL includes a continuum switching model in a single control law, which is useful for generating current references in grid-following converters. By using this synchronization system, there is no need to switch between synchronization algorithms even in the case of large disturbances, such as severe voltage sags and swells [30]. It is shown that this synchronization algorithm can be used together with a dual reference frame controller (DSRF) [9], [31] and work properly during balanced and unbalanced voltage sags.

The rest of the article is organized as follows. In Section II, the structure of the MLC is proposed and a FLL is added to deal with frequency variations. Numerical and experimental results are presented in Sections III and IV, respectively. A comparison between the MLCO-FLL and other linear and nonlinear synchronization algorithms is presented in Section V. Finally, the conclusions are drawn in Section VI.

II. Model of an MLCO

A SLC is a type of dynamic process with two dimensions. In a limit cycle, the trajectories of the states converge to a closed orbit as time tends to infinity. An isolated periodic orbit emerges from this process and it is commonly called limit cycle [18]. A nonlinear self-sustained sinusoidal oscillator with this property can be represented by a second-order dynamic system in polar coordinates [23]

$$\dot{r} = \omega r \left(1 - \frac{r^2}{A^2}\right) \tag{1a}$$

$$\dot{\theta} = -\omega \tag{1b}$$

where ω is the angular frequency, r is the radius of the oscillation and A is the peak amplitude of r.

The differential (1a) has three equilibrium points: two of them are stable ($r^* = \pm A$) while the other one is unstable ($r^{**} = 0$). For simplicity, it will be assumed that $r > 0$ in the rest of the article. Fig. 1(a) shows the vector field of (1). It can be seen that the entire vector field points to a drain in $r = A$

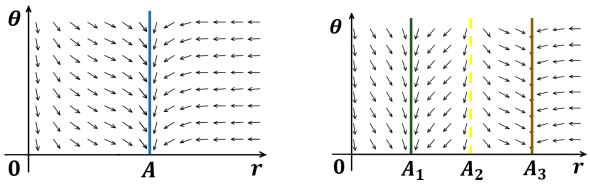

Fig. 1. (a) Vector field of an LCO in polar coordinates (A: Blue line). (b) Vector field of an MLCO in polar coordinates, with two SLCs (A_1: green, A_3: brown) and one unstable limit cycle (A_2: yellow).

with a speed $-\omega$. Therefore, if $r < A$ then $\dot{r} > 0$, and if $r > A$ then $\dot{r} < 0$.

The dynamic system presented in (1) can be extended in order to include more equilibrium points

$$\dot{r} = \omega r \left(1 - \frac{r^2}{A_1^2}\right)\left(1 - \frac{r^2}{A_2^2}\right) ... \left(1 - \frac{r^2}{A_n^2}\right) \tag{2a}$$

$$\dot{\theta} = -\omega \tag{2b}$$

where every value of $A_{j=1,2,...,n}$ represents a fixed point of (2a), with $A_1 < A_2 < ... < A_n$. To understand these equations, the properties of the $n+1$ equilibrium points of (2a) can be inspected, for $r \geq 0$. To simplify the explanations, this will be done for a specific value of n and then generalized for $n+1$. For $n = 3$, (2) becomes

$$\dot{r} = \omega r \left(1 - \frac{r^2}{A_1^2}\right)\left(1 - \frac{r^2}{A_2^2}\right)\left(1 - \frac{r^2}{A_3^2}\right) \tag{3a}$$

$$\dot{\theta} = -\omega. \tag{3b}$$

The characteristics of fixed points can be studied with the partial derivative of (3a) with respect to r. At $r = 0$, the result is

$$\frac{\partial \dot{r}}{\partial r}_{r^*=0} = \underbrace{\omega}_{+}. \tag{4}$$

The sign of $\partial\dot{r}/\partial r$ in $r = 0$ is positive. This means that the fixed point is unstable. For $r = A_1$ the expression becomes

$$\frac{\partial \dot{r}}{\partial r}_{r^*=A_1} = -2\omega \underbrace{\left(1 - \frac{A_1^2}{A_2^2}\right)}_{+}\underbrace{\left(1 - \frac{A_1^2}{A_3^2}\right)}_{+}. \tag{5}$$

The sign of $\partial\dot{r}/\partial r$ in $r = A_1$ is negative, so the fixed point is stable. For $r = A_2$

$$\frac{\partial \dot{r}}{\partial r}_{r^*=A_2} = -2\omega \underbrace{\left(1 - \frac{A_2^2}{A_1^2}\right)}_{-}\underbrace{\left(1 - \frac{A_2^2}{A_3^2}\right)}_{+}. \tag{6}$$

The sign of $\partial\dot{r}/\partial r$ in $r = A_2$ is positive. Therefore, the fixed point is unstable. For $r = A_3$

$$\frac{\partial \dot{r}}{\partial r}_{r^*=A_3} = -2\omega \underbrace{\left(1 - \frac{A_3^2}{A_1^2}\right)}_{-}\underbrace{\left(1 - \frac{A_3^2}{A_2^2}\right)}_{-}. \tag{7}$$

The sign of (7) is negative. Consequently, the fixed point is stable. From the examples above, it is clear that there is a pattern in the nature of the equilibrium points (they alternate between stable and unstable fixed points). This pattern can be observed in Fig. 1(b). It can be seen that the direction of the vector field changes between fixed points. This pattern will be repeated even if n increases. Also, it can be observed that the vector field has a different shape in the surroundings of each limit cycle. This means the transient response of the output signal will be different depending on the input signal.

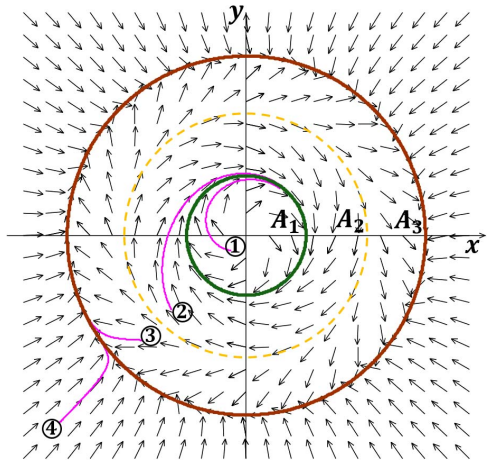

Fig. 2. Vector field of an MLCO with two stable limit cycles (A_1: green, A_3: brown) and one unstable limit cycle (A_2: yellow).

For convenience, (3) can written in Cartesian coordinates

$$\dot{x} = \left\{\left[x\left(1 - \frac{r^2}{A_1^2}\right) ... \left(1 - \frac{r^2}{A_3^2}\right)\right] + y\right\}\omega \tag{8a}$$

$$\dot{y} = \left\{\left[y\left(1 - \frac{r^2}{A_1^2}\right) ... \left(1 - \frac{r^2}{A_3^2}\right)\right] - x\right\}\omega \tag{8b}$$

where x and y are the Cartesian axes and $r^2 = x^2 + y^2$. The vector field of (8) is shown in Fig. 2. In that figure, it can be seen that the fixed points at values A_j (in (3)) turn into limit cycles with different values of A_j. In (8), two limit cycles are stable (represented in Fig. 2 in green and brown). There is one unstable limit cycle (yellow dashed line). Also, there is one unstable fixed point in the origin. Notice that the unstable limit cycle creates a boundary region between the region of attraction of the two SLCs (e.g., the yellow dashed line divides the region of attraction of the green and brown lines). These regions can be defined as follows:

$$\mathbb{R}_1 : \forall x, y \in D_{A_1} = \left\{0 < r < A_2,\ \omega > 0 \mid r^2 = x^2 + y^2\right\} \tag{9}$$

$$\mathbb{R}_3 : \forall x, y \in D_{A_3} = \left\{A_2 < r,\ \omega > 0 \mid r^2 = x^2 + y^2\right\}. \tag{10}$$

Fig. 2 shows how the unstable limit cycle divides attractive regions of stable limit cycles. For instance, for the initial conditions 1 and 2, which are contained in the domain (9), the trajectories are attracted to the stable limit cycle A_1. However, the initial conditions 3 and 4 contained in (10) are attracted to the stable limit cycle A_3. Therefore, by observing the vector field presented in Fig. 2, it is clear that (8) ensures a soft transient between any initial condition to any of the stable limit cycles. As a consequence, it can be demonstrated by the Poincare–Bendixson theorem [32] that (8) has two stable closed orbits

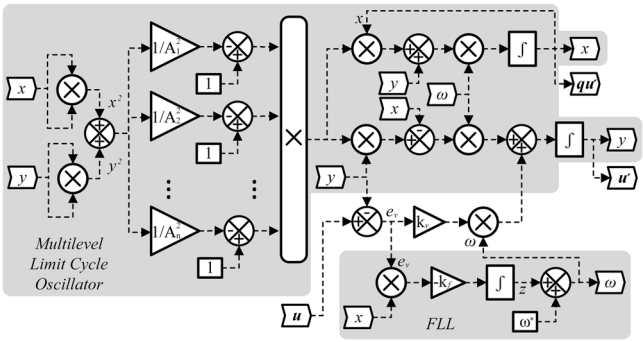

Fig. 3. Block diagram of the MLCO-FLL.

defined in the domains (9) and (10). Here, these are called stable limit cycle oscillators (green and brown orbits in Fig. 2). This result can be extended for the following set of SLCs

$$\text{SLC}: \left\{ a \in Z^+ / a = \frac{n+1}{2}, n \in Z^+ \right\} - \left\{ a \in Z^+ / a = 2n, n \in Z^+ \right\}. \quad (11)$$

This means that the MLC will have $(n+1)/2$ SLCs. In other words, (11) establishes that a stable MLC can be achieved with an odd number of limit cycles (n). In this case, the whole system will be stable. For instance, the MLCO depicted in Fig. 2 has three limit cycles. Among them, two are stable (A_1 and A_3) while one is unstable (A_2).

A. Frequency Adaptive MLCO-FLL

The MLCO presented in the previous section was not frequency adaptive. This problem can be solved by using an additional FLL linked with the frequency signal used by the LCO [23]. This frequency adaptive MLCO will be named MLCO-FLL. The dynamic equations of the MLCO-FLL are

$$\dot{x} = \left\{ \left[x \left(1 - \frac{r^2}{A_1^2}\right) \ldots \left(1 - \frac{r^2}{A_n^2}\right) \right] + y \right\} \omega \quad (12a)$$

$$\dot{y} = \left\{ \left[y \left(1 - \frac{r^2}{A_1^2}\right) \ldots \left(1 - \frac{r^2}{A_n^2}\right) \right] - x \right\} \omega + k_v \omega e_v \quad (12b)$$

$$\dot{z} = -k_f x e_v \quad (12c)$$

where k_v, $k_f \in R^+$ are gains that modulate the voltage error signal (e_v), which is defined as the difference between the input signal (u) and the synchronized signal (y), $(e_v = u - y)$. The angular frequency $\omega = z + \omega^*$ is defined by the sum of the angular frequency (z) and a constant (ω^*). As written in (12c), the FLL is the product of the constant gain k_f and two variables: the quadrature signal x and the voltage error e_v. More details on FLLs, their applications and similarities compared to PLLs can be found in [23], [33], [34]. Fig. 3 shows the implementation of the equations in (12). There are two main outputs, the quadrature signal $qu' = x$ and the signal $u' = y$, which is synchronized with the input u.

TABLE I
MLCO-FLL PARAMETERS FOR SIMULATIONS AND EXPERIMENTAL TESTS

Parameter	Value	Sim.	Exp.
ω^*, k_v, k_f (*)	90π, 1, $\sqrt{2}$	*	*
Number of LC (n)	3	*	*
A_1 (stable LC)	0.4 pu	*	*
A_2 (unstable LC)	0.7 pu	*	*
A_3 (stable LC)	1 pu	*	*
Input signal freq.	50 Hz	*	*
Volt. slope (first test)	2.1 pu/s	*	
Volt. range (first test)	(0.9 - 1.2) pu	*	
Volt. slope (second test)	-2.1 pu/s	*	
Volt. range (second test)	(1.2 - 0.3) pu	*	
Time (first, second test)	(0 - 550) ms	*	
(L_i, L_o)	(2.3, 1) mH		*
C_f	8.8 μF		*
k_p, k_i	2.43, $1.35 \cdot 10^3$		*
Sag for tests (a)-(b)	0.4 pu		*
Sag for test (c)	0.7-0.55-0.55 pu		*
Test(d): ω_{ref}, $K_{\omega p}$, $K_{\omega i}$	100π, 7.1, 16.4	*	

* Optimized according to the methodology in [35].

III. NUMERICAL RESULTS

1) Description of the Tests: The proposed MLCO-FLL shown in Fig. 3 was simulated in MATLAB-Simulink, first, without any connection to the rest of the control system in order to analyse its transient response. For this test, the order of the MLCO-FLL in (12) was set to $n = 3$ to show the performance of the synchronization system with two stable LCs. The parameters and gains of the MLCO-FLL used in the test are presented in Table I. Integrals were discretized by using the backward Euler rule and this gave adequate results as the sampling period was small enough. However, for slower sampling periods, a detailed discretization might be required [36]. The selection of the control gains was done according to the optimal procedure proposed in [35]. Therefore, the MLCO-FLL has one unstable equilibrium point in the origin, one unstable limit cycle (A_2), and two stable LCs (A_1, A_3). For the simulation tests the voltage reference (u) is a pure sinusoidal signal: $u = A_r \sin\theta_r$, where A_r and θ_r are the peak amplitude and the phase of the reference signal, respectively. In addition, the dynamic equation of the frequency should be described: $\dot{\theta}_r = -\omega_r$, where ω_r is the angular frequency ($2\pi 50$ rad/s in this work).

2) Amplitude Increment (First Test): For the first test, the amplitude of the voltage reference is gradually increased from $t = 0$ s to $t = 120$ ms. The rate of variation will be 2.1 pu/s, and from 0.9 to 1.2 pu. Fig. 4(a) shows the results of this case. It can be seen that the signal y of the MLCO (blue line) is in phase with the voltage reference signal (green line). As a consequence, their frequency is the same. It can be seen in an instant where there is a step between the LCs. This step can be clearly identified in Fig. 4(a), since there is a red arrow that points to it. The transition is also marked in Fig. 4(b) with a red arrow. The orbits resemble rings, and their center is always the origin of coordinates. It can be noticed that the step is produced in a smooth way. The stable LCs associated with A_1 and A_3 have the shape of "rings" in Fig. 4(b).

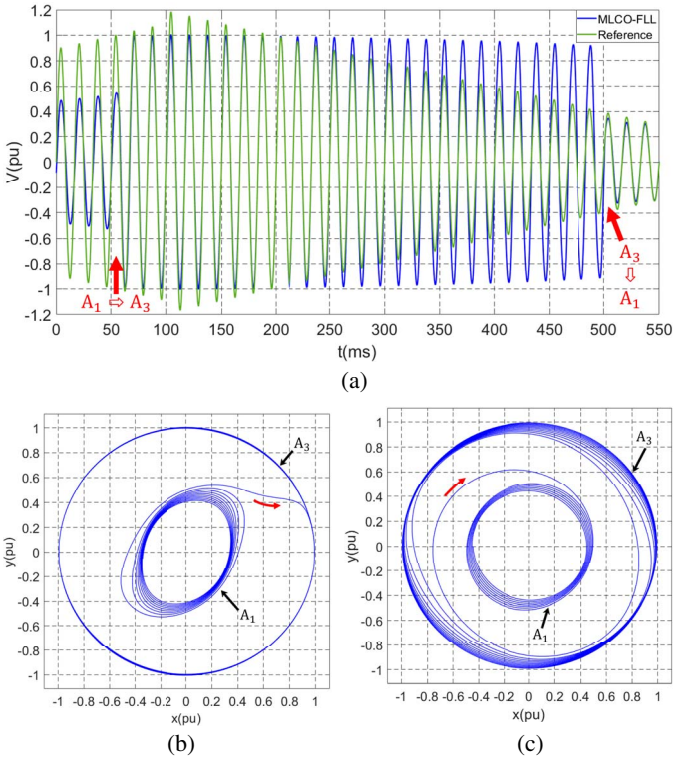

Fig. 4. MLCO-FLL dynamic performance ($n = 3$). Voltage variation from 0.12 to 2.1 pu. (a) Trajectory of MLCO-FLL (in blue) when the amplitude of the reference (in green) change with a slope of 2.1 pu/s. (b) Phase space trajectory, amplitude between 0.12 and 2.1 pu. (c) Phase-space trajectory, amplitude between 2.1 and 0.12 pu (slope of -2.1 pu/s).

3) Amplitude Decrement (Second Test): In this simulation, the amplitude of the input signal is decreased from 1.2 to 0.3 pu, in a period of time of 430 ms. The reduction of the input voltage can be observed on the right side of the graph presented in Fig. 4(a). The output signal of the MLCO (y, in blue) is synchronized and in phase with the voltage reference signal (in green). In Fig. 4(c), it can be seen that the trajectory has two different stages, which depend on the amplitude of the voltage reference. Moreover, it can be seen that the paths are different compared to previous test (this is marked with a red arrow). Therefore, the results obtained in these simulations verify the reversibility property.

4) Analysis of Simulations: By observing the results, it can be noticed that the strength of attraction of the different limit cycles is different. The LC with the weakest strength of attraction is the one associated with A_1, and the strength increases as A_j increases. Clearly, for A_3 the attraction is stronger than for A_1. Also, Fig. 4(a) shows that synchronization is never lost when the trajectory shifts from one LC to the other one. Consequently, an accurate synchronization is ensured even if the input signal changes. Finally, by analyzing Fig. 4(b) and 4(c), it can be seen that the trajectories of the states x and y are different when the amplitude reference changes from 0.9 to 1.2 pu, and from 1.2 to 0.3 pu. This means that the MLCO-FLL has hysteresis properties, since the output voltage depends on the "history" of the input voltage. In other words,

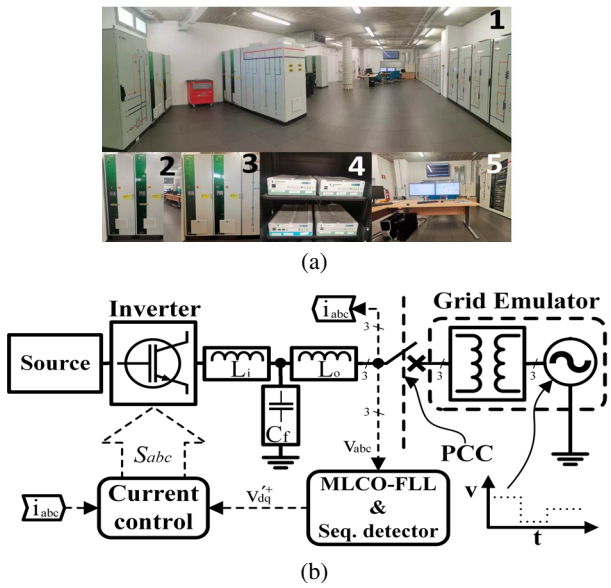

Fig. 5. (a): 1) Laboratory overview; 2) 15 kVA VSCs; 3) 75 kVA VSCs; 4) real-time computers; and 5) external computers. (b) Experimental setup.

it distinguishes the direction of the input voltage variation and takes different paths depending on whether the input voltage increases or decreases. This special characteristic is unique, and the differences compared to other synchronization algorithms will be highlighted in the comparative analysis, in Section V.

IV. Experimental Results

The theoretical developments were validated in the Smart Energy Integration Laboratory (SEIL) (Fig. 5(a)). The grid was emulated by using a 75 kVA VSC. Another VSC of 15 kVA and 10 kHz sampling frequency was used to measure the grid voltage and execute the control system. Fig. 5(b) shows the diagram of the experimental setup. The measurements of the three-phase voltage sensors (v_{abc}) are used as inputs for the MLCO-FLL and the voltage sequence detector. The sequence detector gives as output signals the positive component of the voltage, which is synchronized with the dq reference frame ($v_{dq}^{'+}$). The voltage sequence detector is shown in Fig. 6(a). Then, the three-phase input signal is transformed to the $\alpha\beta$ reference frame. The signals v_α and v_β are processed by two MLCO-FLL blocks to obtain a signal in phase ($v_{\alpha\beta}^{'}$) and a quadrature signal ($qv_{\alpha\beta}^{'}$). After that, the following transformation matrix is used to calculate the positive and negative sequence signals ($v_{\alpha\beta}^{'+}$ and $v_{\alpha\beta}^{'-}$) [35]

$$T^{\pm} = \frac{1}{2}\begin{pmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{pmatrix}. \tag{13}$$

Lastly, the positive sequence signal ($v_{\alpha\beta}^{'+}$) is transformed to the rotating reference frame (dq), by using the angular frequency generated by the MLCO-FLL. Therefore, the voltage sequence detector shown in Fig. 6(a) consists of two parts. One part is

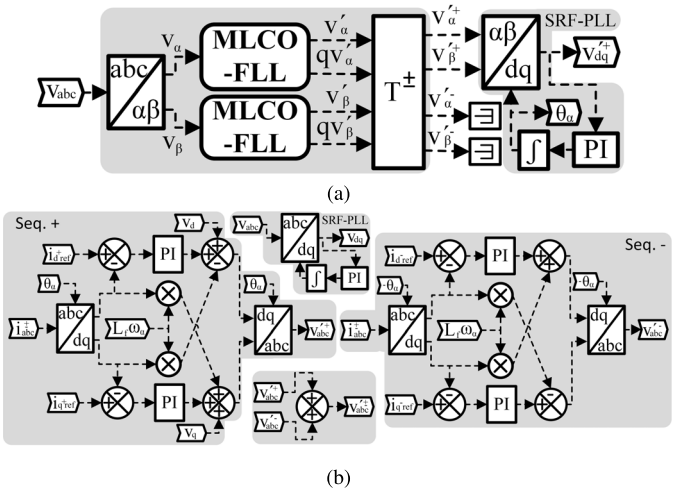

Fig. 6. (a) Voltage sequence component detector consisting of a SRF-PLL with a MLCO-FLL as a prefilter. (b) Double synchronous reference frame current controller.

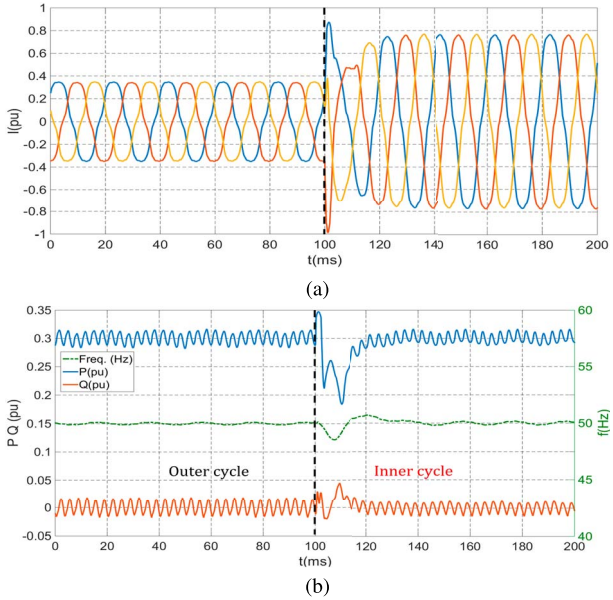

Fig. 7. Inverter operation during a voltage sag. (a) Three-phase current. (b) Active and reactive powers (blue and brown lines, respectively). (green-dashed line) Frequency signal.

the MLCO-FLL which is frequency adaptive and eliminates harmonics. The other part is the SRF-PLL which detects the phase of the voltage by using a PI controller.

The control system implemented in the inverter is shown in Fig. 6(b), and it is based on a double synchronous reference frame (DSRF) current controller with decoupling and feed-forward terms. Its basic structure can be found in [9] and additional details regarding coupling terms can be found in [31]. The input signals are the current references ($i_{dq_{\text{ref}}}$), the voltage in dq (v_{dq}) and the measured current (i_{abc}). The voltage feed-forward is only included in the positive sequence, as this signal has not been filtered. Park transformations are used to refer signals to the dq^+/dq^- reference frames. During sags, the positive-sequence reference is modified to provide reactive-power support. The system configuration and the parameters for the experimental tests are shown in Table I. For simplicity, the negative-sequence references are set to zero in the tests. However, the injection of negative sequence currents will be requirement in future grid codes [37].

The order of the MLCO-FLL is set to $n = 3$. Therefore, it has two stable LCs and one unstable LC. The outer LC is used when the grid voltage is under normal conditions while the inner one is used when there is voltage sag. The vector field of the MLCO-FLL tested in the experiments is shown in Fig. 2. The algorithm was implemented in embedded (real-time) computers NEXTCOM NISE3140 and the results were collected by using MATLAB/Simulink. See [38] for a detailed description of the laboratory. The fundamental frequency was 50 Hz and the fault profiles were developed for realistic conditions (i.e., opening and reclosing of protections).

Three experimental tests and one simulation test were conducted. In the first test, a balanced voltage sag was applied in order to analyze the response of currents, powers, and the frequency. In the second test, a FRT test with harmonics was carried out. In the third test, the converter is used to inject active and reactive power during an unbalanced voltage sag. In the last test, a simulation of a fault that causes a zero-voltage ride-through scenario is presented.

a) Three-Phase Voltage Sag: A balanced voltage sag was applied to the system of Fig. 5(b). The voltage was modified from 0.9 to 0.4 pu. The results of this test are presented in Fig. 7. Before the voltage sag, the MLCO-FLL was operating in the outer limit cycle (brown cycle, A_3, in Fig. 2). The current control ensured the injection of 0.3 pu of power during normal operation. The inverter current is shown in Fig. 7(a). The active power, the reactive power, and the frequency signal are depicted in Fig. 7(b). Previous to the sag, the inverter was operating in steady state. The harmonics in the powers appear due to the voltage harmonics components in the grid voltage and the converter current. Current harmonics could be eliminated with resonant controllers [36].

A voltage sag of 0.4 pu took place at $t = 100$ ms. At that instant, the MLCO-FLL switched from the outer to the inner limit cycle (green cycle of A_1, in Fig. 2). Fig. 7(a) shows that, when the sag started, the injected current increased to keep the active and reactive power injection constant. During this transient, the MLCO-FLL was synchronized with its inner limit cycle. The transient was smooth and only a small disturbance at $t = 100$ ms in Fig. 7(a) and 7(b) was observed. This produces a small transient with an amplitude of ± 1.5 Hz in the frequency signal, which is reflected in the powers. The currents also exhibit transients that vanish in 20 ms, approximately.

b) Fault Ride-Through Test with Harmonics: The performance of the grid-connected inverter was tested for a sag with voltage harmonics. The voltage profile generated by the grid emulator was configured to change from 1 to 0.4 pu, with harmonics. Typical harmonics (5th, 7th, 11th, and 13th) of both positive and negative sequence were used. The corresponding values of magnitude, phase and sequence can be found in Table II.

TABLE II
HARMONIC COMPONENTS ADDED FOR TEST (B)

Harmonic	Seq. comp.	Mag. (pu)	Phase (°)
5, 11	−	0.1, 0.05	0, 65
7, 13	+	0.07, 0.02	20, 10

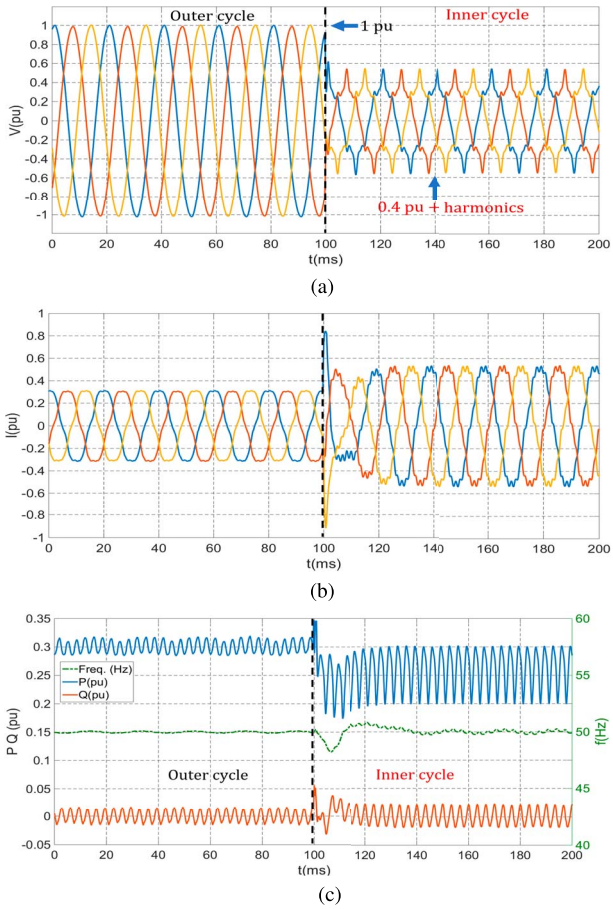

Fig. 8. Results of an inverter connected to the grid, for a voltage sag of 0.4 pu with harmonics. (a) Grid voltage. (b) Inverter current. (c) Active and reactive powers (blue and brown, respectively). The frequency is shown in green.

The three-phase waveform before and after the voltage sag is shown in Fig. 8(a).

Fig. 8(b) shows the current injected to the grid. The fundamental component of the current increased. The current is now slightly distorted due to the voltage harmonics present in the grid voltage. Fig. 8(c) shows the active and reactive powers injected to the grid. For this test, the reference power (P) was set to 0.3 pu. At $t = 100$ ms a voltage sag took place, and then the active and reactive powers had small transients that lasted for 25 ms, approximately. The ripple of the active power, the reactive power and the frequency signal increased. This happened due to the harmonics present in the grid voltage. The MLCO-FLL compensated the voltage harmonic disturbances by adding a ripple of $\pm$ 0.5 Hz over a constant value of the frequency. Thanks to that, the output signal remained synchronised with

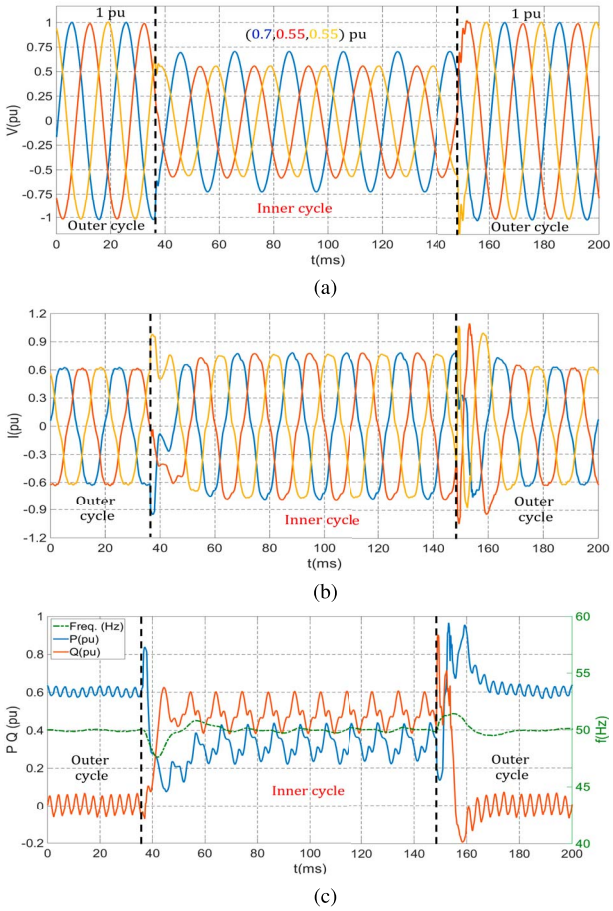

Fig. 9. Reactive current supply during an unbalanced voltage fault (0.7-0.55-0.55 pu). (a) Grid voltage. (b) Inverter current. (c) Active and reactive powers (blue and brown, respectively). The frequency is shown in green.

the internal limit cycle (A_1) (Fig. 2). From this result, it can be concluded that the inverter remained well synchronized with the grid even in the case of voltage sags with harmonics.

c) Reactive Current Support During Unbalanced Voltage Sags: The performance of the MLCO-FLL was evaluated for unbalanced voltage sags with reactive power compensation. The controller increases the reactive power during the sag to support the grid. Fig. 9(a) shows the unbalanced voltage sag, which lasts for 120 ms. During the sag, the MLCO-FLL operates in the inner cycle. Therefore, as shown in Fig. 9(b), the reactive current injection increases.

Fig. 9(c) shows the active and reactive powers (blue and brown, respectively), and the frequency signal (green) of the grid-following converter. The active and reactive powers oscillate at twice the grid frequency during the voltage sag. This happens because the controller forces constant currents, in dq^+, while the voltage is unbalanced [9]. The small oscillations in the beginning appear due to presence of harmonics in the current. The powers and the frequency have fast transients (less than 25 ms), which is relatively fast for unbalanced sags. Also, the overshoot in the powers is less than 0.4 pu, and for the frequency signal, less than 2.5 Hz.

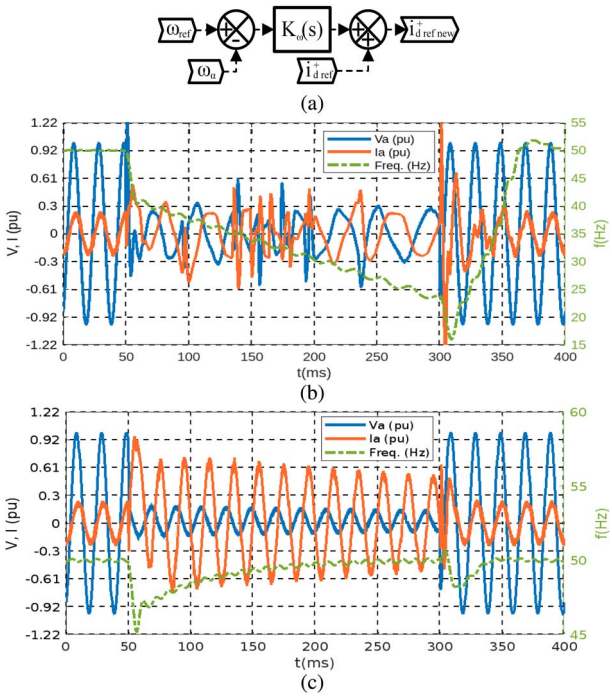

Fig. 10. Zero-voltage ride-through operation test. (a) Block diagram of the frequency correction loop. Test (b) without and (c) with the loop.

d) Zero-Voltage Ride-Through Operation Test: A zero-voltage ride-through operation test has been performed according to the ENTSO-E grid code [5], [37]. A weak grid was considered ($L = 6.7$ mH and X/R is 10). In this test, the converter should remain connected to the grid even when the voltage drops to zero, for a minimum period of 250 ms. To avoid losing synchronism during the event, a control loop is applied over the frequency error, see Fig. 10(a). This additional control loop was first presented in [5]. The frequency error is processed by PI compensator, $K_\omega(s)$. The result is added to i^+_{dref}, giving a new reference signal, i^+_{drefnew}. The parameters of this test are shown in the last row of Table I.

Fig. 10(b) shows the voltage and current of the phase-a, together with the frequency, when the fault occurs at $t = 50$ ms. In this case, the additional control loop is not active. As a consequence, the current injected to the grid (red line) becomes out of control and the frequency of the MLCO-FLL (dotted green line) decreases. At $t = 300$ ms, the grid voltage grid is restored and the current experiences a large transient. After some milliseconds, the MLCO-FLL becomes synchronised with the grid, again.

Fig. 10(c) shows the results obtained when the frequency correction loop is used. At $t = 50$ ms the fault takes place and the additional loop is activated. Consequently, the converter starts injecting a current (red line) proportional to the frequency error. This produces a voltage rise at the connection point that helps in retaining synchronism. One relevant feature of the MLCO-FLL is the fast convergence during this type of events (even when the correction loop was not used).

V. Comparison with Other Linear and Nonlinear Synchronization Algorithms

In this section, a comparison with the other three linear and nonlinear synchronization techniques was conducted. More specifically, the PLL, the SOGI-FLL and the nonlinear LCO-FLL were selected. Different tests were used to analyze their response to frequency and phase jumps, filtering capability, and robustness of the output. The simulation conditions were similar to those of the real-time application. Matlab/Simulink with the Bogacki–Shampine solver and a step size of 100 μs was used. The parameters used in each of the cases are presented in the second row of Table III. A summary of the states, multiplications, additions/subtractions, and trigonometric functions is shown in the last part of Table III.

a) Frequency Variation: A frequency step of +5 Hz (from 50 to 55 Hz) was applied to the input signal of the synchronization algorithms. Fig. 11(a) (blue), shows the transient response of the MLCO-FLL, which operates in the outer orbit (A_3). It has the shortest settling time (37 ms) with an overshoot of 0.2 Hz. However, when it operates in the inner orbit (A_1), the settling time is higher (90 ms) and it does not have overshoot (dashed-blue line). This happens because the inner orbit is weaker than the outer orbit.

Fig. 11(a) shows the frequency signal of the LCO-FLL (orange line) and the SOGI-FLL (green line). They are slower than the proposed technique (39 and 56 ms, respectively), and without overshoot. For the PLL, the response time is 140 ms and the overshoot is 0.35 Hz. These results are shown in the second section of Table III (rows 3–5).

b) Phase Step Variation: Fig. 11(b) shows the transient response of the frequency signal for a phase jump of 30 degrees. In real applications, this test would trigger the protections of power converters. Here, it is only used to compare the performance of the different synchronization algorithms. The MLCO-FLL has the fastest response (49 ms) when it operates in the outer orbit (A_3). The overshoot is 5.15 Hz. The settling time of the MLCO-FLL in the inner orbit has a settling time of 82 ms and a smaller overshoot (2.5 Hz). The MLCO-FLL for $n = 3$ has undershoot, but for $n = 1$ it does not.

The transient responses of LCO-FLL and the SOGI-FLL are similar, but slower compared to the MLCO-FLL. Their settling times are 50 ms and 60 ms, and their overshoots 3.9 Hz and 3 Hz, respectively. The PLL has the slowest settling time (130 ms) and the smallest overshoot (1.65 Hz). Compared to the other techniques, the MLCO-FLL is faster (for $n = 3$ is faster than for $n = 1$). The results are summarized in the third section of Table III (rows 6–9).

c) Filtering: The total harmonic distortion (THD) of the output signals is between 2% and 3%, for all the cases. However, the internal frequency in the MLCO-FLL operating in the outer orbit exhibits the widest amplitude variation (1.2 Hz). This action compensates for the fast variations in the input signal, which has a THD of 12.4%. This information is shown in the fourth section of Table III (rows 10–12).

d) Input Signal Amplitude Variation: The voltage reference generated by the MLCO-FLL in FRT applications is compared

TABLE III
SUMMARY OF THE MOST RELEVANT RESULTS OBTAINED IN THE COMPARATIVE ANALYSIS

	MLCO-FLL A_3	**MLCO-FLL** A_1	**LCO-FLL**	**SOGI-FLL**	**PLL**
Optimized parameters	[d]	[d]	k_v=1, $k_f=\sqrt{2}$	$k=\sqrt{2}$, $\gamma=1$	k_p=96.1,k_i=3850 ω_p=73.44π
Frequency step (+5Hz)					
Settling time (2 %)	37 ms	90 ms	39 ms	56 ms	140 ms
Overshoot	0.2 Hz	-	-	-	0.35 Hz
Phase step (30 deg)					
Settling time (2 %)	49 ms	82 ms	50 ms	60 ms	130 ms
Overshoot	5.15 Hz	2.5 Hz	3.9 Hz	3 Hz	1.65 Hz
Filtering					
THD output[a]	2.49 %	2.9 %	2.92 %	2.26 %	-
Steady-state (peak-to-peak) frequency control signal	Δ1.2 Hz	Δ0.23 Hz	Δ0.43 Hz	Δ0.2 Hz	Δ0.02 Hz
Amplitude variation					
Hysteresis properties	yes	yes	no	no	no
Output amplitude robustness	yes	yes	yes[b]	no	-
Implementation details[c]					
State variables, Mult. (x)	3, 13	3, 11	3, 10	3, 5	2, 9
Additions/subtractions	18	14	8	3	7
Trigonometric functions	no	no	no	no	yes

[a]Input THD, 12.4 %; [b]Amplitude range, 0.76 pu-1.22 pu; [c]MATLAB-Simulink, Bogacki–Shampine solver, step size 100 μs; [d]Same as Table I.

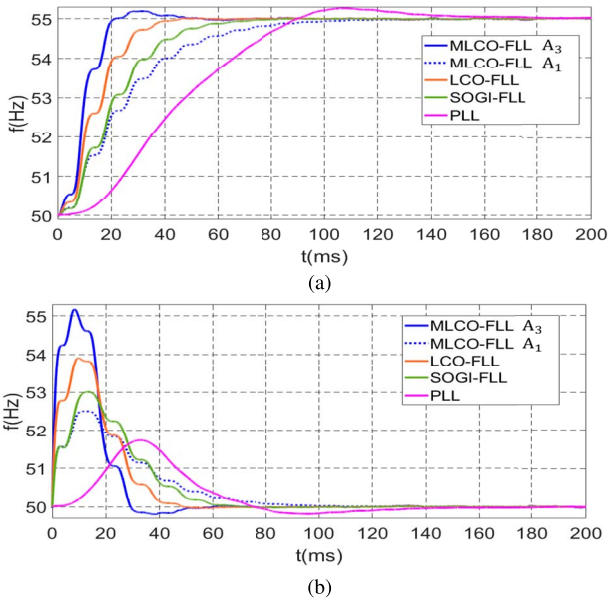

Fig. 11. Comparison of the MLCO-FLL with other synchronization techniques, for frequency and phase variations. MLCO oscillating in (blue) A_3, (dashed blue line) A_1, (orange) LCO, (green) SOGI and (pink) PLL. (a) Response to a step variation of 5 Hz. (b) 30 degrees.

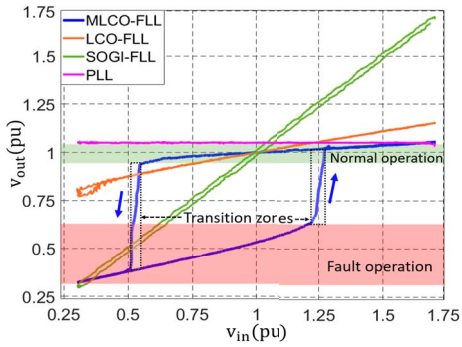

Fig. 12. Comparison of the MLCO-FLL with other representative synchronization techniques, for variations in the voltage amplitude.

to that generated by the other algorithms. Fig. 12 shows the relation between the input and the output voltage. For the PLL (in pink), the relation is completely flat since the PLL is fully based on detecting the phase of the input voltage. It is important to mention that this technique does not have state machines to switch between control systems depending the grid voltage level. Therefore, this method does not show any special behavior or characteristic during voltage sags. Fig. 12 (green) shows the response of the SOGI-FLL. The relation between the input and the output voltages is linear and starts at zero. Therefore, any disturbance in the input voltage will be reflected in the output voltage. In this case, if there is the need to react in a certain way in LVRT or HVRT scenarios, additional processing blocks would be required. Fig. 12 (orange) shows the response of the LCO-FLL, which is another nonlinear synchronization algorithm. It can be seen that this algorithm has a slight slope over the full range of the input voltage. As a consequence, it cannot be used to distinguish between LVRT and HVRT operation. Finally, the response of the MLCO-FLL is depicted in Fig. 12, in blue. This algorithm exhibits hysteresis. This means that the output voltage switches between orbits according to the voltage level. The direction of the input voltage variation determines that change. In other words, the output voltage depends on the "history" of the input voltage. This feature is useful for LVRT and HVRT applications, as it allows to distinguish between these operating modes without additional logical conditioning. Hence, the MLCO-FLL provides a robust reference over a wide voltage range in normal operation, and it provides hysteresis features in case of sags and swells. This information

is gathered in Table III (rows 12–14). In summary, the MLCO-FLL is an alternative technique based on nonlinear theory that offers a competitive performance in comparison with conventional techniques.

VI. Conclusion

In this article, a nonlinear synchronization technique for power inverters in LVRT and HVRT applications has been proposed. This algorithm is based on a nonlinear limit cycle and it is called MLCO-FLL. The MLCO-FLL has been explained and compared with other algorithms found in the literature. Finally, its performance was validated by using simulations and experimental results.

The results show that the MLCO-FLL is robust against voltage disturbances and phase-frequency variations. Moreover, it produces soft amplitude changes with hysteresis properties when there are voltage sags. Even though this is not a mandatory requirement (i.e., this detection can be done by adding additional logic conditions), it is a relevant feature that is useful in other applications. The results from the comparison with other synchronization algorithms showed that the MLCO-FLL represents an alternative method with a competitive performance. Moreover, it is based on a novel theory and, therefore, its performance can be improved in future. The experimental results verified the performance of the MLCO-FLL for balanced and unbalanced voltage sags. Also, it has been shown that the MLCO-FLL is suitable for zero-voltage ride through scenarios. The MLCO-FLL is a generalization of the LCO-FLL. Therefore, it has more degrees of freedom than the LCO-FLL since it has more than one LC. Also, it has intrinsic hysteresis properties. Finally, it is considered that being able to choose the level of attraction of each LC, individually, is a topic of interest for further research.

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